MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI0220IT

Revision	
Engineering	
Date	
Our Reference	

DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2007.10.17	First Release.	ZHANG	LUO

CONTENTS

Preliminary Specification
of
LCD Module Type
Model No.: MI0220IT

1. General Description

- 2.2",176 (RGB) x220 dots,262k colors,transmissive,positive,amorphous silicon TFT LCD module.
- Viewing angle: 12 o'clock
- Drive scheme: 1/220 duty.
- Driving IC:'Magnachip' MC2TA7402 (COG) controller driver for a liquid crystal TFT display or equivalent.
- Data interface: 8080 system 8-bit/16-bit/ (16-bit default) parallel bus interface.
- Logic voltage: 2.8V.
- White LED backlight.
- Touch panel.
- FPC connection.
- "RoHS" compliance.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter		Specifications	Unit
Outline dimensions		40.3(W) x 55.26(H) x 4.3(D) (Exclude FPC and backlight and Touch panel and component area)	mm
Color TFT 176 (RGB) x220	Viewing area (T.P)	37.0(W) x 49.56(H)	mm
	Active area (T.P)	37.0(W) x 49.56(H)	mm
	Active area (LCD)	34.85(W) x 43.56(H)	mm
	Display format	176 (RGB) x 220	dots
	Color configuration	RGB stripes	-
	Dot pitch	0.198(RGB)(W) x 0.198(H)	mm
Weight		TBD	gram

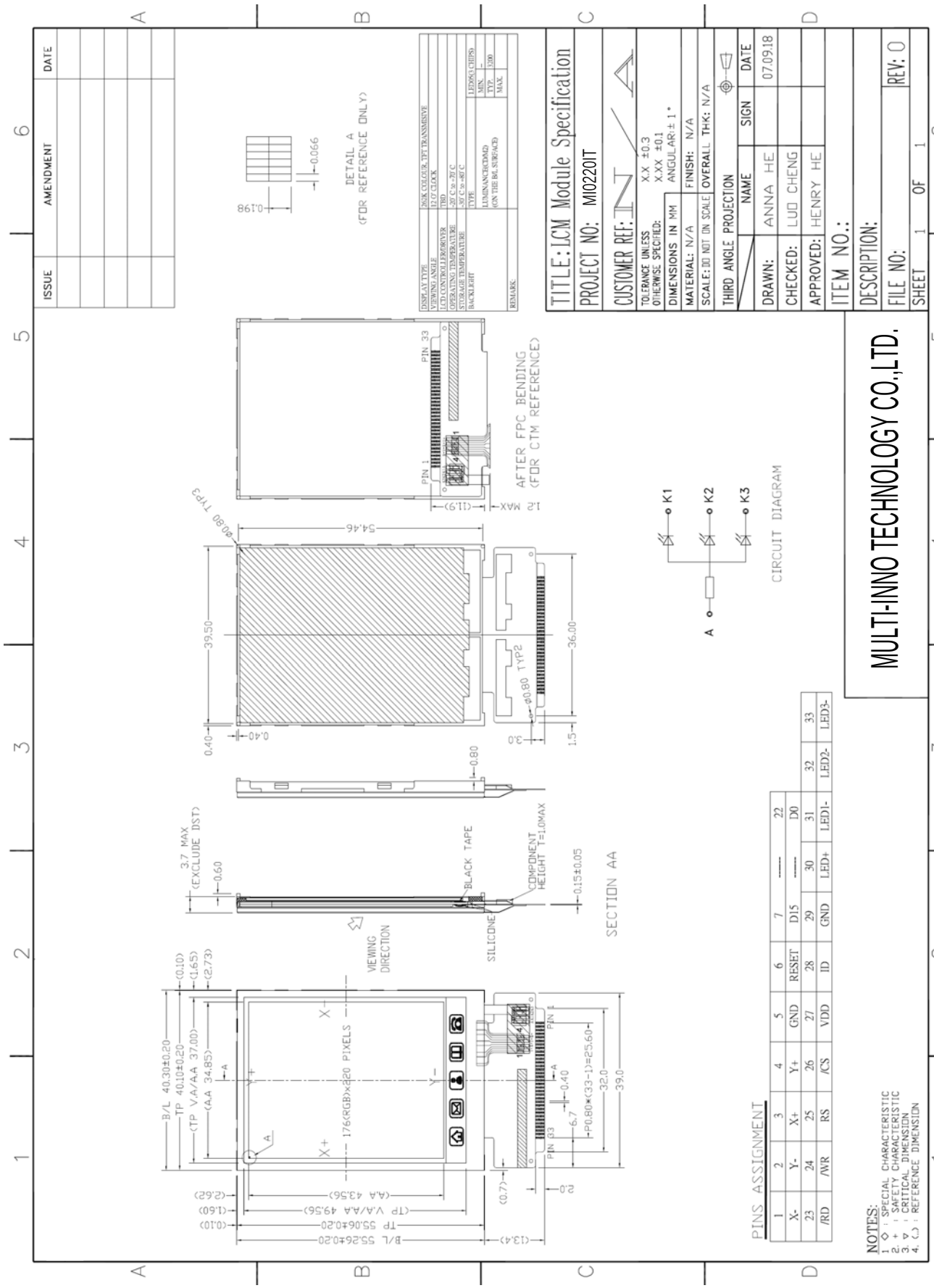


Figure 1: Module Specification

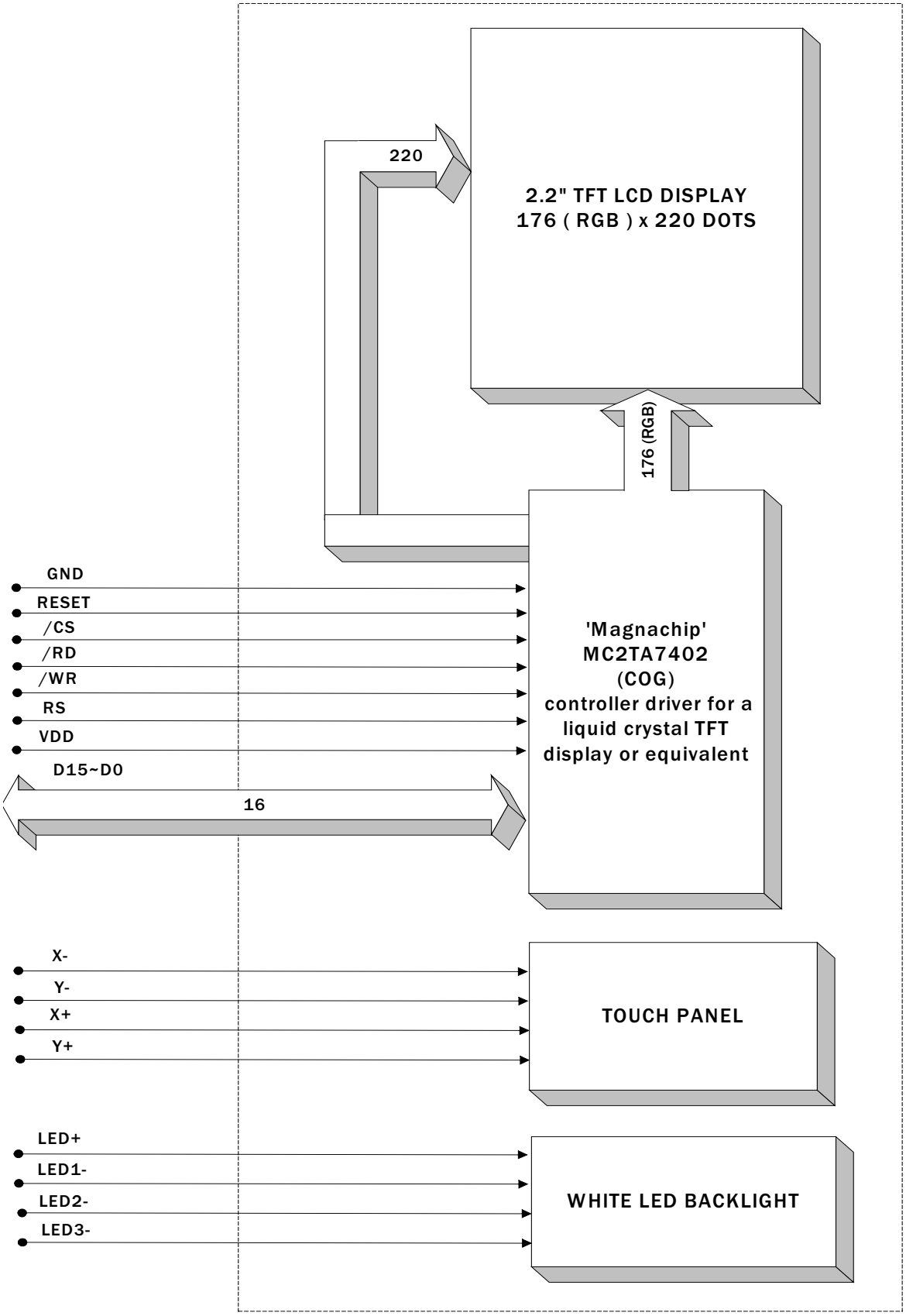


Figure 2: Block Diagram

3. Interface signals

Table 2: Pin assignment

Pin No.	Symbol	Description
1	X-	X- input position for touch panel.
2	Y-	Y- input position for touch panel.
3	X+	X+ input position for touch panel.
4	Y+	Y+ input position for touch panel.
5	GND	Ground.
6	RESET (NRESET)	A reset pin. Initializes the MC2TA7402H when the signal is low. Make sure to execute a power-on reset after supplying power.
7	D15	An 16-bit parallel bi-directional data bus for 80-system interfaces 16-bit bus: D17~10,D8~D1 8-bit bus: D17~D10
8	D14	
9	D13	
10	D12	
11	D11	
12	D10	
13	D9	
14	D8	
15	D7	
16	D6	
17	D5	
18	D4	
19	D3	
20	D2	
21	D1	
22	D0	
23	/RD (NRD)	Inputs a read strobe signal in 80-system bus interface mode and enables an operation to read out data when the signal is low.
24	/WR (NWR)	Inputs a write strobe signal in 80-system bus interface mode and enables an operation to write data when the signal is low.
25	RS	A register selecting signal. Low: select the Index or status register High: select a control register
26	/CS (NCS)	Selects the MC2TA7402H Low: the MC2TA7402H is selected and accessible High: the MC2TA7402H is not selected and not accessible
27	VDD	Power supply for logic and the DDRAM: VDD
28	ID	No connection.
29	GND	Ground.
30	LED+	Anode of LED backlight input.
31	LED1-	Cathode of LED backlight input.
32	LED2-	Cathode of LED backlight input.
33	LED3-	Cathode of LED backlight input.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage (1)	VDD-GND level	-0.3	+2.2	V	1,2,8
	IOVCC-GND level	-0.3	+4.6		
Power supply voltage (2)	VCI,VCILVL-GND level	-0.3	+4.6	V	1,3
Power supply voltage (3)	DDVDH-GND level	-0.3	+6.0	V	1,4
Power supply voltage (4)	GND level-VCL	-0.3	+4.6	V	1
Power supply voltage (5)	DDVDH-VCL	-0.3	+9.0	V	1,5
Power supply voltage (6)	VGH-GND level	-0.3	+18.5	V	1,6,8
Power supply voltage (7)	GND level-VGL	-0.3	+18.5	V	1,7,8
Power supply voltage (8)	VGHmax-VGLmin	<32	-	V	1,6,7,9
Input signal voltage	Vt	-0.3	IOVCC+0.3	V	1

Note 1) If used beyond the absolute maximum ratings, the LSI may be permanently damaged. It is strongly recommended to use the LSI at a condition within the electrical characteristics for normal operation. Exposure to a condition not within the electrical characteristics may affect device's reliability.

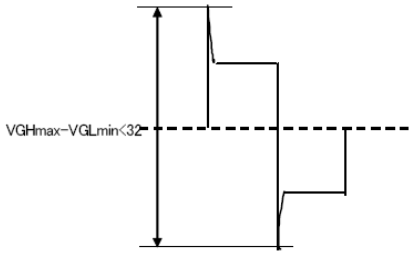
Note 2) Make sure: VDD > GND level, IOVCC > GND level.

Note 3) Make sure: VCI > GND level. Note 4) Make sure: DDVDH > GND level.

Note 5) Make sure: DDVDH > VCL. Note 6) Make sure: VGH > GND level.

Note 7) Make sure: GND level > VGL. Note 8) "GND level" symbolizes "AGND" and "VSS".

Note 9) Not over than absolute maximum voltage including the panel in On/Off and the ripple voltage of wave pattern.



4.2 Environmental Condition

Table 4

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C< 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note 1: Product cannot sustain at extreme storage conditions for long time.

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 2.8V, GND=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VDD-GND		2.7	2.8	2.9	V
Supply voltage (for analog power supply)	VCI		-	2.8	-	V
TFT gate ON voltage	VGH	Note 1	12	-	18	V
TFT gate OFF voltage	VGL	Note 2	-12	-	-7	V
TFT common electrode voltage	Vcom	Note 3	-2	-	5	V
TFT Kick-Back Voltage Max	△Vp Max	-	0.2	-	1.5	V
TFT Kick-Back Voltage Min	△Vp Min	-	0.2	-	1.5	V
Input signal voltage	V_{IH}	"H" level	0.8IOVCC	-	IOVCC	V
	V_{IL}	" L" level	GND	-	0.2IOVCC	V
Supply current (logic & LCD)	IDD	VDD=2.8V	-	TBD	-	mA
Supply voltage of white LED backlight	VLED	Forward current =15mA x 3 =45mA Number of LED dies = 3	3.0	3.2	3.4	V
Luminance (on the backlight surface)			3200	-	-	cd/m^2

Note (1): VGH is TFT Gate operating voltage.

Note (2): VGL is TFT Gate operating voltage.

Note (3): Vcom must be adjusted to optimize display quality: cross talk, contrast ratio and etc.

5.2 Timing Specification

5.2.1 Reset Timing Characteristics

Table 6

Item	Symbol	Unit	Min	Typ	Max
NRESET "Low" level width	tRES	μs	1	–	–
NRESET rise time	trRES	ns	-	-	10

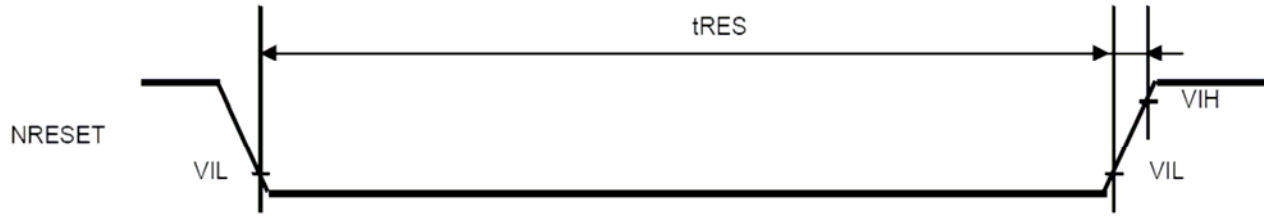


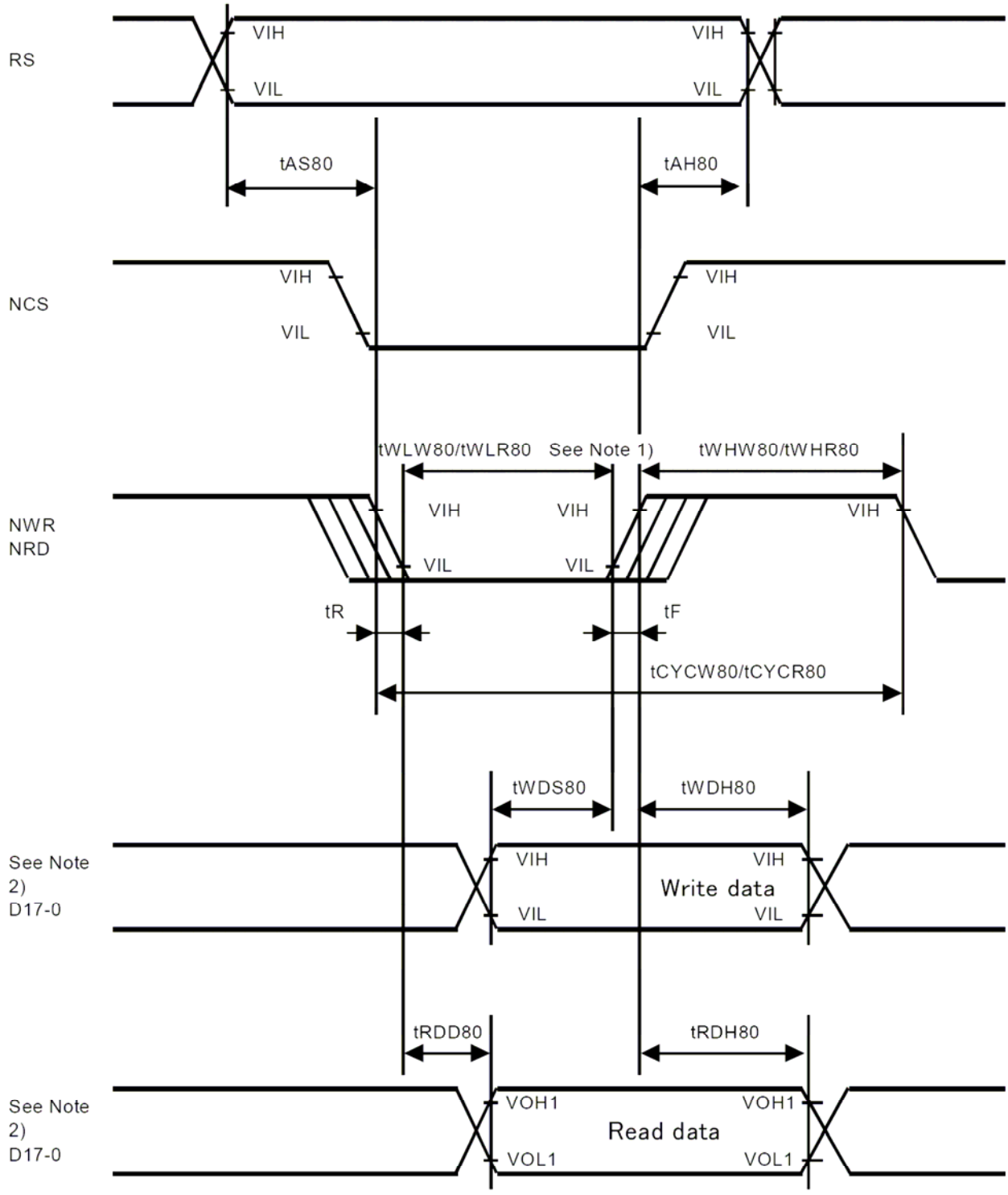
Figure 3: Reset Timing

5.2.2 80-system bus interface operation

Table 7

Item		Symbol	Unit	Min	Typ	Max
Cycle time	Write	tCYCW80	ns	100 *1	-	-
	Read	tCYCR80		500	-	-
Pulse width low	Write	tWLW80	ns	40	-	-
Read "Low" level pulse width	Read	tWLR80		250	-	-
Pulse width high	Write	tWHW80	ns	40	-	-
Read "High" level pulse width	Read	tWHR80		200	-	-
Pulse rise/fall time		tR, tF	ns	-	-	25
RW,RS and CSB setup time		tAS80	ns	10	-	-
RW,RS and CSB hold time		tAH80		0	-	-
			ns	2	-	-
Write data setup time		tWOS80	ns	60	-	-
Write data hold time		tWDH80	ns	15	-	-
Read data delay time		tRDD80	ns	-	-	200
Read data hold time		tRDH80	ns	5	-	-

Note *1) If you set the horizontal dot's number "odd", the Min of tCYCW will be 200nS



Note 1) PWLW and PWLR are defined by the overlap period when NCS is "Low" and NWR or NRD is "Low".

Note 2) Unused data innput pins must be fixed at either "IOVCC" or "GND".

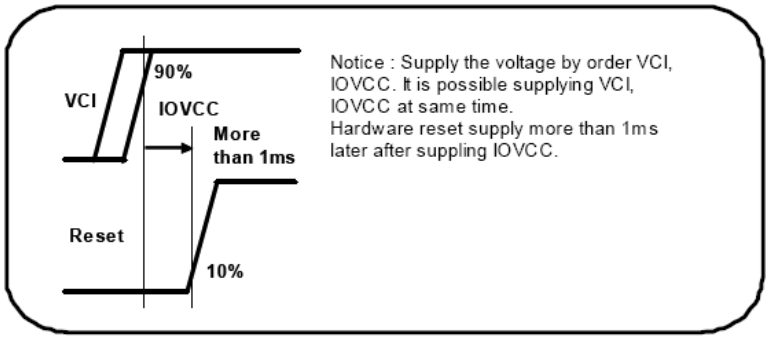
Figure 4: 80-systems bus interface operation

5.3 Power Supply Setting

As for power supply setting, follow the sequence below.

The setting time for oscillators, step-up circuits and operational amplifiers depends on the panel's wiring resistance, ACF connection resistance, used capacitance and panel's load.

Set according to the actual LCD module.



Power ON sequence

Step	Register	Register Value	Waiting time	Operation
1	Power-on		50ms	Power-on (VCI and IOVCC power supply start)
2	Hardware Reset		10ms	Intializing LSI by using NRESET pin.
User Setting				
3	R01h	xxxxh	-	Driver Output Control (VSPL,HSPL,DPL,EPL,SM,GS,SS,NL4-0)
4	R02h	xxxxh	-	LCD Driver AC Cntrol (FLD1-0,BC, EOR)
5	R03h	xxxxh	-	Entry Mode (TR1,DFM1-0,BGR,I/D1-0,AM)
6	R07h	xx0xh	-	Display Cntrol (1) (PT1-0,VLE1-0,SPT,GON=0,CL,REV, D1-0=00)
7	R08h	xxxxh	-	Display Control (2) (FP3-0,BP3-0)
8	R09h	xxxxh	-	Display Control (3) (PTG2-0,ISC3-0)
9	R0Bh	xxxxh	-	Frame Cycle Adjustment (NO1-0,SDT1-0,ECS2-0,DIV1-0,DCR_EX,DCR2-0,RTN1-0)
10	R0Ch	xxxxh	-	RGB/VSYNC Interface (RM,DM1-0,RIM1-0)
11	R21h	xxxxh	-	DDRAM Addess Set (AD15-0)
12	R30h	xxxxh	-	Gamma Control (PKP12-10,PKP02-00)
13	R31h	xxxxh	-	Gamma Control (PKP32-30,PKP22-20)
14	R32h	xxxxh	-	Gamma Control (PKP52-50,PKP42-40)
15	R33h	xxxxh	-	Gamma Control (PRP12-10,PRP02-00)
16	R34h	xxxxh	-	Gamma Control (PKN12-10,PKN02-00)
17	R35h	xxxxh	-	Gamma Control (PKN32-30,PKN22-20)
18	R36h	xxxxh	-	Gamma Control (PKN52-50,PKN42-40)
19	R37h	xxxxh	-	Gamma Control (PRN12-10,PRN02-00)
20	R38h	xxxxh	-	Gamma Control (VRP14-10,VRP03-00)
21	R39h	xxxxh	-	Gamma Control (VRN14-10,VRN03-00)
22	R40h	xxxxh	-	Gate Scan Start Position (SCN)
23	R42h	xxxxh	-	First Screen Drive Position (SE17-10, SS17-10)
24	R43h	xxxxh	-	Second Screen Drive Position (SE27-20,SS27-20)
25	R44h	xxxxh	-	Horizontal DDRAM Address Position (HEA7-0,HSA7-0)
26	R45h	xxxxh	-	Vertical DDRAM Address Position (VEA7-0, VSA7-0)
Initial Power Control Sequence (fosc=285kHz±10%) VCI=VCILVL=2.8V				
27	R11h	2F04h	-	VREG1OUT, VCI1 Setting (GVD5-0=2F, VC1-0=100)
28	R14h	xxxxh	10ms	Power Control (4) (VCMR, VCM5-0,VML5-0)
29	R10h	0580h	-	Power Control (1) (SAP[2:0]=000,BT[2:0]=101,DC[2:0]=100,SLP=0,STB=0)
30	R13h	0040h	40ms	CP1/CP3 ON (PON=1,PON1=0,AON=0)
31	R13h	0060h	40ms	CP2 ON (PON=1, PON1=1,AON=0)
32	R13h	0070h	20ms	AMP ON (PON=1,PON1=1,AON=1)
User Setting for Power Control Registers				
33	R11h	xx04h	10ms	GVD5-0,VC1-0=100
34	R10h	xxx0h	-	Power Control (1) (SAP[2:0],BT[2:0],DC[2:0],SLP=0,STB=0) SAP setting
Start transfering display image data Display ON sequence				
35	R07h	081xh	40ms	PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=10
36	R07h	081xh	40ms	PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=11

"x"stands for "user preference"

Note1) Waiting time on the list is for reference.(variable depending on penel's wiring resistance, ACF conection resistance, FPC wiring , etc.)
Note2) "Initial Power Control" should not be changed.
Note3) Set the following voltage within the limits : DDVDH=max. 5.5V, VCL=min. -3.3V, VGH=max. 16.5V, VGL=min. -16.5V, VGH-VGL<27.5V

Power Off sequence

Step	Register	Register Value	Waiting time	Operation
Display OFF sequnce				
1	R07h	081xh	40ms	Display On (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=10)
2	R07h	080xh	40ms	Display On- Normaly Color (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=10)
3	R07h	080xh	-	Display Off (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=00)
Power Off sequence				
4	R10h	0xxxh	-	Source Amp Off (SAP[2:0]=000(halt),BT[2:0], DC[2:0], SLP, STB)
5	R13h	0060h	5ms	Amp Off (PON=1, PON1=1, AON=0)
6	R13h	0000h	5ms	CP1/3(PON=0), CP2 stop (PON1=0)

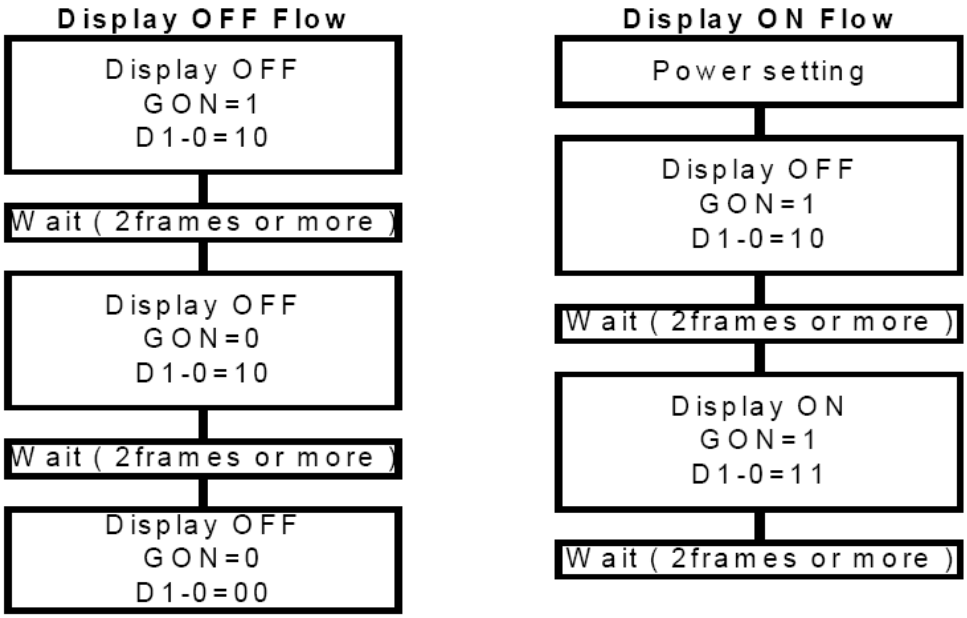
"x"stands for "user preference"

Note) Waiting time on the list is for reference.(variable depending on penel's wiring resistance,ACF conection resistance, FPC wir ing, etc.)

5.4 Instruction Setting

When setting the following instructions, follow the sequences below.

5.4.1 Display ON / OFF



5.4.2 Standby Mode

Standby-in sequence

Step	Register	Register Value	Waiting time	Operation
1	R07h	081xh	40ms	Display On (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=1,CL,REV, D[1:0]=10)
2	R07h	080xh	40ms	Display On- Normaly Color (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=10)
3	R07h	080xh	-	Display Off (PT[1:0]=01,VLE[2:1]=00,SPT=0,GON=0,CL,REV, D[1:0]=00)
4	R10h	0xx0h	-	Source Amp Off (only SAP[2:0]=000,BT[2:0], DC[2:0], SLP=0, STB=0)
5	R13h	0060h	5ms	AMP Off (PON=1, PON1=1, AON=0)
6	R13h	0000h	5ms	CP1/CP3 Off (PON=0),CP2 Off (PON1=0)
7	R5Ah	0002h	-	Standby setting (STBM[1:0]=010) VCI=2.75V
8	R10h	0001h	(30ms)	Standby in (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=0, STB=1)

"x"stands for "user preference"

Note) Waiting time on the list is for reference.(variable depending on penel's wiring resistance,ACF conection resistance,FPC wiring ,etc.)

Standby -release sequence

Step	Register	Register Value	Waiting time	Operation
1	R00h	0001h	10ms	OSC Satat- in Standby Mode
2	R10h	0000h	10ms	Standby out (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=0, STB=0)
3				Execute from step 3 to 36 of "Power-on sequence"

"x"stands for "user preference"

Note) Waiting time on the list is for reference.(variable depending on penel's wiring resistance,ACF conection resistance,FPC wiring,etc.)

5.4.3 Sleep Mode

Standby-> Sleep Sequence

Step	Register	Register Value	Waiting time	Operation
1	R00h	0001h	10ms	OSC Start- in Standby Mode
2	R10h	0000h	5ms	Standby out (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=0, STB=0)
3	R10h	0002h	30ms	Sleep in (SAP[2:0]=000,BT[2:0]=000, DC[2:0]=000, SLP=1, STB=0)

"x"stands for "user preference"

Note) Waiting time on the list is for reference.(variable depending on penel's wiring resistance, ACF conection resistance, FPC wi ring, etc.)

6. Optical Characteristics (for panel only)

The test of Optical specifications shall be measured in a dark room (ambient luminance ≦1 lux and temperature = 25±2℃) with the equipment of Luminance meter system and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θand Φ equal to 0°., The center of the measuring spot on the Display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. Optimum viewing angle direction is 12 o'clock.

Table 8

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Threshold voltage		Vsat		2.2	2.3	2.4	V	Fig. 5
		Vth		1.3	1.4	1.5	V	
Viewing Angle range	Horizontal	Θ_3	CR > 10	40	45		Deg.	Note 1
		Θ_9		40	45		Deg.	
	Vertical	Θ_{12}		45	50		Deg.	
		Θ_6		15	20		Deg.	
Contrast ratio		CR	Θ = 0°	300	350			Note 2
Transmittance		T(%)	Θ = 0°		7			Note 3
White Chromaticity		x_w	Θ = 0°	0.287	0.307	0.327		Note 4 *Color Filter Glass
		y_w		0.315	0.335	0.355		
Reproduction Of color	Red	x_R	Θ = 0°	0.624	0.644	0.664		
		y_R		0.326	0.346	0.366		
	Green	x_G		0.285	0.305	0.325		
		y_G		0.561	0.581	0.601		
	Blue	x_B		0.115	0.135	0.155		
		y_B		0.116	0.136	0.156		
Response Time		Tr+Tf	Θ = 0°		30	40	msec	Note 5

Note: 1.Viewing angle is the angle at which the contrast ratio is greater than 10.
The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Fig.6)

2. Contrast measurements shall be made at viewing angle of Θ= 0°and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Fig. 6) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Transmittance is the value with Polarizer.
4. The color chromaticity coordinates specified in Table 8 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the C/F. Measurement condition is C -light source & Halogen Lamp.
5. The electro-optical response time measurements shall be made as Fig. 7 shown in Appendix by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is Tr, and 90% to 10% is Td.

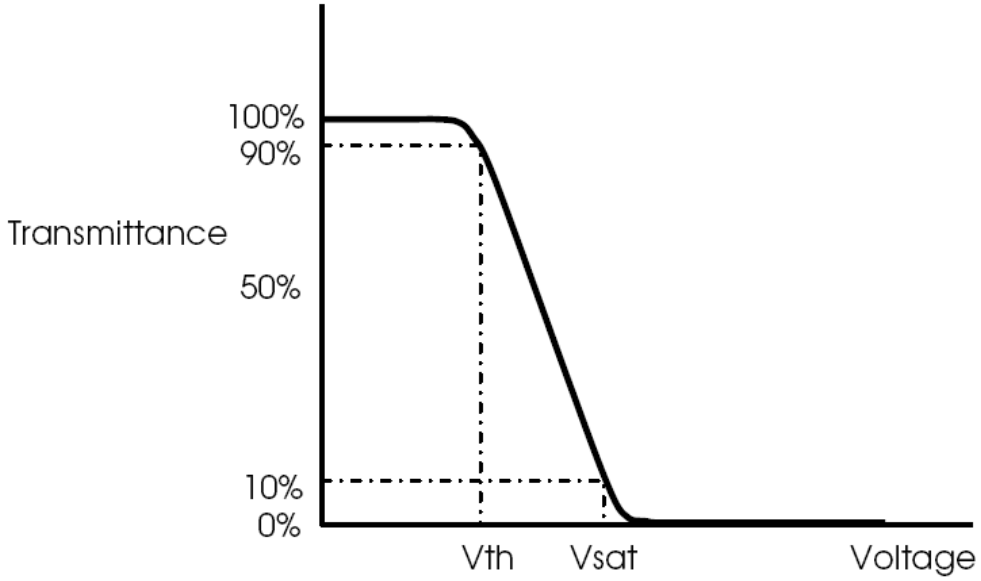


Figure 5. The definition of Vth & Vsat

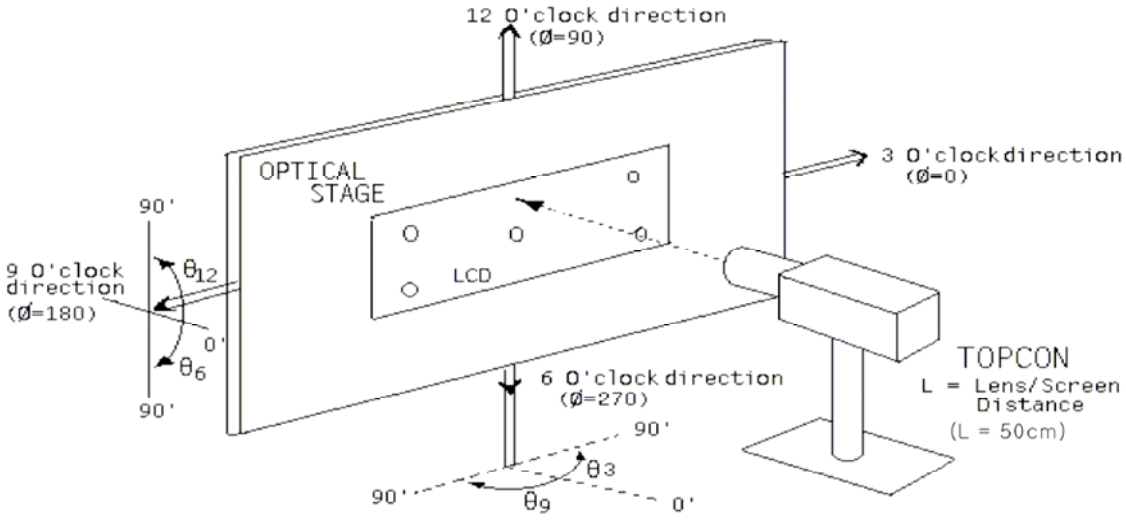


Figure 6. Measurement Set Up

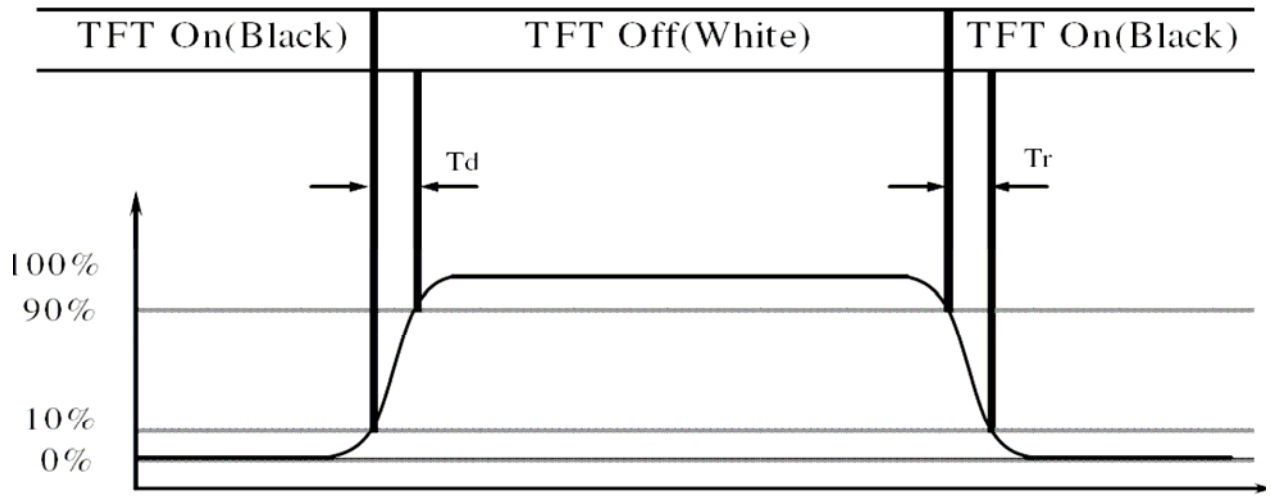
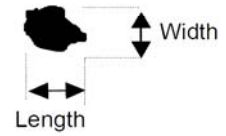
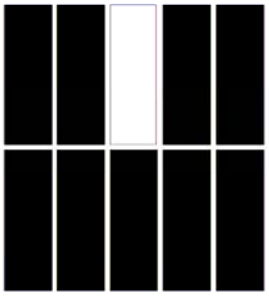
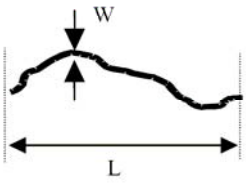
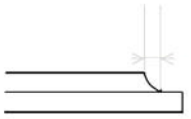
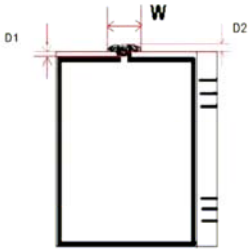
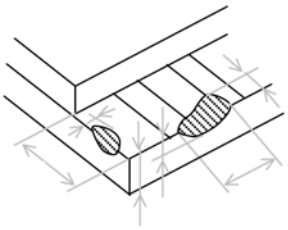
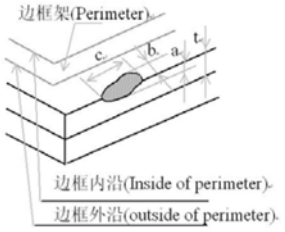
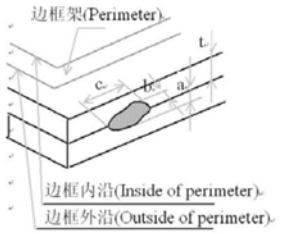
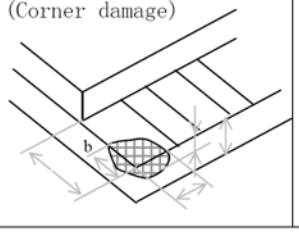


Figure 7. Response Time Testing

7. TFT panel inspection specification

壞品名稱 Failure mode	圖例說明 Illustration	分类 Category(Unit: mm)		可接受数量 Acceptable count	
				可视区 Viewing area	非可视区 non-Viewing area
黑點 Black spot 白點 White spot	 Φ= (Length+width)/2	A	Φ≦0.10	不计 Not count	不计 Not count
		B	0.10<Φ≦0.15	2, 两点间距离不小于 5mm The gap between the two spots should be 5 mm and above.	
		C	0.15<Φ≦0.20	1	
		D	0.20<Φ	0	
亮點(因爲濾光片損壞造成的紅點，綠點，藍點等) Bright spot (Red spot, green spot and blue spot caused by damaged colour filter)		A	缺陷面積小於或等於一個單基色面積 Area≦1 sub-pixel	1	N/A
黑线 Black line 白线 White line		A	W≦0.03	不计 Not count	不计 Not count
		B	0.03<W≦0.05, L≦3.0	2	
		C	0.05<W	按黑白点判定 Judged by spot spec	
以下为外观标准(Below are cosmetic inspection specifications)					
玻璃毛刺 Excess glass		b≦1.0且不影响外形尺寸及装配(注意COG工序对b的要求，不同尺寸LCD的b都不同) b≦1.0, this defect shall not affect the outline dimension or assembly process.(Remarks: For COG process, the defect size is decided by the dimension of LCD panel.)			
		不影响外形尺寸及装配. This defect shall not affect the outline dimension or assembly process.			
进胶尺寸 The depth of UV glue entered in LCD cell		進膠深度大於等於 0.2mm 且不可進入視域范圍，膠水凸出玻璃邊高度小于等于 0.8mm,长度=（注入口宽度）+（2~6 mm） a. D1≥0.2，not enter into viewing area b. D2≦0.8, c. W=End mouth width + (2~6 mm)			

<table>
<tr><td rowspan="5">玻璃缺陷划伤、缺损

Glass defect
(scratch, damage)</td><td>① 台阶破损 (LCD ledge damage)
  </td><td colspan="2">分类 Category</td></tr>
<tr><td rowspan="3"></td><td>A</td><td>非电极区，台阶破损不得影响装配及外形尺寸
The defect shall not affect the outline dimension or assembly process at non ITO zone.</td></tr>
<tr><td>B</td><td>电极区的破损，b 不得超过邦定电极长度（该长度应不小于 1.2mm）的 1/4, a、c 方向不限制
b≦1/4w, a & c not count (at ITO zone)</td></tr>
<tr><td>C</td><td>台阶两侧的缺损不得损伤对位标识或走线
Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td>②非封接面破损 (Outside of perimeter damage)
  </td><td colspan="2">b 方向破损不得到达边框内沿
b can’t reach inside of perimeter.</td></tr>
<tr><td>③ 封接面破损
(Joint glass damage)
  </td><td colspan="2">b 方向破损不得到达边框外沿或走线
b can’t reach outside of perimeter or ITO layout.</td></tr>
<tr><td rowspan="2">④角上破损
(Corner damage)
  </td><td>A</td><td>a ≦ t， b ≦ 3.0， c ≦ 3.0</td></tr>
<tr><td colspan="2">B. 玻璃破损不允许损伤电极图形和/或对位标识
Alignment mark on LCD ledge shall not be damaged.</td></tr>
<tr><td colspan="3">注：a:表示崩角厚度；b:表示崩角深度；c:表示崩角长度；t;表示单片玻璃厚度；单位：mm
Remark: a stands for thickness of damage, b for width, c for length and t for glass thickness. (Unit: mm)</td></tr>
</table>

8. Remark

HANDLING LCD AND LCD MODULES

1. Liquid Crystal Display (LCD)

LCD is made up of glass, organic sealant, organic fluid and polymer based polarizers. The following precautions should be taken when handling:

(1) Keep the temperature within range for use and storage. Excessive temperature and humidity could cause polarization degredation, polarizer peel-off or bubble generation. When storage for a long period over 40° C is required, the relative humidity should be kept below 60%.
(2) Do not contact the exposed polarizers with anything harder than an HB pencil lead. To clean dust off the display surface, wipe gently with cotton, chamois or other soft material soaked in petroleum benzin. Never scrub hard.
(3) Varitronix does not responsible for any polarizer defect after the protective film has been removed from the display
(4) Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause polarizer deformation or color fading, while an active LCD with water condensation on its surface will cause corrosion of ITO electrodes.
(5) PETROLEUM BENZIN is recommended to remove adhesives used to attach front/rear polarizers and reflectors, while chemicals like acetone, toluene, ethanol and isopropyl alcohol will cause damage to the polarizer. Avoid oil and fats. Avoid lacquer and epoxies which might contain solvents and hardeners to cause electrode errosion. Some solvents will also soften the epoxy covering the DIL pins and thereby weakening the adhesion of the epoxy on glass. This will cause the exposed electrodes to erode electrochemically when operating in high humidity and condensing environment.
(6) Glass can be easily chipped or cracked from rough handling, especially at corners and edges.
(7) Do not drive LCD with DC voltage.
(8) When soldering DIL pins, avoid excessive heat and keep soldering temperature between 260°C to 300°C for no more than 5 seconds. Never use wave or reflow soldering.

2. Liquid Crystal Display Modules (MDL)

2.1 Mechanical Considerations

MDL's are assembled and adjusted with a high degree of precision. Avoid excessive shocks and do not make any alterations or modifications. The following should be noted.
(1) Do not tamper in any way with the tabs on the metal frame.
(2) Do not modify the PCB by drilling extra holes, changing its outline, moving its components or modifying its pattern.
(3) Do not touch the elastomer connector (conductive rubber), especially when inserting an EL panel.
(4) When mounting a MDL make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
(5) Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels.
(6) If FPCA need to be bent, please refer the suggested bending area on the specification. The stiffener and component area on FPC/FFC/COF must not be bent during or after assembly (Note: for those models with FPC/FFC/COF +stiffener).
(7) Sharp bending should be avoided on FPC to prevent track cracking.

2.2 Static Electricity

MDL contains CMOS LSI's and the same precaution for such devices should apply, namely:

(1) The operator should be grounded whenever he comes into contact with the module. Never touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any part of the human body.
(2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
(3) Only properly grounded soldering irons should be used.
(4) If an electric screwdriver is used it should be well grounded and shielded from commutator sparks.
(5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended.
(6) Since dry air is inducive to statics, a relative humidity of 50 - 60% is recommended.

2.3 Soldering

(1) Solder only to the I/O terminals.
(2) Use only soldering irons with proper grounding and no leakage.
(3) Soldering temperature is 280°C ± 10°C .
(4) Soldering time: 3 to 4 seconds.
(5) Use eutectic solder with resin flux fill.
(6) If flux is used. the LCD surface should be covered to avoid flux spatters. Flux residue should be removed afterwards.
(7) Use proper de-soldering methods (e.g. suction type desoldering irons) to remove lead wires from the I/O terminals when necessary. Do not repeat the soldering/ desoldering process more than three times as the pads and plated through holes may be damaged.

2.4 Label

Identification labels will be stuck on the module without obstructing the viewing area of display.

3. Operation

(1) The viewing angle can be adjusted by varying the LCD driving voltage Vo.
(2) Driving voltage should be kept within specified range, excess voltage shortens display life.
(3) Response time increases with decrease in temperature.
(4) Display may turn black or dark Blue at temperatures above its operational range; this is however not destructive and the display will return to normal once the temperature falls back to range.
(5) Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear "fractured". They will recover once the display is turned off.
(6) Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.
(7) Display performance may vary out of viewing area. If there is any special requirement on performance out of viewing area, please consult Varitronix.

4. Storage and Reliability

(1) LCD's should be kept in sealed polyethylene bags while MDL's should use antistatic ones. If properly sealed, there is no need for desiccant.
(2) Store in dark places and do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C and the relative humidity low. Please consult MULTI-INNO for other storage requirements.
(3) Water condensation will affect reliability performance of the display and is not allowed.
(4) Semi-conductor device on the display is sensitive to light and should be protected properly.
(5) Power up/down sequence.
   a) Power Up: in general, LCD supply voltage, Vo must be supplied after logic voltage, VDD becomes steady. Please refer to related IC data sheet for details.
   b) Power Down: in general, LCD supply voltage, Vo must be removed before logic voltage, VDD turns off. Please refer to related IC data sheet for details.

5. Safety

If any fluid leaks out of a damaged glass cell, wash off any human part that comes into contact with soap and water. Never swallow the fluid. The toxicity is extremely low but caution should be exercised at all times.

LIMITED WARRANTY

MULTI-INNO LCDs and modules are not consumer products, but may be incorporated by MULTI-INNO 's customers into consumer products or components thereof. MULTI-INNO does not warrant that its LCDs and components are fit for any such particular purpose.

1. The liability of MULTI-INNO is limited to repair or replacement on the terms set forth below. MULTI-INNO will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user.

   Unless otherwise agreed in writing between MULTI-INNO and the customer, MULTI-INNO will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with MULTI-INNO LCD Acceptance Standards (copies available on request), for a period of one year from the date of shipment. Confirmation of such date shall be based on freight documents.

2. No warranty can be granted if any of the precautions stated in HANDLING LCD and LCD Modules above have been disregarded. Broken glass, scratches on polarizers, mechanical damages as well as defects that are caused by accelerated environmental tests are excluded from warranty.
3. In returning the LCD and Modules, they must be properly packaged and there should be detailed description of the failures or defects.

IMPORTANT NOTICE

The information presented in this document has been carefully checked and is believed to be accurate, however, no responsibility is assumed for inaccuracies. MULTI-INNO reserves the right to make changes to any specifications without further notice for performance, reliability, production technique and other considerations, MULTI-INNO does not assume any liability arising out of the application or use of products herein. Please see Limited Warranty in the previous section.

- END -