RAiO

RA8802/8820

Character/Graphic

LCD-Controller

Specification

Version 1.1

April 26, 2004

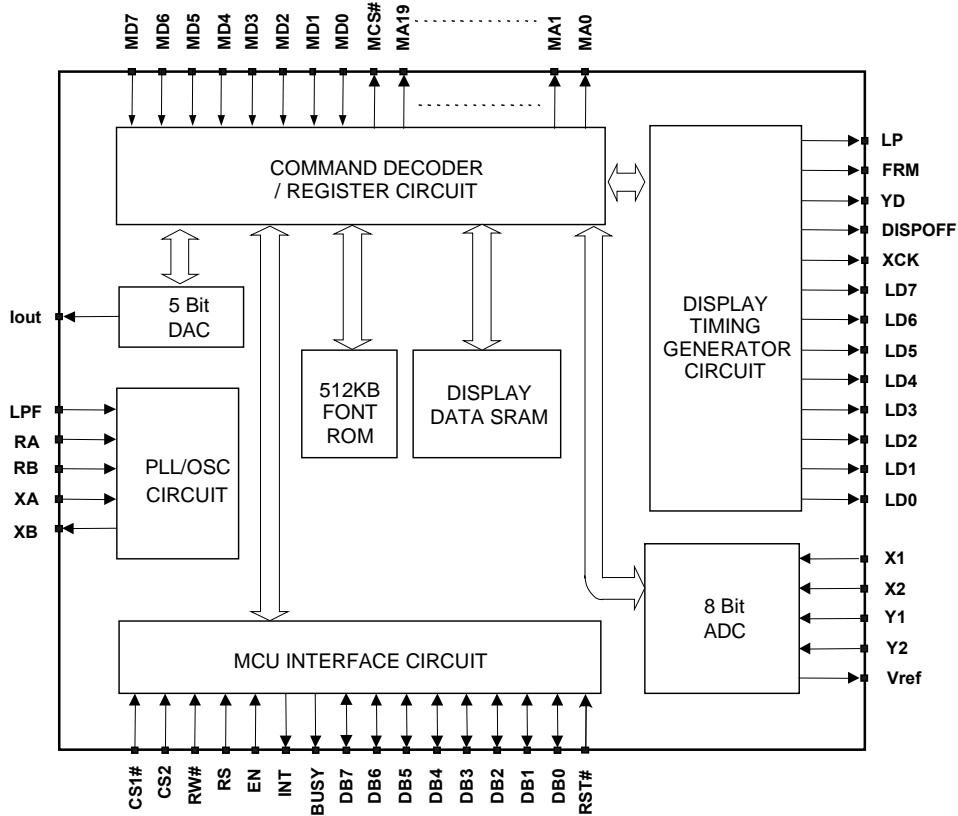RAiO Technology Inc.

1. General Description

The RA8802/8820 is a Character/Graphic dot-matrix liquid crystal display controller (LCD) with embedded 512K Byte Font ROM. The RA8802 supports up to 320x240 LCD panel size and RA8820 supports up to 240x160. In tradition, users need a graphic LCM to display Chinese characters. Now Chinese character's display of RA8802/8820 presents a revolution. The RA8802/8820, instead of a MCU, can directly deal with the access of Chinese/English fonts that consist of BIG5 or GB, and ASCII code.

The RA8802/8820 have some main functions as following. It's equipped with 8-bit ADC, supporting touch panel interface. DAC is 5-bit, providing the brightness control of the LCD panel. The RA8802/8820 built in PLL/OSC two circuits provides user choice to generate system clock. The interface of RA8802/8820 fits both of 8080/6800 series' MCU and 4/8-bit data bus. Besides that, the interface of LCD driver is compatible with many types of LCD drivers on the market.

2. Feature

◆ Dot matrix liquid crystal display controller supporting the display of Character/Graphic.

◆ Fast Character/Graphical Mode for ASCII & Chinese (Big5 Code and GB Code) support.

◆ Display Control Capacity ➔
　 RA8802: 320×240 dots (Max), 20×15 full-size character or 40×15 half-size character
　 RA8820: 240x160 dots (Max), 15x10 full-size character or 30x10 half-size character

◆ Display of 16x16 dot for full-size fonts consisting of Chinese, 8x16 dots for half-size fonts of alphanumeric characters and symbols in the same display.

◆ Clock source: RC Oscillator or 32K crystal for PLL (External 32KHz Crystal need).

◆ Built-in 9.6Kbyte/4.8Kbyte Display Data RAM

◆ High-speed 4/8-bit MCU interface allowing direct connection to both the 8080 and 6800.

◆ LCD interface: LCD driver compatible for data bus 4/8 bit supports.

◆ Built in 8-Bit ADC and 5-Bit DAC.

◆ Embedded 512KByte Font ROM and provide 512KByte Font ROM Interface.
　 BIG5:
　 --Includes standard font: 13094 Chinese words
　 --Includes special font: 408 Chinese words
　 --Includes two set ASCII codes
　 GB:
　 --Total font: 7602 Chinese words

◆ Various instruction functions
　 --White black inversion, cursor on/off/blink/bold/cursor height and cursor-width.
　 --Define the Active/Display window address.

◆ Low Power Consumption.

◆ Operating Voltage:
　 _ RA8802: 2.7~4.0V
　 _ RA8820: 2.7~5.0V

◆ Package: DIE, PQFP 100, LQFP 100

3. Block Diagram

MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0 MCS# MA19 .... MA1 MA0

COMMAND DECODER / REGISTER CIRCUIT

LP
FRM
YD
DISPOFF
XCK
LD7
LD6
LD5
LD4
LD3
LD2
LD1
LD0

DISPLAY TIMING GENERATOR CIRCUIT

Iout

5 Bit DAC

512KB FONT ROM

DISPLAY DATA SRAM

LPF
RA
RB
XA
XB

PLL/OSC CIRCUIT

X1
X2
Y1
Y2
Vref

8 Bit ADC

MCU INTERFACE CIRCUIT

CS1# CS2 RW# RS EN INT BUSY DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 RST#

4. Pin Definition

4.1 MCU Interface

Pin Name	I/O	Description
DB[7..0]	I/O	Bi-direction 8 bit data bus connected to MCU data bus. The high nibble DB[7..4] should be connected to GND when 4 bit data bus mode is used.
RD# (EN)	I	Active low RD# signal when 8080 MCU is used. Active high EN signal when 6800 series MCU are used.
WR# (R/W#)	I	Active low WR# signal when 8080 MCU is used. The data are latched at the rising edge of the WR# signal. Connected to 6800 series MCU R/W# pin when 6800 MCU is used. The MCU data will be read from RA8802/8820 when R/W# is high and will be written to RA8802/8820 when R/W# is low.
RS	I	Register/Data select pin.

		Usually connect to MCU address bus A0. The MCU will access Instruction Register when RS is high and access Data Register when RS is low.
CS1# CS2	I	Chip select pin. The RA8802/8820 is active when CS1# is low and CS2 is high
INT	O	Interrupt signal Active high or low Interrupt signal
BUSY	O	Active high or low busy signal. The RA8802/8820 can't be access when BUSY pin is high. It's should be connected to MCU I/O input. The MCU have to poll this pin before accessing RA8802/8820.

4.2 Driver Interface

Pin Name	I/O	Description
YD	O	LCD Driver control signal YD will produce a pulse at the starting address of each Frame.
FRM	O	AC-converting signal input for LCD driver waveform. Normally inputs a frame inversion signal The LCD driver output pin's output voltage level can be set to the line latch output signal and the FR signal
LP	O	**For Column:** Latch pulse input pin for display data ▪Data is latched on the falling edge of the clock pulse. **For Row:** Bi-directional shift register shift clock pulse input pin ▪Data is shift on the falling edge of the clock pulse.
XCK	O	Shift clock signal for LCD driver IC. Data is shifted on the falling edge of the XCK.
DISPOFF	O	Display off control signal used to control LCD power supply or backlight. The pin is controlled by LCR bit 2. The status of this pin is the same as LCR bit 2.
LD7 SYS_MI	I/O	Alternative function pin LD7/SYS_MI. It's connected to LCD driver IC D7, when 8-bit LCD driver IC is used. SYS_MI is for CPU type selection. It's active on reset period. Non-Pull when 6800 MCU is used. Pull low when 8080 MCU series are used.
LD6 SYS_DB	I/O	Alternative function pin LD6/SYS_DB. It's connected to LCD driver IC D6, when 8-bit LCD driver IC is used. SYS_DB is for MCU data bit selection. Non-Pull when 8-bit CPU is used. Pull low when 4-bit CPU is used. The high nibble data bus DB[7..4] Should tied to GND When 4-bit CPU is used.

LD5 SYS_FQ	I/O	Alternative function pin LD5/SYS_FQ. It's connected to LCD driver IC D5, when 8-bit LCD driver IC is used. SYS_FQ is for RA8802/8820 clock source selection. Non-Pull will enable internal PLL circuit and X'tal will be the clock source of RA8802/8820. Pull low when RC oscillator is used and it will disable internal PLL.
LD4	I/O	LD4 It's connected to LCD driver IC D4. When 8 bit LCD driver IC is used.
LD3 SYS_LD	I/O	Alternative function pin LD3/SYS_LD. This pin is connected to D3 pin of LCD driver IC. SYS_LD is for LCD driver data bus selection. Non-Pull when 8-bit LCD driver is used. Pull low when 4-bit LCD driver is used.
LD2 SYS_PLR	I/O	It's connected to LCD driver IC D2. SYS_PLR is polarity select. It's connected to LCD driver IC D2. SYS_PLR is for RS polarity selection. When Non-Pull, then "RS" = 0 means Register Access Cycle, and "RS" = 1 means Data Access Cycle. When Pull Low, then "RS" = 1 means Register Access Cycle, and "RS" = 0 means Data Access Cycle.
LD1 OPM1	I/O	Alternative function pin LD1/OPM1. It's connected to LCD driver IC D1. OPM1 and OPM0 are used to choose the test model of RA8802/8820. Do not Pull-Low for this pin.
LD0 OPM0	I/O	Alternative function pin LD0/OPM0. It's connected to LCD driver IC D0. OPM1 and OPM0 are used to choose the test model of RA8802/8820. Do not Pull-Low for this pin.

4.3 Clock Interface

Pin Name	I/O	Description
XA	I	Oscillator Input. This is the input signal of internal oscillator. Normally it connects to a 32768Hz X'tal. The XA, XB and LPF are used for X'tal and internal PLL. If in RC_OSC mode, then XA, XB and LPF should be Floating.
XB	O	Oscillator Output. This is the output signal of internal oscillator. Normally it connects to a 32768Hz X'tal.
LPF	I	LPF (Low Pass Filter) Input. This input is used for internal PLL circuit.
RA	I	Connect Resistance.

		The RA, RB are used for RC-Oscillator mode.
		If in X'tal/PLL mode then RA and RB should be Floating.
RB	I	Connect Resistance.

4.4 Power Signal

Pin Name	I/O	Description
VDD	I	Power supply
GND	I	Power ground
AVDD	I	Analog power supply signal.
AGND	I	Analog ground.

4.5 Misc. Signal

Pin Name	I/O	Description
RST#	I	Active low reset signal. (The reset pulse do not less than 100mS after MCU stable)
X1	I	Normally connected to touch panel Left pin XL.
X2	I	Normally connected to touch panel Right pin XR.
Y1	I	Normally connected to touch panel Top pin YU.
Y2	I	Normally connected to touch panel Bottom pin YD.
Iout	O	DAC current source output used to contrast voltage control.
Vref	O	ADC voltage reference signal.
MA[19..0]	O	20-bit Address Bus connected to the address bus of external character pattern ROM. **Note: MA0 need to be Pulled High (10K)** If do not use the external Font ROM, the MA[7:0] should tied to VDD to reduce the power consumption.
MCS#	O	Character pattern ROM chip select and output enable
MD[7..0]	I	8-bit Data Bus connected to the data bus of external character pattern ROM. Note: If do not use the external Font ROM, the MD[7:0] should tied to VDD to reduce the power consumption.
SEL0	I	Test pin must be tied to GND for normal use.
SEL1	I	Test pin must be tied to VDD for normal use.

5. System Application

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  ┌──────────┐           ┌─────────────┐      ┌──────────┐        ┌──────────┐
  │   MCU    │ ◄────────►│             │─────►│   LCD    │───────►│   LCD    │
  └──────────┘           │             │      │  Driver  │        │  Panel   │
                         │             │      └──────────┘        └──────────┘
  ┌──────────┐           │   RA8802    │      ┌──────────┐
  │Extendible│ ◄────────►│   RA8820    │─────►│ Contrast │
  │ Font ROM │           │             │      │ Circuit  │
  └──────────┘           │             │      └──────────┘
                         │             │
  ┌──────────┐           │             │      ┌──────────┐
  │ Hardware │           │             │◄─────│  Touch   │
  │Pin Initial│─────────►│             │      │  Panel   │
  │  Setup   │           │             │      └──────────┘
  └──────────┘           └─────────────┘
  ┌──────────┐
  │  Clock   │────────────────►
  └──────────┘
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