



Revision 1.4.1

Data Sheet

IT600

This document describes operation, connectivity and electrical specifications of Fastrax IT600 OEM GNSS receiver module.

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Fastrax Ltd

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REFERENCES

Ref. #	File name	Document description
(1)	STA8088EX Databrief Rev1.pdf	STA8088EX Datasheet
(2)	ST GNSS NMEA specification and commands 3.2.pdf	ST GNSS NMEA specification and commands, rev 3.2
(3)	NMEA 0183 - Standard For Interfacing Marine Electronic Devices Version 3.01 - January 1, 2002	Available from www.nmea.org
(4)	reflow_sodering_profile.pdf	Module Soldering Profile

CHANGE LOG

Rev.	Notes	Date
0.1	First Draft	2011-03-24
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1.1	Added operational modes; draft status	2011-07-12
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1.4	Release status; updated performance spec; corrected XSTANDBY signal to level sensitive; corrected and clarified Standby mode operation; named firmware configuration to ITX; updated absolute and electrical characteristic tables; added and updated notes to cover all I/O; added notes and limitation on Antenna Bias current & switch dissipation.	2011-10-05

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2 Overview

2.1 General

The Fastrax IT600 is an OEM GPS receiver module, which provides the ST Teseo II, ref (1), GNSS receiver functionality using the state of the art ST STA8088EX chip. The module has small form factor 16.2x18.8 mm, height is 2.30 mm nominal (2.60 mm max). The Fastrax IT600 receiver provides simultaneous GPS, Glonass, QZSS, Galileo, and Compass (BeiDou 2) open service L1 reception capability. IT600 supports Dead Reckoning using 3-axis digital Gyro and Odometer Pulse from car. Support for DWP (Differential Wheel Pulse) based DR through CAN interface will be available later.

The Fastrax IT600 module is an advanced multi-constellation positioning and it has single RF input with separate GPS/Galileo and Glonass IF outputs combined with 32 dedicated tracking channels that can be assigned to acquire and track any mix of GPS, Glonass, QZSS Galileo and Compass signals. Unused tracking channels can be turned off for power saving. Enabling GPS + Glonass reception, the number of visible satellites goes up typically by a factor of two compared to for instance a GPS-only receiver. This means that e.g. in urban canyons with limited visibility of the sky GNSS fix is guaranteed with higher accuracy when compared to GPS-only receivers. IT600 is also Galileo and Compass ready with future software upgrades.

IT600 supports St Microelectronics ST-AGPS™ Self Trained Assisted-GPS technology, able to provide both fully-autonomous Ephemeris prediction and server-based, predictive assistance using GPStream™ Server technology provided by Rx Networks. The autonomous predictions are providing accurate fix for 5 days on observed satellites with no server needs. Using server-based GPStream™ technology from Rx Networks, the access of a very compact information (2KB payload) ensures full-constellation predicted ephemeris valid for 7 days.

IT600 offers a wide range of interfaces in a tiny form factor. Two UART's are available for NMEA and RTCM104. A third UART/USB is also available. I2C provides a convenient interface for adding for instance MEMS sensors, EEPROM or other I2C compatible peripherals. A standard 1PPS output is also available. CAN bus is available for DR. The I/O voltages are 3.3V CMOS levels.

A JTAG interface is also available for custom firmware implementations and debugging. Currently ARM Realview 3.1 compiler and Lauterbach ICE are supported. Support for GNU compilers will be available later.

2.2 Block diagram

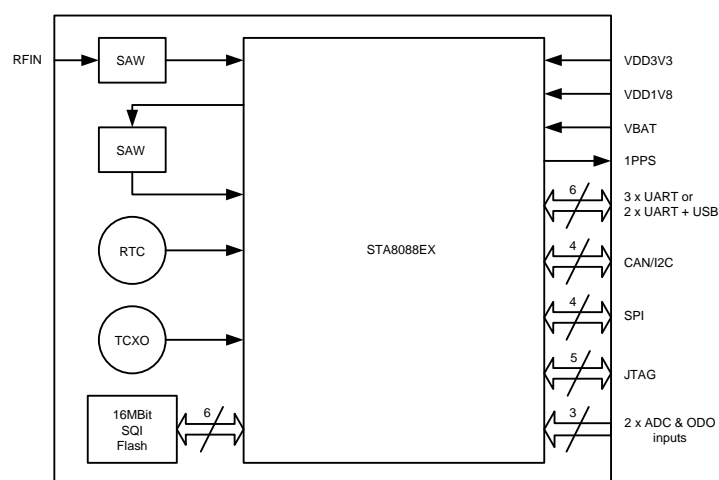


Figure 1 Block Diagram

2.3 General Specifications

Table 1 General Specifications

Receiver	Multi GNSS: GPS (SPS), Glonass (SP), QZSS, Galileo (OS), Compass (BeiDou 2 open service)
Chip	STMicroelectronics STA8088EX
Channels	32
Tracking sensitivity	-160 dBm typ.
Navigation sensitivity	-157 dBm typ.
Navigation sensitivity, cold acq.	-146 dBm typ.
Update rate	1 Hz (configurable w/ future FW 5 Hz max)
Time to First Fix, Cold acq.	35 s typ.
Time to First Fix, Hot acq.	2 s typ.
Navigation accuracy: GPS, Glonass or Hybrid GPS&Glonass (Note 4)	3m Horizontal (RMS) (Note 1) 5 m Vertical (RMS) 0.05 m/s Velocity 1 μ s Time 1PPS (RMS)
Acceleration range (Note 4)	5 g max (Note 1)
Velocity range (Note 4)	515 m/s max
Altitude range (Note 4)	18000 m max
Assisted GPS support	ST Self-Trained Assisted GPS (ST-AGPS™) 5 days, GPStream™ 7 days
Dead Reckoning support	Future FW: Odometer pulse + 3-axis digital Gyro, CAN bus ODO and DWP
Differential GPS support	RTCM104, SBAS (WAAS, Egnos)
Digital Supply voltage, VDD1V8	+1.71...+1.89 V
RF&I/O Supply voltage, VDD3V3	+3.0... +3.6 V
Backup Supply Voltage, VBAT	+1.62... +3.6 V
Power consumption	235 mW typ. (Note 2)
Antenna bias (internal)	VDD3V3 – 0.15V typ.
Storage temperature	-40°C...+85°C
Operating temperature	-40°C...+85°C (Note 3)
Peripheral ports	SPI & I ² C master/slave, CAN 2.0 A/B, JTAG
Host port	UART, port 2
Serial port protocol	NMEA-0183 rev. 3.01
Serial data format (UART)	8 bits, no parity, 1 stop bit
Serial data speed (UART)	115200 baud rate

Note 1: Live signal conditions, roof top antenna with good visibility

Note 2: In GPS + Glonass Navigation mode (VDD1V8=1.8 V, VDD3V3=3.3V, VBAT = 3V)

Note 3: In temperature range -40°C...-30°C GNSS performance, e.g. TTFF can be degraded.

Note 4: Please see Appendix A for detailed information on accuracy

3 Operation

3.1 Navigation mode

After power up the module boots from internal flash memory for Navigation operation mode. The NMEA data output is available at UART2 port output (TX signal) at 115200 baud. The UART0 port is reserved for debugging and for auxiliary purposes.

3.2 Run mode

When navigation is stopped (no GNSS) by a NMEA command \$PSTMGPSUSPEND, see ref (2), the module's CPU is still fully active and system is in Run mode and can receive commands and can execute e.g. custom firmware.

3.3 Wait For Interrupt mode

The device to save power may enter in a low power mode using Wait For Interrupt (WFI) condition. A number of interrupt lines (TBD) are available as alternate function or general purpose I/O lines to be programmed as interrupt to wake up the system and exit from low power mode. In this WFI mode the GNSS Task may be suspended, and the logic related to this function may be partially switched off. All the non-used logic has the clock gated, in order to prevent any operation and reduce power consumption. This mode is reserved for custom firmware operation.

3.4 Standby mode

Standby mode stops Navigation operation and it is entered by pulling XSTANDBY signal to LOW state. In this mode all supply inputs are powered but power drain is reduced down to 3.3 mW typ., see also Table 5.

During Standby mode digital output signals are switched to high impedance state; also antenna bias voltage at antenna input RFIN is switched off internally.

Exit from Standby mode to Navigation mode is set by relaxing XSTANDBY signal back to HIGH state; input has internal pull up to 1.2V. GNSS navigation will perform fastest possible start using internal aiding from previous fix.

3.5 Backup state

The backup state retains backup RAM content and RTC/GPS time and is the state is achieved when VBAT is kept active while other power supplies VDD1V8 and VDD3V3 are switched off. Abrupt power removal is safe since internal SQI Flash uses double buffering for code/data storage.

During Backup state all 3.3V digital I/O signals (except 1.2V CMOS signals XRESET and XSTANDBY) should be forced externally to low state since the I/O supply voltage VDD3V3 is switched off and the internal protection diode in every I/O will otherwise leak I/O current back to VDD3V3.

Exit form Backup state is switching power on back again (note 10ms delay in VDD1V8 relative to VDD3V3). GNSS navigation will perform fastest possible start using internal aiding from previous fix.

NOTE

During Backup state all 3.3V digital I/O signal levels should be forced to LOW state in order to avoid current leakage via I/O protection diode.

3.6 Programming mode

The internal Flash memory can be reprogrammed by entering to programming mode. The mode is achieved by keeping UART2_TX signal low at least 200 ms after reset state is released; see also chapter 3.7 and 4.4.

Reprogramming uses either UART0 or UART2 port to transfer a new flash image to the module and needs a suitable application running on host (or on PC).

3.7 Reset state

Reset state is forced as a Power On Reset (POR) during initial power up and POR is generated from rising edge of the VBAT supply. The XRESET signal has an internal POR delay circuit that will introduce suitable delay 100ms for automatic boot up for Normal mode. Reset state is can be also generated by host when keeping XRESET signal low.

3.8 Default firmware configuration

Current firmware configuration (ITX) has the following settings:

- Port 2: NMEA 115200 baud
 - Enabled messages: GPRMC, GPGGA, GPVTG, GNGSA, GPGSV, GLGSV, PSTMSBAS
- Port 0: Proprietary Debug messages
- SBAS, GPS, Glonass and 1PPS enabled

Firmware features not supported with rev. 7.1.9.29:

- Galileo, Compass (BeiDou 2)
- RTCM input
- USB interface
- DR
- CAN
- SPI and I2C

Example of NMEA output shown below. (See reference [2] for details).

```
$GPRMC,101522.000,A,6016.322,N,02458.328,E,0.2,0.0,030811,0.0,W*76
$GPGGA,101522.000,6016.32161,N,02458.32798,E,1,09,1.0,027.62,M,19.5,M,,*67
$GPVTG,0.0,T,,M,0.2,N,0.3,K*61
$GNGSA,A,3,09,27,22,24,15,17,14,12,28,,,,,1.8,1.0,1.5*24
$GPGSV,3,1,12,09,66,274,47,11,07,018,,12,23,243,38,14,10,328,33*7C
$GPGSV,3,2,12,15,34,205,42,17,53,101,47,18,10,273,,22,16,308,37*7C
$GPGSV,3,3,12,24,16,030,35,26,09,174,,27,79,223,46,28,24,071,38*7A
$GLGSV,3,1,10,65,10,109,,67,57,110,,68,22,268,,71,55,297,*67
$GLGSV,3,2,10,72,63,102,,74,39,041,,81,57,110,,83,16,171,*6A
$GLGSV,3,3,10,84,05,293,,90,54,123,,,,,,,,,*6D
$PSTMSBAS,1,0,124,21,184,33*11
$PSTMSBASMCH,0,124,21,184,33*4A
$PSTMSBASMCH,1,0,0,,,,,*42
```

Please note. \$GPRMC outputs lat/lon with 3 decimals. Use \$GPGGA for increased lat/lon resolution.

NOTE

Glonass (and hybrid navigation) introduces changes in NMEA output. Make sure your NMEA parser is able to handle. Please see reference [3] for details: NMEA 0183 - Standard for Interfacing Marine Electronic Devices Version 3.01 - January 1, 2002 Complete NMEA specification is available from www.nmea.org

Highlights of NMEA message changes due to Glonass & Hybrid navigation:

- **\$__GSV:**
 - Number of satellites (SV) in view, satellite ID numbers, elevation, azimuth, and SNR value. Four satellites maximum per transmission. Total number of sentences being transmitted and the number of the sentence being transmitted are indicated in the first two fields.
 - If multiple GPS, GLONASS, etc. satellites are in view, use separate GSV sentences with talker ID GP to show the GPS satellites in view and talker GL to show the GLONASS satellites in view, etc.
 - Example: IT600 NMEA output in hybrid mode – GSV messages
 - \$GPGSV,3,1,12,03,19,041,41,05,50,246,49,06,15,028,38,07,61,084,50*74
 - \$GPGSV,3,2,12,08,80,186,51,10,24,189,41,13,15,116,40,15,04,294,*79
 - \$GPGSV,3,3,12,19,15,071,40,21,13,341,39,26,38,286,46,28,26,172,43*75
 - \$GLGSV,3,1,11,65,46,237,37,69,21,039,,70,78,060,34,72,67,102,*6C
 - \$GLGSV,3,2,11,73,18,329,18,75,00,104,,76,21,004,19,77,36,043,*63
 - \$GLGSV,3,3,11,85,23,056,24,91,45,196,23,92,61,285,24,,,,*5F
- **\$__GSA**
 - GNSS DOP And Active Satellites
 - GSA messages are output as follows:
 - in Glonass or GPS mode only, the GSA-messages are output as \$GPGSA or \$GLGSA respectively
 - In hybrid mode, GSA messages are output as combined \$GNGSA message:
 - \$GNGSA,A,3,13,10,07,15,05,19,08,21,26,06,70,28,1.1,0.7,0.9*2B
 - \$GNGSA,A,3,92,65,85,03,,,,,,,,,1.1,0.7,0.9*24
 - There may be several lines of messages depending on the mode
- **\$GPRMC**
 - Recommended Minimum Specific GPS/Transit Data
 - NOTE: firmware only outputs \$GPRMC messages, which in hybrid mode contains hybrid position and speed data
 - Note: Position resolution is only 3 decimal minutes, which corresponds to about 1 m horizontal resolution; use preferably \$GPGGA with better resolution 5 decimal minutes
- **\$GPGGA**
 - Global Positioning System Fix Data
 - NOTE: firmware only outputs \$GPGGA messages, which in hybrid mode contains hybrid position and speed data
- **\$PSTMSBAS**
 - SBAS Satellite Data
 - Note: SBAS satellite usage and tracking information is outputted in \$PSTMSBAS message, not in \$__GSV messages
 - Note: default FW configuration uses SBAS PRN is 124. SBAS satellite can be set via NMEA command \$PSTMSBASSAT followed by cold start command \$PSTMCOLD; setting parameter to zero will allow automatic search for the SBAS satellite available in the user region.

3.9 Changing firmware settings

Existing firmware parameters can be polled using \$PSTMGETPAR command. It is possible to change firmware settings using \$PSTMSETPAR command. Details can be found in reference [2].

Changing parameters permanently requires also \$PSTMSAVEPAR command followed by a system re-boot. Then the new parameters are stored into internal Non-volatile memory of IT600 as long as the VBAT supply is active.

One quite useful Configuration Data Block ID is number 200. With this ID different navigation modes can be enabled and disabled.

Default value for ID 200 is 0x1639604, which enables SBAS, 1PPS, GPS and Glonass hybrid navigation.

The following procedure allows changing navigation constellation modes using e.g. Fastrax WorkBench 4.

1. Configuration command
 - Glonass only: \$PSTMSETPAR,1200,1229604*22<cr><lf>
 - GPS only: \$PSTMSETPAR,1200,1419604*27<cr><lf>
 - GPS & Glonass hybrid navigation: \$PSTMSETPAR,1200,1639604*27<cr><lf> (default configuration)
 - Restore factory configuration: \$PSTMRESTOREPAR*11<cr><lf>
2. Save Configuration
 - \$PSTMSAVEPAR*58<cr><lf>
3. Reboot
 - Cold start after constellation change: \$PSTMCOLD*1E<cr><lf>
 - Or system reboot (Reset) after other configuration changes

Note that intentional or unintentional wrong parameter settings in Data Block ID 200 may stop the system from working and/or degrade the system performance.

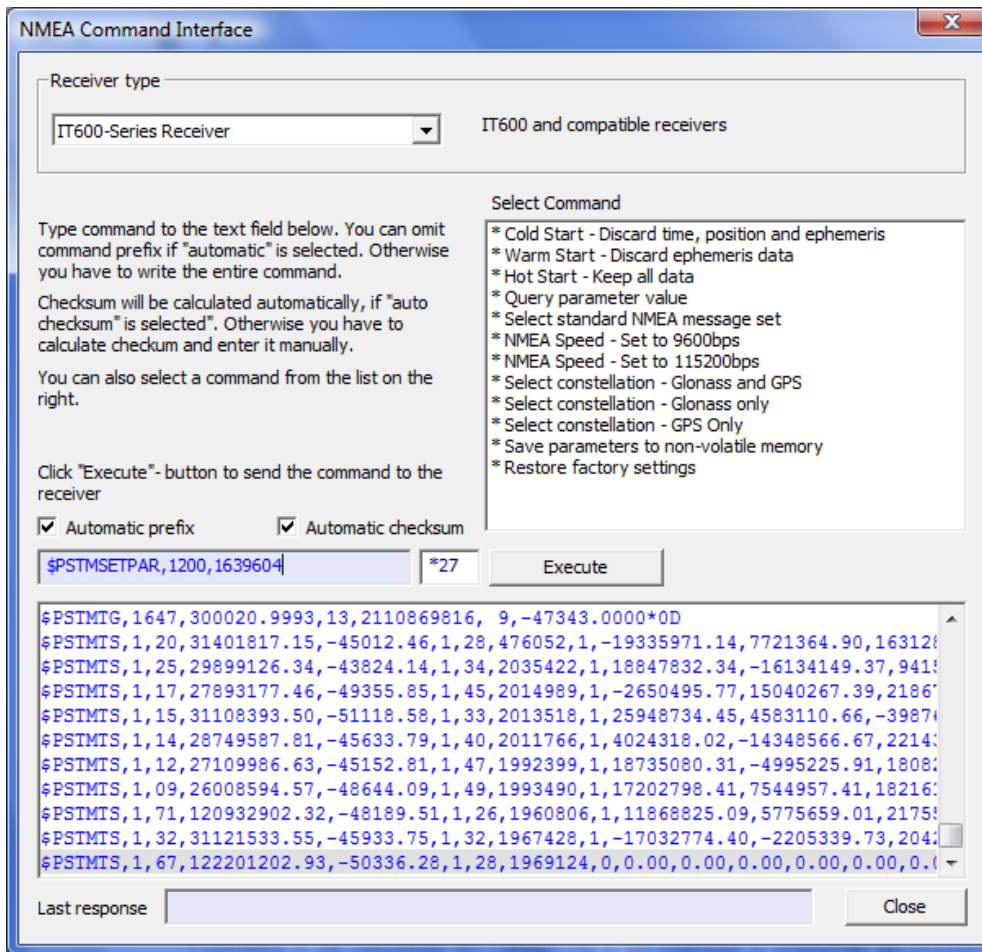


Figure 2 GPS WorkBench 4 NMEA Command Interface

NOTE

Modifying a wrong parameter or value intentionally or unintentionally may stop the system from working and/or degrade the system performance.

4 Connectivity

4.1 Pin Assignments

The I/O signals are available as soldering (castellated) pads on the bottom side of the module. These pads are also used to attach the module on the motherboard. All I/O signal levels are 3.3V CMOS compatible and inputs are 3.6V tolerable except XRESET, XSTANDBY and WAKEUP signals which are in the internal 1.2V domain.

All unconnected I/O signals can be left floating when not used, unless instructed to use external pull up/down resistor. Signals 37... 42 (TCK, TRSTN, TDO, TDI, TMS, GND) are available under the module as LGA pads for JTAG interface, which is used for firmware development and debugging purposes. The JTAG signals are suggested to be left unconnected for production devices.

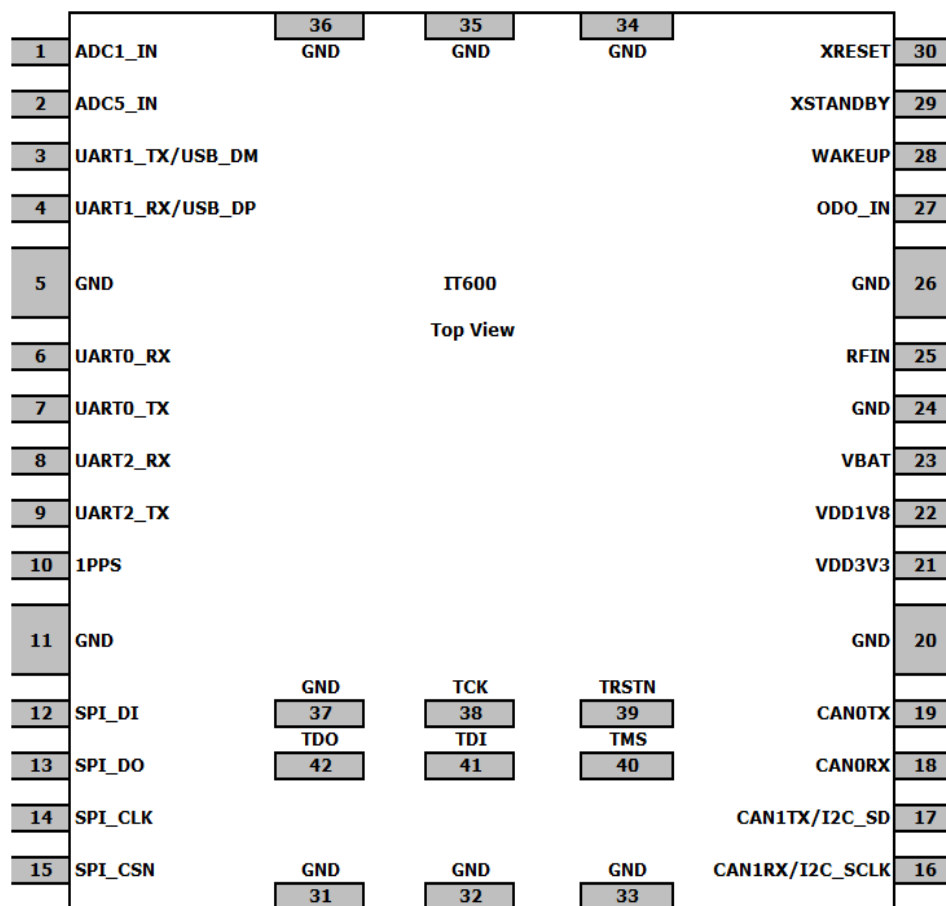


Figure 3 Pin-out

4.2 Signal Description

Table 2 Signal Description

Pin	Signal name	I/O type NAV RUN	I/O type Backup	I/O type Reset	Signal description
1	ADC1_IN	A,I			ADC input 1. Signal level 0...+1.4V
2	ADC5_IN	A,I			ADC input 5. Signal level 0...+1.4V
3	UART1_TX /USB_DM	C,B			UART1 transmit or USB DataM
4	UART1_RX /USB_DP	C,B			UART1 receive or USB DataP
5	GND	G	G	G	Ground
6	UART0_RX	C,B			UART0 receive or GPIO(P1.6)
7	UART0_TX	C,B,PU		C,B,PU	UART0 transmit or GPIO(P1.7). BOOT1 @ Reset Internal 10 kohm pull-up
8	UART2_RX	C,B			UART2 receive or GPIO(P1.4)
9	UART2_TX	C,B,PU		C,B,PU	UART2 transmit or GPIO(P1.5) BOOT0 @ Reset Internal 10 kohm pull-up
10	1PPS	C,O			1PPS Output
11	GND	G	G	G	Ground
12	SPI_DI	C,B			SPI Data Input or GPIO(P1.2)
13	SPI_DO	C,B			SPI Data Output or GPIO(P1.3)
14	SPI_CLK	C,B			SPI Clock or GPIO(P1.1)
15	SPI_CSN	C,B,PU			SPI Chip Select or GPIO(P1.0) 10 kohm internal pull-up
16	CAN1RX/ I2C_SCLK	C,B			CAN1 Receive, I2C serial clock or GPIO(P0.9)
17	CAN1TX/ I2C_SD	C,B			CAN1 Transmit, I2C serial data or GPIO(P0.8)
18	CAN0RX	C,I			CAN0 Receive
19	CAN0TX	C,O			CAN0 Transmit
20	GND	G	G	G	Ground
21	VDD3V3	P,I		P,I	RF & I/O Power supply, 3.3 V nom.
22	VDD1V8	P,I		P,I	Core Supply, 1.8 V nom. Use externally a 10 ms Power On Delay after VDD3V3 has been applied.

Pin	Signal name	I/O type NAV RUN	I/O type Backup	I/O type Reset	Signal description
23	VBAT	P,I	P,I	P,I	Battery backup input, 3 V nom.
24	GND	G	G	G	Ground
25	RFIN	A,I,P			RF Input, 50ohm. Antenna bias is provided internally (same as VDD3V3)
26	GND	G	G	G	Ground
27	ODO_IN	C,B			Odometer Input or GPIO(P0.17)
28	WAKEUP	C,I,PD			<p>Wakeup input, active high. Internal 10 kohm pull-down.</p> <p>An external control signal can toggle this pin to high state to wake up the receiver from Standby mode.</p> <p>Can be left unconnected when not used.</p> <p>Note 0... +1.2V signal levels.</p>
29	XSTANDBY	OC,I,PU			<p>Standby input, active low.</p> <p>Internal 100 kohm pull-up to internal digital 1.2 V + 47 nF delay capacitor.</p> <p>An external control signal (Open Collector) can drive this pin to GND to force the module to Standby mode.</p> <p>Can be left unconnected when not used.</p> <p>Note 0... +1.2V signal levels with Open Collector drive.</p>
30	XRESET	OC,I,PU, H		OC,I,PU, H	<p>External reset input, active low.</p> <p>Internal 100 kohm pull-up to internal VBAT(1.2 V) + 2.2 uF delay capacitor.</p> <p>An external control signal (Open Collector) can drive this pin to GND to force the module to Reset state. Note that the input is 1.2 V CMOS level compatible.</p> <p>Can be left unconnected when not used.</p> <p>Note 0... +1.2 V signal levels with Open Collector drive.</p>
31	GND	G	G	G	Ground
32	GND	G	G	G	Ground
33	GND	G	G	G	Ground
34	GND	G	G	G	Ground
35	GND	G	G	G	Ground

Pin	Signal name	I/O type NAV RUN	I/O type Backup	I/O type Reset	Signal description
36	GND	G	G	G	Ground
37	GND	G	G	G	Ground
38	TCK	C,I,PD		C,I,PD	JTAG TCK signal only for FW development purposes. Internal 10 kohm pull-down. Can be left unconnected when not used.
39	TRSTN	C,I,PU		C,I,PU	JTAG TRSTN signal only for FW development purposes . Internal 10 kohm pull-up. Can be left unconnected when not used.
40	TMS	C,I,PU		C,I,PU	JTAG TMS signal only for FW development purposes . Internal 10 kohm pull-up. Can be left unconnected when not used.
41	TDI	C,I,PU		C,I,PU	JTAG TDI signal only for FW development purposes . Internal 10 kohm pull-up. Can be left unconnected when not used.
42	TDO	C,O		C,O	JTAG TDO signal only for FW development purposes . Can be left unconnected when not used.

Legend: A=Analogue, B=Bi-directional, C=CMOS, OC=Open Collector, G=Ground, H=Hysteresis, HZ=High Impedance, I=Input, O=Output, P=Power, PU=Internal Pull-up, PD=Internal Pull-down. Note that with Bi-directional I/O the firmware has control for input vs. output I/O type depending on the firmware function.

4.3 Supply inputs

The IT600 module has 3 supply inputs: VDD3V3 (3.3V nom.) for RF and I/O, VDD1V8 (1.8V nom.) for Digital and VBAT (3V nom.) for Battery backup RAM & RTC. Normally these supply inputs shall be powered up at the same time and in this condition the IT600 handles Power On Reset (POR) internally driven from VBAT supply. In case VBAT is powered first, e.g. when installing the backup battery for the first time, the successive power up of VDD3V3 and VDD1V8 must be followed by reset condition controlled by host at XRESET signal.

The VBAT backup supply can then be left active all the time and consequent power up is achieved by delaying VDD1V8 supply by 10 ms after VDD3V3 is powered up. The reference circuit diagrams at the end of this document show an example of how a delay for VDD1V8 is generated.

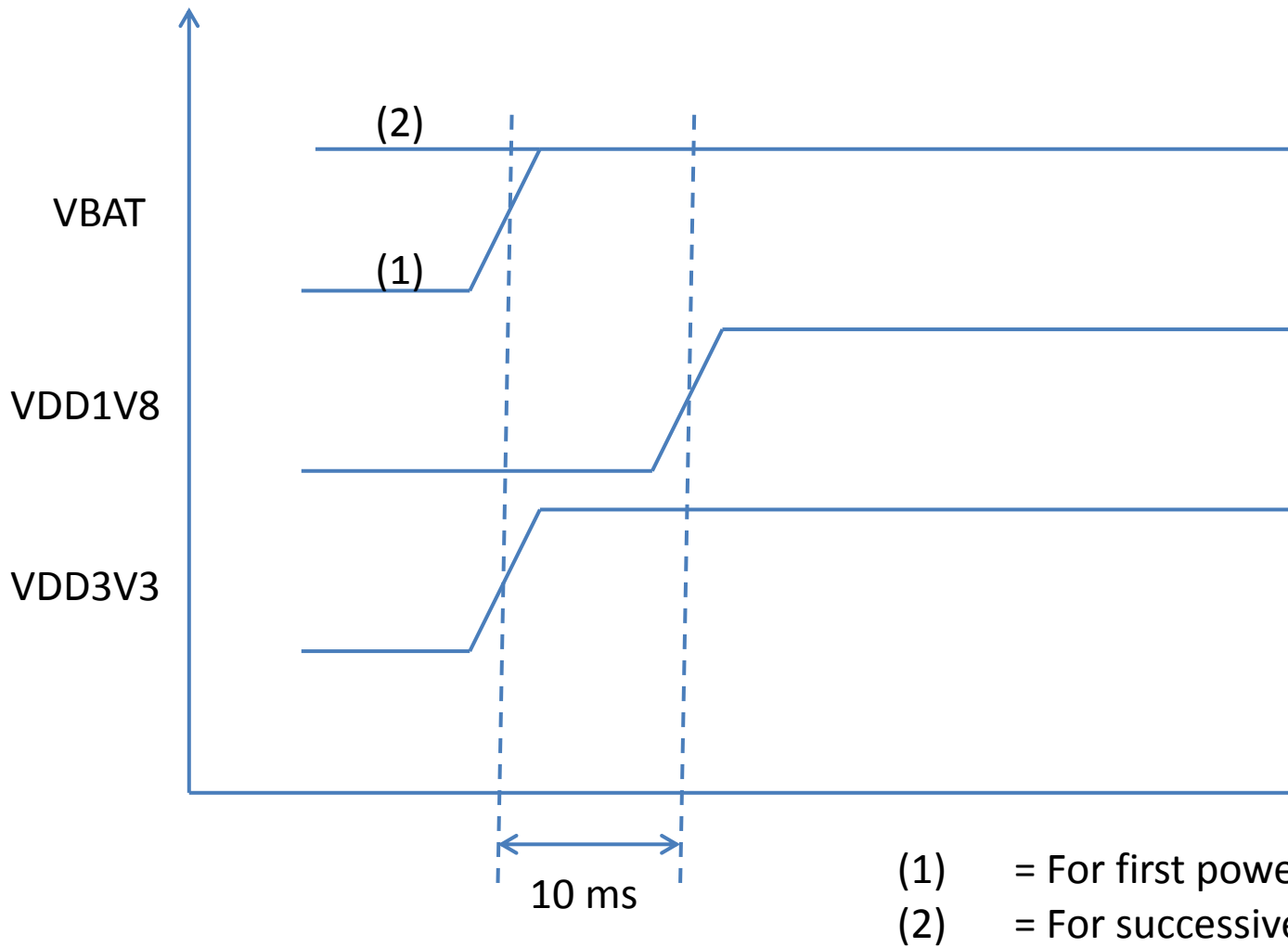


Figure 4 Power supply timing

Abrupt power removal is allowed since internal SQI flash uses double buffering for code and data.

NOTE

Use an externally generated delay 10ms at VDD1V8 supply after VDD3V3 is powered up.

4.4 Boot Mode Configuration (UART2_TX and UART0_TX)

User can select the boot mode configuration between UART2 (programming flash memory) and internal SQI Flash during power up. IT600 has internal pull-up resistors in both lines so if the pins are left unconnected then IT600 will boot from internal SQI Flash for Navigation operation mode.

In case the firmware needs to be upgraded then UART2_TX can be driven low at power-up; these boot mode signals are latched at rising edge at the release of a Reset state (XRESET signal low to high transition). Keep the boot configuration valid at least 50ms after Reset state is released; UART0_TX needs to be pulled to high state at power-up in either case.

Table 3 Boot Mode Configuration

Boot Mode	UART0_TX (Internal 10kohm PU)	UART2_TX (Internal 10 kohm PU)
UART	High	Low
SQI Flash (default)	High	High
Reserved	Low	Low
Reserved	Low	High

NOTE

When used UART2_TX requires Open Collector drive from host in order to allow normal UART operation after reset.

4.5 Reset Input

The XRESET (active low) signal provides external override of the internally generated Power On Reset (POR), which is generated internally when VBAT is applied. When VBAT is applied first to the module before other supply inputs, the host must force Reset state via pulling XRESET signal to low state when VDD1V8 and VDD3V3 power are applied; release the XRESET signal about 50ms after VDD1V8 power up.

When XRESET is used, the driving source must have an Open Collector output in order to allow internally generated RC-delay to be formed properly. The XRESET signal is internally pulled up to internal VBAT(1.2V) by 100 kohm/2.2 uF RC-network and it also has Schmitt-Trigger characteristics with hysteresis.

NOTE

When used XRESET input requires Open Collector drive from host.

4.6 XSTANDBY Input

XSTANDBY input is active low and the LOW level input is used to force the module from Navigation mode to the Standby mode. The input has internal 10 kohm pull-up to internal digital 1.2 V and a 47 nF delay capacitor; the input can be left unconnected when not used.

An external control signal (Open Collector) can drive this pin to GND to force the module to Standby mode. Typical delay in transition from Navigation mode to Standby mode is 0.5 ms. Exit from Standby mode is done by relaxing XSTANDBY input to HIGH state.

Note that the signal has 0... +1.2V signal levels with Open Collector drive requirement.

NOTE

When used XSTANDBY input requires Open Collector drive from host.

4.7 WAKEUP Input

WAKEUP input is active high and the HIGH level input is used to wake up firmware operation from Standby mode to Navigation mode. The input has internal 10 kohm pull-down to GND; the input can be left unconnected when not used.

Normally the Standby mode is controlled by the host via the XSTANDBY signal and WAKEUP usage is reserved for the case when Standby mode has been entered by a SW command (TBD).

4.8 Host port configuration

The default host port configuration is UART (ports 0 and 2). Other host port configurations (CAN, USB, SPI, I²C) are not yet supported. UART ports can be configured by \$PSTMSETPAR command.

4.9 ADC

There are two muxed 10-bit Analog-to-Digital Converter (ADC) inputs, ADC1 and ADC5. Conversion range is 0... +1.4 V at 500ksps. The usage of ADC is limited for custom firmware.

4.10 JTAG Interface

The JTAG interface is available for test/emulation purposes with custom firmware as test points at the bottom of the module. For normal usage these signals shall be left unconnected (floating).

4.11 Antenna Input

The module supports passive and active antennas. The antenna input RFIN impedance is 50 ohms and it provides also a bias supply low-pass filtered from VDD3V3 supply; note that the internal switching transistor has typical drop-out voltage 0.15 V @ 15 mA load current.

Antenna bias voltage is switched off internally during Standby mode and during Backup state. The antenna bias current is limited to about 60 mA (typ.) during RFIN short circuit condition and the module can withstand short circuited RFIN only for short periods, a few seconds typ.

NOTE

Antenna input can withstand antenna bias short circuit condition only for a few seconds; internal switch abs. max. dissipation is 150 mW. When needed a more robust antenna bias current limiting must be handled externally.

For combined GNSS usage it is suggested that the antenna covers both L1 GPS/Galileo and Glonass bands with good RHCP Axial Ratio ($AR \leq 3$ dB typ.), i.e. 1573.4... 1577.4 MHz & 1598... 1606 MHz.

The RF input signal path contains first a SAW band-pass filter, which provides good out-of-band protection against GPS blocking caused by possible near-by wireless transmitters. Note that the antenna input is ESD sensitive; when needed use external transient voltage suppressors at RFIN.

NOTE

Note that module is Electrostatic Sensitive Device (ESD), rating 50V max (Machine Model) at RFIN.

**4.11.1 Active GPS antenna**

The customer may use an external active GPS antenna when antenna cable loss exceeds > 1dB. It is suggested the active antenna has a net gain *including cable loss* in the range from +10 dB to +25 dB. Specified sensitivity is measured with external low noise ($NF \leq 1\text{dB}$, $G \geq 15\text{dB}$) amplifier, which gives about 3dB advantage in sensitivity when compared to a passive antenna.

4.12 1PPS output

The 1PPS output signal provides pulse-per-second signal for timing purposes. Pulse length (high state) is by default 500 m and it has 20 ns typ. jitter (Standard Deviation) typ. and it is synchronized at rising edge to full UTC second at 1 μs accuracy. 1PPS pulse length, polarity and external delay are configurable by \$PSTMSETPAR command; parameter ID 301 and 302.

Note that prior valid fix and after loss of valid fix the 1PPS outputs free-wheel timing estimate, which may have large offsets to full UTC second; thus use timing pulse only during a valid fix.

4.13 Mechanical Dimensions

General tolerance of dimensions is +/- 0.3 mm.

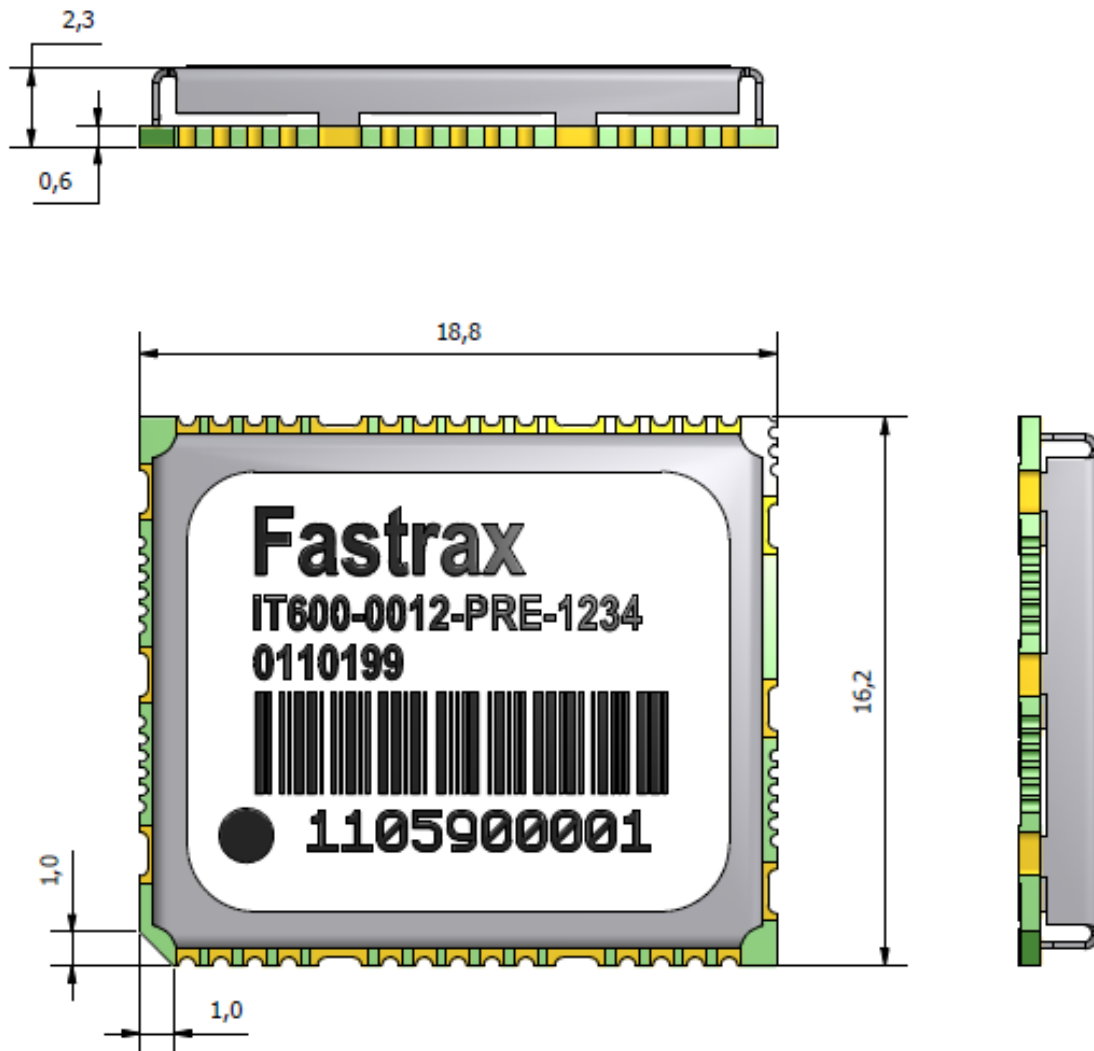


Figure 5 Mechanical Dimensions

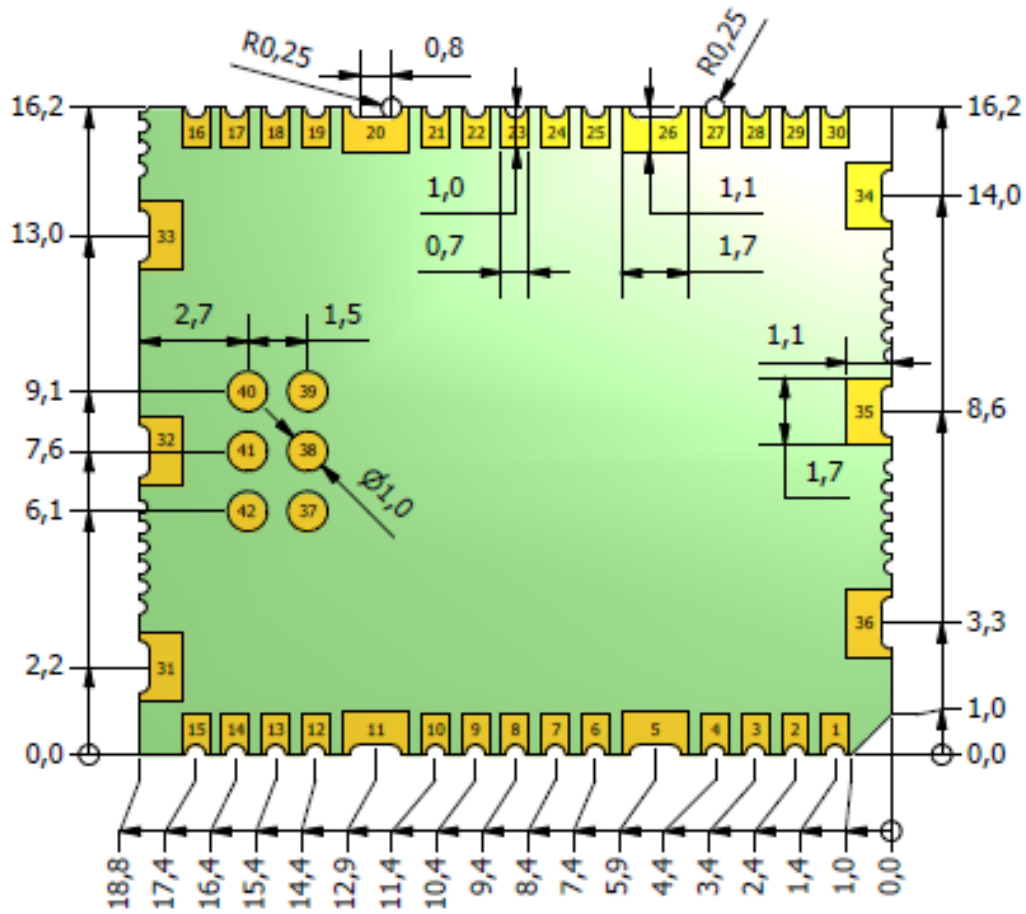


Figure 6 I/O Pad numbering and dimensions, Bottom View

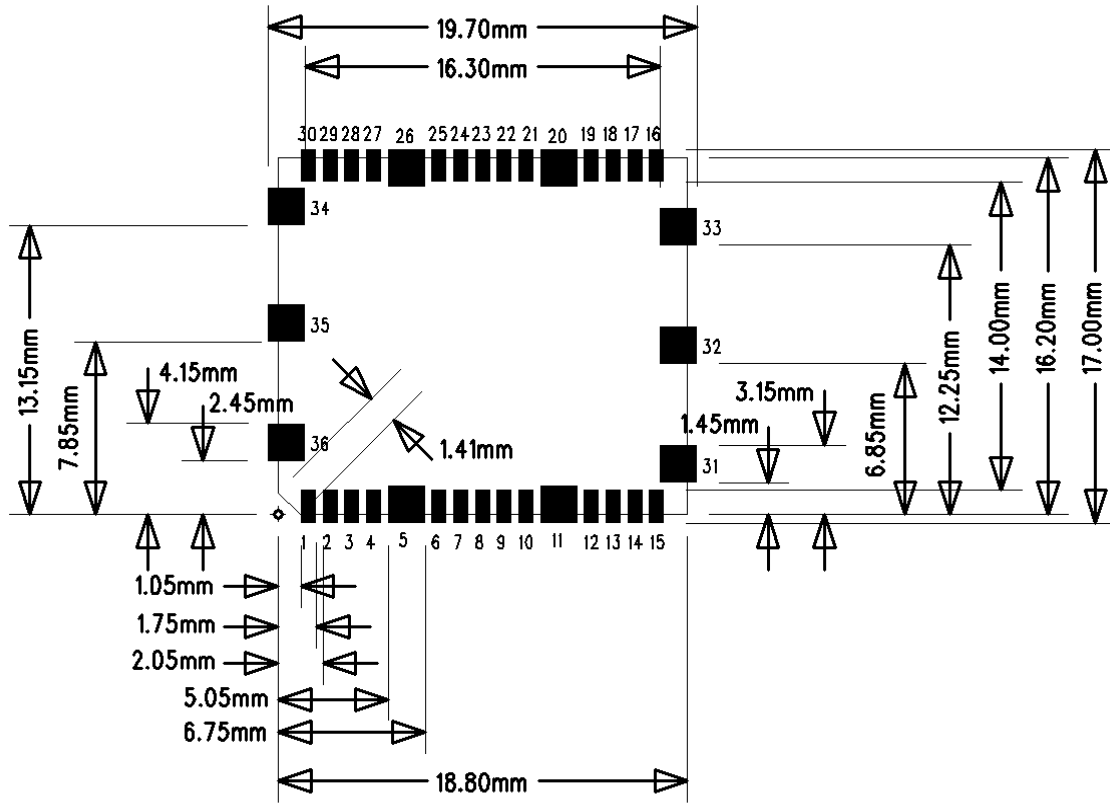


Figure 7 Suggested pad layout and occupied area, Top view. Suggested paste mask openings equal pad layout

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{AMB}	Operating and storage temperature	-40	+85	°C
VDD3V3	Supply voltage input	-0.3	+3.63	V
VDD1V8	Supply voltage input	-0.3	+1.98	V
VBAT	Supply voltage input	-0.3	+3.6	V
V_{IO}	Input voltage on any input connection @ 3.3V levels	-0.3	+3.63	V
$V_{IO,1V2}$	Input voltage on any input connection @ 1.2V levels	-0.3	+1.50	V
$V_{IO}(ESD)$	I/O ESD voltage (excluding RFIN, HBM model)	-1000	+1000	V
$V_{RFIN}(ESD)$	RFIN ESD voltage, Machine model	-50	+50	V
P_{RF}	RF_IN input power (in band 1575 +/- 30 MHz)	-	-60	dBm
P_{RF}	RF_IN input power (out of band <1460 MHz or >1710 MHz)	-	+15	dBm
$P_{DISS(RFIN)}$	Antenna bias switch dissipation		150	mW

NOTE

Note that module is Electrostatic Sensitive Device (ESD), rating 50V max (Machine Model) at RFIN.



5.2 DC Electrical Specifications

The following table describes DC electrical characteristics in GPS + Glonass Navigation mode.

Table 5 DC electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T _{AMB}	Operating Temperature	-40 [1]		+85	°C
VDD3V3	Supply voltage input, RF & I/O	+3.0	+3.3	+3.60	V
VDD1V8	Supply voltage input, Core	+1.71	+1.8	+1.89	V
VBAT	Supply voltage input, Backup	+1.62	+3.0	+3.60	V
I _{VDD1V8}	Supply current, peak acq.		82		mA
I _{VDD1V8}	Supply current average, tracking		74		mA
I _{VDD3V3}	Supply current average, Navigation mode		31		mA
I _{VBAT}	Supply current, Navigation mode		630		µA
I _{VDD1V8}	Supply current, Standby mode		160		µA
I _{VDD3V3}	Supply current, Standby mode		0.9		mA
I _{VBAT}	Supply current, Standby & Backup state		65		µA
I _{I(LEAK)}	Leakage current, Digital Input	-TBD		+TBD	µA
V _{OL}	Low level output voltage, I _{OL} 2 mA			+0.4	V
V _{OH}	High level output voltage, I _{OH} 2 mA	VDD3V3 - 0.4			V
V _{IL}	Low level input voltage	-0.3		+0.8	V
V _{IH}	High level input voltage	+2.0		VDD3V3 +0.3	V
V _{IL,1V2}	Low level input voltage @ 1.2V inputs	-0.3		+0.48	V
V _{IH,1V2}	High level input voltage @ 1.2V inputs	+0.84		+1.5	V
V _{RFIN}	Antenna bias supply @ I _{RFIN} 15 mA		VDD3V3 - 0.15		V
V _{REF}	ADC reference voltage	+1.35	+1.40	+1.45	V
V _{ADC_IN}	ADC conversion range	0		V _{REF}	V
R _{ADC_IN}	ADC input resistance	1.5	2.0	2.5	kohm
C _{IN}	I/O input capacitance, excluding RFIN		7.0		pF

Note 1: In temperature range -40... -30°C GNSS performance, e.g. TTFF may degrade

5.3 AC Electrical characteristics

Operating conditions are T_{AMB} =+25°C and nominal supply voltages unless stated otherwise.

Table 1 AC Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TM}	TM (PPS) cycle time		1		s
$t_{TM,H}$	TM, high state pulse duration		500		ms
Δt_{PPS}	TM accuracy, rising edge (<i>note 1</i>)	-1		+1	μ s

Note 1: with nominal GPS signal levels -130dBm.

6 Manufacturing

6.1 Assembly and Soldering

The IT600 module is intended for SMT assembly and soldering in a Pb-free reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume. If required paste mask pad openings can be increased to ensure proper soldering and solder wetting over pads.

Use pre-heating at 150... 180 °C for 60... 120 sec. Suggested peak reflow temperature is 235... 245°C (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260°C. For details see Fastrax document 'Soldering Profile', ref (4).

Note that module is Electrostatic Sensitive Device (ESD). Rated voltage is 50V max (Machine Model) at RF_IN signal.

Avoid also ultrasonic exposure due to internal crystal and SAW components.

The IT600 module meets the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). For details contact Fastrax support.

6.2 Moisture Sensitivity

IT600 module is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

Moisture barrier bag shelf life is 1 year; thus it is suggested to assemble modules prior shelf life expiration. If the moisture barrier bag shelf life is exceeded, the modules must be baked prior usage; contact Fastrax support for details.

6.3 Marking

Module marking includes type & batch code and serial number.

Type code is e.g. IT600-xxxr-FFF-yyyy (may vary), where

- **IT600** is module type code
- **xxx** is firmware (SDK) revision x.x.x and r is incremental firmware release revision (e.g. 719A, may vary)
- **FFF** is firmware configuration set (default ITX)
- **yyyy** is BOM (Bill-of-Materials) revision code (e.g. 4186, may vary)

Batch code is e.g. **100208** (may vary), where

- **1** is factory code
- **0** is last digit of the year (e.g. 20**10**)
- **02** is month (e.g. February)
- **08** is incremental number of the production batch during the month

Serial number is unique for each module having 10 digits including tester code, last two digits of the year, julian date-of-year and incremental number.



Figure 8 Module marking

6.4 Tape & Reel Specification

One reel contains 500 modules.

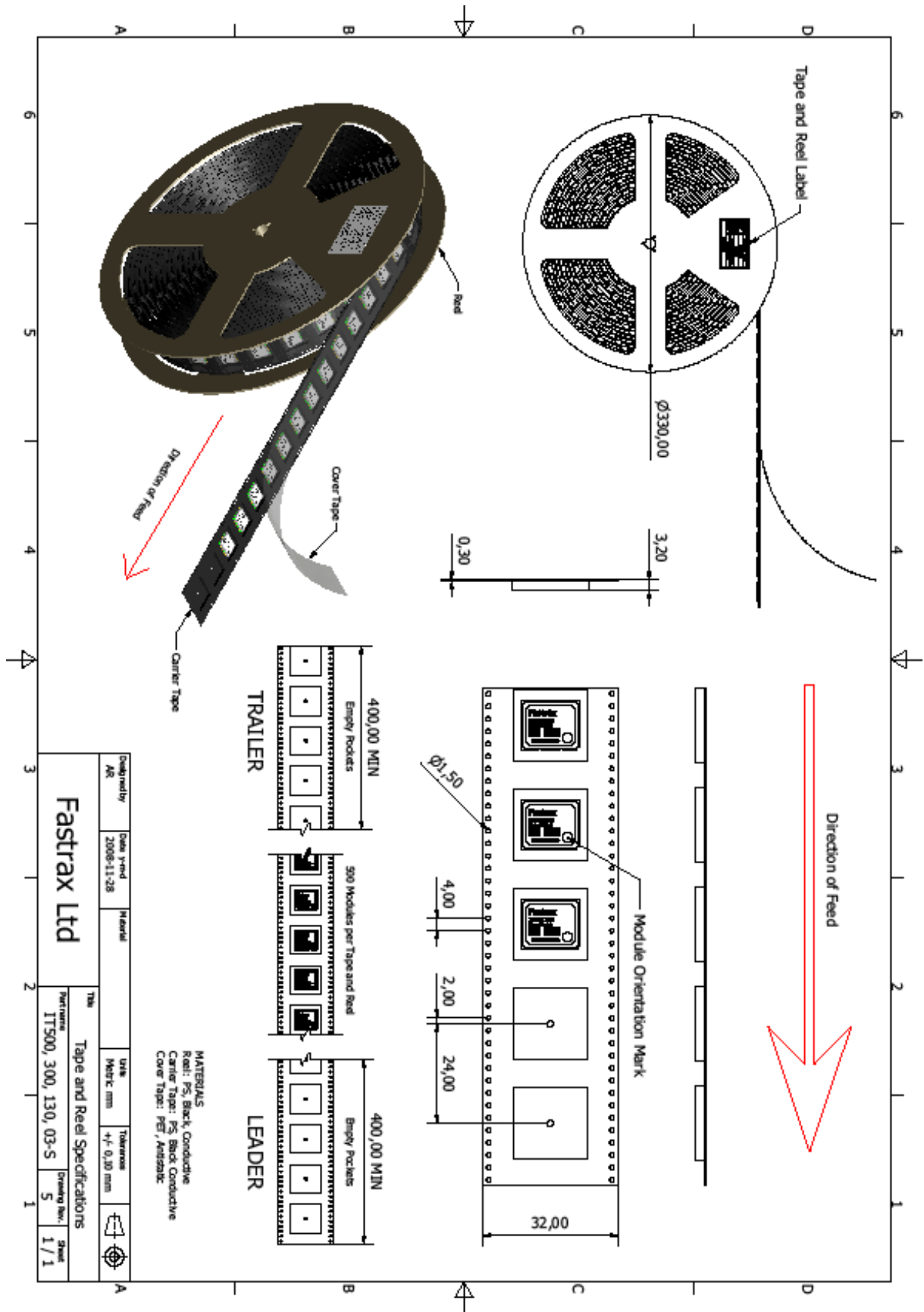


Figure 9 Tape & Reel

7 Reference Design

The idea of the reference design is to give a guideline for the applications using the OEM GNSS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing the GPS receiver in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

7.1 Reference Circuit Diagram

The following picture shows a typical power supply connection for IT600 assuming 3.3V supply from host.

For basic GNSS standalone applications the module needs just three power supplies, RFIN and UART2 port for NMEA data. However, since IT600 is very versatile in terms of functionality and external interfaces and these auxiliary connections can be referenced to AP600 Application Board for IT600.

Note that all I/O signal levels are CMOS 3.3V compatible and inputs are 3.6 V tolerable except for XSTANDBY, XRESET and WAKEUP that are 1.2V CMOS compatible. When used BOOT control, XRESET and XSTANDBY signals require also an open collector driving source from host.

Some I/O signals have series resistors (100... 220 ohm), which are intended for RF-decoupling purposes to improve rejection to internally generated EMI that may couple to nearby GPS antenna. If GPS antenna is away > 10cm from module and/or I/O signals are routed under the ground plane these series resistor may be omitted.

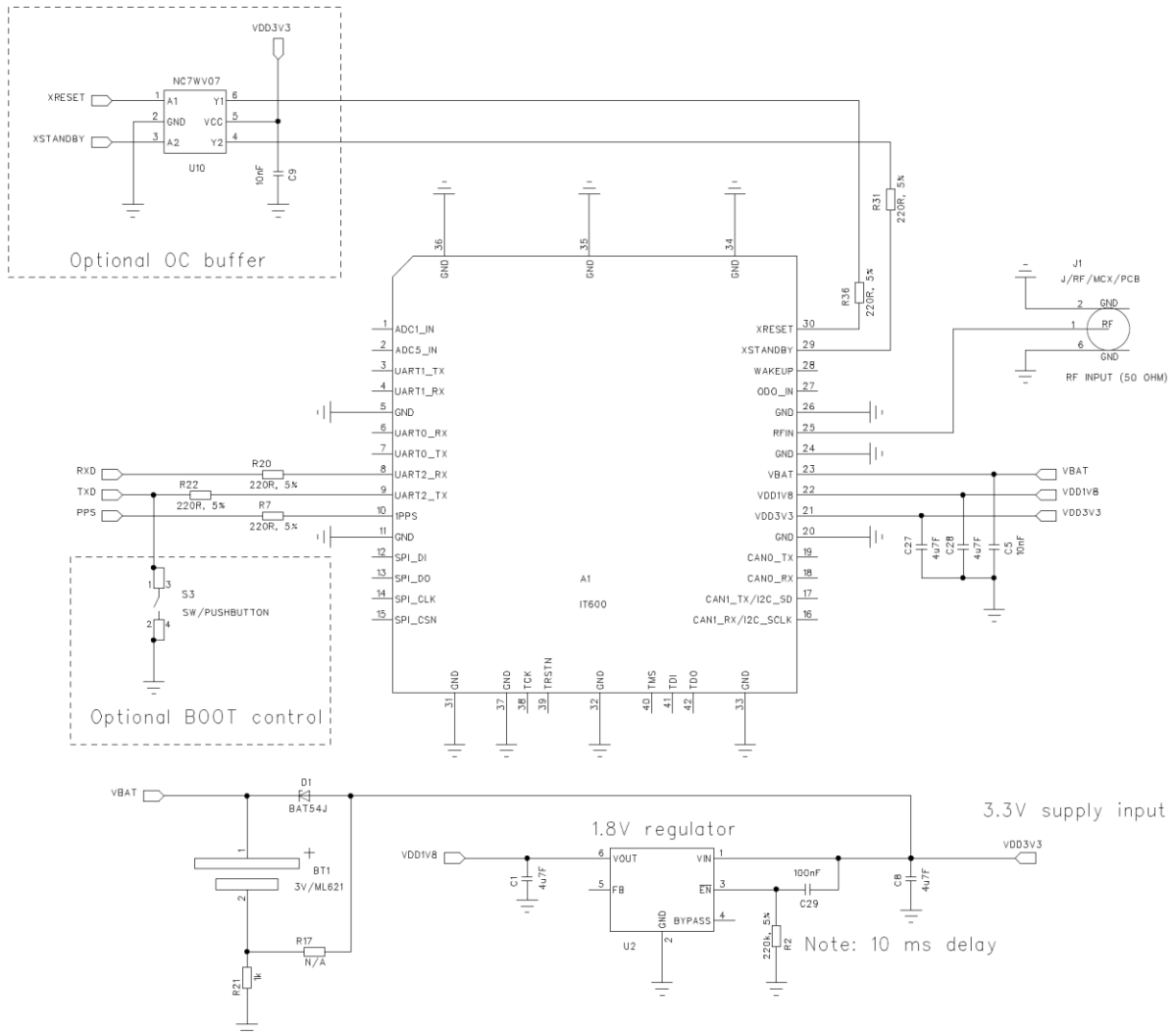


Figure 10 IT600 reference circuit diagram

7.2 PCB Layout Issues

The suggested 4-layer PCB build up is presented in the following table.

Table 2. Suggested PCB build up.

Layer	Description
1	Signal + Ground with copper keep-out below IT600
2	Ground plane
3	Signal + Ground or VDD plane
4	Signal (short traces) + Ground

Routing signals on top layer directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT600 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should placed very near to the IT600 module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C4 and C5 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT600 to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes for each GND pad.

The RF input should be routed clearly away from other signals. This minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

8 AP600 Application Board

AP600 provides access to all IT600 GNSS receiver interfaces. AP600 is also a reference design for using IT600. It plugs into Fastrax Fastrax Mini Evkit frame. The two main UART ports are available on the Mini Evkit, the third UART is available either on the USB connector (as USB), or on the pin-header as serial port. Reset button is also available on the Mini Evkit whereas AP600 contains the other control buttons (Boot, Standby and Wakeup).

Software development is supported through the JTAG connector. Lauterbach In-Circuit Emulator and ARM Realview 3.1 compiler are supported. GNU compiler support will be available later during 2011.

AP600 contains a versatile set of MEMS sensors. All MEMS sensors and an E2PROM are accessed through I2C bus. The user can develop custom sensor libraries and algorithms with the SDK. Standard firmware supports 3-axis digital gyro and odometer signals for DR. Later on DWP information from CAN interface will also be supported for DR. AP600 contains a CAN driver for the physical interface. I2C and SPI signals are available at connectors also for connecting external devices.

The following physical interfaces are available on the AP600:

- J1: Active GNSS antenna input
- J2: 40-pin Mini Evkit connector
- J3: VDD3V3 supply header
- J4: USB (UART1) connector
- J5: VDD1V8 supply header
- J6: VBAT supply header
- J7: JTAG connector
- J8: CAN interface
- J9: SPI interface connector
- J10: 2xADC and ODOMETER inputs
- J11: UART1 header
- J12: I2C signal header
- S3: WAKEUP button
- S4: STANDBY button

The main components are:

- M1: IT600 OEM Receiver
- U1: 3.0V regulator
- U2: 1.8V regulator
- U3: 3-axis Gyroscope
- U4: 3-axis Accelerometer
- U5: CAN driver
- U6: Pressure Sensor
- U7: E²PROM
- U8: 3-axis Magnetometer
- U9: Single gate inverter for Odometer input
- U10: Open collector buffer for XRESET and BOOT
- U11: 3-axis Accelerometer
- U12: 3-axis Gyroscope

Each of these are discussed in details later on in this document.

8.1 Physical Interfaces

J1 is a MCX connector for an active GNSS antenna. A bias voltage is provided from IT600 module. It the same as VDD3V3 input voltage, albeit filtered internally.

Pin headers J3, J5 and J6 are used for current consumption measurements of IT600 module. Note! J3 supplies only 3.0V to IT600, all other 3.0V circuitry on AP600 is not powered through J3.

J4 and J11 are used for UART1. In case firmware has configured UART Port 1 as USB then a USB compliant signal is available on J4. In case firmware has configured UART Port 1 as UART then UART signals are available on pin-header J11.

Optional J7 is used for JTAG. The 20-pin connector is compatible with Lauterbach ICE probes.

Optional J8 is for CAN interface. The signals on J8 are connected through an industry standard CAN driver IC to IT600.

Connector J9 carries the SPI interface pins. These SPI pins can also be configured in firmware as GPIO pins.

J10 is available for two ADC inputs and Odometer input. The external Odometer signal must be 0...12V level. The ADC inputs need to be in 0...1.4V range.

J12 can be used for monitoring the I2C signals. Additional I2C circuits can be connected to J12 also.

Push buttons S3, S4 along with XRESET and BOOT buttons (from Mini EvKit) are used for controlling various operating modes of IT600.

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the Fastrax Evaluation Kit pin header J4. I/O signal levels are CMOS 3.0V compatible unless stated otherwise.

Table 6 AP600 Application Board connectivity

Pin	Signal name (IT600)	I/O	Alternative GPIO name	Interface to Fastrax Evaluation Kit
1	UART2_TX	I/O	BOOT0/P1.5	TXD2_CON
2	GND	-	-	Ground
3	UART2_RX	I/O	P1.4	RXD2_CON
4	GND	-	-	Ground
5	UART0_TX	I/O	BOOT1/P1.7	TXD0_CON
6	GND	-	-	Ground
7	UART0_RX	I/O	P1.6	RXD0_CON
8	GND	-	-	Ground
9	VDD3V3	I	-	VDD_CON
10	GND	-	-	Ground
11	1PPS	O	-	1PPS signal output

12	GND	-	-	Ground
13	XRESET	I	-	Active low async. system reset
14	-	-	-	Not connected
15	-	-	-	Not connected
16	-	I	-	Not connected
17	GND	-	-	Ground
18	-	-	-	Not connected
19	-	-	-	Not connected
20	-	-	-	Not connected
21	GND	-	-	Ground
22	-	-	-	Not connected
23	-	-	-	Not connected
24	-	-	-	Not connected
25	GND	-	-	Ground
26	SPI_CSN	I/O	P1.0	UI indicator B
27	GND	-	-	Ground
28	-	-	-	Not connected
29	-	-	-	-
30	SPI_CLK	I/O	P1.1	UI indicator A
31	GND	-	-	Ground
32	-	-	-	-
33	GND	-	-	Ground
34	-	-	-	-
35	GND	-	-	Ground
36	-	-	-	-
37	GND	-	-	Ground
38	-	-	-	-
39	GND	-	-	Ground
40	-	-	-	-

8.2 Bill-of-Materials

DESIGNATOR	QTY	TECHNICALDESCRIPTION	VALUE
BT1	1	PANASONIC ML621/F9D, 3V 5mAh	3V/ML621
C1	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C2	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C3	1	Capacitor chip, 100nF 6.3V +-20% X5R 0402	100nF
C4	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C5	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C6	1	Capacitor chip, 27pF 50V 5% NPO 0402	27pF
C7	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C8	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C10	1	Capacitor tantal, 10uF 6.3V A 20% A	10uF/6V
C11	1	Capacitor chip, 470nF 6.3V +-10% X5R 0402	470nF
C12	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C13	1	Capacitor chip, 100nF 6.3V +-20% X5R 0402	100nF
C14	1	Capacitor tantal, 10uF 6.3V A 20% A	10uF/6V
C15	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C16	1	Capacitor chip, 100nF 6.3V +-20% X5R 0402	100nF
C17	1	Capacitor chip, 100nF 6.3V +-20% X5R 0402	100nF
C18	1	Capacitor chip, 470nF 6.3V +-10% X5R 0402	470nF
C19	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C20	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C21	1	Capacitor chip, 10nF 16V 10% X7R 0402	10nF
C22	1	Capacitor chip, 1uF 6.3V +-20% X5R 0402	1uF
C23	1	Capacitor chip, 470pF 16V 5% NPO 0402	470pF
C24	1	Capacitor chip, 470pF 16V 5% NPO 0402	470pF
C25	1	Capacitor chip, 100nF 6.3V +-20% X5R 0402	100nF
C26	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C27	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C28	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
C35	1	4,7uF 6,3V X5R 0805 +-20%	4u7F
D1	1	Diode 75V 225mA, BAT54J	BAT54J
D2	1	Diode 75V 225mA, BAT54J	BAT54J
J1	1	50 Ohm male MCX connector PCB	MCX/Straight PCB jack
J2	1	EDGE MOUNT SOCKET STRIP 40 PINS	2X20/EDGE
J3	1	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J4	1	USB connector, SMD with plastic pegs	Molex 67503-1020
J5	1	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J6	1	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J7	1	2x10 pin-header, straight, 2.54mm	2x10P2.54/1
J8	1	1x3 pin-header, straight, 2,54mm	1x3P2.54
J9	1	2x3 pin-header, straight, 2,54mm	2x3/2P54
J10	1	1x4 pin-header, straight, 2,54mm	1x4P2.54
J11	1	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
J12	1	1x2 pin-header, straight, pitch 2.54mm	1x2P2.54
M1	1	IT600 OEM GPS/Glonass Receiver Module	IT600A04
R1	1	Resistor chip, 4.7k 5% 0402 63mW	4.7k, 5%
R3	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R4	1	Resistor chip, 4.7k 5% 0402 63mW	4.7k, 5%
R5	1	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R6	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R7	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R8	1	Resistor chip, 100k 5% 0402 63mW	100k
R9	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R10	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R11	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R12	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R13	1	Resistor chip, 0R 0402	0R
R14	N/A	Resistor chip, 0R 0402	N/A
R15	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R16	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R17	N/A	Resistor chip, 27k 5% 0402 63mW	N/A
R18	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%

R19	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R20	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R21	1	Resistor chip, 1k 5% 0402 63mW	1k
R22	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R23	1	Resistor chip, 0R 0402	0R
R24	1	Resistor chip, 0R 0402	0R
R25	1	Resistor chip, 0R 0402	0R
R26	1	Resistor chip, 0R 0402	0R
R27	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R28	1	Resistor chip, 10k 5% 0402 63mW	10k, 5%
R29	1	Resistor chip, 33k 5% 0402 63mW	33k, 5%
R30	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R31	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R32	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R33	1	Resistor chip, 8.2k 5% 0402 63mW	8.2k, 5%
R34	1	Resistor chip, 100k 5% 0402 63mW	100k, 5%
R35	1	Resistor chip, 180K 5% 0402 63mW	180k, 5%
R36	1	Resistor chip, 220R 5% 0402 63mW	220R, 5%
R37	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R38	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R39	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R40	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R41	1	Resistor chip, 100R 5% 0402 63mW	100R, 5%
R42	1	Resistor chip, 0R 0402	0R
R43	1	Resistor chip, 0R 0402	0R
R44	1	Resistor chip, 15k 1% 0402 63mW	15k, 1%
R45	1	Resistor chip, 33k 1% 0402 63mW	33k 1%
R46	1	Resistor chip, 100k 5% 0402 63mW	100k, 5%
S1	1	Jumper, Pitch, 2.54mm, Black colour	Jumper
S2	1	Jumper, Pitch, 2.54mm, Black colour	Jumper
S3	1	Switch, SMD PUSH BUTTON	SW/PUSHBUTTON
S4	1	Switch, SMD PUSH BUTTON	SW/PUSHBUTTON
S6	1	Jumper, Pitch, 2.54mm, Black colour	Jumper
U1	1	Reg. 3V0, 150mA	3V0, 150mA
U2	1	REG. 1.8V	TPS79101
U3	1	3-Axis Gyro, ST	L3G4200D
U4	N/A	3-Axis Accelerometer, ST	LIS3DH
U5	N/A	SN65HVD231 Can transceiver with sleep mode	SN65HVD231
U6	N/A	Pressure Sensor, Bosch	BMP085
U7	N/A	EEPROM 1Mbit, 1.8-5.5V, I2C, SO8N	M24M01
U8	N/A	3-Axis Magnetometer, Aichi Steel	AMI304
U9	1	Single logic inverter, Schmitt trigger input	NC7SV14
U10	1	Open Collector Buffer	NC7WV07
U11	N/A	3-Axis Accelerometer, VTI	CMA3000
U12	N/A	3-Axis Gyro, VTI	CMR3000

Note that some of the components (mainly sensors) are not assembled on AP600. There is a custom variant called DB600 available also with all components assembled. DB600 is targeted for SDK use mainly.

8.3 AP600 circuit diagram

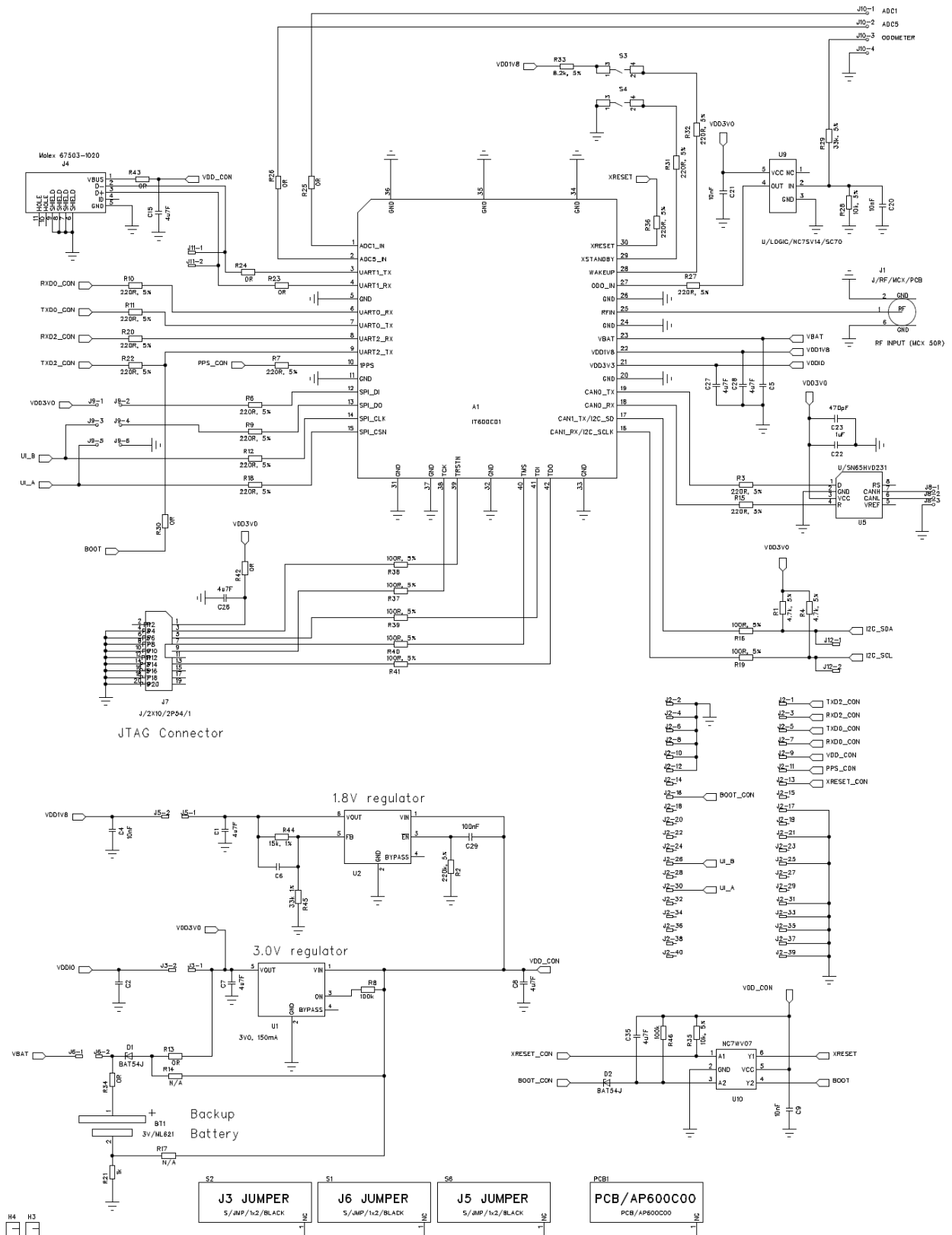


Figure 11 AP600 Circuit Drawing (1/2)

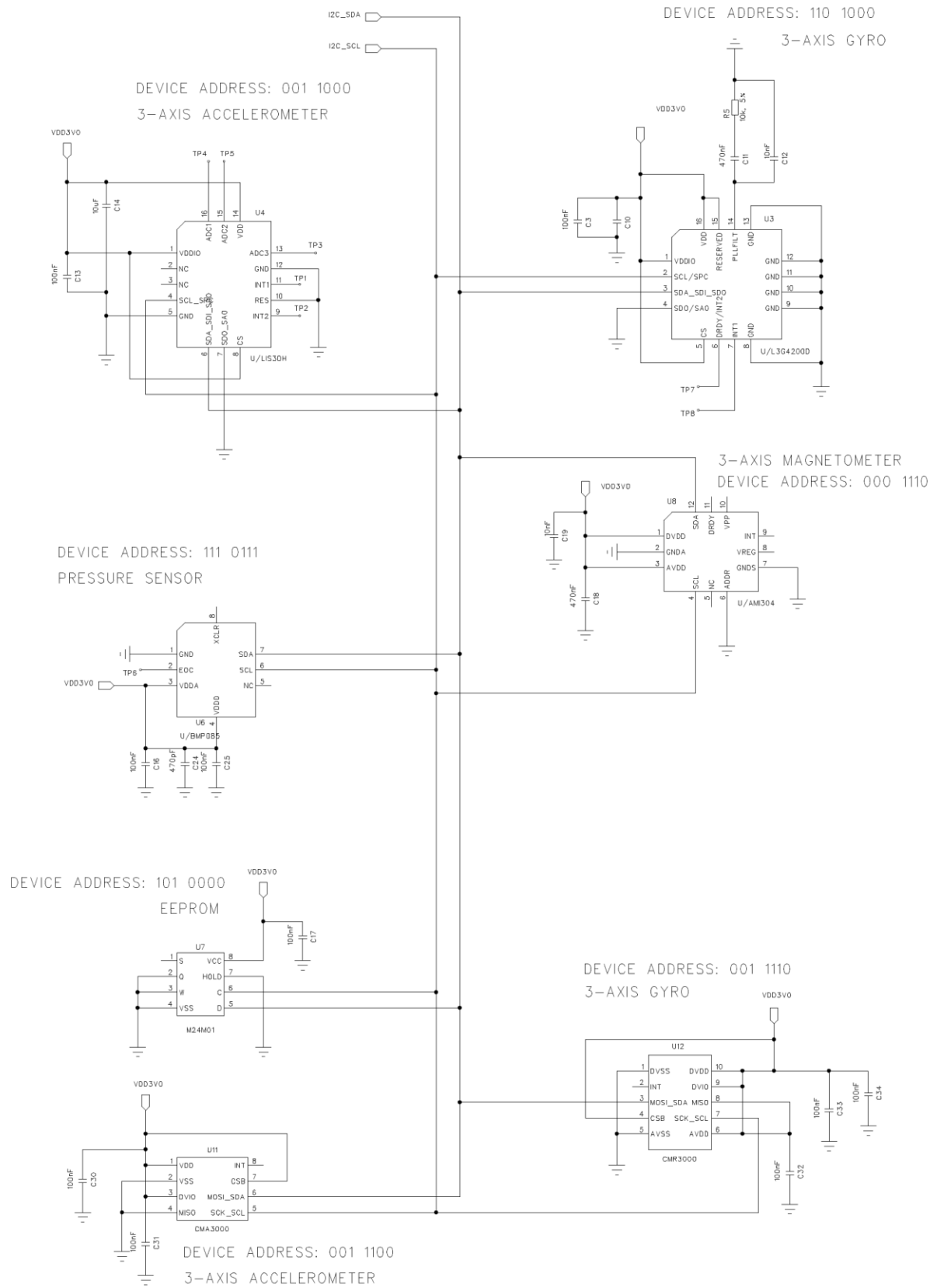
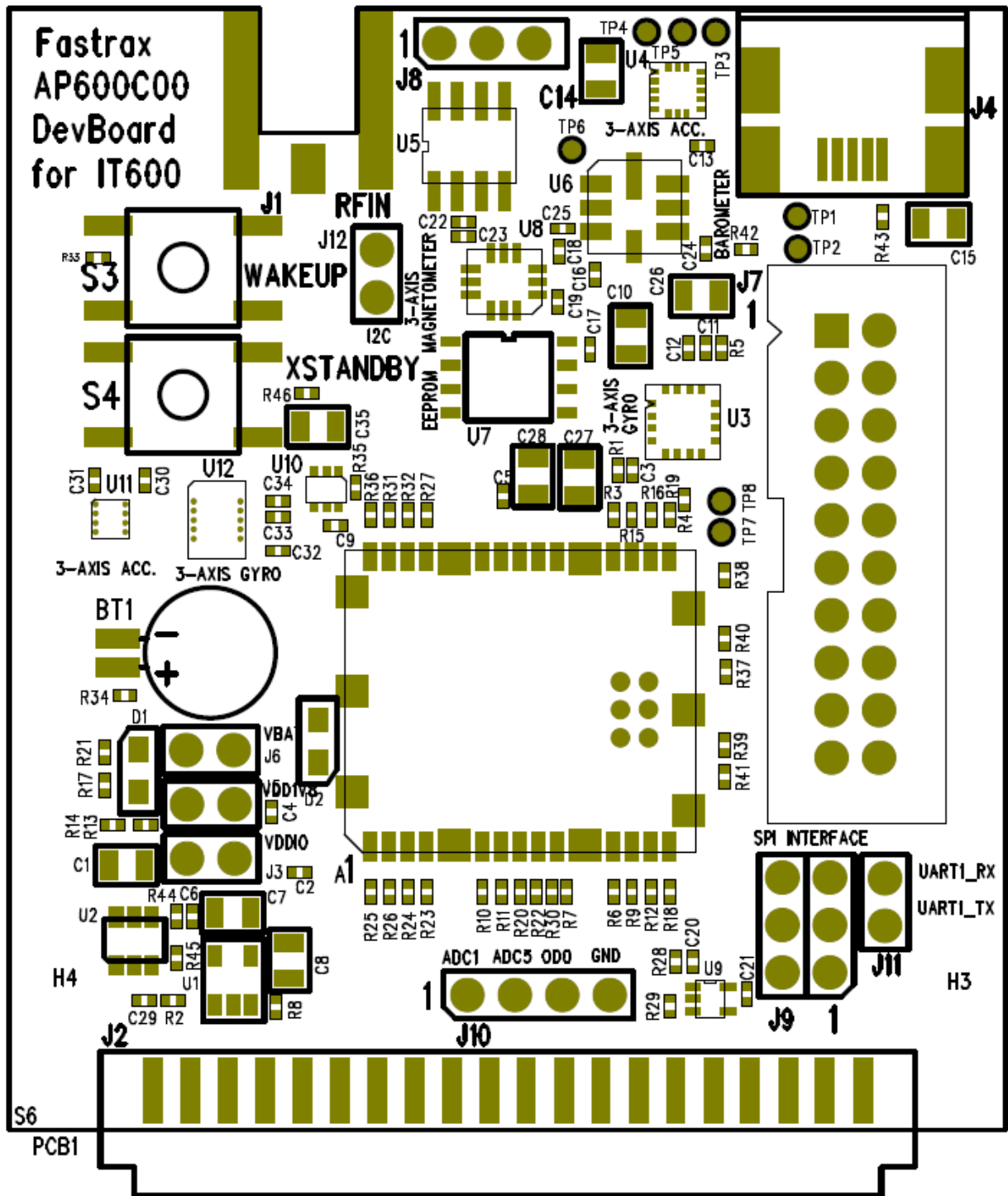
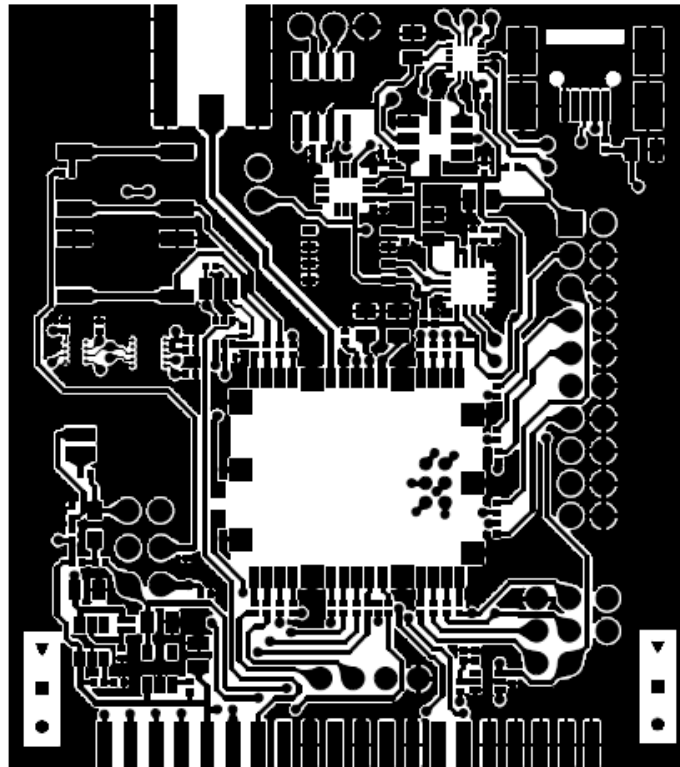


Figure 12 AP600 Circuit Drawing (2/2)

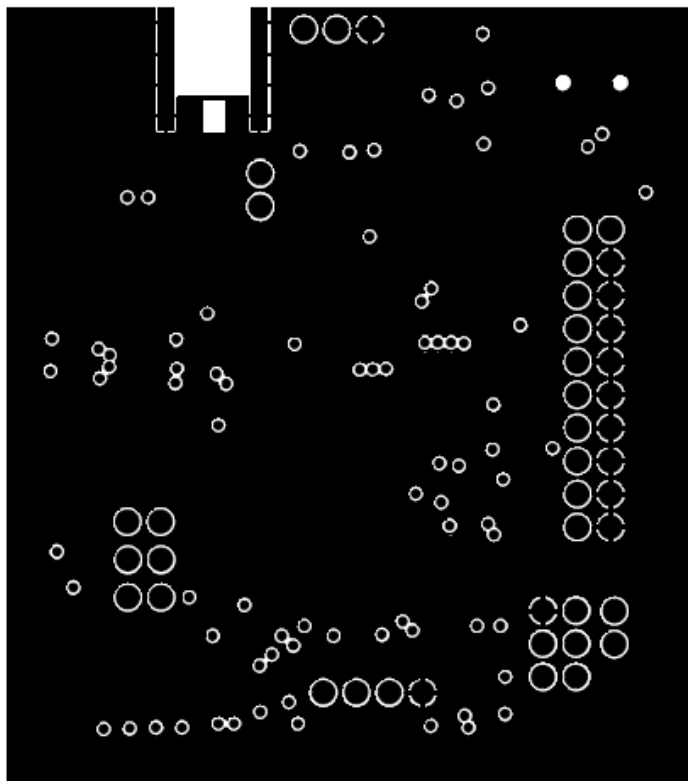
8.4 Assembly Drawing Top Side



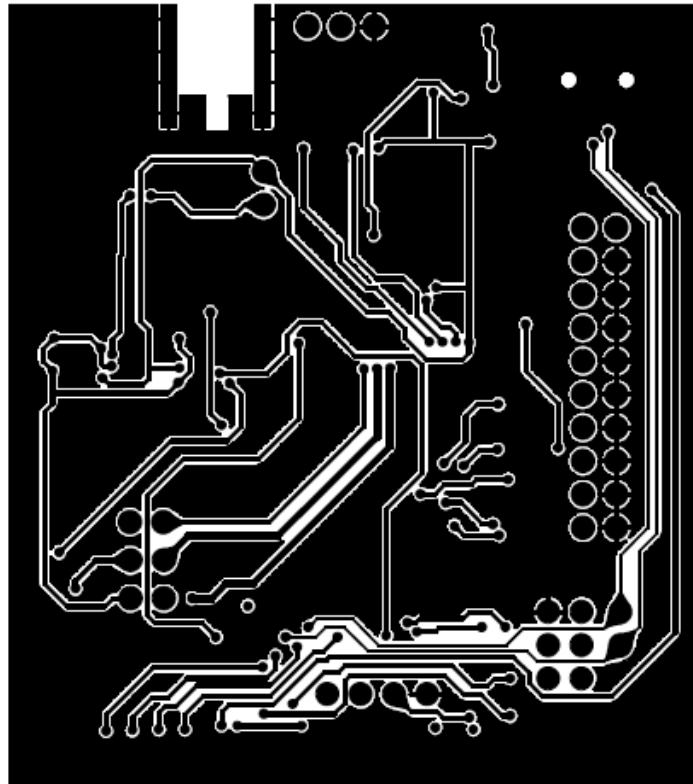
8.5 Artwork Layer 1 (Top)



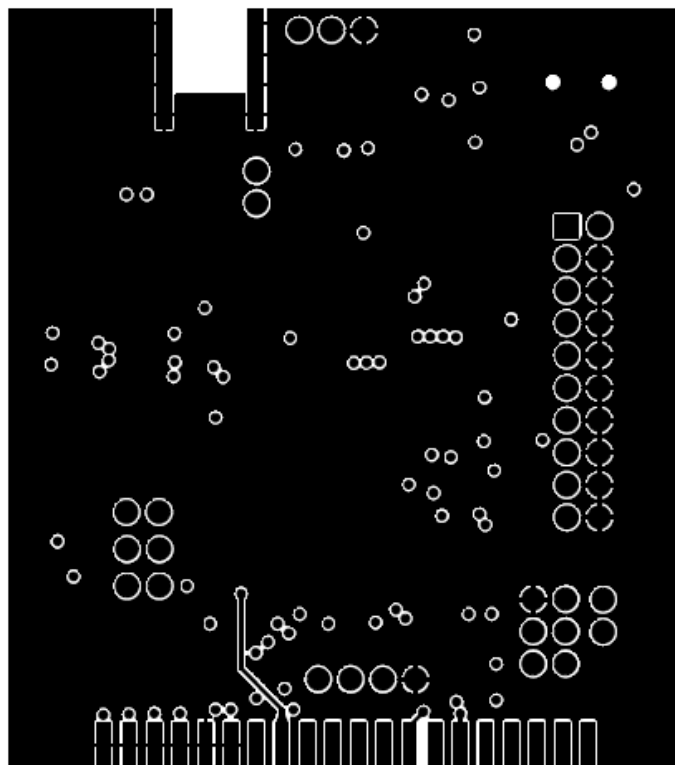
8.6 Artwork Layer 2



8.7 Artwork Layer 3



8.8 Artwork 4, Bottom Layer



9 Appendix A: Accuracy

Accuracy (RMS) (Note A)	
Operating on signals from GPS/GLONASS	
- Horizontal autonomous mode	3 m
- Height	5 m
- Velocities	0,05 m/s
Operating on signals from GLONASS	
- Horizontal autonomous mode	3 m
- Height	5 m
- Velocities	0,05 m/s
Operating on signals from GPS	
- Horizontal autonomous mode	3 m
- Height	5 m
- Velocities	0,05 m/s
Time (1PPS) (Note B)	1 μ s Time 1PPS (RMS)
Dynamic range of velocities	0 ... 515 m/s
Acceleration	5g
Altitude	18000 m

Note A: Limit allowed by the RMS of the random component of implementation error (at confidence probability 0,67) positioning in the absolute mode.

Note B: Limit allowed by the RMS of the random component of implementation error (at confidence probability 0,67) positioning in the absolute mode at operating on signals from GPS/ GLONASS based on UTC (US) time scale

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