Features

- matched to Infineon's PEB2096, PEB2196 & PEB2197 chipsets
- excellent and consistent balance between windings
- compact sizes in surface mount packages
- complies fully with all international standards for U-Interface
- manufactured in ISO-9001 approved Talema facility
- operating temberature -40° to +85°C

Electrical Specifications @ 25°C

Turns Ratio: **Bold** = IC Side Windings

Surface Mount U_{PO} Interface Transformer Modules
Complies with Basic Insulation Level EN60950, UL1950 and UL1459

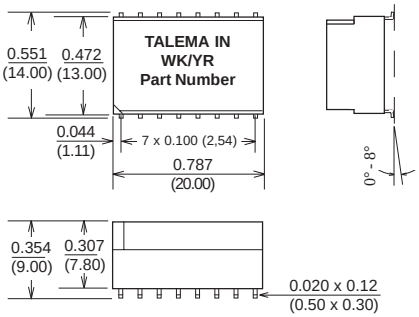
Part Number	Turns Ratio ±2%	L_P (mH min)	$\hat{}I_{DC}$ (mA)	L_L (µH)	C_C (pF Max)	DCR (Ohms per winding)		V_P (Vrms)	Schematic
						Pri	Sec		
UAJ-140C	1:1:**2:2**	1.7	75	5	150	0.8	1.6	1500	C

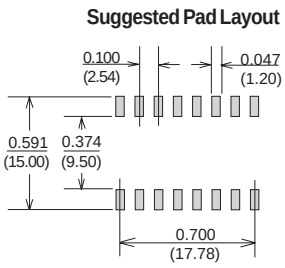
Test Conditions:

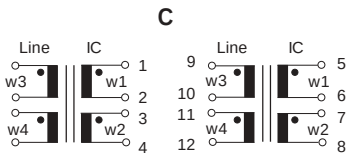
Inductance:	Line side windings in series - measurement @ 10kHz, 100mVrms
Leakage Inductance:	Line side windings in series, IC side winding/s short circuited - measurement @ 100kHz, 100mVrms
Coupling Capacitance:	IC side winding (windings in series) to Line side windings in series @ 10kHz, 100mVrms
Test Voltage:	1.5kV for 2 sec. - w1+w2 to w3+w4
	0.5kV for 2 sec. - w1+w3 to w2+w4
High VoltageTest:	U_{PULSE}(w1+w2 to w3+w4); 2kV_{OP} for 10µs/700µs wave form, 10 pulses in 10 second cycle with changing polarity.

Dimensions & Schematic

UAJ







Surface Coplanarity will be 0.004(0.10)

Dimensions: Inches (Millimeters)
Tolerance: ±0.010 (0.25) unless specified otherwise

ISDN • U_{PO} SMD Interface Transfomer Modules

Features

- designed for optimum compatability with all established interface IC's
- excellent and consistent balance between windings
- compact sizes in surface mount packages
- complies fully with all international standards for U-Interface
- manufactured in ISO-9001 approved Talema facility
- operating temberature -40° to +85°C

Electrical Specifications @ 25°C

Turns Ratio: **Bold** = IC Side Windings

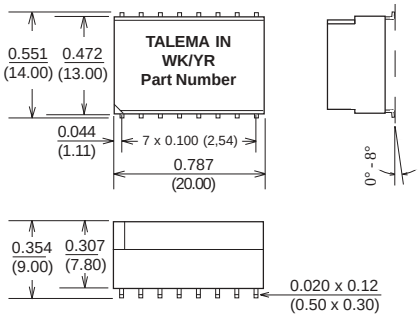
Surface Mount U_{PO} Interface Transformer Modules Complies with Basic Insulation Level EN60950, UL1950 and UL1459											
Part Number	Turns Ratio ±2%	L_P (mH min)	$\hat{I}_{DC}$ (mA)	L_L (µH)	C_C (pF Max)	DCR (Ohms per winding)		V_P (Vrms)	Schematic	Double Choke	
						Pri	Sec			L_N (mH)	DCR (Ohms)
UAJ-120A-502	1:1:**2**	1.7	75	5	100	0.8	1.6	1500	A	5	0.4
UAJ-130A-502	1:1:**2,5**	1.7	75	5	100	0.5	1.0	1500	A	5	0.4
UAJ-140B-502	1:1:**2:2**	1.7	75	5	180	0.8	1.6	1500	B	5	0.4

Test Conditions:

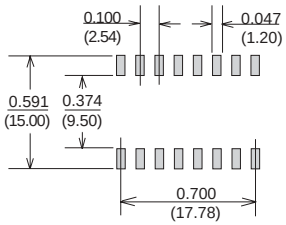
Inductance:	Line side windings in series - measurement @ 10kHz, 100mVrms
Leakage Inductance:	Line side windings in series, IC side winding/s short circuited - measurement @ 100kHz, 100mVrms
Coupling Capacitance:	IC side winding (windings in series) to Line side windings in series @ 10kHz, 100mVrms
Test Voltage:	1.5kV for 2 Sec. - Line side windings in series to IC side winding (IC windings in series)
Inductance CM Choke:	Measured @ 10kHz, 100mVrms

Dimensions & Schematic

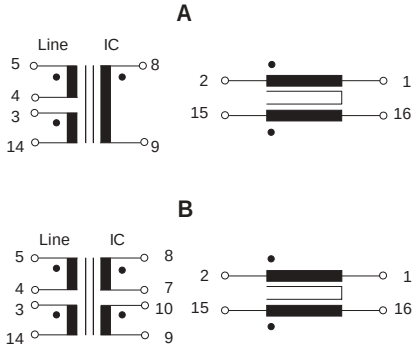
UAJ



Suggested Pad Layout



Schematic



Surface Coplanarity will be 0.004(0.10) maximum

Dimensions: Inches (Millimeters)
Tolerance: ±0.010 (0.25) unless specified otherwise