



a module solution provider

WG7310-0A WLAN/BT/FM Module

TI WL1271 IEEE 802.11b/g/n

BT 2.1+EDR & FM solution

Datasheet

Revision 0.3

Index

1. OVERVIEW	3
1.1. GENERAL FEATURES.....	3
2. FUNCTIONAL FEATURES	4
2.1. MODULE BLOCK DIAGRAM	4
2.2. BLOCK FUNCTIONAL FEATURE	4
2.2.1. <i>WLAN Features</i>	4
2.2.2. <i>Bluetooth Features</i>	5
2.2.3. <i>FM Radio (RX/TX) Features</i>	6
3. MODULE SPECIFICATION	7
3.1. ABSOLUTE MAXIMUM RATINGS.....	7
3.2. RECOMMENDED OPERATING CONDITIONS	7
3.3. RF CHARACTERISTIC	7
3.3.1. <i>WLAN RF</i>	7
3.3.2. <i>Bluetooth RF</i>	9
3.3.3. <i>FM Radio Electrical Characteristics</i>	9
3.4. EXTERNAL SLOW CLOCK INPUT (SLEEP_CLK).....	11
4. POWER CONSUMPTION	13
4.1. DEVICE SHUTDOWN CURRENT.....	13
4.2. WLAN POWER CONSUMPTION.....	13
4.2.1. <i>Active Mode</i>	13
4.2.2. <i>Inactive and Dynamic Modes</i>	14
4.3. BT POWER CONSUMPTION.....	15
4.3.1. <i>Static State</i>	15
4.3.2. <i>Dynamic State</i>	15
5. MODULE OUTLINE	17
5.1. SIGNAL LAYOUT (TOP VIEW)	17
5.2. PIN DESCRIPTION	18
6. POWER SEQUENCE	21
6.1. WLAN POWER ON SEQUENCE	21
6.2. BLUETOOTH POWER UP SEQUENCE	22

7. INTERFACE CHARACTERISTICS	23
7.1. WLAN SDIO CHARACTERISTIC	23
7.1.1. SDIO Read Timing	23
7.1.2. SDIO Interface Write Timing	23
7.1.3. SDIO Clock Timing	24
7.2. WLAN wSPI CHARACTERISTICS	25
7.2.1. SPI Read/Write Timing	25
7.2.2. SPI Clock Timing	26
7.3. BLUETOOTH HCI INTERFACE	27
7.4. BLUETOOTH PCM INTERFACE	28
8. DEBUG INTERFACE.....	29
8.1. WLAN RS232 TESTING PORT	29
8.2. BLUETOOTH HCI TESTING PORT	29
9. REFERENCE SCHEMATIC.....	30
10. LAYOUT RECOMMENDATION	32
10.1. RECOMMENDED BUMP PAD DESIGN	32
10.2. RECOMMENDED STENCIL DESIGN	32
10.3. RECOMMENDED TRACE LAYOUT	32
11. PACKAGE INFORMATION	35
11.1. MODULE MECHANICAL OUTLINE	35
11.2. ORDERING INFORMATION	36
11.3. PACKAGE MARKING	36
12. SMT AND BAKING RECOMMENDATION	37
12.1. BAKING RECOMMENDATION	37
12.2. SMT RECOMMENDATION	37
13. HISTORY CHANGE.....	38

1. OVERVIEW

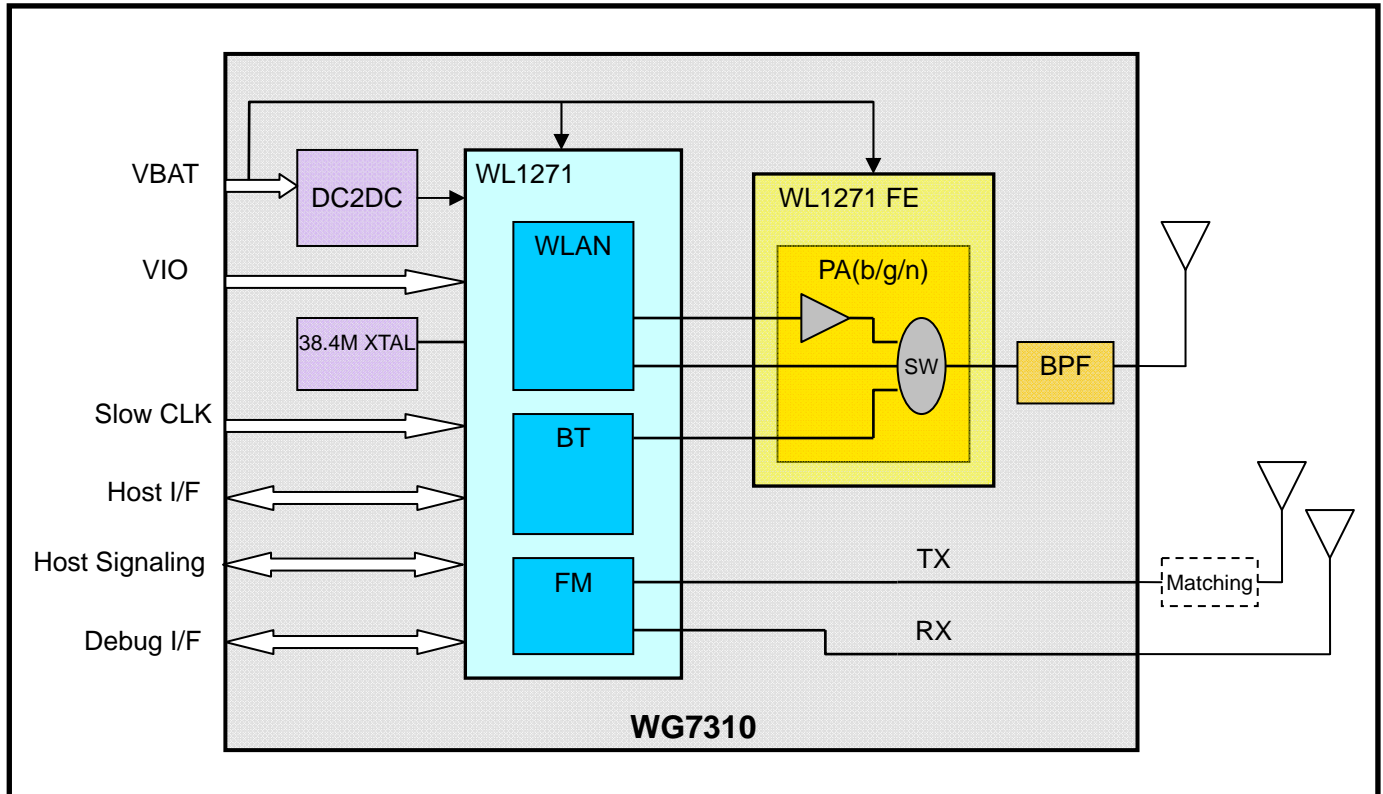
WG7310, a WiFi , Bluetooth and FM SiP (system in package) module, is the most demanded design for all handset and portable devices with TI WL1271 IEEE 802.11b/g/n and BT v2.1 EDR solutions to provide the best WiFi and BT coexistence interoperability and power saving technologies from TI.

1.1. General Features

- WLAN, Bluetooth and FM radio on a SiP module
- LGA96 pin package
- Dimension 10mm(L) x 10mm(W) x 1.4mm(H)
- Based on TI WL1271 65-nm CMOS technology packaged in WSP for module
- Seamless integration with TI OMAP application processor and GSM-GPRS-UMTS chipset
- Internal support for WLAN and Bluetooth Co-existence (bandwidth sharing, antenna sharing)
- Direct connection to battery using external switching mode power supply supporting 5.5V to 2.3V operation
- VIO in the 1.8V domain

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram



2.2. Block Functional Feature

2.2.1. WLAN Features

- Support 802.11 2.4GHz b/g/n mode
- Optimized for ultra low current consumption in all operating modes including extremely low power modes
- IEEE Std 802.11d, e, h, i, k, r, s PICS compliant
- Supports Cisco Client eXtensions (CCX) standard
- Support Secure Digital Input/Output (SDIO), Serial Peripheral Interface (SPI) Host Interfaces
- Medium-Access Controller (MAC)

- Embedded ARM Central Processing Unit (CPU)
- 292kByte (Used for Program code, data and packet data) Embedded Random-Access Memory (RAM)
- Hardware-Based Encryption/Decryption Using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys
- Supports Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [Includes Hardware-Accelerated Advanced-Encryption Standard (AES)]
- Designed to Work with IEEE Std 802.1x for Virtual Private Network (VPN) Solutions
- Baseband Processor
 - All IEEE Std 802.11b/g and 802.11n Data Rates up to 72.2Mbps
- 2.4 GHz Radio
 - Digital Radio Processor (DRP) implementation
 - Internal LNA
 - Supports: IEEE Std 802.11b, 802.11g, 802.11b/g, and 802.11n

2.2.2. Bluetooth Features

- Bluetooth 1.1, 1.2, 2.0+EDR and 2.1+EDR specification compliant – up to HCI level
- BT Enhanced Data Rate (2 and 3 Mbps)
- Support for Bluetooth 2005 core release
- Enhanced host Interfaces (UART)
- Very low power consumption
- On-chip Embedded radio
- Embedded ARM Microprocessor System
- Temperature detection and compensation mechanism ensure minimal variation in the RF performance over the entire temperature range
- A2DP support
- Wide-Band Speech support
- Full support for the Ultra Low Power (ULP) Bluetooth standard (previously known as Wibree)

2.2.3. FM Radio (RX/TX) Features

- On-Chip FM Receive
- On-Chip 0dBm output FM Transmitter
- Operation through BT host interface (UART/btSPI) or separate I²C interface for control and RDS data transfer
- Up to 48k Samples/sec audio sampling for stereo headsets
- Frequency resolution: 50-kHz step tuner
- Compatibility with Europe/US (87.5-108MHz) and Japan (76-90 MHz) FM Bands
- Full digital implementation
- Digital MPX signal, thus eliminating need for noise blanking circuits
- Integrated RDS/RDBS features
- Soft Mute
- Stereo/Mono blend based on signal condition for RX
- Selectable 50/75-us de-emphasis filter
- I²S format for stereo/mono digital audio data
- Analog stereo audio inputs/outputs
- Software selectable level for soft mute and stereo/mono blend level for RX
- Fast independent up/down tuning function
- Supports a dedicated enable pin for the FM IP

3. MODULE SPECIFICATION

3.1. Absolute Maximum Ratings

Over operating free-air temperature range

Characteristics		Value	Unit
Supply Voltage Range	VBAT	-0.5 to 5.5	V
	VIO	-0.5 to 2.1	V
Input Voltage to Analog Pins		-0.5 to 2.1	V
Input Voltage to all Other Pins		-0.5 to VIO + 0.5V	V
Operating Ambient Temperature Range		-20 to 70	°C
Storage Temperature Range		-40 to 85	°C

3.2. Recommended Operating Conditions

The WG7310 requires two supplies: VBAT and VIO.

Power Supply	Voltage		
	Min.	Typ.	Max.
VBAT	2.3V	3.3V	4.8V
VIO	1.62V	1.8V	1.92V

3.3. RF Characteristic

3.3.1. WLAN RF

WLAN Transmitter						
Characteristics	Condition	Max EVM	Min	Typ	Max	Unit
11b Output Power	11M CCK	35%	16	18	-	dBm
	5.5M CCK	35%	16	18	-	
	2M DSSS	35%	16	18	-	
	1M DSSS	35%	16	18	-	

Characteristics	Condition	Max EVM	Min	Typ	Max	Unit
11g Output Power	54M OFDM	-25	11.5	13.5	---	dBm
	48M OFDM	-25	11.5	13.5	---	
	36M OFDM	-19	13.5	15.5	---	
	24M OFDM	-19	13.5	15.5	---	
	18M OFDM	-13	15	17	---	
	12M OFDM	-13	15	17	---	
	9M OFDM	-8	15	17	---	
	6M OFDM	-8	15	17	---	
11n Output Power	MCS7	-28	11	12.5	---	dBm
	MCS0	-5	15	17	---	

WLAN Receive					
Characteristics	Condition	Min	Typ	Max	Unit
11b Rx Sensitivity	11M CCK	---	-86	-82	dBm
	5.5M CCK	---	-90	-86	
	2M DSSS	---	-93	-89	
	1M DSSS	---	-96	-92	
11g Rx Sensitivity	54M OFDM	---	-73	-69	dBm
	48M OFDM	---	-74	-70	
	36M OFDM	---	-79	-75	
	24M OFDM	---	-83	-79	
	18M OFDM	---	-85	-81	
	12M OFDM	---	-87	-83	
	9M OFDM	---	-89	-85	
	6M OFDM	---	-90	-86	
11n Rx Sensitivity	MCS7	---	-69	-65	dBm
	MCS0	---	-88	-84	

Note: (1) For CH13, sensitivity is degraded up to 2dB in 802.11g/n.
(2) For CH14, sensitivity is degraded up to 2dB in 802.11b/g/n.

3.3.2. Bluetooth RF

BT Transmitter, GFSK, Class 2 & Class 1.5					
Characteristics		Min	Typ	Max	Unit
RF output power	CLASS1P5 = VBAT	8.5	10	---	dBm
	CLASS1P5 = 1.8V	5.5	7.5		dBm
Power variation over BT band		-1		1	dB
Gain control range			30		dB
Power control step		2	5	8	dB

BT Receiver Characteristics, In-Band Signals					
Characteristics		Min	Typ	Max	Unit
Sensitivity	GFSK, BER = 0.1%	-86	-90	---	dBm
	Pi/4-DQPSK, BER = 0.01%	-86	-90	---	
	8DPSK, BER = 0.01%	-80	-84	---	
Max. useable input power	GFSK, BER = 0.1%	-5	---	---	dBm
	Pi/4-DQPSK, BER = 0.1%	-10	---	---	
	8DPSK, BER = 0.1%	-10	---	---	

3.3.3. FM Radio Electrical Characteristics

Characteristics	Condition	Min	Typ	Max	Unit
Audio output impedance	FM function enabled and during auto-search			50	Ω
	FM function disabled and when muted	50			K Ω
Audio input impedance		30			K Ω
Selectable RF Rx input impedance	With external matching circuitry – Default = 50 Ω		50	200	Ω
RF input return loss	With external matching circuitry			-10	dB

For all FM bands: 87.5-108MHz Europe/USA, 76-90MHz Japan

FM RF Rx Characteristics							
Characteristics	Condition		Min	Typ	Max	Unit	
Frequency step			50			kHz	
RF input power level	Max input power		105			dB μ V	
RDS Sensitivity	For an RDS deviation of 1.2kHz. 95% of blocks decoded with no errors, taken over 5000 blocks.			13	20	dB μ V	
	For an RDS deviation of 2kHz.			8	15	dB μ V	
Sensitivity	fmod=1kHz, Δ f=22.5kHz, A-weighted(S+N)/N=26dB (BW of 300 Hz to 15kHz), De-emphasis=50s			0	5	dB μ V	
RF conducted emissions	LO breakthrough measured on the reference port				-55	dBm	
	925-960MHz, 1805-1880MHz, 1930-1990MHz				-90		
RF out-of-band emissions	869-960MHz (GSM, CDMA)				-140	dBm/Hz	
	1570-1580MHz (GPS)				-150		
	1805-1990MHz (GSM, PCS, CDMA, WCDMA)				-150		
	2110-2170MHz (WCDMA)				-150		
	2402-2483.5MHz (BT, WLAN)				-150		
FM RF Tx Characteristics							
Characteristics	Condition		Min	Typ	Max	Unit	
Frequency accuracy				\pm 1	\pm 10	kHz	
Channel spacing	User configurable		50	100	200	kHz	
Output Power	Max level	Maximum o/p level when driving into L=120nH, Q > 30. All Frequencies, TX=ON, L=R=0 (no modulation), power level=0	US /Europe	117	118	dB μ V	
			Japan	117	118		
	Flatness	For outputs 105-117dB μ V			\pm 0.5	\pm 2	dB
	Range				26		dB

Out of band spurious emission (at maximum power)	US/EU: 87.5 – 108 MHz	746 - 764MHz			22	dBμVrms
		869–894, 925–960MHz			20	
		1570 -1580MHz			25	
		1805–1880, 1930–1990MHz			28	
		2110 - 2170MHz			20	
		2400 - 2483.5MHz (BT band)			20	
	Japan: 76 – 90 MHz	746 - 764MHz			26	
		869–894, 925–960MHz			19	
		1570 -1580MHz			25	
		1805–1880, 1930–1990MHz			28	
		2110 - 2170MHz			20	
2400 - 2483.5MHz (BT band)			20			

3.4. External Slow Clock Input (SLEEP_CLK)

The external slow clock input SLEEP_CLK must be present at all times. The slow clock is used to maintain timers that synchronize the device to the access point (AP) beacons.

Table 1. External Slow Clock Input Requirements

Characteristics (1)	Condition	Min.	Typ.	Max.	Unit
Frequency			32.768		KHz
Reference Frequency Accuracy	WLAN, BT, FM_RX			+/-150	ppm
	FM_TX (2)			+/- 40	
Input Transmit Time	10% ~ 90%			100	ns
Frequency Duty Cycle		30	50	70	%
Fail Safe Maximum Value				2.0	V
Input Voltage Limits (Square Wave)	V _{IH}	0.65xV _{IO}		V _{IO}	V _{peak}
	V _{IL}	0		0.35xV _{IO}	
Input Impedance		1			MΩ
Input Capacitance				5	pF

Rise and fall time				100	ns
Phase noise	1kHz		-125		dBc/Hz
Jitter (3)	Integrated over 300Hz ~ 15000Hz			1	Hz

(1) Slow clock is a fail safe input

(2) If the available slow clock source does not meet the +/-40ppm requirement, there are two options;

- Use the fast clock for the FM_TX functionality. This is configured using a vendor-specific command to switch to Fref operation after enabling the FM core with the slow clock source.
- Enable clock error calibration in the FM core to compensate for the clock source error. The calibration can be done using a known vendor-input clock error or intrinsically to the core (self-calibration).

(3) Not required if fast clock is used for FM TX and RX

4. POWER CONSUMPTION

4.1. Device Shutdown Current

The SDIO/CLK_REQ lines should be driven by the host to prevent leakage in sleep/shutdown modes.

Mode Description	Power Supply	Typ.	Max.	Unit
Shutdown mode (BT, WLAN and FM sections in shutdown mode) Values are over process and at room temperature	1.8V (VIO)	6.5	7.5	uA
	Total VBAT at 3.6V	14	26	

4.2. WLAN Power Consumption

WLAN supply current was measured using the HDK and the TrioScope tool, over process and temperature at F_{ref} 38.4MHz unless otherwise specified.

4.2.1. Active Mode

- During Listen Mode operation, the radio is in a low power mode optimized to receive only 11b beacons. The DC2DC, FEM and WL1271 devices are active but consume less current.
- In STBY mode, no RF operation required. The DC2DC, FEM and WL1271 device are active but consume lower current.
- In TX and RX modes, all devices are active and consume maximum currents.

Mode Description		Power Supply		11Mbps IEEE802.11b		54/65Mbps IEEE802.11g/n		Unit
				Typ (1)	Max (2)	Typ (1)	Max (2)	
Transmit Data	11b/g: Packet size =2048 bytes	1.8V (VIO)		0.26	0.3	0.26	0.3	mA
	11n: Packet size =1024 bytes	Total VBAT =3.6V	FEM current only	195	214	113	122	
	11b delay=0.004ms		System current	270	292	195	207	
11g/n delay=0.002ms								
Receive Data (3)		1.8V (VIO)		0.23	0.3	0.23	0.3	mA
		Total VBAT=3.6V		96	105	96	105	
Listen (3)		1.8V (VIO)		0.23	0.3	n/a	n/a	mA
		Total VBAT=3.6V		68	74	n/a	n/a	
STBY		1.8V (VIO)		0.23	0.3	0.23	0.3	mA
		Total VBAT=3.6V		6	9	6	9	

(1) Nominal process at 25°C

(2) Over process and temperature

(3) CH14 values add up to 2mA

4.2.2. Inactive and Dynamic Modes

Mode Description	Power Supply	Typ	Max	Unit
Sleep mode (BT and FM in reset) (1) (2)	1.8V (VIO)	11	17	uA
	Total VBAT at 3.6V	96	109	

(1) Values indicate current between beacons

(2) Room temp over process

Mode Description (1)	Power Supply	Max	Unit
Dynamic mode Beacon (DTIM = 1 : TBTT = 100ms) Beacon duration~1.6ms : Rate= 1Mbps Beacon in Listen mode	Total VBAT at 3.6V to TPS62611	0.82	mA

(1) This mode reflects results with software drivers and not the Triscope tool.

4.3. BT Power Consumption

BT supply current was measured using the HDK and HCI Tester tool at F_{ref} 38.4MHz.

4.3.1. Static State

Characteristics		Typ	Max	Unit
Supply current in deep sleep mode	VIO	12	15	uA
	VBAT	62	80	

4.3.2. Dynamic State

Transmit power at 4dBm, nominal, room temperature, $V_{BAT}=3.6V$, F_{ref} at 38.4MHz.

Use Case	Mode Description	Full VBAT Source (Using DC2DC)	Unit
Idle current (ARM off) (3)	Master/Slave	1.8	mA
SCO link HV3	Master/Slave	8	
eSCO link EV3 64Kbps, no retransmission	Master/Slave	8.2	
eSCO link 2-EV3 64Kbps, no retransmission	Master/Slave	5.6	
GFSK full throughput: Tx=DH1, RX=DH5	Master/Slave	23.5	
EDR full throughput: Tx=2-DH1, RX=2-DH5	Master/Slave	24.3	
EDR full throughput: Tx=3-DH1, RX=3-DH5	Master/Slave	24.9	
Sniff, 1 attempt, 1.28sec	Master/Slave	100/110	uA
Page or Inquiry Scan 1.28s, 11.25ms	Master/Slave	230	
Page scan 1.28s, 11.25msec and Inquiry Scan 2.56s, 11.25ms	Master/Slave	320	
Low power scan, 1.28 interval	Master/Slave	145	

(1) Voltage Input at INPUT_VBAT_SUPPLY

(2) Voltage input at BT_CLASS_1P5

- (3) IDLE is a state in which the BT is awake and communicates with the host, but there is no RF activity.

5. Module Outline

5.1. Signal Layout (Top View)

	1	2	3	4	5	6	7	8	9	10	11																									
A 1	A1 GND	A2 NC.	A3 VBAT	A4 VIO	A5 PM_DC_REQ	A6 GND	A7 CM_XTALM	A8 GND	A9 FA_AUD_IN_L	A10 GND	A11 FA_AUD_IN_R																									
B 2	B1 BD_WU	B2 GND	B3 CLASSIFS	B4 I1V8	B5 NC.	B6 NC.	B7 GND	B8 CM_XTALP	B9 GND	B10 FA_AUD_OUT_L	B11 GND																									
C 3	C1 NC.	C2 BD_TX_DBG	WG7310 Pin Assignment Top View <table border="1" style="margin: auto;"> <tr> <td>D4 BD_AUD_CLK</td> <td>D5 BD_AUD_FSYNC</td> <td>D6 BD_HCI_CTS</td> <td>D7 BD_HCI_RTS</td> <td>D8 NC.</td> </tr> <tr> <td>E4 BD_AUD_IN</td> <td>E5 BD_AUD_OUT</td> <td>E6 GND</td> <td>E7 GND</td> <td>E8 BD_HCI_TX</td> </tr> <tr> <td>F4 GND</td> <td>F5 GND</td> <td></td> <td>F7 GND</td> <td>F8 BD_HCI_RX</td> </tr> <tr> <td>G4 NC.</td> <td>G5 GND</td> <td>G6 GND</td> <td>G7 GND</td> <td>G8 WD_IRQ</td> </tr> <tr> <td>H4 GND</td> <td>H5 NC.</td> <td>H6 NC.</td> <td>H7 WD_UART_DBG</td> <td>H8 MD_CLK_REQ_OUT</td> </tr> </table>							D4 BD_AUD_CLK	D5 BD_AUD_FSYNC	D6 BD_HCI_CTS	D7 BD_HCI_RTS	D8 NC.	E4 BD_AUD_IN	E5 BD_AUD_OUT	E6 GND	E7 GND	E8 BD_HCI_TX	F4 GND	F5 GND		F7 GND	F8 BD_HCI_RX	G4 NC.	G5 GND	G6 GND	G7 GND	G8 WD_IRQ	H4 GND	H5 NC.	H6 NC.	H7 WD_UART_DBG	H8 MD_CLK_REQ_OUT	C10 GND	C11 FA_RX_ANT
D4 BD_AUD_CLK	D5 BD_AUD_FSYNC	D6 BD_HCI_CTS								D7 BD_HCI_RTS	D8 NC.																									
E4 BD_AUD_IN	E5 BD_AUD_OUT	E6 GND								E7 GND	E8 BD_HCI_TX																									
F4 GND	F5 GND									F7 GND	F8 BD_HCI_RX																									
G4 NC.	G5 GND	G6 GND								G7 GND	G8 WD_IRQ																									
H4 GND	H5 NC.	H6 NC.								H7 WD_UART_DBG	H8 MD_CLK_REQ_OUT																									
D 4	D1 NC.	D2 GND								D10 FA_AUD_OUT_R	D11 GND																									
E 5	E1 GND	E2 NC.								E10 GND	E11 FA_TX_ANT																									
F 6	F1 NC.	F2 GND								F10 MD_SLOWCLK	F11 GND																									
G 7	G1 GND	G2 NC.	G10 GND	G11 FD_I2S_DO																																
H 8	H1 NC.	H2 GND	H10 FD_I2S_DI	H11 FD_I2S_CLK																																
J 9	J1 NC.	J2 NC.	J10 FD_IRQ	J11 FD_SCL																																
K 10	K1 GND	K2 NC.	K3 NC.	K4 BD_BV	K5 GND	K6 WD_RS232_RX	K7 WD_RS232_TX	K8 DS_SPL_CSX	K9 DS_SPL_DOUT	K10 FD_I2S_FSYNC	K11 FD_SDA																									
L 11	L1 NC.	L2 GND	L3 FD_BV	L4 GND	L5 WB_RF_ANT	L6 GND	L7 DS_SDIO_D1	L8 DS_SDIO_D0	L9 DS_SPL_DIN	L10 DS_SPL_CLK	L11 WD_BV																									

5.2. Pin Description

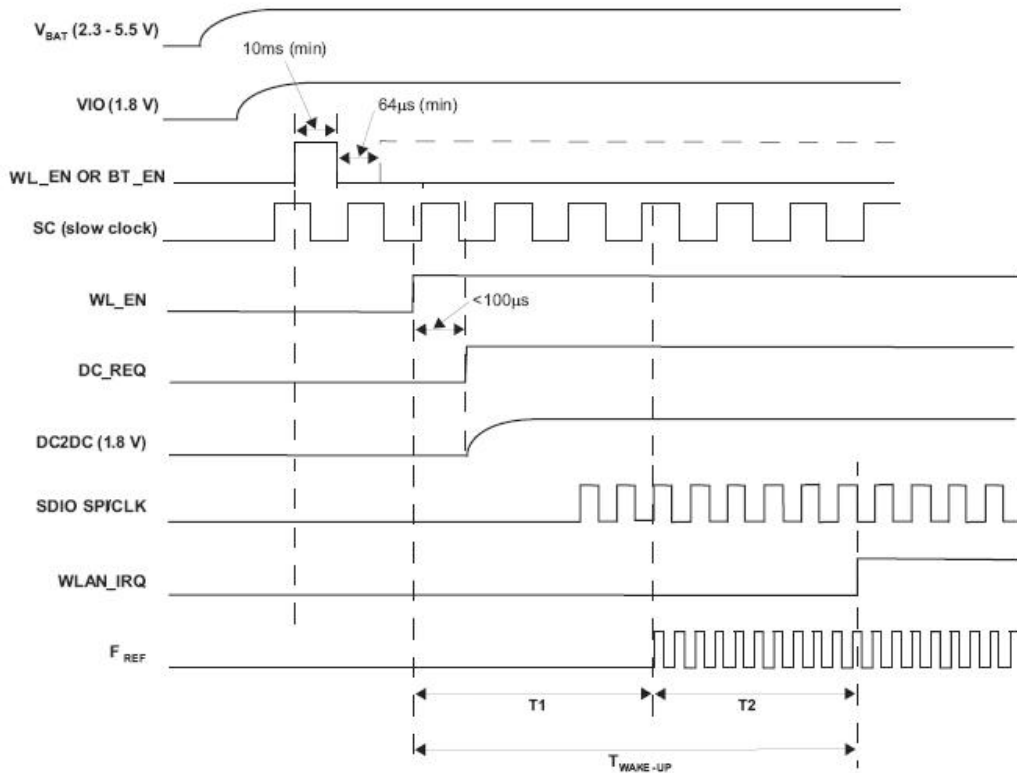
No.	Index	Name	Type	Description
1	A1	GND	GND	GROUND
2	A2	N.C.	-	Not connected
3	B1	BT_FUNC2: BT_WU/ DC2DC	O	BT WU (default) or BT DC2DC
4	B2	GND	GND	GROUND
5	C1	N.C.	-	Not connected
6	C2	BT_FUNC4: BT_TX_DBG	O	BT UARTD (reserved for debug)
7	D1	N.C.	-	Not connected
8	D2	GND	GND	GROUND
9	E1	GND	GND	GROUND
10	E2	N.C.	-	Not connected
11	F1	N.C.	-	Not connected
12	F2	GND	GND	GROUND
13	G1	GND	GND	GROUND
14	G2	N.C.	-	Not connected
15	H1	N.C.	-	Not connected
16	H2	GND	GND	GROUND
17	J1	N.C.	-	Not connected
18	J2	N.C.	-	Not connected
19	K1	GND	GND	GROUND
20	K2	N.C.	-	Not connected
21	L1	N.C.	-	Not connected
22	L2	GND	GND	GROUND
23	L3	FM_EN	I	FM RST
24	K3	N.C.	-	Not connected
25	L4	GND	GND	GROUND
26	K4	BT_EN	I	BT RST
27	L5	WB_RF_ANT	I/O	WL/BT RF ANT
28	K5	GND	GND	GROUND
29	L6	GND	GND	GROUND
30	K6	WL_RS232_RX/ I2S_M_SCL	I	RS232_RX (default) or I2C_M_SCL (reserved for debug)
31	L7	SDIO_D1	I/O	SDIO IF

No.	Index	Name	Type	Description
32	K7	WL_RS232_TX/ I2S_M_SDA	O	RS232_TX (default) or I2C_M_SDA (reserved for debug)
33	L8	SDIO_D2	I/O	SDIO IF
34	K8	SPI_CSX/ SDIO_D3	I/O	SDIO IF
35	L9	SPI_DIN/ SDIO_CMD	I/O	SDIO IF
36	K9	SPI_DOUT/ SDIO_D0	I/O	SDIO IF
37	L10	SPI_CLK/ SDIO_CLK	I	SDIO IF
38	K10	FM_I2S_FSYNC	I/O	FM I2S IF
39	L11	WL_EN	I	WL RST
40	K11	FM_SDA	I/O	FM I2C IF
41	J11	FM_SCL	I/O	FM I2C IF
42	J10	FM_IRQ	O	FM I2C IF
43	H11	FM_I2S_CLK	I/O	FM I2S IF
44	H10	FM_I2S_DI	I	FM I2S IF
45	G11	FM_I2S_DO	O	FM I2S IF
46	G10	GND	GND	GROUND
47	F11	GND	GND	GROUND
48	F10	SLOWCLK	I	SLEEP CLK
49	E11	FM_TX_ANT	O	FM TX ANT
50	E10	GND	GND	GROUND
51	D11	GND	GND	GROUND
52	D10	FMAUDROUT	O	FM AUD OUT
53	C11	FM_RX_ANT	I	FM RX ANT
54	C10	GND	GND	GROUND
55	B11	GND	GND	GROUND
56	B10	FMAUDLOUT	O	FM AUD OUT
57	A11	FMAUDRIN	I	FM AUD IN
58	A10	GND	GND	GROUND
59	A9	FMAUDLIN	I	FM AUD IN
60	B9	GND	GND	GROUND
61	A8	GND	GND	GROUND
62	B8	XTALP	O	FREF INPUT (internal use only)
63	A7	XTALM	O	FREF INPUT (internal use only)
64	B7	GND	GND	GROUND

No.	Index	Name	Type	Description
65	A6	GND	GND	GROUND
66	B6	DC2DC_MODE	-	Connect to B5
67	A5	DC_REQ	O	DC_REQ to INTERNAL DC2DC
68	B5	DC2DC_MODE	-	Connect to B6
69	A4	VIO	I	1.62~1.92V POWER SUPPLY, 1.8V TYP
70	B4	1V8	O	1.8V DC2DC POWER SUPPLY
71	A3	VBAT	I	2.3~4.8V POWER SUPPLY, 3.3V TYP
72	B3	VDD_LDO_IN_CLASS1P5	I	BT CLASS2/CLASS1.5 POWER SUPPLY
73	D4	PCM_AUD_CLK	I/O	PCM I/F
74	E4	PCM_AUD_IN	I/O	PCM I/F
75	F4	GND	GND	GROUND
76	G4	N.C.	-	Not connected
77	H4	GND	GND	GROUND
78	H5	N.C.	-	Not connected
79	H6	N.C.	-	Not connected
80	H7	WL_UART_DBG	O	WL_UART_DBG (reserved for debug)
81	H8	CLK_REQ_OUT	O	CLK_REQ positive polarity
82	G8	WLAN_IRQ	O	WLAN interrupt request
83	F8	HCI_RX	I	BT UART I/F
84	E8	HCI_TX	O	BT UART I/F
85	D8	N.C.	-	Not connected
86	D7	HCI_RTS	I/O	BT UART I/F
87	D6	HCI_CTS	I/O	BT UART I/F
88	D5	PCM_AUD_FSYNC	I/O	PCM I/F
89	E5	PCM_AUD_OUT	O	PCM I/F
90	F5	GND	GND	GROUND
91	G5	GND	GND	GROUND
92	G6	GND	GND	GROUND
93	G7	GND	GND	GROUND
94	F7	GND	GND	GROUND
95	E7	GND	GND	GROUND
96	E6	GND	GND	GROUND

6. Power Sequence

6.1. WLAN Power on Sequence



WLAN Power on sequence

The duration of T1 is defined as the time from WL_EN=high until Fref is valid for the SoC.

T1 ~ 55ms

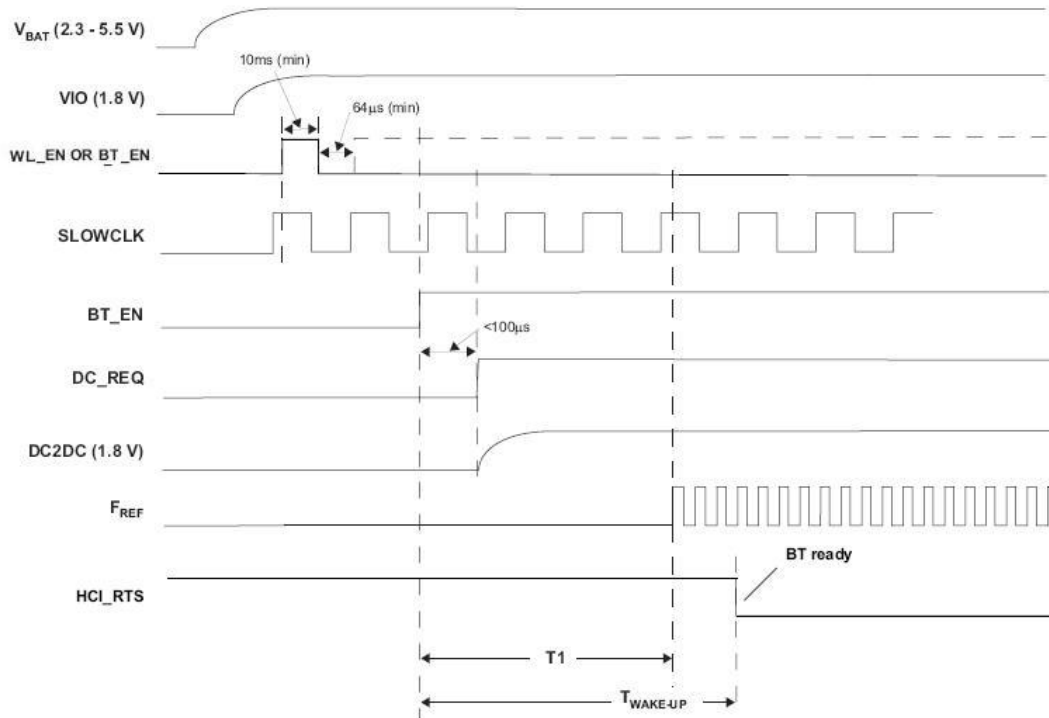
The duration of T2 depends on:

- Operation system
- Host enumeration for the SDIO/SPI
- PLL configuration
- Firmware download
- Releasing the core from reset
- Firmware initialization

6.2. Bluetooth Power Up Sequence

Power up requirements:

1. BT_EN must be low
2. VIO must be stable before releasing BT_EN.
3. Slow clock must be stable within 2 ms of BT_EN high.



Bluetooth Power Up sequence

WG7310 indicates completion of power up sequence by asserting RTS low. This occurs up to 100ms after BT_EN goes high.

7. Interface Characteristics

7.1. WLAN SDIO Characteristic

7.1.1. SDIO Read Timing

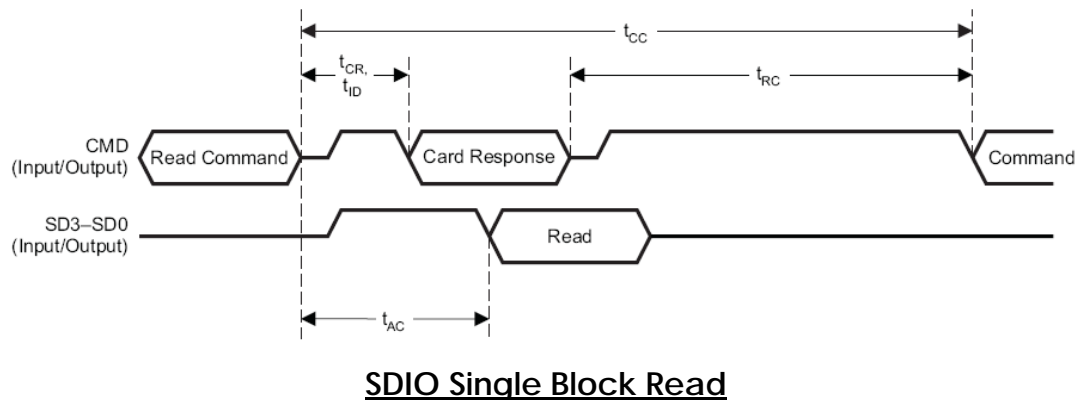
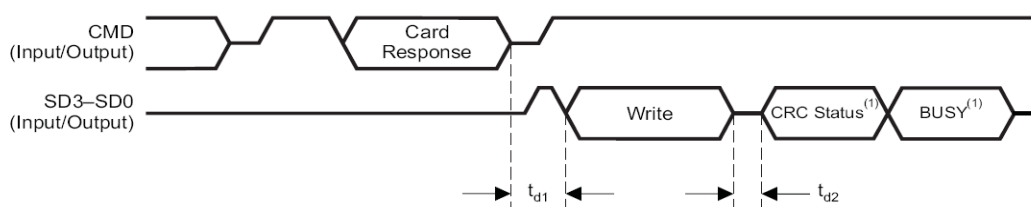


Table 2. SDIO Read Switching characteristics

Table 3.

PARAMETER		MIN	MAX	UNIT
t_{CR}	Delay time, assign relative address or data transfer mode Read-command CMD valid to card-response CMD valid	2	64	Clock cycles
t_{CC}	Delay time, CMD command valid to CMD command valid	58		Clock cycles
t_{RC}	Delay time, CMD response valid to CMD command valid	8		Clock cycles
t_{AC}	Access time, CMD command valid to SD3-SD0 read data valid	2		Clock cycles

7.1.2. SDIO Interface Write Timing



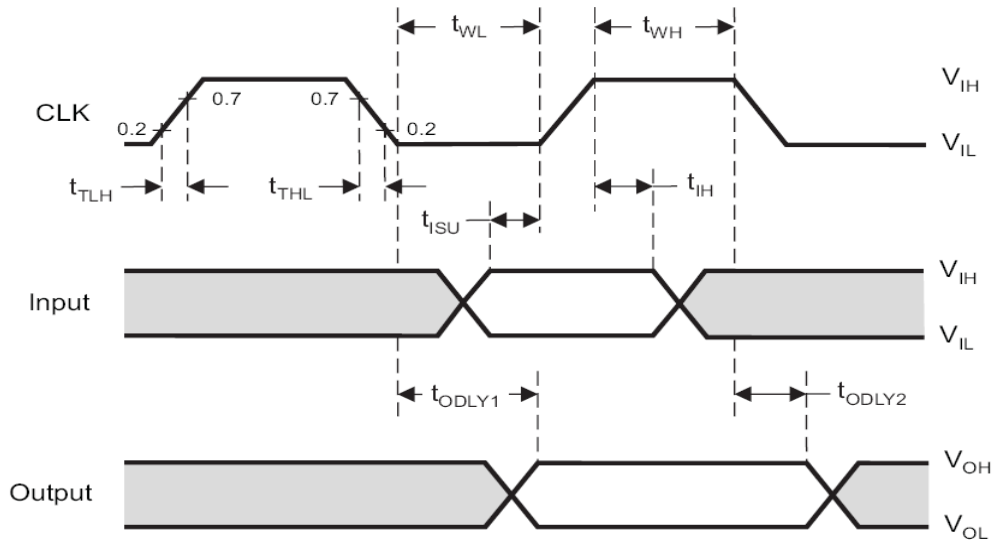
(1) CRC status and busy waveforms are only for data line 0. Data lines 1-3 are N/A. The busy waveform is optional and may not be present.

SDIO Single Block Write

Table 4. SDIO Write Switching characteristics

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, CMD card response invalid to SD3-SD0 write data valid	2		Clock cycles
t_{d2}	Delay time, SD3-SD0 write data invalid end to CRC status valid	2	2	Clock cycles

7.1.3. SDIO Clock Timing



SDIO Clock Timing

Table 5. SDIO Timing requirement

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	$C_L \leq 30$ pF	0 26	MHz
DC	Low/high duty cycle	$C_L \leq 30$ pF	40 60	%
t_{TLH}	Rise time, CLK	$C_L \leq 30$ pF	4.3	ns
t_{THL}	Fall time, CLK	$C_L \leq 30$ pF	3.5	ns
t_{ISU}	Setup time, input valid before CLK \uparrow	$C_L \leq 30$ pF	4	ns
t_{IH}	Hold time, input valid after CLK \uparrow	$C_L \leq 30$ pF	5	ns
t_{ODLY}	Delay time, CLK \downarrow to output valid	$C_L \leq 30$ pF	2 12	ns

7.2. WLAN wSPI Characteristics

The SPI interface signals are shared with the SDIO bus in the WG7310.

7.2.1. SPI Read/Write Timing

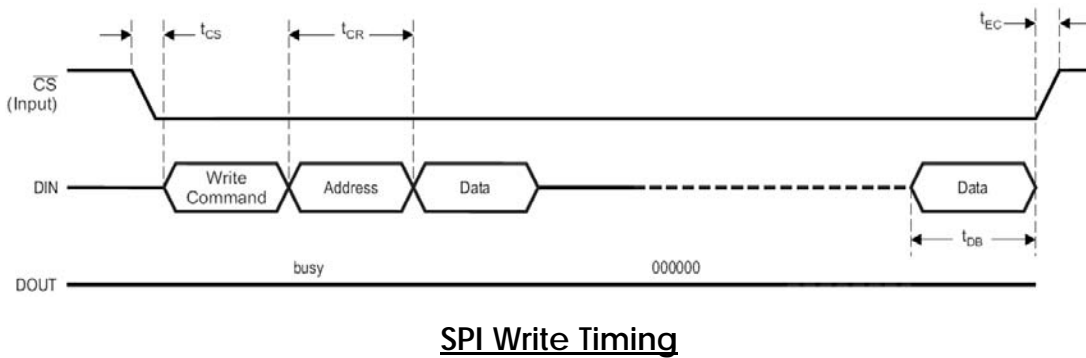
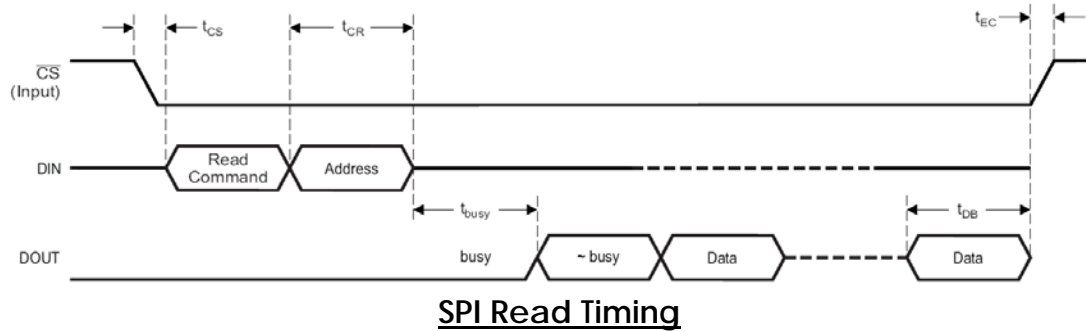
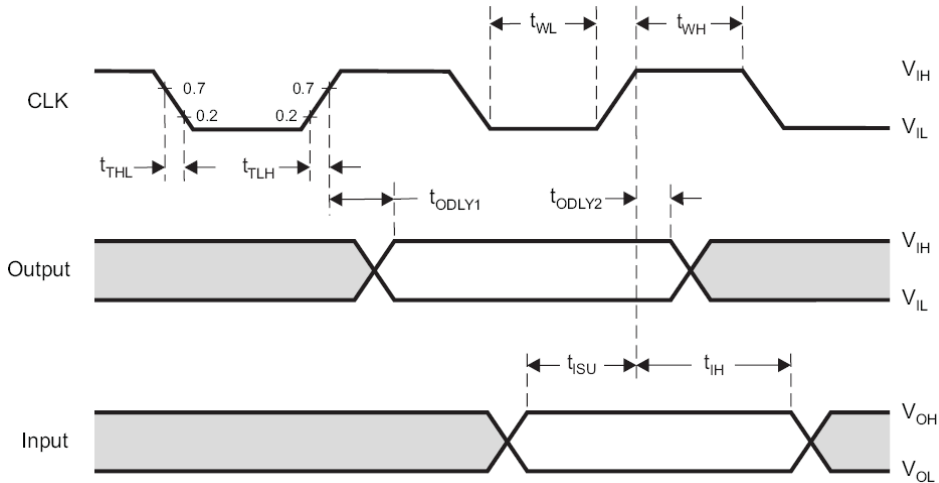


Table 6. SPI Read/Write Switching characteristics

Parameter		Min.	Max.	Unit
t_{CS}	Delay time, CS ↓ to DIN read/write command valid	0		16 Clock Cycles
t_{CR}	Delay time, DIN read command invalid to DOUT/DIN card response valid		1	16 Clock Cycles
t_{busy}	Fixed busy delay till DOUT data valid	1	7	16/32 Clock Cycles
t_{EC}	Delay time, DOUT data invalid CS ↑	0		16 Clock Cycles
t_{DB}	Data block size		1	16/32 Clock Cycles

7.2.2. SPI Clock Timing



SPI Clock Timing

Table 7. SPI Timing requirement

Parameter		Min.	Max.	Unit
f_{clock}	Clock frequency, CLK	0	48	MHZ
DC	Low/high duty cycle	40	60	%
t_{WL}	Pulse duration, CLK low	5		ns
t_{WH}	Pulse duration, CLK high	5		ns
t_{TLH}	Rise time, CLK		4.3	ns
t_{THL}	Fall time, CLK		3.5	ns
t_{ISU}	Setup time, input valid before CLK \uparrow	5		ns
t_{IH}	Hold time, input valid after CLK \uparrow	5		ns
t_{ODLY1}	Delay time, CLK \uparrow to output valid	4	15	ns
t_{ODLY2}	Delay time, CLK \downarrow to output invalid	5	15	ns

7.3. Bluetooth HCI Interface

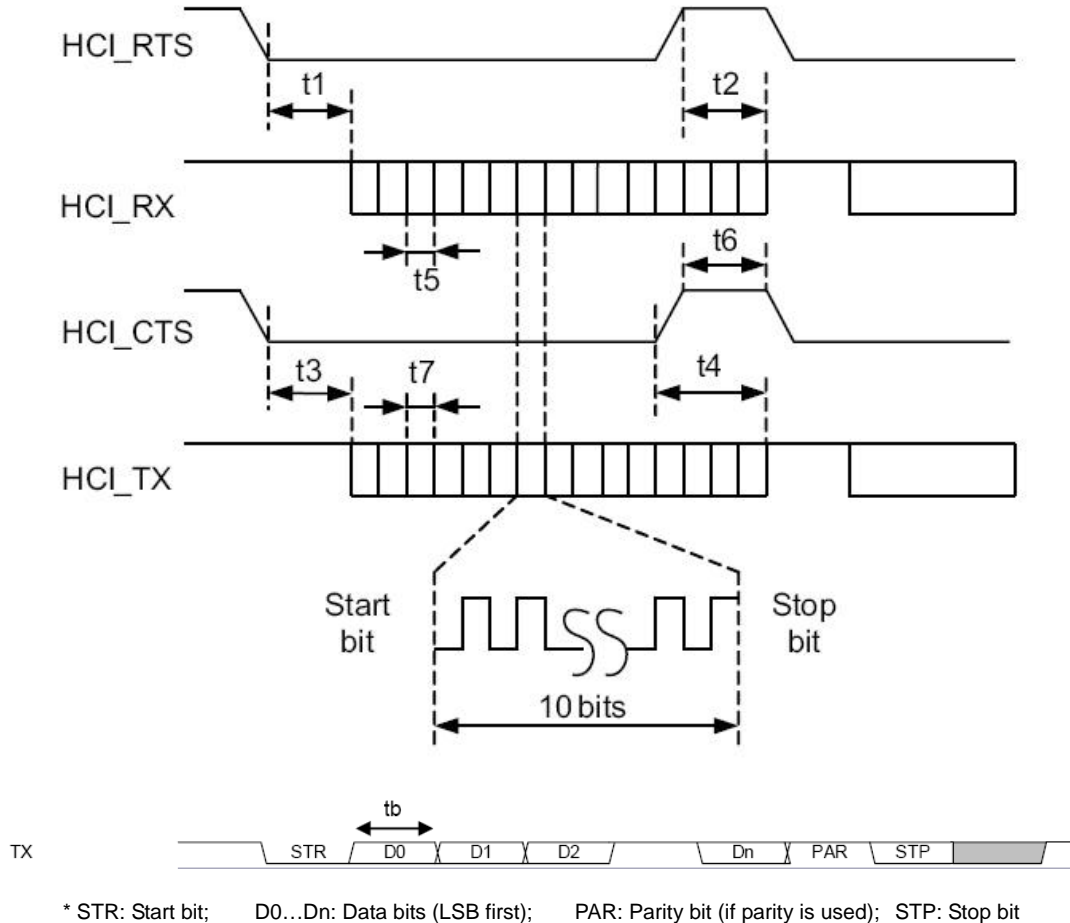


Table 8. BT HCI Timing characteristics

Characteristics	Condition	Symbol	Min	Typ.	Max	Unit
Baud rate	Any rate (1)		37.5	115.2	4000	kbps
Baud rate accuracy	Receive, Transmit	t5, t7			-2.5to+1.5	%
CTS low to TX_DATA on		t3	0	2		us
CTS high to TX_DATA off	Hardware flow control	t4			1	Byte
CTS high pulse width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes

Exception for 19.2MHz: Maximum baud rate = 3.84Mbps.

7.4. Bluetooth PCM Interface

Bluetooth can be setting as master or slave mode. For more stable voice performance, slave mode is recommended.

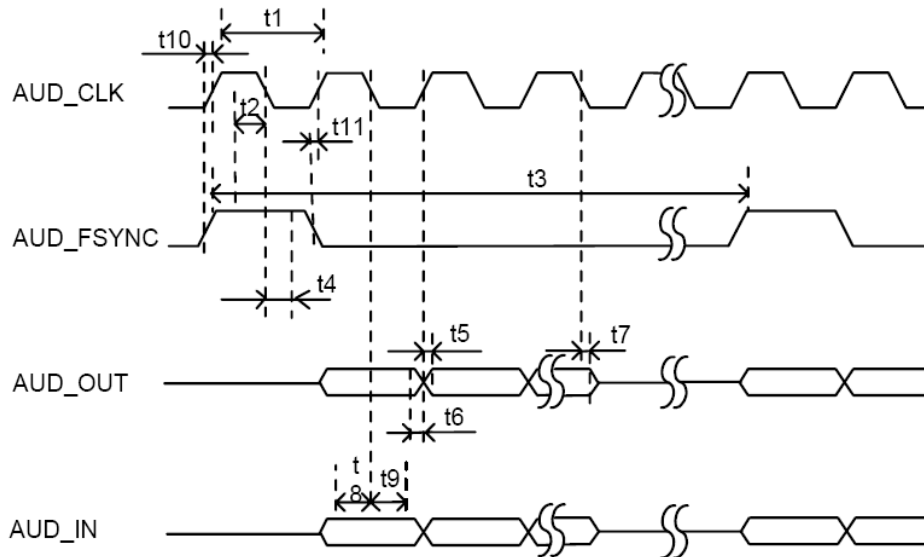


Table 9. BT PCM Slave mode Timing characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit
Master clock frequency	$1/t_1$	64		16000	KHz
Clock duty cycle		40	50	60	%
Synchronization clock frequency	$1/t_3$	$1/(8 \times t_1)$		$1/(65535 \times t_1)$	KHz
Synchronization signal width		t_1		$165545 \times t_1$	
Setup time for AUD_FSYNC high to AUD_CLK low	t_2	5			ns
Hold time from AUD_CLK low to AUD_FSYNC low	t_4	8			ns
Setup time for AUD_IN valid to AUD_CLK low	t_8	5			ns
Hold time from AUD_CLK low to AUD_IN invalid	t_9	8			ns
Delay time from AUD_CLK high to AUD_OUT data valid	t_5			20	ns
Delay time from AUD_CLK low to last data bit of AUD_OUT output set to high impedance	t_7			20	ns

8. Debug Interface

The debug interface helps customers to evaluate the HW/SW features for their application. It also helps to debug during the development stage. The WG7310 module support RS232 signals and UART signals for debug purpose. Connect RS232 and UART signals to the test points for future debug support.

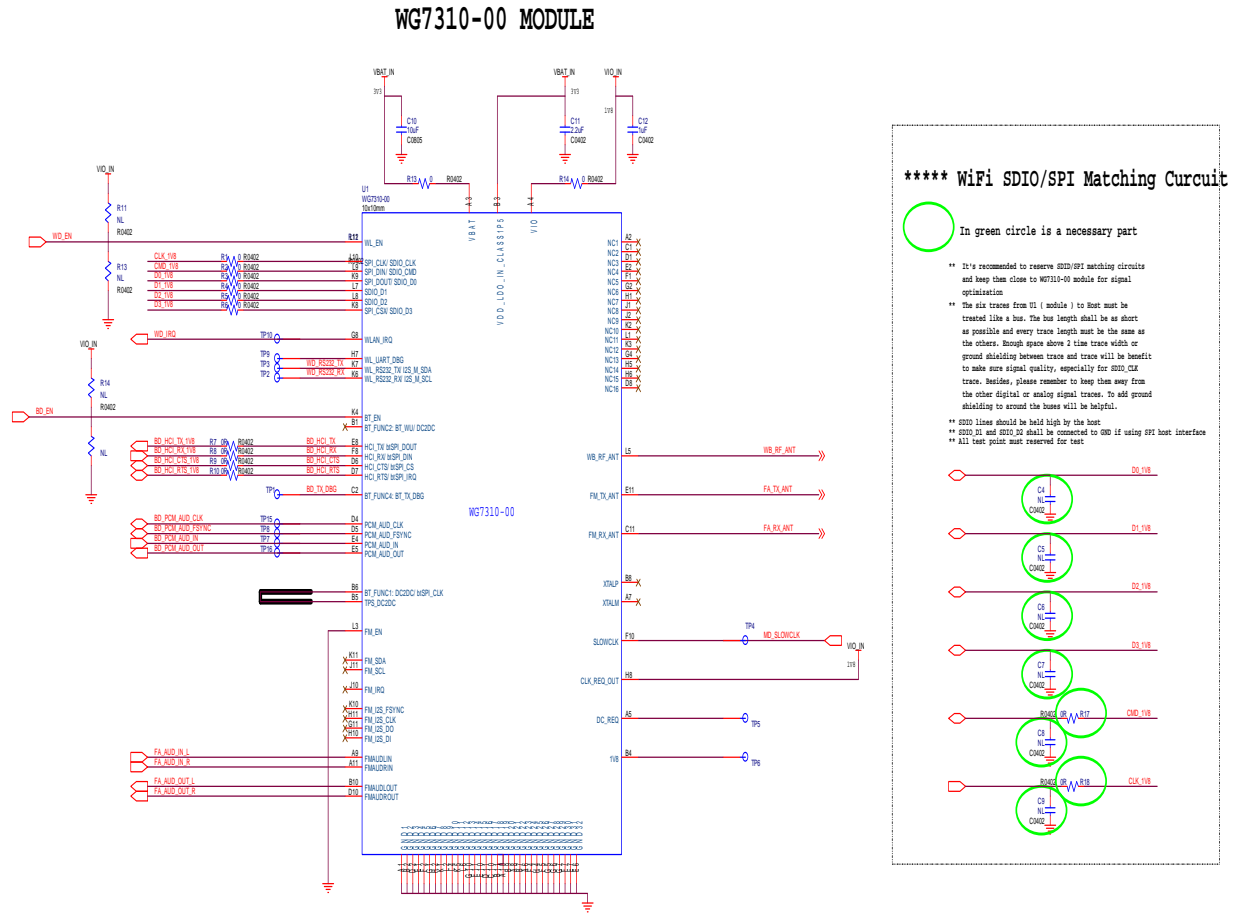
8.1. WLAN RS232 Testing Port

“Direct” serial interface (RS232_TX, RS232_RX) used by WLAN TrioScope software package for WLAN RF performance test, debug and manufacturing application.

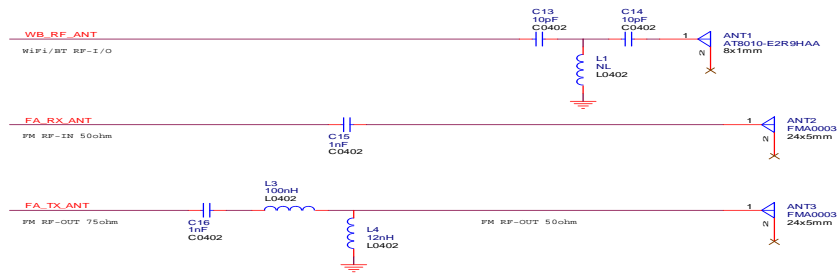
8.2. Bluetooth HCI Testing Port

HCI_TX and HCI_RX are used by Bluetooth “HCI Tester” software package for Bluetooth RF performance test, debug and manufacturing application.

9. Reference Schematic

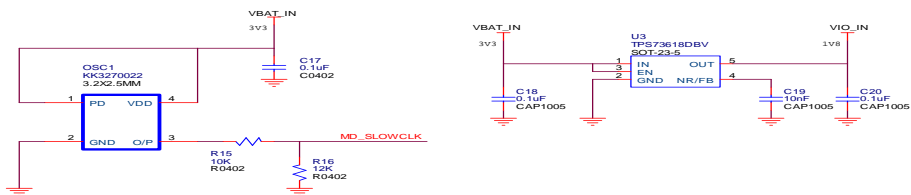


ANTENNA CIRCUITS

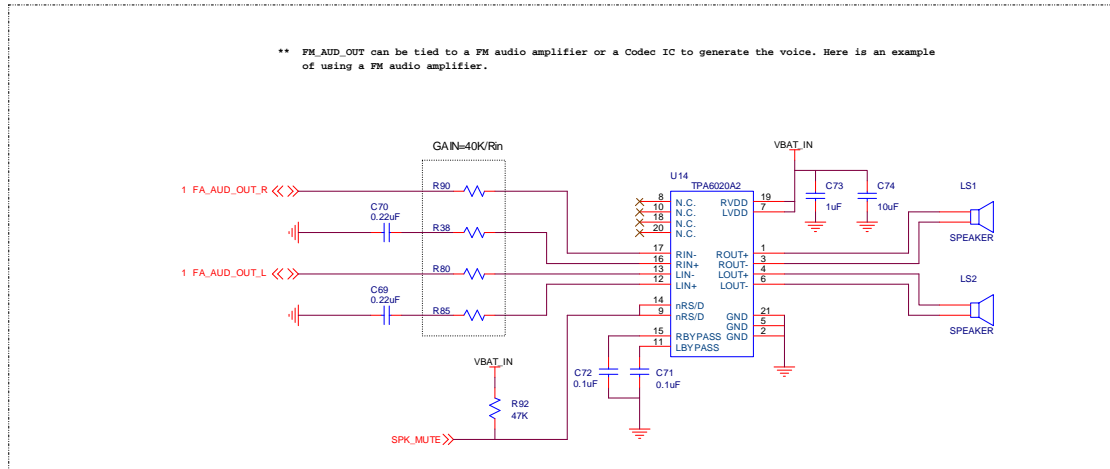


32.768K XOSC

1.8V LDO

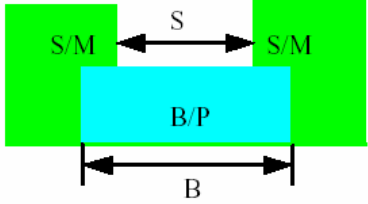


1V8 FM AUDIO Output (Option)



10. Layout Recommendation

10.1. Recommended Bump Pad Design

	Item	Recommend	Unit
	"B" Bump pad diameter on SMD PCB	600	um
	"S" Solder Mask Opening	400	um

Recommended Bump Pad Design for WG7310

COMMENT:

SMD = Solder Mask Define

S/M= Solder Mask

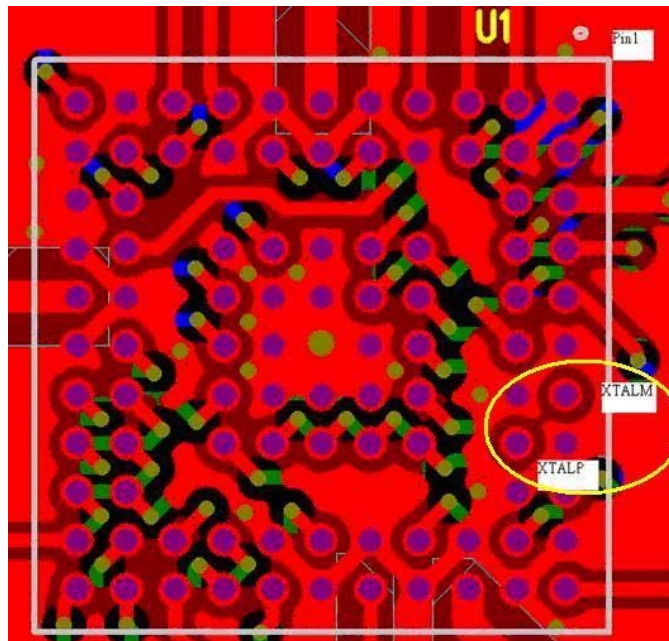
B/P= Bump Pad

10.2. Recommended Stencil Design

The bump pad size, it's solder mask opening and the relevant stencil Via diameter described in **Section 10.1** and **Section 10.2** shall be followed completely otherwise the module mounting yield rate couldn't be insured. The recommended stencil via diameter is 570um.

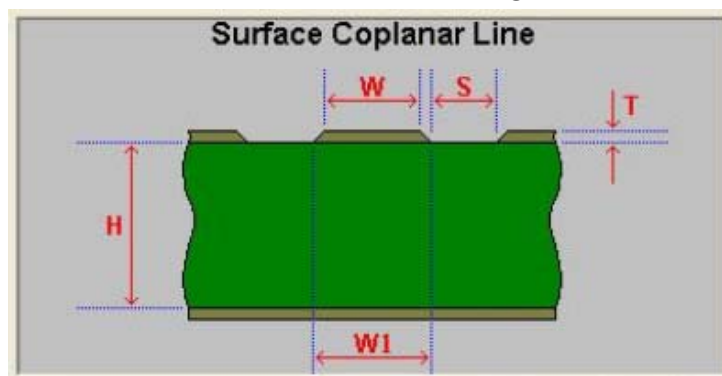
10.3. Recommended Trace Layout

- **XTALP and XTALM**
 - Having ground plane in Layer2 under the two floating pins to avoid unwanted central frequency offset



- **Digital Signals Layout**
 - SDIO signals traces (CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible.
 - SDIO/SPI Clock, Audio Clock (PCM_AUD_CLK), FM I2S Clock (FM_I2S_CLK), FM I2C Clock (FM_SCL), these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.

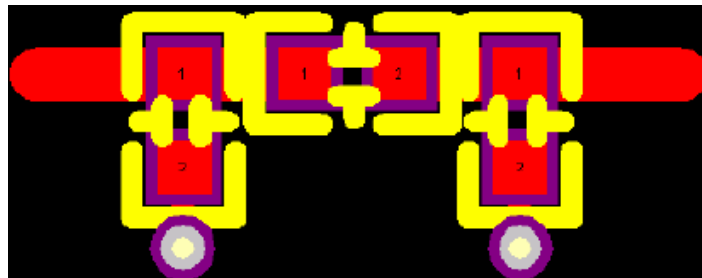
- **RF Trace & Antenna**
 - 50 ohm trace impedance match on the trace to the antenna.
 - Recommended 50ohm trace design for PCB layout



Height Between L1 and L2 (H): 10.0 mil

Trace (W):	14.3 mil
(W1):	14.3 mil
Thickness (T):	2.1 mil
Separation (S):	10.0 mil
Dielectric (Er):	4.3

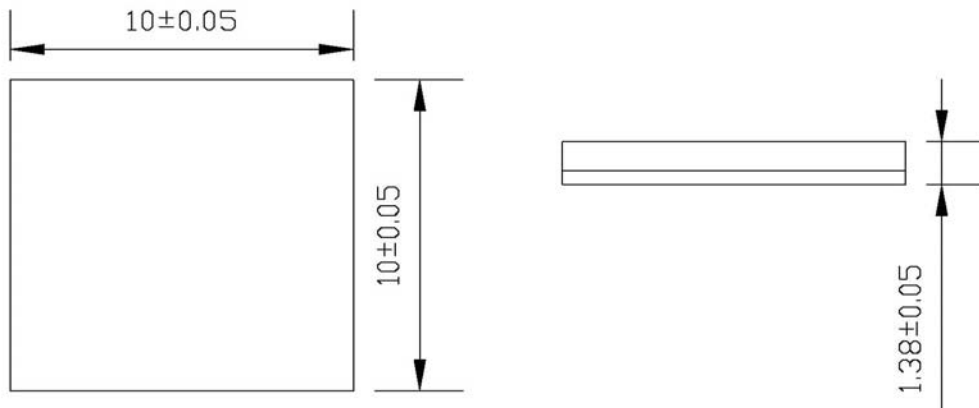
- Move all the high-speed traces and components far away from the antenna.
- Check ANT vendor for the layout guideline and clearance.
- Matching circuit layout should be as following figure.



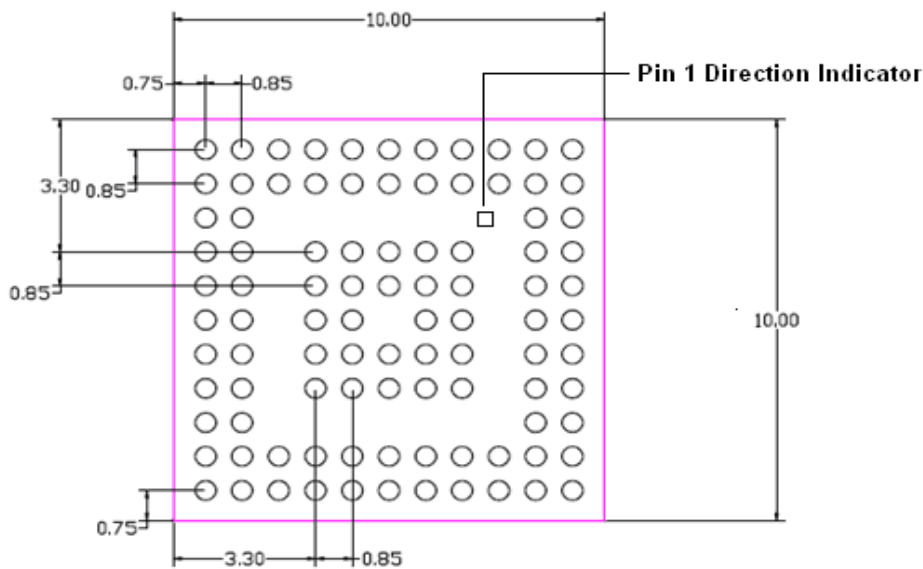
- **Power Trace**
 - Power trace for VBAT should be 40mil wide. 1.8V trace should be 18mil wide.
- **Ground**
 - Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation as following figure.
 - Have a complete Ground pour in layer 2 for thermal dissipation.
 - Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
 - Move GND vias close to the pad.
- **Slow Clock**
 - FM RF module uses the 32-kHz clock, it is extremely important that the slow-clock trace not be routed next to any digital signals.
 - The slow clock trace should not be routed above or below digital signals on other layers.

11. PACKAGE INFORMATION

11.1. Module Mechanical Outline



Top and Side View



unit: mm

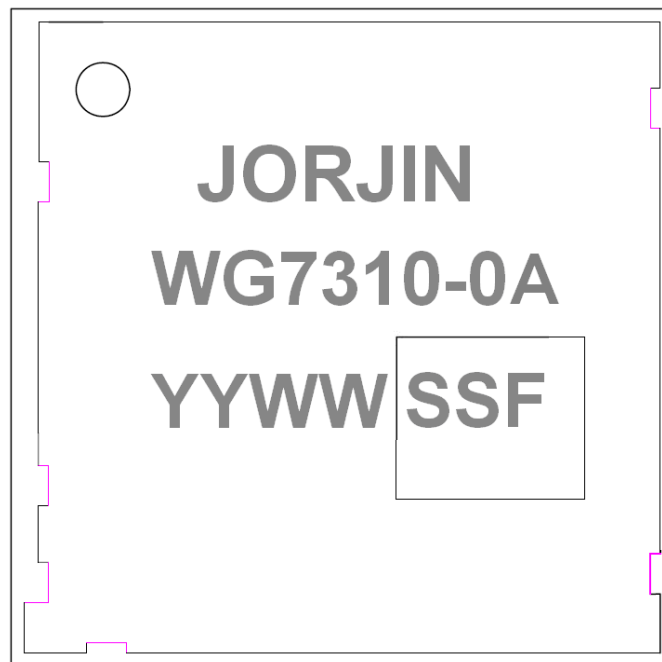
Bottom View

- Pin array = 11x11
- Pin number = 96 pins
- Bump pitch = 0.85mm
- Bump diameter = 0.5mm
- Dimension tolerance ± 0.05 mm

11.2. Ordering Information

Part number:	WG7310-0A
--------------	-----------

11.3. Package Marking



Date Code: **YYWWSSF**

YY = Digit of the year, ex: 2008=08

WW = Week (01~53)

SS = Serial number from 01 ~99 match to manufacture's lot number

F = Reserve for internal use

12. SMT and Baking Recommendation

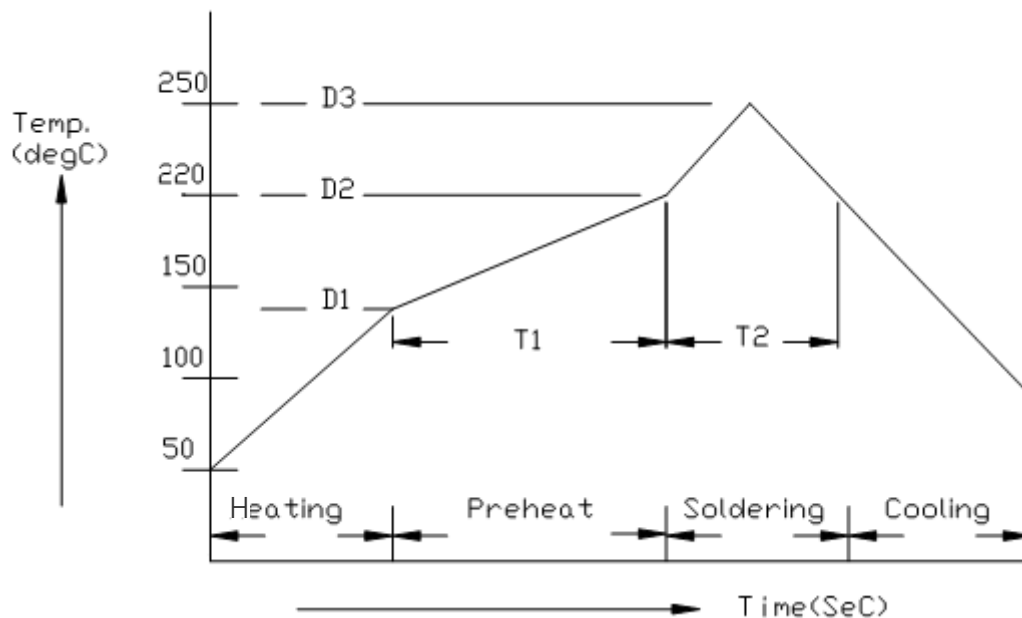
12.1. Baking Recommendation

- Baking condition :
 - Follow MSL Level 4 to do baking process.
 - After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within 72 hours of factory conditions <math> < 30^{\circ}\text{C}/60\% \text{ RH}</math>, or
 - b) Stored at <math> < 10\% \text{ RH}</math>.
 - Devices require bake, before mounting, if Humidity Indicator Card reads >10%

If baking is required, Devices may be baked for 8 hrs at 125 °C.

12.2. SMT Recommendation

- Recommended Reflow profile :



No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.
 (2) Add Nitrogen while Reflow process : SMT solder ability will be better.

- **Stencil thickness** : 0.1~ 0.15 mm (Recommended)
- **Soldering paste (without Pb)** : Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

13. History Change

Revision	Date	Description
R 0.1	2010/10/4	Release 0.1
R 0.2	2011/05/04	Update the FM RF characteristics
R 0.3	2011/06/20	Update the power consumption Update the WIFI & BT power on sequence Update the HCI interface Timing chart.