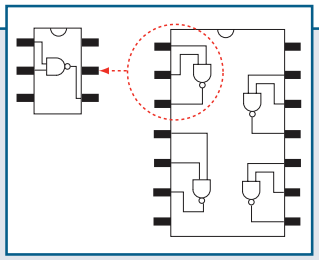
FAIRCHILD SEMICONDUCTOR®

TinyLogic®

Fairchild's Offering

Fairchild's TinyLogic® family consists of a broad spectrum of high speed, low power, CMOS single and dual gate logic functions in a choice of six space saving packages: SOT23-5, SC70 6-lead, US8 8-lead, and MicroPak 6 and 8 terminal leadless packages.

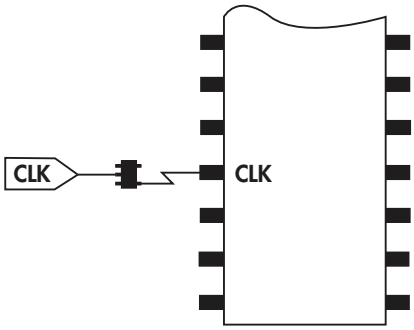
TinyLogic can facilitate efficient system designs in any application. Placement of single and dual logic functions exactly where needed simplifies signal routing while minimizing propagation delays and noise generation.



Benefits

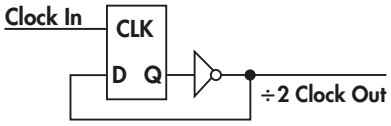
- Reduces routing complexity
- Allows shorter metal traces to minimize EMI generation
- Prevents unnecessary power consumption from unused gates
- HS and HST family intended for 5V or very low speed applications
- UHS family ideal for high speed, low voltage operation
- ULP family ideal for extremely high speed low voltage operation
- ULPA family ideal for low power consumption, low voltage operation

Single Gate for Added Clock Frequency and Buffering



Use a single-gate inverter, such as NC7SZ04M5 or NC7SZ14M5, to clean clock signals traveling lengthy distances across a board or when signals are compromised by layout conditions. Buffering a clock signal near its destination ensures signal integrity.

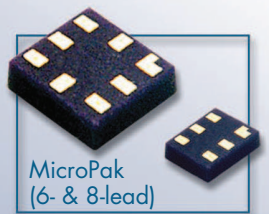
Utilizing Fairchild's TinyLogic parts NC7SZ374 and NC7SZ04 enables the additional clock.



Family Comparison

Family	Standard Logic Family Equivalent	I_{cc} (µA)	V_{cc} (V)	Drive (mA @ V)	Speed (ns @ V)
HS	HC	10	2–6	±1.1 @ 3.0; ±2.0 @ 4.5	25 @ 4.5
HST	HCT	10	4.5–5.5	±2.0 @ 4.5	20 @ 2.0
UHS	LCX/LVC	20	1.8–5.5	±4.0 @ 1.65; ±24.0 @ 3.3	4.7 @ 3.3
ULP		0.9	0.9–3.6	±1.0 @ 1.5; ±2.6 @ 3.0	16 @ 1.5; 7.0 @ 3.3
ULP-A	VCX	0.9	0.9–3.6	±4.0 @ 1.5; 24.0 @ 3.3	7.2 @ 1.5


SOT23, SC70 (5- & 6-lead)


MicroPak (6- & 8-lead)


US8

Note: package photos are not to scale.

the power franchise™

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Functional Description (S Single-Bit Logic; W Dual-Bit Logic; N Triple-Bit Logic)	Device Type	Family				Packages					
		HS (NC7)	HST (NC7xT)	UHS (NC7xZ)	ULP/ ULP-A (NC7xP/ NC7xV)	SOT23 5-lead	SC70 5-lead	SC70 6-lead	US8 8-lead	MicroPak 6-lead	MicroPak 8-lead
NAND Gate	00	S	S	S W	S W	S	S		W	S	W
NOR Gate	02	S	S	S W	S W	S	S		W	S	W
Inverter	04	S	S	S W N	S W N	S	S	W	N	S W	N
Unbuffered Inverter	U04	S		S W N	S	S	S	W	N	S W	N
Inverter w/ Open Drain Output	05			S	S	S	S			S	
Buffer w/ Open Drain Output	07			W	W			W		W	
AND Gate	08	S	S	S W	S W	S	S		W	S	W
3-Input NAND Gate	10			S				S		S	
3-Input AND Gate	11			S	S			S		S	
Inverter w/ Schmitt Trigger Input	14	S		S W N	S W N	S	S	W	N	S W	N
Dual Buffer	16			W				W		W	
Buffer w/ Schmitt Trigger Input	17			W N	S W		S	W	N	S W	N
1 of 2 Demux w/ 3-STATE Output	18			S				S		S	
1 of 2 Decoder/Demultiplexer	19				S			S		S	
3-Input NOR Gate	27			S				S		S	
OR Gate	32	S	S	S W	S W		S		W	S	W
Buffer	34			N	S N		S		N	S	N
NAND Gate w/ Open Drain Output	38			S W	S W		S	S	W	S	W
Universal Configurable 2-Input Gate	57			S	S			S		S	
Universal Configurable 2-Input Gate	58			S	S					S	
D Flip-Flop w/ Pre-Set and Clear	74			S	S				S		S
XOR Gate	86	S	S	S W	S W	S	S		W	S	W
Buffer w/ Low-Enabled 3-STATE Output	125			S W	S W	S	S		W	S	W
Buffer w/ High-Enabled 3-STATE Output	126			S W	S W	S	S		W	S	W
NAND Gate w/ Schmitt Trigger Input	132			W	W				W		W
2-Input Non-Inverting Multiplexer	157			S	S			S		S	
2-Input Inverting Multiplexer	158				S			S		S	
D Flip-Flop w/ Asynchronous Clear	175			S				S		S	
Inverting Buffer w/ 3-STATE Output	240			W	W				W		W
Inverting Buffer w/ High-/ Low-Enabled 3-STATE Output	241			W	W				W		W
3-Input OR Gate	332			S				S		S	
D Latch w/ 3-STATE Output	373			S				S		S	
D Flip-Flop w/ 3-STATE Output	374			S				S		S	
3-Input XOR Gate	386			S				S		S	

Note: x is a variable (either S, W, or N).