Analog for Altera FPGAs

Solutions Guide

national.com/altera

2010 Vol. 1

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- Power Limiting
- Signal Conditioning
- Wireless Rx/Tx
- SerDes
- Ethernet
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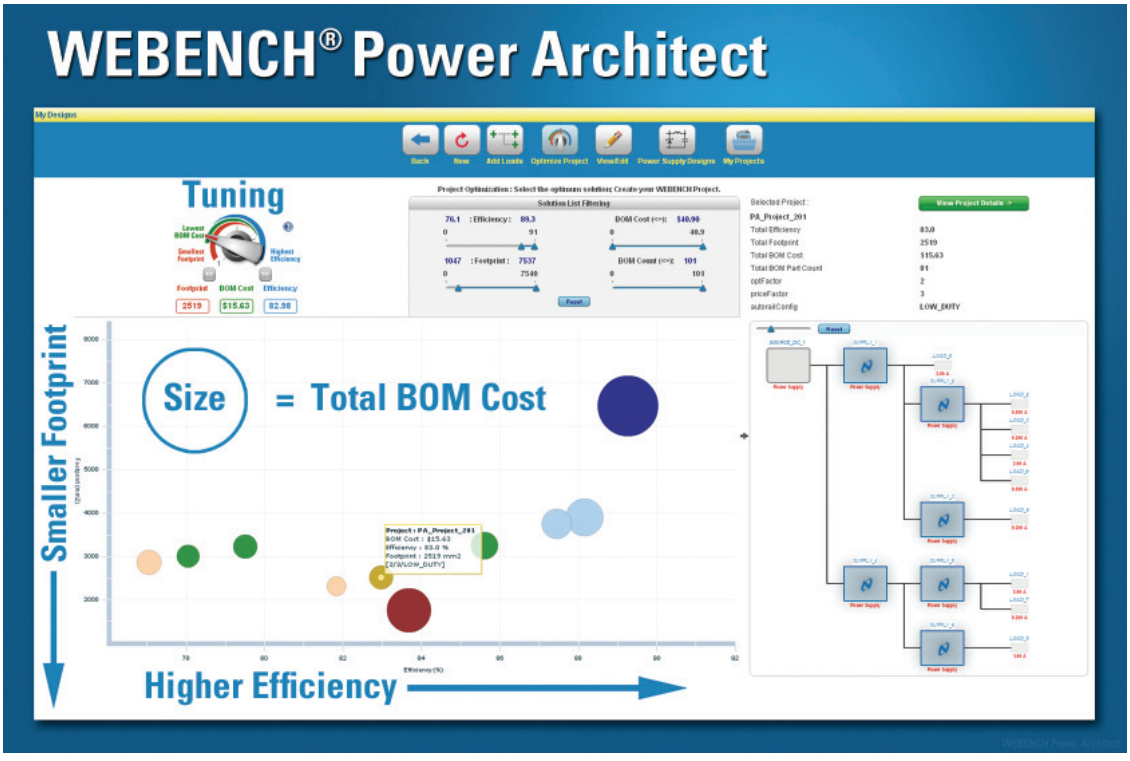
PowerWise®

National Semiconductor

Solutions for Altera FPGAs

Altera FPGAs include high logic densities and extensive I/O capability allowing them to fit a multitude of applications. With core processing algorithms implemented in the digital fabric, analog ICs interface them to the external world. National Semiconductor, a leader in high-performance, energy-efficient solutions, offers a broad product portfolio to complement Altera FPGAs. National provides power, analog signal conditioning, data converters, and serial data-transfer solutions to meet the needs of technically-demanding applications for displays, communications infrastructure and electronics such as medical, automotive, and test and measurement devices.

For the latest from National Semiconductor for Altera FPGAs see: **national.com/altera**



WEBENCH® Power Architect is the industry's first design tool to create, model, and implement multiple-output, high-performance DC-DC power supplies for an entire system. WEBENCH Power Architect can instantly optimize multiple power supplies across several performance parameters including topology, intermediate voltage rails, footprint, efficiency, component count, and bill of materials (BOM) cost.

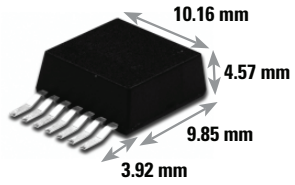
This is especially useful for FPGA system designers as there are always multiple loads to power. By using WEBENCH Power Architect, system designers can get a complete, end-to-end power supply for their entire product. The tool generates a system summary report including schematics, BOMs, and electrical operating values. Users can also run simulations and alter the chosen components.

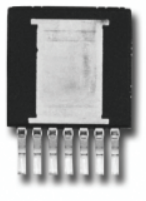
To start your design, visit: **national.com/powerarchitect**

SIMPLE SWITCHER® Power Module Families

Product ID	Input Voltage (V)	Output Voltage (V)	Output Current (A)	Peak Efficiency
LMZ10504	2.95 to 5.5	0.8 to 5	4	96% (3.3V to 1.2V)
LMZ12003	4.5 to 20	0.8 to 6	3	92% (12V to 3.3V)
LMZ14203	6 to 42	0.8 to 6	3	90% (24V to 3.3V)

- Supports needs unique to FPGAs
  - Startup into pre-biased loads with monotonic rise
  - Soft-start limits inrush current
  - 2% output voltage accuracy over full temperature range
  - Chip enable to sequence individual supplies
- Ease-of-use package: one solid exposed pad on bottom with standard IC leads
- Best-in-class thermal performance – no airflow required
- Low EMI with shielded inductor (EN55022 Class B compliant)
- Fully WEBENCH® enabled





See **national.com/switcher**

Powering Altera FPGAs

National's Power Expert tool automatically finds National power solutions for your design and populates the online WEBENCH® environment to quickly design, simulate and build a prototype. Otherwise, the following tables are a guide to help you in choosing an appropriate voltage regulator for your FPGA's specific needs.

See: **national.com/analog/altera/power_expert**

V_{CCINT} / V_{CC}

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
Cyclone IV (GX), Cyclone III - 1.2V		
<0.5A	**LP38851 (LDO), LM2830 LM3671**	**LM2734, LM3103**
1A	**LM2831, LM3678**	**LM2734, LM3100, LM20242**
2A/3A	**LM2832 LM2852, LM20123/33/43** LMZ10504 (4A)	**LM3102, LM20323/33/43, LM27342** LMZ12003
5A	**LM2854 (4A) LM20125/45, LM21305**	**LM21305** LM2743, LM3150
10A	**LM2743,** LM3743 , LM3495	**LM2743, LM3150,** LM3495
20A+	**LM2743,** LM3000, LM3753/54	**LM2743,** LM3000, LM3753/54

V_{CCINT} / V_{CC}

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
Stratix III (GX and E), Stratix IV (GX and E) - 0.9V, Stratix IV GT - 0.95V, Arria II - 0.9V, Cyclone IV (E) - 1.0V, Stratix III (GT) - 1.1V		
1A	**LM2831**	**LM2734, LM3100, LM20242**
2A/3A	**LM2832 LM2852, LM20123/33/43** LMZ10504 (4A)	**LM2738 (1.5A) LM3102, LM20323/33/43** LMZ12003
5A	**LM2854 (4A) LM20125/45, LM21305**	**LM21305** LM2743, LM3150
10A	**LM2743** LM3000, LM3743	**LM2743, LM3150** LM3000, LM3495
20A+	**LM2743,** LM3000, LM3753/54	**LM2743,** LM3000, LM3753/54

Legend

■ Non Sync ■ Sync Reg ■ Power Module ■ Controller **BOLD** = WEBENCH Enabled

Powering FPGAs

V_{CCIO} = 1.5V

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
<0.5A	**LM2830, LP38852 (LDO)** **LM3671**	**LM2734, LM22671/74** **LM3103**
1A	**LM2831** **LM2852**	**LM2738, LM22672/75** **LM3100, LM20242**
2A/3A	**LM2832** **LM2853, LM20123/33/43**	**LM22680** **LM3102, LM20323/33/43, LM27342,** LMZ12003
5A	**LM20125/45, LM21305**	**LM22677/78/79** **LM21305,** LM3150
10A	**LM2743,** LM3743	**LM2743, LM3150**
20A+	**LM2743** LM5642/X, LM3753/54	**LM2743,** LM25116, LM3753/54, LM5642/X

V_{CCIO} = 1.8V

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
<0.5A	**LM2830, LP38852 (LDO)** **LM3671**	**LM2734, LM22671/74** **LM3103**
1A	**LM2831** **LM2852**	**LM2738, LM22672/75** **LM3100, LM20242**
2A/3A	**LM2832** **LM2853, LM20123/33/43**	**LM22680** **LM3102, LM20323/33/43, LM27342,** LMZ12003
5A	**LM20125/45, LM21305**	**LM22677/78/79** **LM21305,** LM3150
10A	**LM2743,** LM3743	**LM2743, LM3150**
20A+	**LM2743** LM5642/X, LM3753/54	**LM2743,** LM25116, LM3753/54, LM5642/X

V_{CCIO} = 2.5V

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
<0.5A	**LM2830, LP38852 (LDO)** **LM3671**	**LM2734, LM22671/74** **LM3103**
1A	**LM2831** **LM2852**	**LM2738, LM22672/75** **LM3100, LM20242**
2A/3A	**LM2832** **LM2853, LM20123/33/43**	**LM22680** **LM3102, LM20323/33/43, LM27342,** LMZ12003
5A	**LM20125/45, LM21305**	**LM22677/78/79** **LM21305,** LM3150
10A	**LM2743,** LM3743	**LM2743, LM3150**
20A+	**LM2743** LM5642/X, LM3753/54	**LM2743,** LM25116, LM3753/54, LM5642/X

V_{CCIO} = 3.3V

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
<0.5A	**LM2830, LP38852 (LDO)** **LM3671**	**LM2734, LM22671/74** **LM3103**
1A	**LM2831** **LM2852**	**LM2738, LM22672/75** **LM3100, LM20242**
2A/3A	**LM2832** **LM2853, LM20123/33/43**	**LM22680** **LM3102, LM20323/33/43, LM27342,** LMZ12003
5A	**LM20125/45, LM21305**	**LM22677/78/79** **LM21305,** LM3150
10A	**LM2743,** LM3743	**LM2743, LM3150**
20A+	**LM2743** LM5642/X, LM3753/54	**LM2743,** LM25116, LM3753/54, LM5642/X

Legend

■ Non Sync ■ Sync Reg ■ Power Module ■ Controller **BOLD** = WEBENCH Enabled

V_{CCA} / V_{CCAUX}

I_{OUT}	V_{IN} ≤ 5V	V_{IN} 12V +
<0.5A	LP3878 (LDO), LP38502 (LDO), LM2830 LM3671	LM2734, LM22671/74, LM25574 LM3103
1A	LM2832 LM2852	LM2738, LM22672/75 LM3100, LM20242
2A/3A	LM2853 LM20123/33/43 LMZ10504 (4A)	LM22680, LM3102, LM20323/33/43, LM27342 LMZ12003
5A	LM20125/45, LM21305	LM21305 LM3150

WEBENCH® Online Design Environment

WEBENCH online design and prototyping tools deliver results faster than ever. Design, optimize, generate your prototype, and download your test vectors – all online.

- ✓ **Select It**
- ✓ **Design It**
- ✓ **Analyze It**
- ✓ **Build It**

And do it all for free, anywhere, anytime.

national.com/webench

Legend

■ Non Sync ■ Sync Reg ■ Power Module ■ Controller **BOLD** = WEBENCH Enabled

Multi-Output FPGA Power Supply Solutions

Key PMIC Selection Criteria	LM26480	LP3906	LP3907	LM26400Y	LM26420	LM26484
Number of Bucks	2	2	2	2	2	2
Buck Output Current	1500 mA	1500 mA	1000/600 mA	2000 mA	2000 mA	2000 mA
Input Voltage Range	2.8V to 5.5V	2.7V to 5.5V	2.8V to 5.5V	3.0V to 20V	3.0V to 5.5V	3.0V to 5.5V
Voltage Output(s)	ADJ	I²C or factory programmable	I²C or factory programmable	ADJ	ADJ	ADJ
Number of LDOs	2	2	2	—	0	1
LDO Output Current	300 mA	300 mA	300 mA	—	—	1000 mA
NPOR (PGood)	—	—	✔	✔	✔	✔
Sync (Input)	—	✔	—	—	—	—
Battery Runtime Enhancement (DVM)	—	✔	✔	—	—	—
Feature Programmability	—	✔	✔	—	—	—
Control Interface	—	I²C	I²C	—	—	—
Packaging (mm)	4x5 LLP-24	5x5 LLP-24	4x4 LLP-24	5x5 LLP-16	5x5 LLP-16	5x4 LLP-24

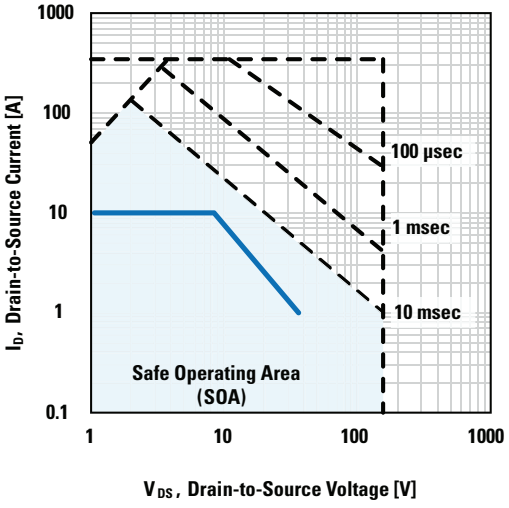
Powering FPGAs and Power Limiting

Memory Solutions (VTT) and Reference (VREF)

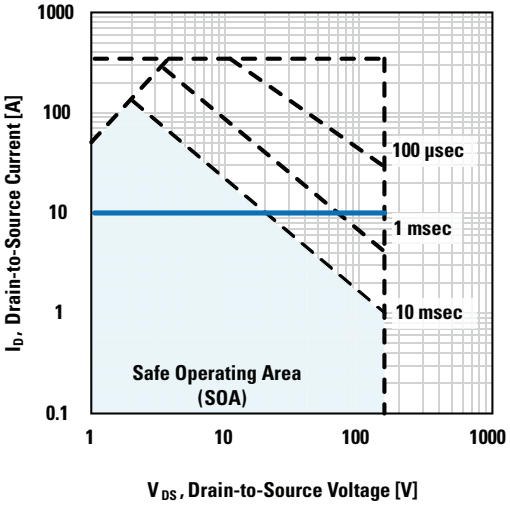
Product ID	Input Max Voltage (V)	Input (PVIN) Min Voltage (V)	Output Current (mA)	Standards	Enable	Suspend to RAM
LP2998	5.5	1.8	Up to 1500	DDR, DDR-II, DDR-III	Y	Y
LM2744	16	1	5000+	DDR, DDR-II, DDR-III	Y	Y

Power Limiting Protects External Pass Device for Improved System Reliability

To ensure system reliability, any MOSFET must operate within its Safe Operating Area (SOA) in order to avoid FET failure. National's LM(2)506x hot swap controllers provide both current and power limiting to dynamically adjust the current limit at large V_{DS} and ensure the MOSFET stays in the SOA at all conditions – maximizing long-term system reliability and robustness.



Conventional Hot Swap: Current Limit Only MOSFET Out of SOA at Large V_{DS}



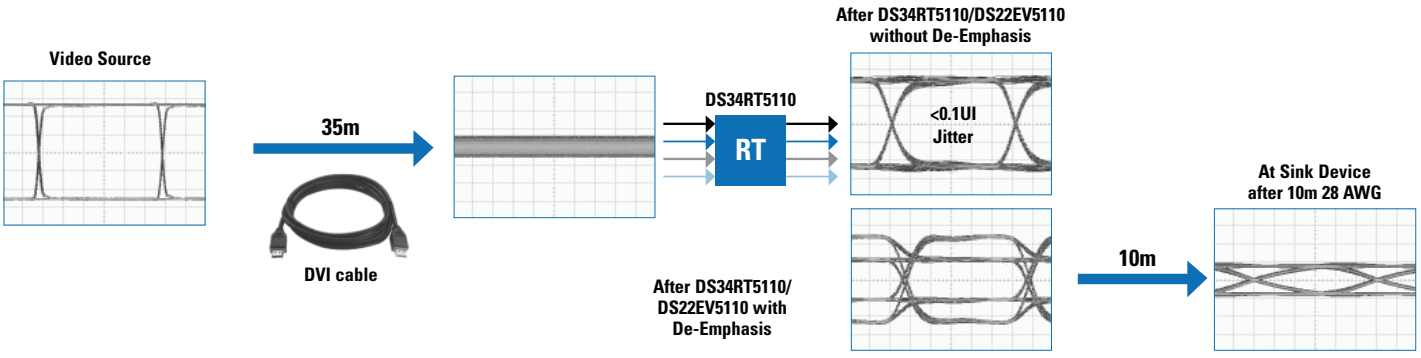
LM(2)506x: Current Limit and Power Limit Optimal Circuit and MOSFET Protection for All V_{DS}

Hot Swap/In-Rush Current Controllers

Product ID	V_{IN} Range (V)	POWER GOOD	PMBus Support	Adj UVLO	Adj OVLO	Active In-Rush Current Limit	Active Current Limiting	Active Power Limiting	EVK
LM5067 [E]	-9 to -80	V_{DS}		✔	✔	✔	✔	✔	LM5067EVAL
LM5069 [E]	+9 to +80	V_{DS}		✔	✔	✔	✔	✔	LM5069EVAL
LM25061 [E]	+2.9 to +17	V_{OUT}(adj)		✔		✔	✔	✔	LM25061MM-2EVAL
LM25066	+2.9 to +17	V_{DS}	✔	✔	✔	✔	✔	✔	Coming soon
LM25069 [E]	+2.9 to +17	V_{DS}		✔	✔	✔	✔	✔	LM25069MM-2EVAL

[E] Evaluation board

Signal Conditioning and Wireless Rx/Tx



Signal Conditioning for High-Speed Transceivers (GX and GT)

Product ID	Function	Channels	Input Compatibility	Output	De-Emphasis (dB)	Receive Equalization (dB)	Max Speed/ Ch (Mbps)	EVK
DS50PCI401	SAS / SATA	8	CML	CML	Up to -12	Up to 26.3	5000	DS50PCI401
DS64BR401	PCIExpress	8	CML	CML	Up to -13	Up to 28.4	6400	DS64BVR401EVK
DS50EV401	PCIExpress Quad settable	4	CML	CML	—	20	8000	DS50EV401
DS64EV400SQ	EQ	4	CML	CML	—	Up to 20	10000	DS64EV400-EVK
DS64EV100SD	Settable EQ	1	CML	CML	—	Up to 20	10000	DS64EV100-EVK
DS16EV5110A	HDMI/DVI	3 (TMDS)	LVDS/CML/LVPECL	CML	—	Up to 30	2250	DS16EV51-AEVKC
DS34RT5110	HDMI / DVI	3 (TMDS)	LVDS/CML/LVPECL	CML	Up to -9	Up to 27	2250	DS34RT5110-EVKH DS34RT4110-EVKC
DS22EV5110	HDMI / DVI	3 (TMDS)	LVDS/CML/LVPECL	CML	Up to -9	Up to 30	3400	DS22EV100-EVKH DS22EV100-EVKC

Wireless Rx/Tx

The explosive growth of mobile handsets coupled with users' appetite for bandwidth continues to drive ever increasing demands from the wireless infrastructure. National Semiconductor offers reference designs for wireless basestation (BTS) radio systems.

"RD-179" is a high IF receiver subsystem for up to 192 MHz input signals.	"RD-170" is a low IF receiver subsystem for up to 52 MHz input signals.	"RD-146" is a high IF receiver circuit with variable gain IF amplification. It provides excellent sensitivity for input signal up to 240 MHz.
Performance for a 192 MHz input signal: • **Small-signal SNR of 72.7 dBFS and SFDR > 92 dBFS** • **Large-signal SNR of 71 dBFS and SFDR > 80 dBFS**	Performance for a 52 MHz input signal: • Small-signal SNR of 78.0 dBFS and SFDR > 94 dBFS • Large-signal SNR of 75.8 dBFS and SFDR > 84 dBFS	Performance for a 169 MHz input signal: • Small-signal SNR of 72 dBFS and SFDR greater than 90 dBFS • Large-signal SNR of 68.3 dBFS and SFDR of 77 dBFS

See these reference designs at: **national.com/refdesigns**
See the video on high IF/high sensitivity radio receiver design at: **http://bit.ly/6VQLmc**

Serializers and Deserializers

World's Most Robust Serial Interface Solutions for Industrial Imaging, Display, and Control Applications

Features

- Wide operating frequency
- Integrated signal conditioning
- Send raw data easily
- No reference clock required
- FPGA friendly
- Low EMI, high ESD protection
- Supports FR-4, cable, fiber

See **national.com/lvds**

SerDes Families

Family	Typ Reach at 1.5 Gbps over CAT-5	Signal Conditioning	Embedded DC-Balance	Product ID Serializer	Product ID Deserializer	Parallel Width	Parallel I/O	Min Freq (MHz)	Max Freq (MHz)	Mux Ratio
FPGA-Link	40m	Advanced Rx EQ, Tx driver redundant I/Os retimed serial output	✔	**DS32EL0421**	**DS32EL0124**	5	LVDS	125	312.5	ANY:1
			✔	**DS32ELX0421**	**DS32ELX0124**	5	LVDS	125	312.5	ANY:1
Channel-Link II	10m	Moderate Rx EQ, Tx driver	—	**DS92LV1021A**	**DS92LV1212A**	10	LVCMOS	16	40	10:1
			—	**SCAN921025H**	**SCAN921226H**	10	LVCMOS	20	80	10:1
			—	**SCAN928028**	**SCAN926260**	nx10	LVCMOS	25/16	66	10:1
			—	**DS92LV16**	**DS92LV16**	16	LVCMOS	25	80	16:1
			—	**DS92LV18**	**DS92LV18**	18	LVCMOS	15	66	18:1
			—	**DS99R103**	**DS99R104**	24	LVCMOS	3	40	24:1
			✔	**DS90UR241Q**	**DS90UR124Q**	24	LVCMOS	5	43	24:1
			✔ NEW	**DS92LV3241**	**DS92LV3242**	32	LVCMOS	20	85	32:4
			✔ NEW	**DS92LV3221**	**DS92LV3222**	32	LVCMOS	20	50	32:2
8-bit/10-bit SerDes	N/A	Moderate Rx EQ, Tx driver	✔	**SCAN25100**	**SCAN25100**	10	LVCMOS	30.72	122.88	10:1

FPD-Link II with Embedded Clock

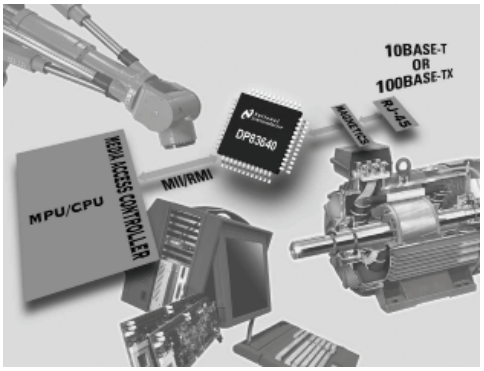
Product ID	Color Depth	Function	Pixel Clock (MHz)	Throughput (Mbps)	Connectivity (Input to Output)	EMI Reduction	Temp (°C)	Packaging
DS90C241Q [E]	18	Serializer	5 to 35	840	LVCMOS to FPD-Link II		-40 to 105	TQFP-48
DS90C124Q [E]		Deserializer	5 to 35	840	FPD-Link II to LVCMOS	Progressive Turn On (PTO) slew rate control	-40 to 105	TQFP-48
DS90UR241Q [E]		Serializer	5 to 43	1032	LVCMOS to FPD-Link II		-40 to 105	TQFP-48
DS90UR124Q [E]		Deserializer	5 to 43	1032	FPD-Link II to LVCMOS	Adjustable PTO slew rate control	-40 to 105	TQFP-64
DS99R421Q [E]		Serializer	5 to 43	1032	FPD-Link to FPD-Link II	LVDS inputs (FPD-Link)	-40 to 105	LLP-36
NEW **DS90UR905Q**	24	Serializer	5 to 65	1560	LVCMOS to FPD-Link II	SSC compatible	-40 to 105	LLP-48
NEW **DS90UR906Q**		Deserializer	5 to 65	1560	FPD-Link II to LVCMOS	SSCG, RDS, PTO	-40 to 105	LLP-60
NEW **DS90UR907Q**		Serializer	5 to 65	1560	FPD-Link II to FPD-Link II	LVDS inputs	-40 to 105	LLP-36
NEW **DS90UR908Q**		Deserializer	5 to 65	1560	FPD-Link II to FPD-Link	SSCG, LVDS outputs	-40 to 105	LLP-48

PowerWise® product [E] Evaluation board

Ethernet

PHYTER® 10/100 Ethernet PHYs

- IEEE1588 v1 and v2 precision time protocol support (DP83640)
  - Enable IEEE 1588 with any MAC-based FPGA, ASIC or microcontroller
  - Node synchronization accuracy to < 10 nS
  - Replace E1/T1 lines and expensive GPS clocks
  - Synchronized clock output
  - Synchronous Ethernet support
  - Industry's lowest deterministic latency



Product ID	Interface	Temp Range (°C)	JTAG	Software Utility	Features
DP83640	MII/RMII	-40 to 85	✔	✔	IEEE 1588 v1 and v2; TDR (Time Domain Reflectometry) cable diagnostics; includes sample code
DP83848C	MII/RMII/SNI	0 to 70	✔	✔	9x9x1.4
DP83848J/K	MII/RMII	0 to 70 / -40 to 85	✔		PHYTER mini (6x6x0.8)
DP83849C/IF	MII/RMII	0 to 70 / -40 to 85	✔	✔	Dual PHYTER (dual transceivers)

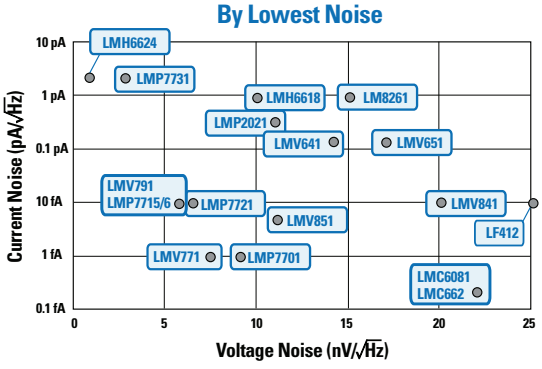
For design information, visit: **national.com/analog/interface/refdesign_demoboards**
See "IEEE1588 Time Sync Demo" at: **http://bit.ly/8qM1O**
See "How To Synchronize Networks with IEEE1588" at: **http://bit.ly/PTPNetworkSync**

The Signal Path

Amplifiers

The signal path consists of, at a minimum, a sensor, an amplifier, and an ADC. This subsystem is used in sensing and detecting precise changes in the external world. The graph at the right serves as a starting point for the designer to quickly choose an amplifier based on flat-band noise density. For clarity, only a selection of op amps suitable for precision applications is shown in the graph. Duals and quads are also available.

See the video on amplifier selection at: **http://bit.ly/7t7tBu**



Data Conversion

Up to 1000 kSPS

8- to 16-bit ADCs and DACs
- Low-power, energy-efficient PowerWise® products
- Pin-and-function compatibility for easy selection
- ADCs guaranteed over sample rate
- Small packaging
- Single-ended input I²C compatible, single-ended input SPI and differential-input SPI

Up to 500 MSPS

8- to 16-bit ADCs
- High-input bandwidth
- Energy-efficient PowerWise products
- Outputs available: CMOS, parallel LVDS, and serial LVDS

Up to 3 GSPS

10-bit ADCs up to 2 GSPS and 8-bit ADCs
- Best-in-class performance vs power
- Energy-efficient PowerWise products
- Full-power bandwidth beyond 3 GHz (ADC083000)

For more information, visit: **national.com/adc**

national.com/altera

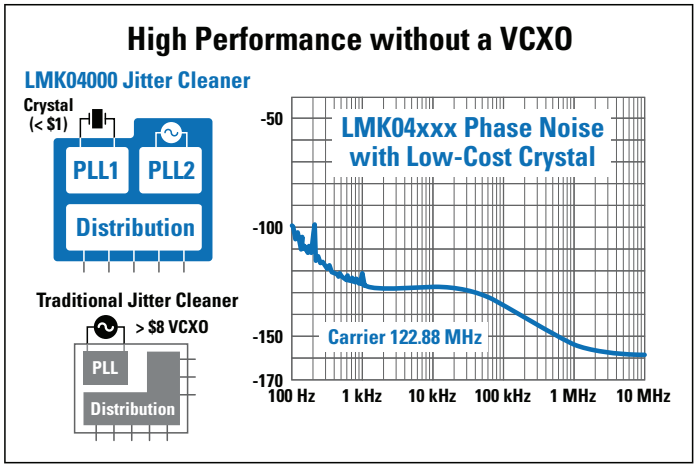
Precision Clock Conditioners

National's families of precision clock conditioners improve system performance and accuracy while enabling a complete clock architecture that achieves the best possible performance for the cost. National's clock conditioner portfolio provides system designers with the capability not only to generate a precision clock, but also to recondition and distribute a derived or externally-generated clock.

These precision clock conditioners are ideal for clocking applications in data converter clocking, wireless infrastructure, wired and optical networking, medical, military/ aerospace, test and measurement, and video systems.

The LMK04000 family of precision clock conditioners provides low-noise jitter cleaning, clock multiplication and distribution without the need for a high-performance voltage-controlled crystal oscillator (VCXO) module. Using the Cascaded PLLatinum® architecture combined with an external crystal and varactor diode, the LMK04000 family provides:

- Under 200 fs RMS jitter
- Cascaded PLLatinum architecture
- Default clock upon power-up
- LVDS, LVPECL, and LVCMOS output options
- Support of clock rates up to 1080 MHz



Design Resources

- Clock Design Tool v1.2.3
- Codeloader 4.2 software
- LMK evaluation boards
- Clock Conditioner Owner's Manual
- Application notes
- Online seminars

Visit: **national.com/timing**

LMK Clock Conditioner Portfolio

LMK Family	Architecture	Output Clock Range (MHz)	Characteristics
LMK04000	5- to 7-output clock cleaner/generator/distributor Cascaded phase-locked loops (PLL) + VCO + Clock Distribution (PLL1 requires external Crystal or VCXO)	Up to 1080	• < 0.2 ps RMS jitter (typ) with external crystal or VCXO • Cascaded PLLatinum PLL architecture • Redundant input and default clock upon power-up • Lower BOM cost using integrated crystal oscillator circuit
LMK03000	4- and 8-output clock cleaner/generator/distributor PLL + VCO + Clock Distribution	Up to 1080	• < 0.4 ps RMS jitter (typ) integrated low-noise VCO • Three performance grades (Premium, Standard, Value) • Lower BOM cost and footprint using internal VCO
LMK02000	4- and 8-output clock cleaner/generator/distributor PLL + Clock Distribution (needs external VCXO)	Up to 860	• < 0.2 ps of RMS jitter (typ) with external VCXO
LMK01000	2-input and 8-output clock buffer, divider and distributor	Up to 1600	• < 30 fs of additive RMS jitter (typ) at 800 MHz

Low-Noise PLLatinum® PLLs and Frequency Synthesizers

National's portfolio of high-performance frequency synthesizers and PLLs includes the industry's lowest noise monolithic PLL-integrated circuits and frequency synthesizers with the industry's best spur performance for better signal sensitivity in voice and data systems.

These performance-leading products are ideal for local oscillator (LO) applications in next-generation basestation radio transceivers, mobile radio and handset, wireless meter reading, test and measurement, broad wireless, satellite, and automotive systems.

The new LMX2541 family is the world's lowest noise-integrated frequency synthesizer. Featuring the world's lowest noise PLL with bypassable integrated VCO, the LMX2541 provides:

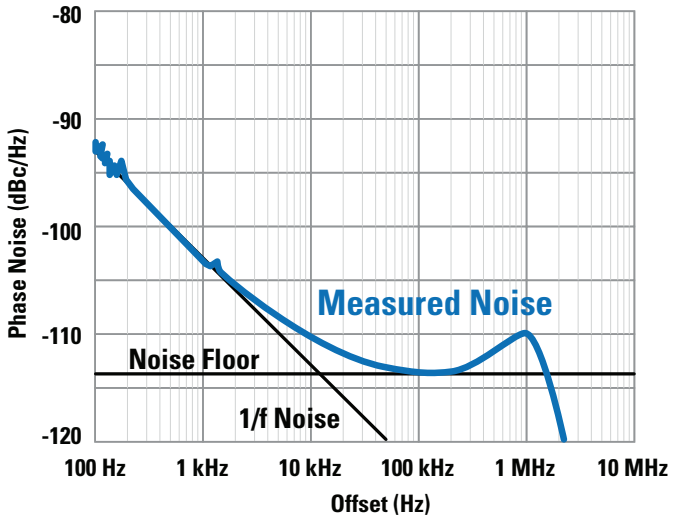
- Fully-integrated, ultra-low noise VCO
- Normalized PLL phase noise of -225 dBc/Hz
- Less than 2 mrad RMS noise at 2.1 GHz and 3.5 mrad RMS noise at 3.5 GHz
- Ultra-low RMS noise and spurs
- Wide frequency range 31.6 MHz to 4 GHz
- VCO output divider, 1 to 63 (odd and even)
- Phase detector frequency up to 104 MHz
- Internal VCO can be bypassed for use with external VCO

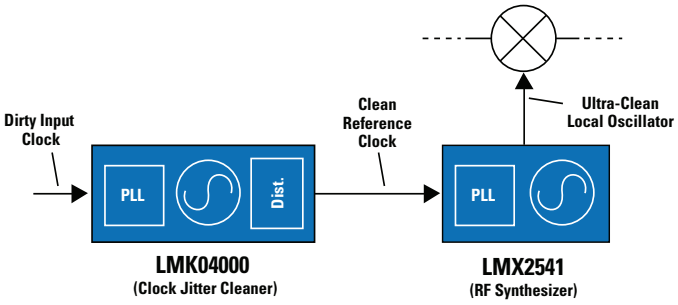
Design Resources

- Clock Design Tool v1.2.3
- EasyPLL WEBENCH® design tool
- Codeloader evaluation software
- LMX PLLatinum PLL/VCO evaluation boards
- PLL Performance, Simulation and Design Handbook, 4th edition
- Application notes
- Online seminars

Visit: **national.com/timing**

Industry's Highest Performance Synthesizer





PLLatinum Portfolio

Product ID Family	Fractional or Integer PLL	Single or Dual PLL	Normalized Phase Noise (dBc/Hz)	Integrated VCO	Min Frequency (MHz)	Max Frequency (MHz)	Supply Voltage (V)
LMX248x	Both	Dual	-210	—	50	7500	2.5 to 3.6
LMX243x	Integer	Dual	-219	—	100	5000	2.25 to 2.75
LMX2531	Both	Single	-212	✔	553	2790	2.8 to 3.2
LMX2541	Both	Single	-225	✔ (can be bypassed)	31.6	4000	3.15 to 3.45

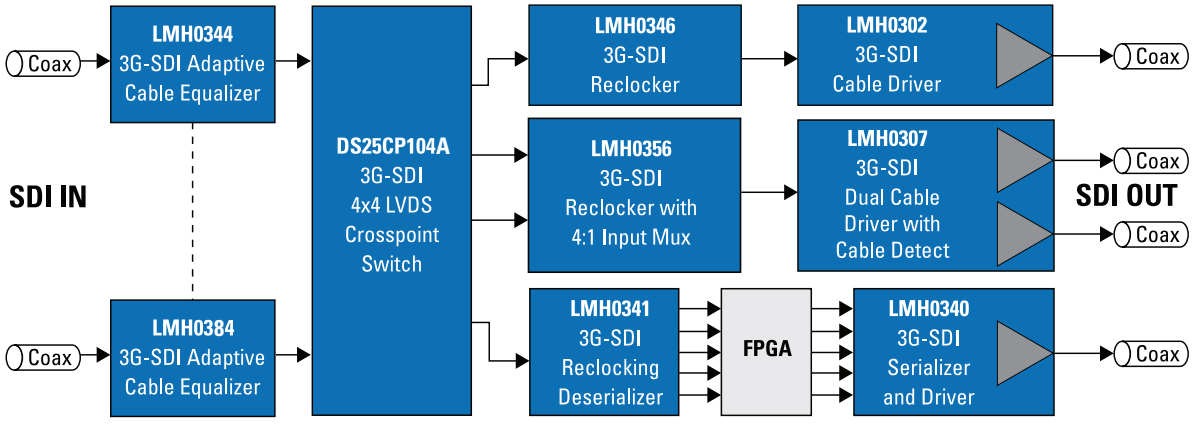
Comprehensive 3 Gbps SDI Solutions

3G/HD/SD SDI Equalizer, Deserializer, Serializer, Reclocker, Cable Driver, and Signal-Conditioning Products

National is the only Tier 1 semiconductor supplier to offer a complete end-to-end solution for the 3 Gbps SDI market. National's broadcast video solutions deliver the right combination of best-in-class jitter performance, system-wide energy efficiency, and small package size for your design.

Each of National's 3G-SDI products has a footprint-compatible counterpart for HD/SD applications to maximize designer flexibility in building a system. For more information on National's SDI portfolio, visit National's SDI website: **national.com/sdi**

3G/HD/SD SDI Switcher
Simplified Block Diagram



Base Portfolio

	Equalizers	Reclockers	Cable Drivers	Serializers	Deserializers	Video Clocking Products
						
3G	LMH0384 LMH0344	LMH0356 LMH0346	LMH0307 LMH0303 LMH0302	LMH0340	LMH0341	LMH1982 LMH1981
HD	LMH0044 LMH0034	LMH0056 LMH0046	LMH0002 LMH0202	LMH0050 LMH0040 LMH0030	LMH0051 LMH0041 LMH0031	
SD	LMH0024 LMH0074	LMH0036 LMH0026	LMH0001	LMH0070	LMH0071	

See the video on SMPTE/SDI jitter reduction at: **http://bit.ly/5QKIcF**
See the video on LMH1981/LMH1982 SDI clocking demo at: **http://bit.ly/3hiV0O**

Triple-Rate SDI Development Platform for Altera FPGAs

In collaboration with Altera, National Semiconductor has developed a triple-rate SDI and video clocking daughter card for Altera FPGA development kits. National's daughter card is compatible with both the **Cyclone-III** and the **Stratix-III** development kits. It plugs directly into the host FPGA development board via Altera's high-speed mezzanine connector (HSMC).

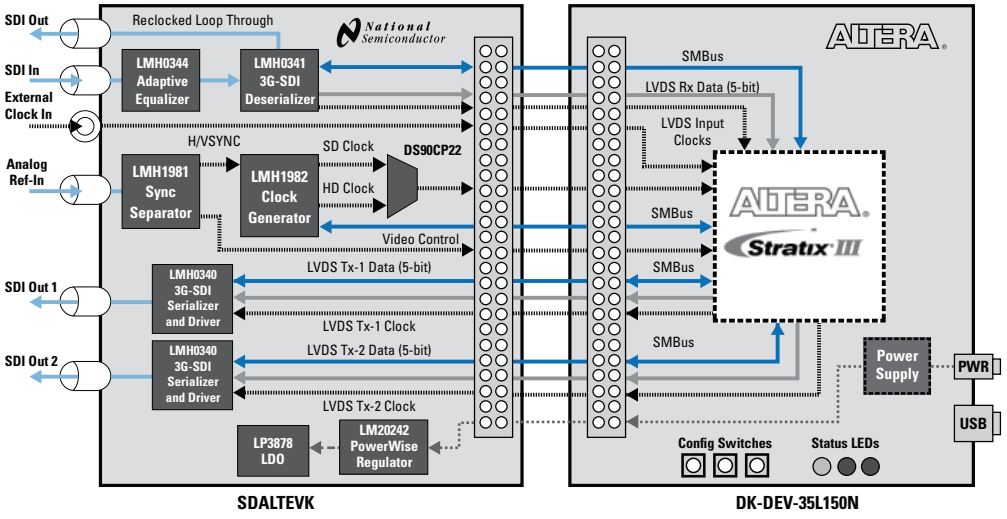
National provides FPGA source code for SMPTE protocol processing (included with the purchase of an evaluation kit or ICs). The FPGA IP along with the daughter card and the FPGA development kit provide broadcast video system designers a comprehensive platform for rapid evaluation and prototyping of new designs, thereby reducing time to market.

See the video on SDALTEVK at: **http://bit.ly/7hJyhK**

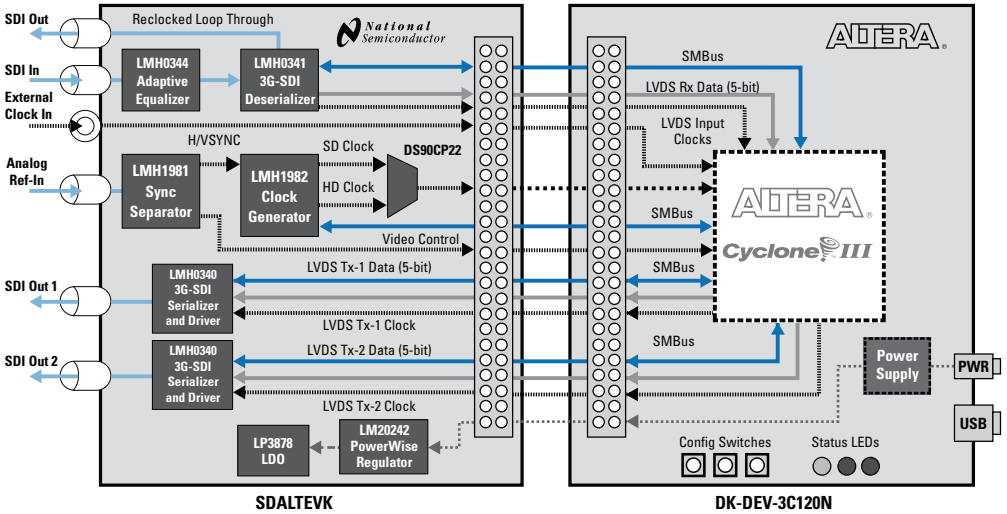
Features

- 3G, HD, and SD compatible
- Comprehensive reference for hardware design and FGPA IP development
- Included HDL (Verilog, VHDL source) supports SDI framing, audio embedding/de-embedding and test pattern generation
  - IP available for both Cyclone-III and Stratix-III FPGAs
- Support for Genlock

SDALTEVK: 3G-SDI Development Platform with Altera Stratix-III FPGA



SDALTEVK: 3G-SDI Development Platform with Altera Cyclone-III FPGA



- Video
- Clocks*
- Parallel
- Data Control
- Power

*Four clocking options available
1. Recovered clock
2. Genlock (analog ref in with LMH1981 + LMH1982)
3. Local generation (free run with LMH1982)
4. External clock

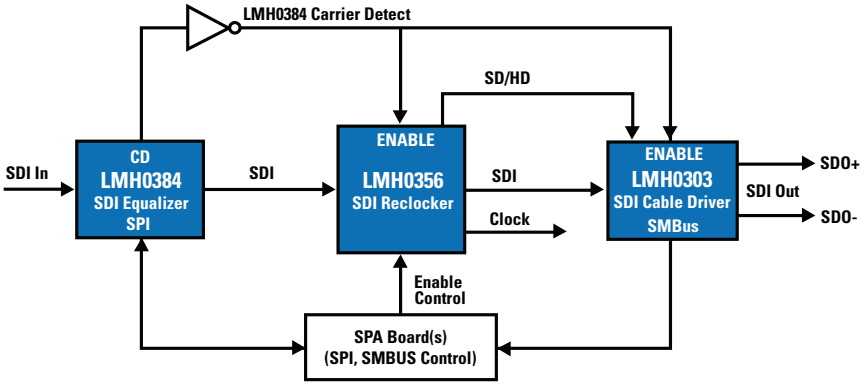
SDI Equalizers, Reclockers, and Cable Drivers

PowerWise® Triple-Rate Distribution Amplifier

Features

- Auto signal detection at equalizer input
- Cable detection at driver output
- Significant power savings
  - 95% power savings in power-save mode
- Triple-rate SMPTE support
  - Supports SMPTE 424M (3G), 292M (HD), 259M/C (SD), and DVB-ASI

Triple-Rate Distribution Amplifier



SDI Equalizers, Reclockers, and Cable Drivers

Product ID	Description	Supply Voltage (V)	Typ Power (mW)	Data Rate (Mbps)	Temp Range[1]	Eval Board Product ID	Packaging
Cable Equalizers							
NEW **LMH0384SQ**	3G/HD/SD extended reach adaptive cable equalizer	3.3	230	143 to 2970	Ind	SD384EVK	LLP-16
NEW **LMH0344GR/SQ**	3G/HD/SD adaptive cable equalizer	3.3	280	143 to 2970	Ind	SD344EVK	microArray-25. LLP-16
LMH0044SQ	HD/SD adaptive cable equalizer	3.3	208	143 to 1485	Ext	SD044EVK	LLP-16
LMH0034MA	HD/SD adaptive cable equalizer	3.3	208	143 to 1485	Ext	SD034EVK	SOIC-16
LMH0074SQ	SD adaptive cable equalizer with cable detect	3.3	208	143 to 540	Ind	SD074EVK	LLP-16
LMH0024MA	3.3V SD adaptive cable equalizer	3.3	198	143 to 540	Ind	SD024EVK	SOIC-16
Reclockers							
NEW **LMH0346MH/SQ**	3G/HD/SD reclocker with dual differential outputs	3.3	370	270 to 2970	Ind	SD3GDAEVK/ SD346EVK	eTSSOP-20, LLP-24
NEW **LMH0356SQ/SQ-40**	3G/HD/SD reclocker with 4:1 input mux and FR4 equalization	3.3	430	270 to 2970	Ind	SD356EVK	LLP-48, LLP-40
LMH0046MH	HD/SD reclocker with dual differential outputs	3.3	330	143 to 1485	Ind	SD046EVK	eTSSOP-20
LMH0056SQ	HD/SD reclocker with 4:1 input mux and FR4 equalization	3.3	360	143 to 1485	Ind	SD046EVK	LLP-48
LMH0026MH	SD reclocker with dual differential outputs	3.3	330	270	Ind	SD046EVK	eTSSOP-20
LMH0036SQ	SD reclocker with 4:1 input mux and FR4 equalization	3.3	350	270	Ind	SD046EVK	LLP-48
Cable Drivers							
NEW **LMH0307GR/SQ**	3G/HD/SD SDI dual cable driver with cable detect, input LOS, selectable slew rate and 4 mW power-down mode	3.3	275	Up to 2970	Ind	SD307EVK	microArray-25, LLP-16
LMH0302SQ	3G/HD/SD cable driver with enable feature	3.3	165	Up to 2970	Ind	SD302EVK	LLP-16
LMH0303SQ	3G/HD/SD SDI cable driver with cable detect, input LOS, selectable slew rate and 4 mW power-down mode	3.3	155	Up to 2970	Ind	SD303EVK	LLP-16
LMH0002MA/TMA	HD/SD serial digital cable driver with selectable slew rate	3.3	149	Up to 1485	Com/ Ind	SD002EVK	SOIC-8
LMH0002SQ	HD/SD serial digital cable driver with selectable slew rate	3.3	149	Up to 1485	Ind	SD002SQ-EVK	LLP-16
LMH0202MT	Dual SD/DS serial cable driver with dual differential input and output	3.3	298	Up to 1485	Com	SD202EVK/ DVB202-EVK	TSSOP-16
LMH0001SQ	SD serial digital cable driver with adjustable output amplitude	3.3	125	Up to 540	Ind	SD001SQ-EVK	LLP-16

PowerWise® Product [1] Temperature ranges: Com: 0°C to 70°C Ext: 0°C to 85°C Ind: -40°C to 85°C

Older products not shown in the table, but still in production include: CLC001AJE, CLC005AJE, CLC006AJE, CLC007AJE

Flexible IP and High-Performance SerDes for Future-Proof System Solutions

National's SDI SerDes devices and SMPTE protocol processing FPGA IP provide a complete system solution. Unlike competing solutions that combine SerDes functionality with SMPTE processing in a single chip, National's solution:

- Enables system designers to match evolving SMPTE specifications just by changing the FPGA bitstream
- Eliminates expensive and time-consuming silicon re-spins
- Eliminates need for additional board qualifications
- Future-proofs system design
- Reduces lifetime cost-of-system maintenance

High-end FPGAs with integrated transceivers use low-geometry CMOS processes and have a high noise floor, causing poor jitter performance. To compensate, designers need additional components such as premium regulators, reference clocks, isolated power and ground planes, and thermal protection that increase design complexity, time, and cost. In contrast, National's SerDes solutions work with cost-effective FPGAs that require few additional components.

National delivers the industry's lowest-output-jitter solution (30 ps p-p) in a package that is 60% smaller than competing solutions. The smaller size enables optimal placement of the SerDes close to BNC connectors, facilitating return loss network design.

Comparison of System Design Options

Features	National SerDes	High-End FPGA with Integrated SerDes	SerDes with Integrated SMPTE Processing
System design flexibility to evolve with changing standards	✔	✔	—
Good jitter performance	✔	—	✔
Small board area (device + additional components)	✔	—	—
Upgradable firmware	✔	✔	—
Low Bill of Materials (BOM) cost	✔	—	—
Fast time to market	✔	—	✔
Embedded audio support (up to 16 channels)	✔	—	—

SDI Serializers and Deserializers

Product ID	Description	Supply Voltage (V)	Typ. Power (mW)	Data Rate (Mbps)	Temp Range[1]	Eval Board Product ID	Packaging
Serializers							
LMH0340	3G/HD/SD serializer with LVDS interface and integrated cable driver	3.3, 2.5	440	270 to 2970	Ind	SDALTEVK (Altera)	LLP-48
LMH0040	HD/SD serializer with LVDS interface and integrated cable driver	3.3, 2.5	440	270 to 1485	Ind		LLP-48
LMH0050	HD/SD serializer with LVDS interface	3.3, 2.5	460	270 to 1485	Ind		LLP-48
LMH0070	SD serializer with LVDS interface and integrated cable driver	3.3, 2.5	400	270	Ind		LLP-48
LMH0030	HD/SD serializer with FIFOs, integrated cable driver, 85 ps typical output jitter, no external VCOs required, BIST, and TPG	3.3, 2.5	430	270 to 1485	Com	SD130EVK	TQFP-64
Deserializers							
LMH0341	3G/HD/SD reclocking deserializer with LVDS interface and active loop through	3.3, 2.5	590	270 to 2970	Ind	SDALTEVK (Altera)	LLP-48
LMH0041	HD/SD reclocking deserializer with LVDS interface and active loop through	3.3, 2.5	550	270 to 1485	Ind		LLP-48
LMH0051	HD/SD reclocking deserializer with LVDS interface	3.3, 2.5	555	270 to 1485	Ind		LLP-48
LMH0071	SD reclocking deserializer with LVDS interface and active loop through	3.3, 2.5	525	270	Ind		LLP-48
LMH0031	HD/SD deserializer / descrambler with FIFOs, 27 MHz reference, BIST, TPG, and automatic EDH/CRC	3.3, 2.5	850	270 to 1485	Com	SD131EVK	TQFP-64

[1]Temperature ranges: Com: 0°C to 70°C Ext: 0°C to 85°C Ind: -40°C to 85°C

Worldwide Design Centers and Manufacturing Facilities

Design Centers

USA:
Chandler, Arizona
Federal Way, Washington
Fort Collins, Colorado
Grass Valley, California
Indianapolis, Indiana
Longmont, Colorado
Norcross, Georgia
Phoenix, Arizona
Salem, New Hampshire
Santa Clara, California
South Portland, Maine
Tucson, Arizona

EUROPE:
Delft, Netherlands
Unterhaching, Germany
Greenock, Scotland
Milan, Italy
Oulu, Finland
Tallinn, Estonia

ASIA:
Bangalore, India
Hong Kong, China

Manufacturing Facilities

Wafer (Die) Fabrication:
Arlington, Texas
South Portland, Maine
Greenock, Scotland

Chip Test and Assembly:
Melaka, Malaysia

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