

# **FDC6330L**

## **Integrated Load Switch**

### **General Description**

This device is particularly suited for compact power management in portable electronic equipment where 3V to 20V input and 2.3A output current capability are needed. This load switch integrates a small N-Channel power MOSFET (Q1) which drives a large P-Channel power MOSFET (Q2) in one tiny SuperSOTTM-6 package.

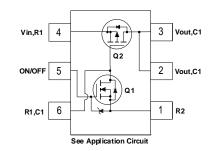
## **Applications**

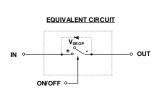
- Power management
- Load actuation

### **Features**

- $\begin{array}{l} \bullet \text{ V} \\ V \\ V \\ DROP \end{array} = 0.2V \text{ @ V} \\ V \\ IN \\ IN \end{array} = 12V, \\ I \\ L \\ = 2.5 \text{ A. R} \\ IN \\ = 0.08 \text{ } \Omega \\ ON) \\ = 0.125 \text{ } \Omega. \end{array}$
- Control MOSFET (Q1) includes Zener protection for ESD ruggedness (>6kV Human Body Model).
- High performance PowerTrench<sup>TM</sup> technology for extremely low on-resistance.
- SuperSOT<sup>TM</sup>-6 package design using copper lead frame for superior thermal and electrical capabilities.







## SuperSOT<sup>™</sup>-6

Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>IN</sub>	Input Voltage Range	(Note 1)	3 - 20	V
V <sub>ON/OFF</sub>	On/Off Voltage Range		1.5 - 8	V
I <sub>D</sub>	Load Current - Continuous	(Note 2)	2.3	A
	- Pulsed		10	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1)	0.7	W
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Temperature Range		-55 to +150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human-Body-Model (100pf/1500 Ohm)		6	kV

## Thermal Characteristics

$R_{ heta^{JA}}$	Thermal Resistance, Junction-to-Ambient	(Note 2)	180	°C/W
$R_{\theta^{JC}}$	Thermal Resistance, Junction-to-Case	(Note 2)	60	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size Tape width		Quantity	
_330 ( _ Denotes pin 1)	FDC6330L	7"	8mm	3000 units	

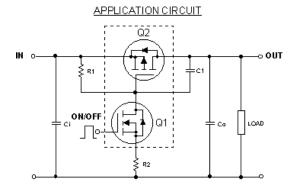
## Electrical Characteristics TA=25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
OFF Ch	aracteristics					
I <sub>FL</sub>	Leakage Current	$V_{IN} = 20 \text{ V}, V_{ON/OFF} = 250 \mu\text{A}$			1	μA
ON Cha	racteristics (Note 3) Conduction Voltage	$V_{IN} = 12 \text{ V}, V_{ON/OFF} = 3.3 \text{ V}, I_L = 2.5 \text{ A}$			0.2	V
$V_{DROP}$	Conduction Voltage	$V_{IN} = 12 \text{ V}, V_{ON/OFF} = 3.3 \text{ V}, I_L = 2.5 \text{ A}$			0.2	V
		$V_{IN} = 5 \text{ V}, V_{ON/OFF} = 3.3 \text{ V}, I_{L} = 1.6 \text{ A}$			0.2	V
R <sub>(ON)</sub>	Q <sub>2</sub> - Static On-Resistance	$V_{GS} = -12 \text{ V}, I_{D} = -2.3 \text{ A}$ $V_{GS} = -5 \text{ V}, I_{D} = -1.9 \text{ A}$		0.054 0.081	0.08 0.125	Ω
IL	Load Current	V <sub>DROP</sub> = 0.2 V, V <sub>IN</sub> = 12 V, V <sub>ON/OFF</sub> = 3.3 V	2.5			Α
		$V_{DROP} = 0.2 \text{ V}, V_{IN} = 5 \text{ V}, V_{ON/OFF} = 3.3 \text{ V}$	1.6			1

#### Notes

- 1. Range of  $V_{in}$  can be up to 30V, but  $R_1$  and  $R_2$  must be scaled such that  $V_{GS}$  of Q2 does not exceed 20V.
- 2.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
- 3. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2.0%.

## FDC6330L Load Switch Application



### **External Component Recommendation:**

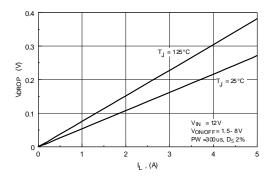
For applications where  $Co \leq 1 \mu F.$ 

For slew rate control, select R2 in the range of 1k -  $4.7 k\Omega$  .

For additional in-rush current control,  $C1 \le 1000 pF$  can be added.

Select R1 so that the R1/R2 ratio ranges from 10 - 100. R1 is required to turn Q2 off.

## Typical Characteristics (continued)



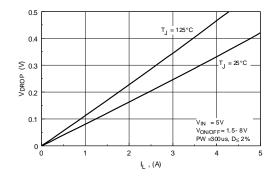


Figure 1. Conduction Voltage Drop Variation with Load Current.

Figure 2. Conduction Voltage Drop Variation with Load Current.

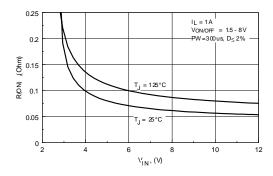


Figure 3. On-Resistance Variation with Input Voltage.

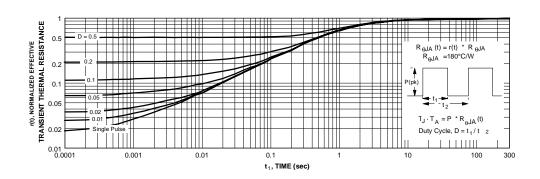


Figure 4.Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 2. Transient themal response will change depending on the circuit board design.

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E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

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