December 2005

FHP3130, FHP3230, FHP3430
Single, Dual, and Quad, High Speed, 2.7V to 12V, Rail-to-Rail Amplifiers

Features at ±5V

- 2.5mA supply current per amplifier
- 0.008% / 0.01˚ differential gain/phase
- 16MHz 0.1dB bandwidth at $V_o = 2V_{pp}$
- Output voltage range at R_L = 150Ω : -4.8V to 4.8V
- Input includes negative rail
- 110V/µs slew rate
- ±100mA output current
- 17nV/√Hz input voltage noise
- >100dB PSRR, CMRR, and Open Loop Gain
- FHP3130 – improved replacement for KM4100
- FHP3230 – improved replacement for KM4200
- FHP3130 lead(Pb)-free package options (SOT23-5, SOIC-8)
- FHP3230 lead(Pb)-free package options (MSOP-8, SOIC-8)
- FHP3430 lead(Pb)-free package options (TSSOP-14, SOIC-14)
- RoHS compliant
- Fully specified at +3V, +5V, and ±5V supplies

Applications

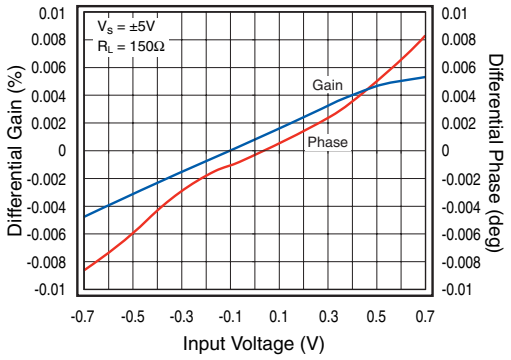
- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- Portable/battery-powered applications
- Twisted pair driver
- Video driver

Description

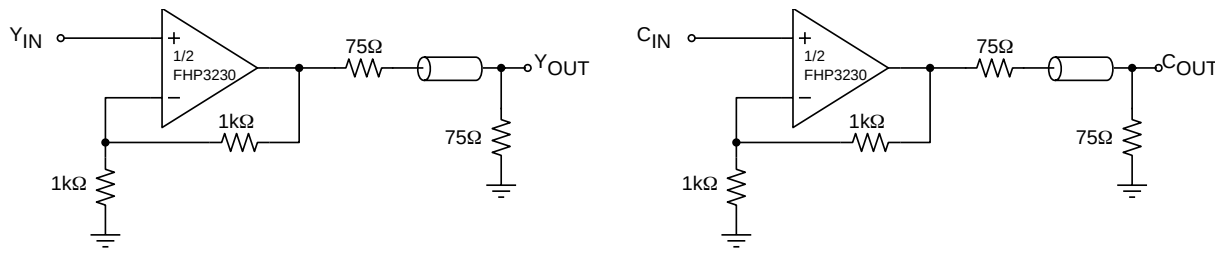
The FHP3130 (single), FHP3230 (dual), and FHP3430 (quad) are low cost, high performance, voltage feedback amplifiers that consume only 2.5mA of supply current per channel while providing ±100mA of output current. These amplifiers are designed to operate from 2.7V to 12V (±6V) supplies. The common mode voltage range extends below the negative rail and the output provides rail-to-rail performance.

The FHP3130, FHP3230, and FHP3430 are designed on a complimentary bipolar process and provide 170MHz of bandwidth and 110V/µs of slew rate at a supply voltage of ±5V. The combination of low power, rail-to-rail performance, low voltage operation, and tiny package options make these amplifiers well suited for use in many general purpose high speed applications.

These amplifiers also provide excellent video specifications. They offer extremely low differential gain and phase (0.008%/0.01˚) and 0.1dB gain flatness to 16MHz for superb standard definition video performance. Their output drive capability effortlessly supports 4 video loads.

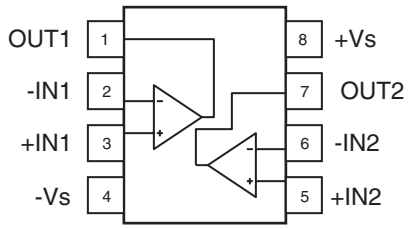


Typical Application - YC Video Line Driver

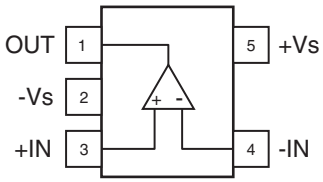


Pin Configurations

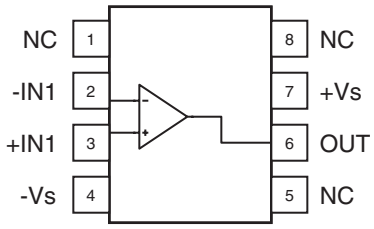
FHP3230
SOIC/MSOP



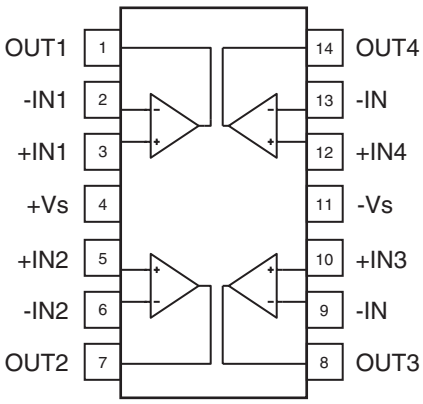
FHP3130
SOT23



FHP3130
SOIC



FHP3430
SOIC/TSSOP



Pin Assignments

FHP3230			
Pin#	**Pin**	**Type**	**Description**
1	OUT1	Output	Output, channel 1
2	-IN1	Input	Negative Input, channel 1
3	+IN1	Input	Positive Input, channel 1
4	-Vs	Input	Negative supply
5	+IN2	Input	Positive Input, channel 2
6	-IN2	Input	Negative Input, channel 2
7	OUT2	Output	Output, channel 2
8	+Vs	Input	Positive supply

FHP3130			
Pin# SOT/SOIC	**Pin**	**Type**	**Description**
1 / 6	OUT	Input	Output
2 / 4	-Vs	Input	Negative supply
3 / 3	+IN	Input	Positive Input
4 / 4	-IN	Input	Negative Input
5 / 7	+Vs	Input	Positive supply
na / 1, 5, 8	NC	-	No Connect

FHP3430			
Pin#	**Pin**	**Type**	**Description**
1	OUT1	Output	Output, channel 1
2	-IN1	Input	Negative Input, channel 1
3	+IN1	Input	Positive Input, channel 1
4	+Vs	Input	Positive supply
5	+IN2	Input	Positive Input, channel 2
6	-IN2	Input	Negative Input, channel 2
7	OUT2	Output	Output, channel 2
8	OUT3	Output	Output, channel 3
9	-IN3	Input	Negative Input, channel 3
10	+IN3	Input	Positive Input, channel 3
11	-Vs	Input	Negative supply
12	+IN4	Input	Positive Input, channel 4
13	-IN4	Input	Negative Input, channel 4
14	OUT4	Output	Output, channel 4

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage	0	12.6	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ + 0.5V	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			150	˚C
Storage Temperature Range	-65		150	˚C
Lead Temperature (Soldering, 10s)			300	˚C
8-Lead SOIC[1]		155		˚C/W
8-Lead MSOP[1]		246		˚C/W
5-Lead SOT23[1]		296		˚C/W
14-Lead TSSOP[1]		130		˚C/W
14-Lead SOIC[1]		128		˚C/W

Note:

1. Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

ESD Protection

Product	FHP3130		FHP3230		FHP3430	
Package	SOT23	SOIC	SOIC	MSOP	SOIC	TSSOP
Human Body Model (HBM)	TBD	TBD	3.5kV	3.5kV	TBD	TBD
Charged Device Model (CDM)	TBD	TBD	2kV	1.5kV	TBD	TBD

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	˚C
Supply Voltage Range	2.7		12	V

Electrical Characteristics at +3V

T_c = 25˚C, V_S = 3V, R_L = 2kΩ to V_S/2, G = 2, R_f = R_g =1kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency Domain Response					
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		160		MHz
BW_{ss}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		50		MHz
BW_{Ls}	Full Power Bandwidth	G = +2, V_{OUT} = 1V_{pp}		45		MHz
$BW_{0.1dBss}$	0.1dB Bandwidth	G = +2, R_L = 150Ω, R_f = R_g = 1.5kΩ, V_{OUT} = 0.2V_{pp}		25		MHz
GBWP	Gain Bandwitdth Product	G = +6, V_{OUT} = 0.2V_{pp}		60		MHz
	Time Domain Response					
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		12		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		45		ns
OS	Overshoot	V_{OUT} = 0.2V step		<1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		90		V/µs
	Distortion / Noise Response					
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		50		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		50		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz, R_L = 100Ω, G = -1		50		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3230 at 1MHz		62		dB
	DC Performance					
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			-5		µV/˚C
I_b	Input Bias Current			-1.8		µA
dI_b	Average Drift			-3.5		nA/˚C
I_{IO}	Input Offset Current			0.01		µA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open Loop Gain	DC, R_L = 150Ω		100		dB
I_S	Supply Current per Amplifier			2.5		mA
	Input Characteristics					
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			1.25		pF
CMIR	Input Common Mode V Range			-0.3 to 2		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_S - 1.5		95		dB
	Output Characteristics					
V_O	Output Voltage Swing	R_L = 2kΩ to V_S/2, G = -1		0.05 to 2.95		V
		R_L = 150Ω to V_S/2, G = -1		0.1 to 2.9		V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short Circuit Output Current	V_O = V_S/2		±120		mA

Electrical Characteristics at +5V

T_c = 25°C, V_S = 5V, R_L = 2kΩ to V_S/2, G = 2, R_f = R_g =1kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency Domain Response					
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		165		MHz
BW_{ss}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		50		MHz
BW_{Ls}	Full Power Bandwidth	G = +2, V_{OUT} = 2V_{pp}		30		MHz
$BW_{0.1dBss}$	0.1dB Bandwidth	G = +2, R_L = 150Ω, R_f = R_g = 1.5kΩ, V_{OUT} = 0.2V_{pp}		18		MHz
GBWP	Gain Bandwitdth Product	G = +6, V_{OUT} = 0.2V_{pp}		60		MHz
	Time Domain Response					
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		12		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		55		ns
OS	Overshoot	V_{OUT} = 0.2V step		<1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		105		V/µs
	Distortion / Noise Response					
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		56		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		75		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		56		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3230 at 1MHz		62		dB
DG	Differential Gain	NTSC (3.58MHz), R_L = 150Ω, AC coupled into 220µF, V_S = ±2.5V		0.02		%
DP	Differential Phase	NTSC (3.58MHz), R_L = 150Ω, AC coupled into 220µF, V_S = ±2.5V		0.04		°
	DC Performance					
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			-5		µV/°C
I_b	Input Bias Current			-1.8		µA
dI_b	Average Drift			-3.5		nA/°C
I_{IO}	Input Offset Current			0.01		µA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open Loop Gain	DC, R_L = 150Ω		100		dB
I_S	Supply Current per Amplifier			2.5		mA
	Input Characteristics					
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			1.2		pF
CMIR	Input Common Mode V Range			-0.3 to 4		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_s - 1.5		95		dB
	Output Characteristics					
V_O	Output Voltage Swing	R_L = 2kΩ to V_S/2		0.05 to 4.95		V
		R_L = 150Ω to V_S/2		0.1 to 4.9		V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short Circuit Output Current	V_O = V_S/2		±120		mA

Electrical Characteristics at ±5V

T_c = 25˚C, V_S = ±5V, R_L = 2kΩ to GND, G = 2, R_f = R_g =1kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency Domain Response					
UGBW	-3dB Bandwidth	G = +1, V_{OUT} = 0.2V_{pp}		170		MHz
BW_{ss}	-3dB Bandwidth	G = +2, V_{OUT} = 0.2V_{pp}		50		MHz
BW_{Ls}	Full Power Bandwidth	G = +2, V_{OUT} = 2V_{pp}		30		MHz
$BW_{0.1dBss}$	0.1dB Bandwidth	G = +2, R_L = 150Ω, R_f = R_g = 1.5kΩ, V_{OUT} = 0.2V_{pp}		16		MHz
GBWP	Gain Bandwitdth Product	G = +6, V_{OUT} = 0.2V_{pp}		60		MHz
	Time Domain Response					
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		12		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		52		ns
OS	Overshoot	V_{OUT} = 0.2V step		<1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -1		110		V/µs
	Distortion / Noise Response					
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		55		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		75		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		55		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3230 at 1MHz		62		dB
DG	Differential Gain	NTSC (3.58MHz), R_L = 150Ω, AC coupled into 220µF		0.008		%
DP	Differential Phase	NTSC (3.58MHz), R_L = 150Ω, AC coupled into 220µF		0.01		˚
	DC Performance					
V_{IO}	Input Offset Voltage[1]		-6	1	6	mV
dV_{IO}	Average Drift			-5		µV/˚C
I_b	Input Bias Current[1]		-3.5	-1.8		µA
dI_b	Average Drift			-3.5		nA/˚C
I_{IO}	Input Offset Current[1]		-0.8	0.002	0.8	µA
PSRR	Power Supply Rejection Ratio[2]	DC	80	100		dB
A_{OL}	Open Loop Gain[2]	DC, R_L = 150Ω	80	100		dB
I_S	Supply Current per Amplifier[1]			2.5	3.5	mA
	Input Characteristics					
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			1.1		pF
CMIR	Input Common Mode V Range			-5 to 4		V
CMRR	Common Mode Rejection Ratio[2]	DC, V_{CM} = -5V to 3.5V	75	100		dB
	Output Characteristics					
V_O	Output Voltage Swing	R_L = 2kΩ		-4.95 to 4.95		V
		R_L = 150Ω[1]	-4.65	-4.8 to 4.8	4.65	V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short Circuit Output Current	V_O = 0V		±120		mA

Notes:

1. 100% tested at 25˚C
2. Min/max guaranteed by design/characterization.

Typical Performance Characteristics

T_c = 25˚C, V_S = 5V, R_L = 2kΩ to V_S/2 for V_S = 5V and 3V, R_L = 2kΩ to ground for V_S = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

Figure 1. Non-Inverting Freq. Response (±5V)

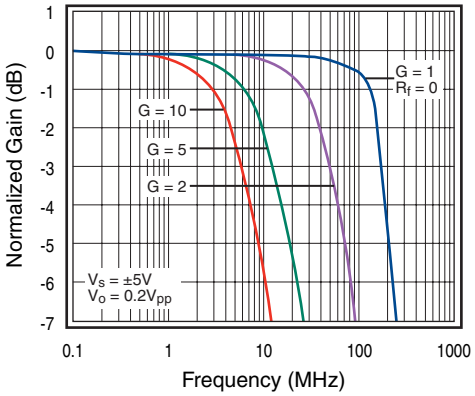


Figure 2. Inverting Freq. Response (±5V)

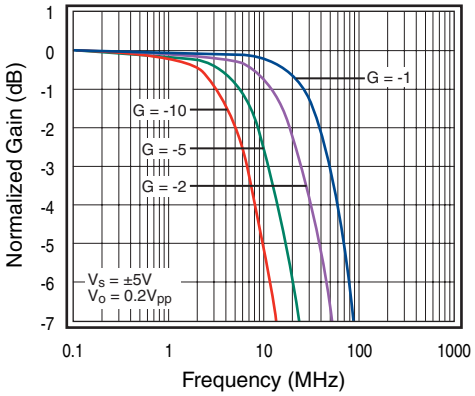


Figure 3. Non-Inverting Freq. Response (+5V)

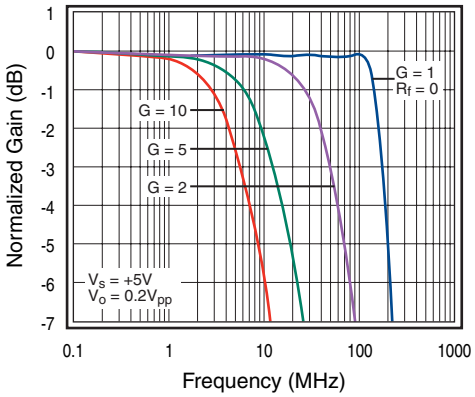


Figure 4. Inverting Freq. Response (+5V)

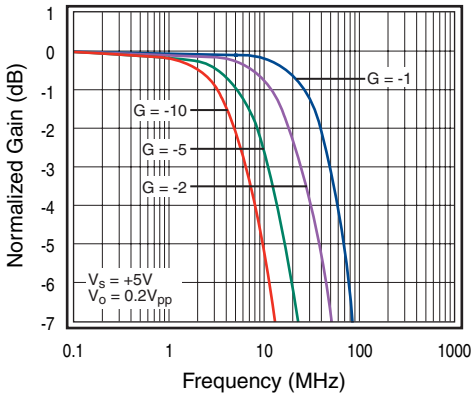


Figure 5. Non-Inverting Freq. Response (+3V)

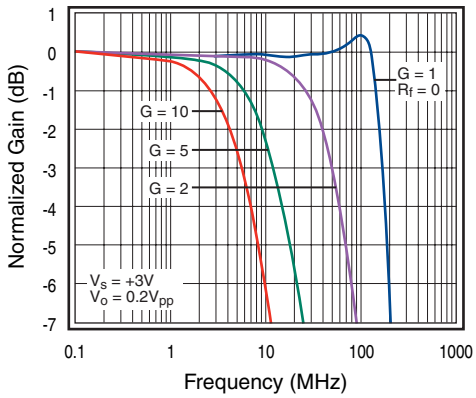
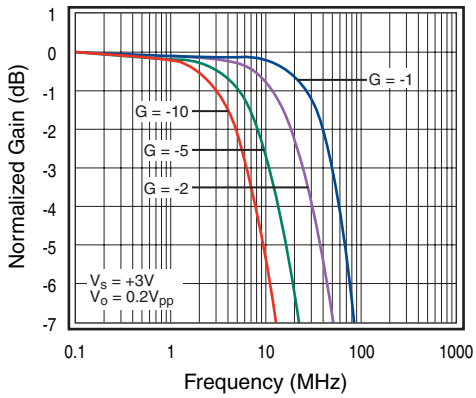


Figure 6. Inverting Freq. Response (+3V)



Typical Performance Characteristics

T_c = 25˚C, V_S = 5V, R_L = 2kΩ to V_S/2 for V_S = 5V and 3V, R_L = 2kΩ to ground for V_S = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

Figure 7. Frequency Response vs. C_L (+3V)

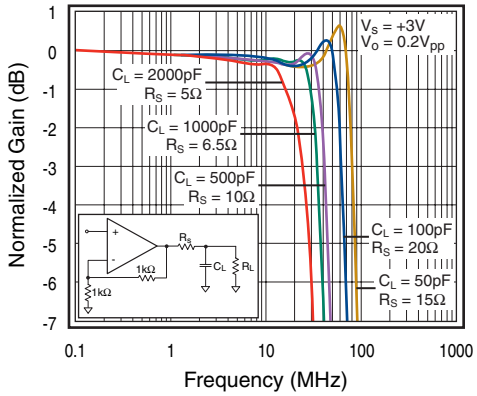


Figure 8. Frequency Response vs. R_L (+3V)

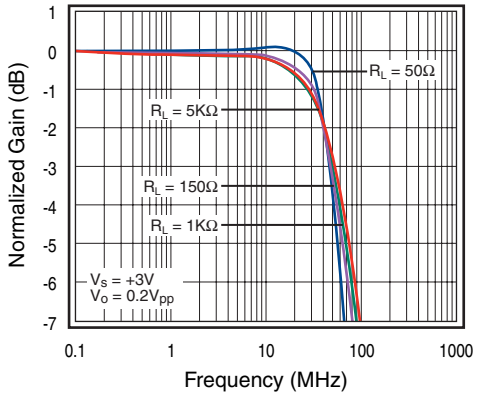


Figure 9. Large Signal Freq. Response (+5V)

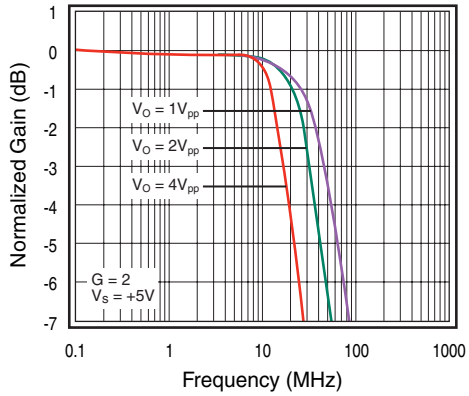


Figure 10. Gain vs. Flattness

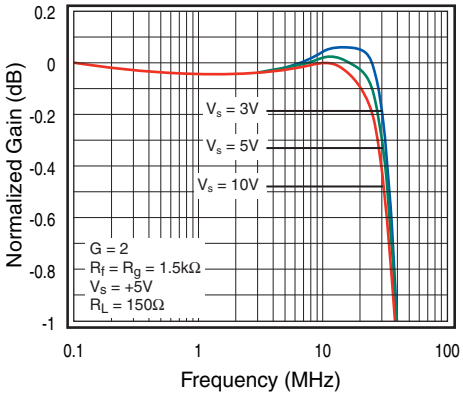


Figure 11. HD2 vs. R_L (+3V)

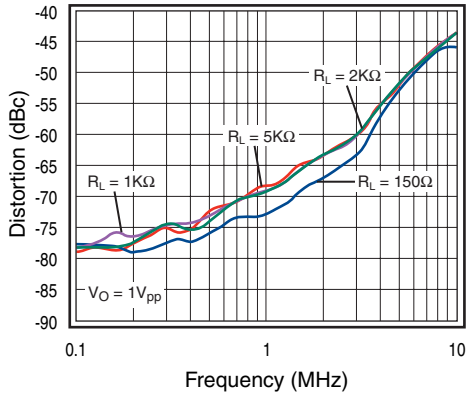
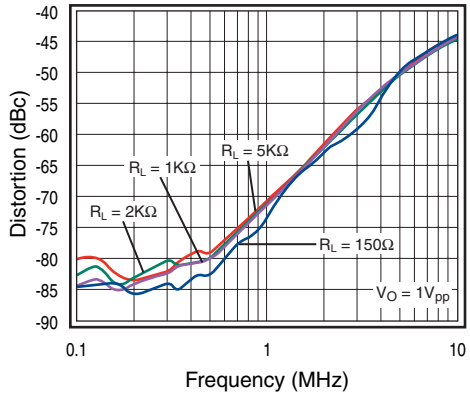


Figure 12. HD3 vs. R_L (+3V)



Typical Performance Characteristics

T_c = 25°C, V_S = 5V, R_L = 2kΩ to V_S/2 for V_S = 5V and 3V, R_L = 2kΩ to ground for V_S = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

Figure 13. HD2 vs. V_O (+5V)

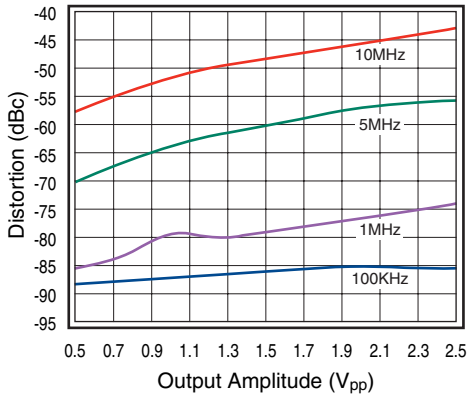


Figure 14. HD3 vs. V_O (+5V)

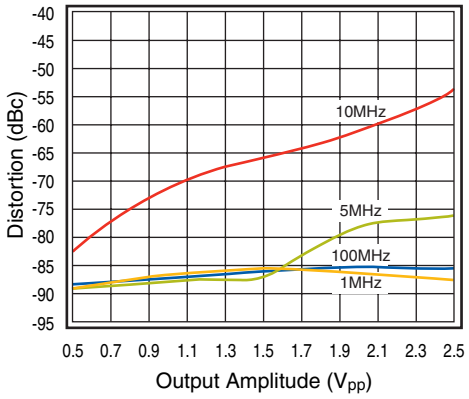


Figure 15. CMRR vs. Frequency

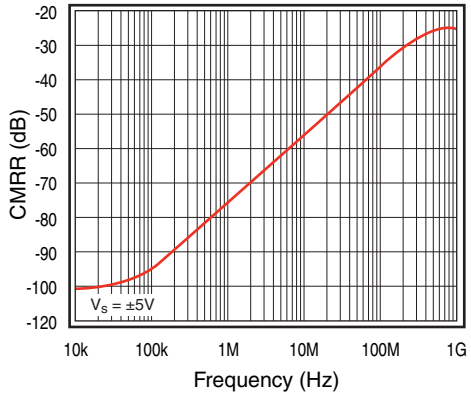


Figure 16. PSRR vs. Frequency

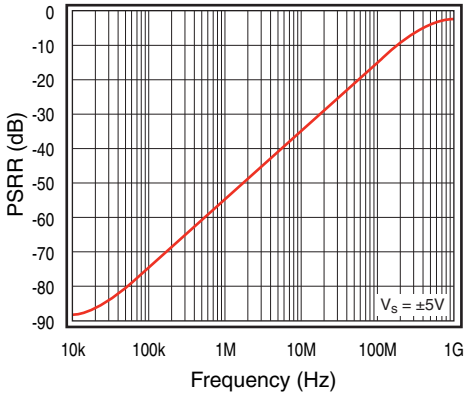


Figure 17. Open Loop Gain and Phase

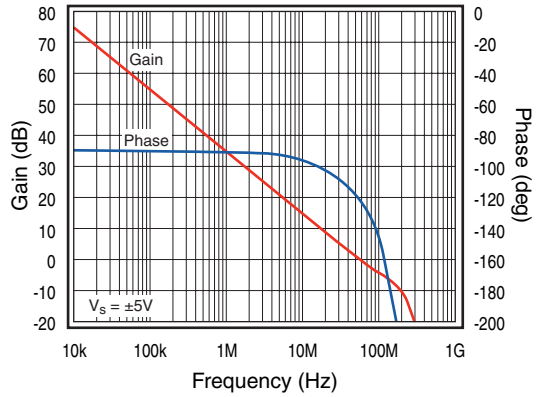
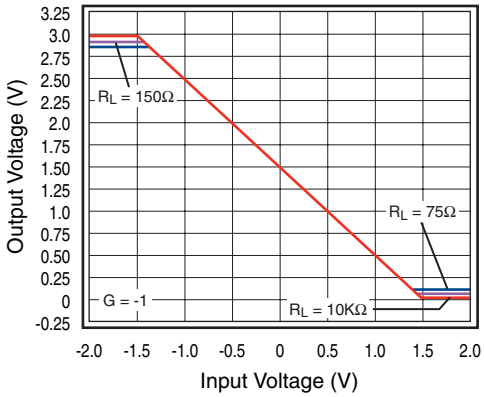


Figure 18. Output Swing vs. Load (+3V)



Typical Performance Characteristics

T_c = 25˚C, V_S = 5V, R_L = 2kΩ to V_S/2 for V_S = 5V and 3V, R_L = 2kΩ to ground for V_S = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

Figure 19. Input Voltage Noise (+3V)

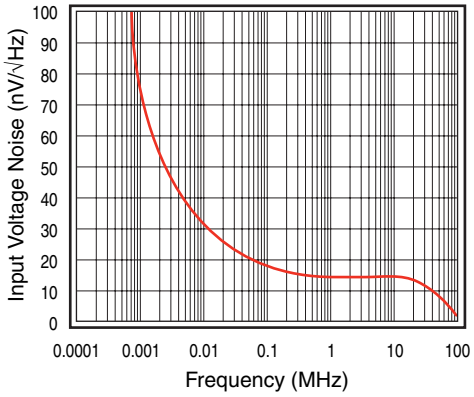


Figure 20. Crosstalk vs. Frequency (+3V)

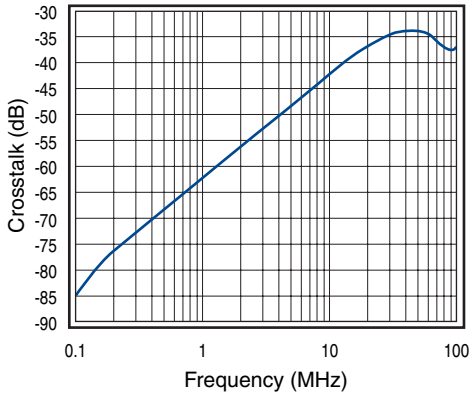


Figure 21. Pulse Resp. vs. Common Mode Voltage

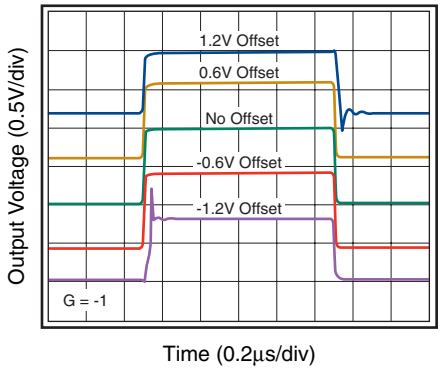


Figure 22. Large Signal Pulse Response (+3V)

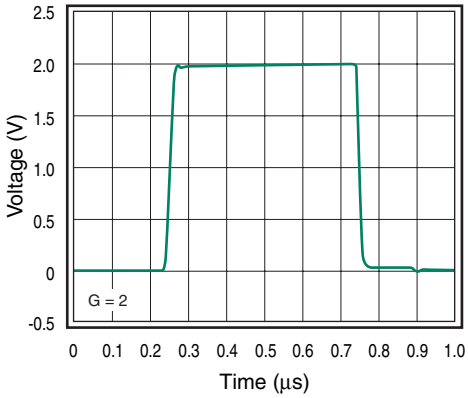


Figure 23. Large Signal Pulse Response (+5V)

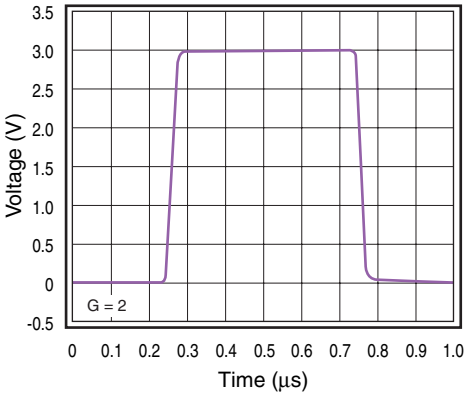
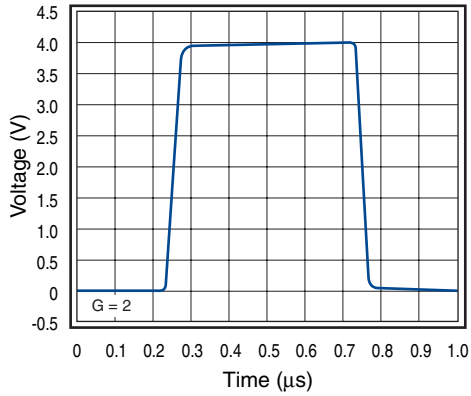


Figure 24. Large Signal Pulse Response (±5V)



Typical Performance Characteristics

T_c = 25°C, V_S = 5V, R_L = 2kΩ to V_S/2 for V_S = 5V and 3V, R_L = 2kΩ to ground for V_S = ±5V, G = 2, R_f = R_g = 1kΩ; unless otherwise noted.

Figure 25. Differential Gain and Phase (±2.5V)

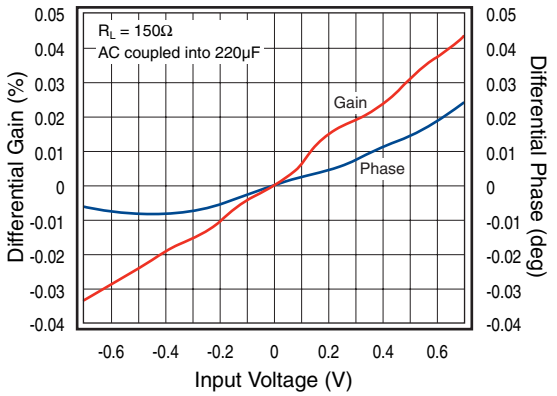
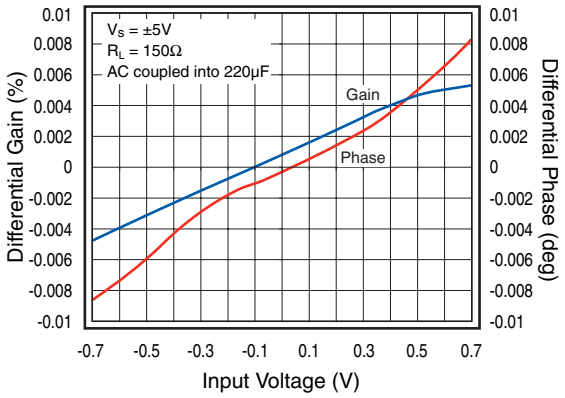


Figure 26. Differential Gain and Phase (±5V)



Applications Information

General Description

The FHP3130 (single), FHP3230 (dual), and FHP3430 (quad) are low cost, high performance, voltage feedback amplifiers that consume only 2.5mA of supply current per channel while providing ±100mA of output current. These amplifiers are designed to operate from 2.7V to 12V (±6V) supplies. The common mode voltage range extends below the negative rail and the output provides rail-to-rail performance.

The FHP3130, FHP3230, and FHP3430 are designed on a complimentary bipolar process and provide 170MHz of bandwidth and 110V/µs of slew rate at a supply voltage of ±5V. The combination of low power, rail-to-rail performance, low voltage operation, and tiny package options make these amplifiers well suited for use in many general purpose high speed applications.

These amplifiers also provide excellent video specifications. They offer extremely low differential gain and phase (0.008%/0.01˚) and 0.1dB gain flatness to 16MHz for superb standard definition video performance. Their output drive capability effortlessly supports 4 video loads.

Driving Capacitive Loads

The Frequency Response vs. C_L plot on page 8, illustrates the response of the FHP3230 Family. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 27, will improve stability and settling performance. R_S values in the *Frequency Response vs. C_L* plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_S.

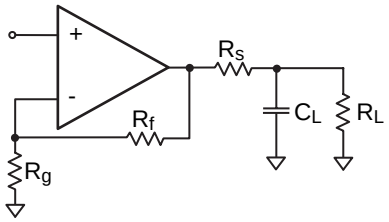


Figure 27. Typical Topology for Driving Capactive Loads

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

The FHP3130, FHP3230 and FHP3430 are short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

Power Dissipation = $I_S * (V_S+ - V_S-) + (V_S+ - V_{O(RMS)}) * I_{OUT(RMS)}$

Where I_S is the supply current, V_S+ is the positive supply pin voltage, V_S- is the negative supply pin voltage, $V_{O(RMS)}$ is the RMS output voltage and $I_{OUT(RMS)}$ is the RMS output current delivered to the load.

Follow the maximum power derating curves shown in Figure 28 below to ensure proper operation.

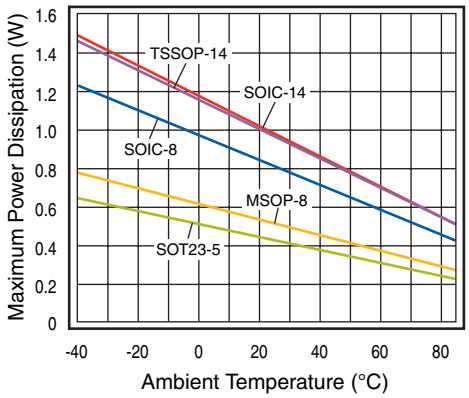


Figure 28. Maximum Power Derating

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3130/3230/3430 will typically recover in less than 50ns from an overdrive condition. Figure 29 shows the FHP3230 in an overdriven condition.

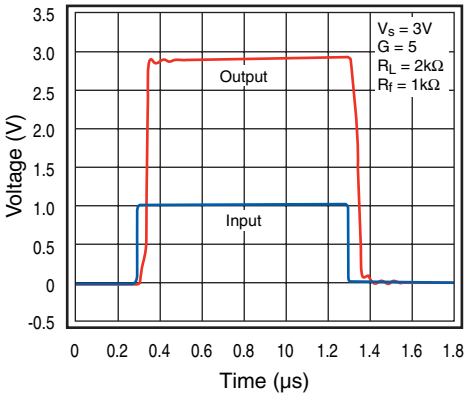


Figure 29. Overdrive Recovery

Composite Video Summer

The bandwidth and differential gain/phase performance of the FHP3130/3230/3430 amplifiers make them well suited for video applications. Figure 30 shows a typical Composite Video Summer. The high output current capability allows for driving multiple video loads. Figure 31 shows the resulting differential gain/phase of this 3-amp configuration driving 4 video loads, 37.5Ω.

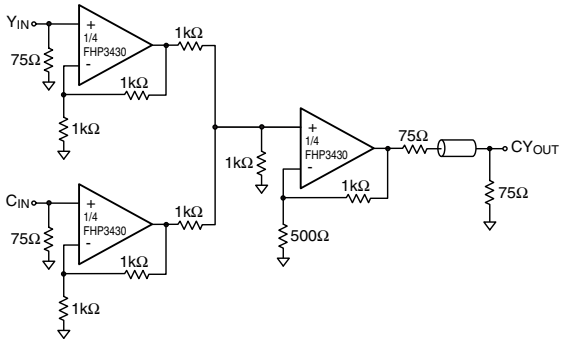


Figure 30. Typical Composite Video Summer

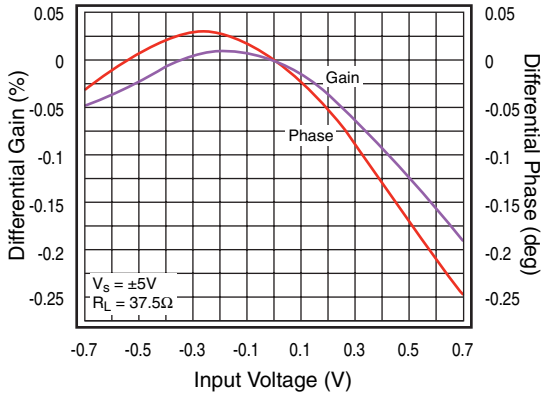


Figure 31. DG/DP of CV Summer Driving 4 Video Loads

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.01µF ceramic capacitors
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.01µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of thes devices:

Evaluation Board #	Products
KEB002	FHP3130IS5X
KEB003	FHP3130IM8X
KEB010	FHP3230IMU8X
KEB006	FHP3230IM8X
KEB012	FHP3430IMTC14X
KEB018	FHP3430IM14X

Evalutaion Board Schematics

Evaluation board schematics and layouts are shown in Figures 32 thru 46. These evaluation boards are built for dual supply operation. Follow these steps to use the board in a single supply application:

1. Short $-V_S$ to ground

2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

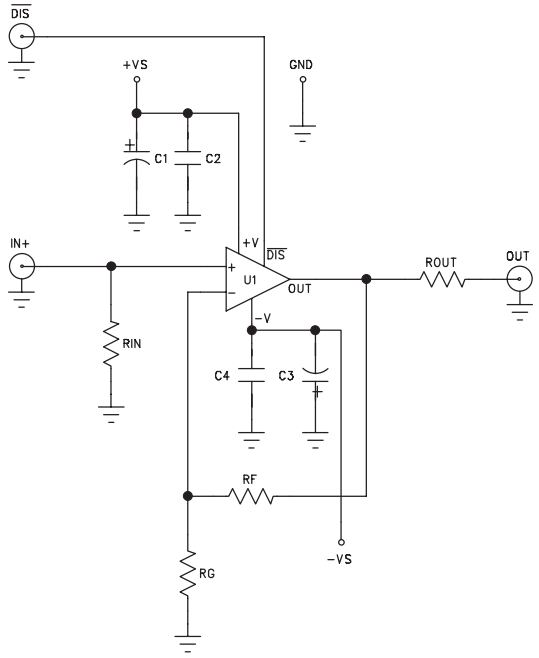


Figure 32. FHP3130 KEB002/KEB003 Schematic

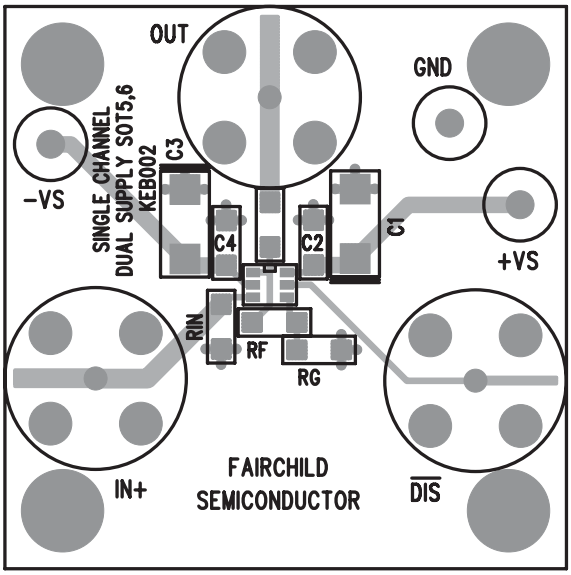


Figure 33. FHP3130 KEB002 (top side)

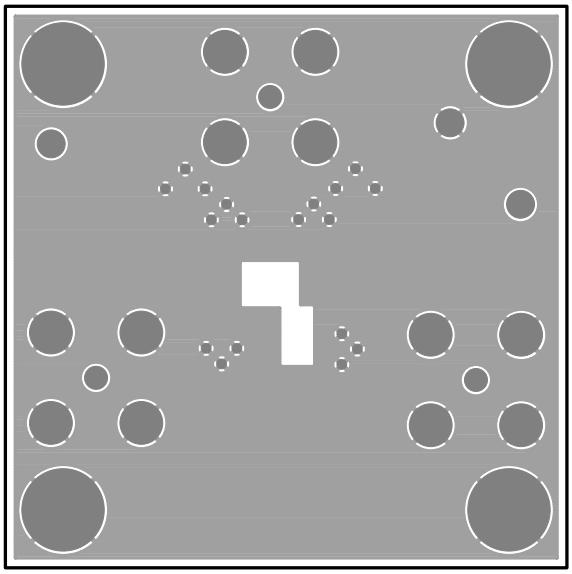


Figure 34. FHP3130 KEB002 (bottom side)

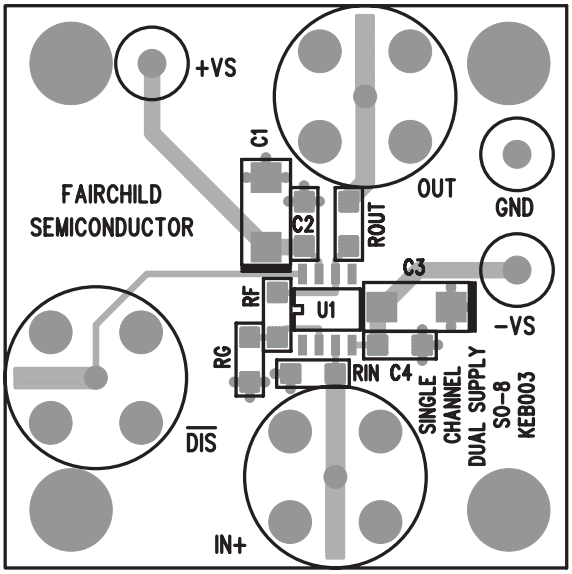


Figure 35. FHP3130 KEB003 (top side)

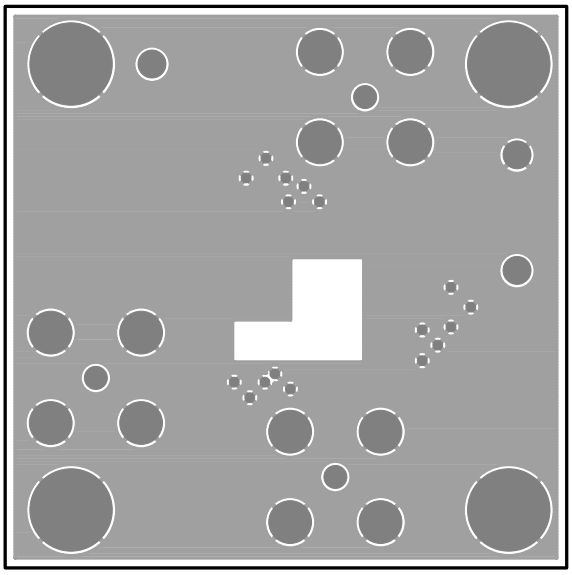


Figure 36. FHP3130 KEB003 (bottom side)

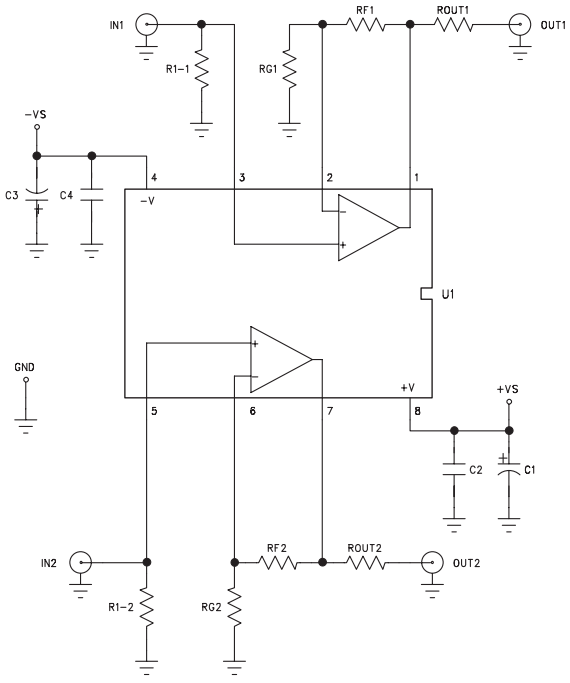


Figure 37. FHP3230 KEB006/KEB010 Schematic

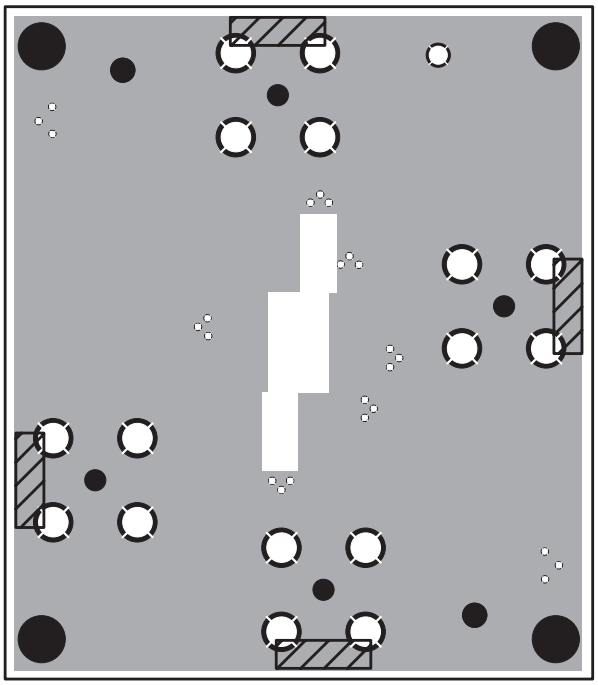


Figure 39. FHP3230 KEB006 (bottom side)

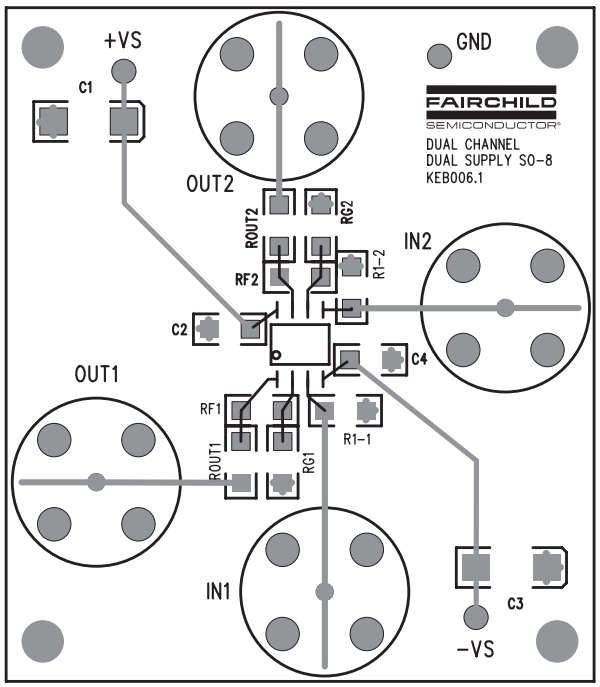


Figure 38. FHP3230 KEB006 (top side)

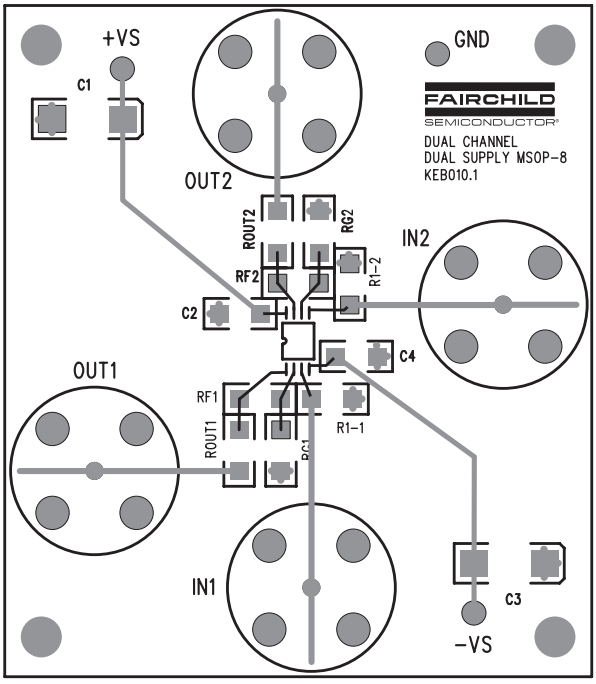


Figure 40. FHP3230 KEB010 (top side)

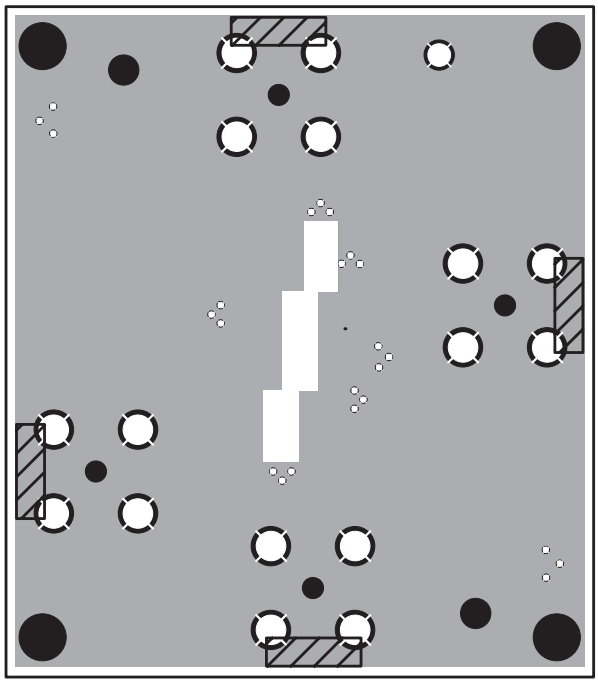


Figure 41. FHP3230 KEB010 (bottom side)

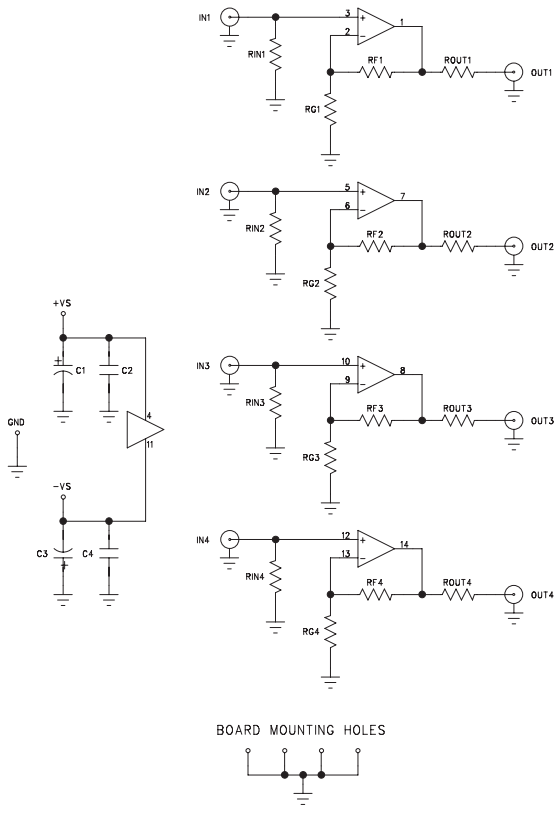


Figure 42. FHP3430 KEB012/KEB018 Schematic

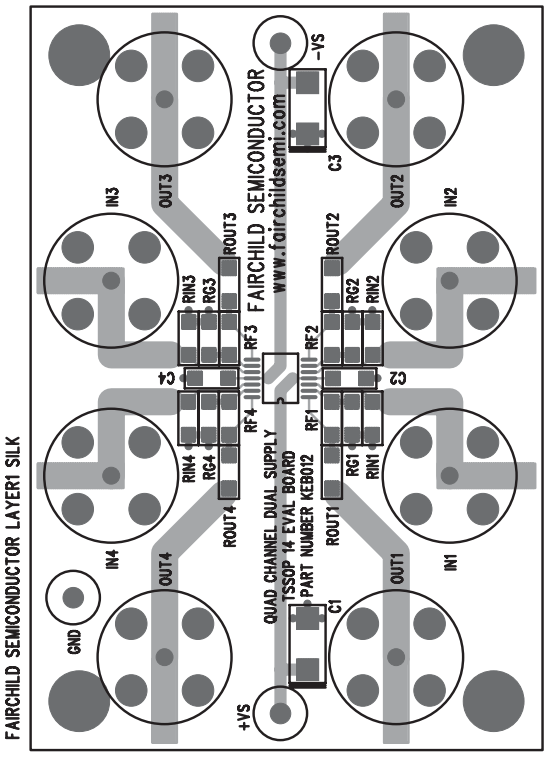


Figure 43. FHP3430 KEB012 (top side)

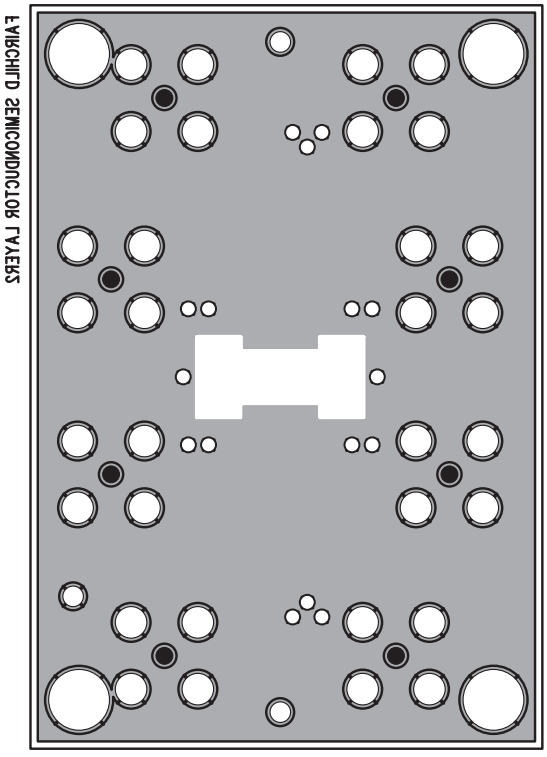


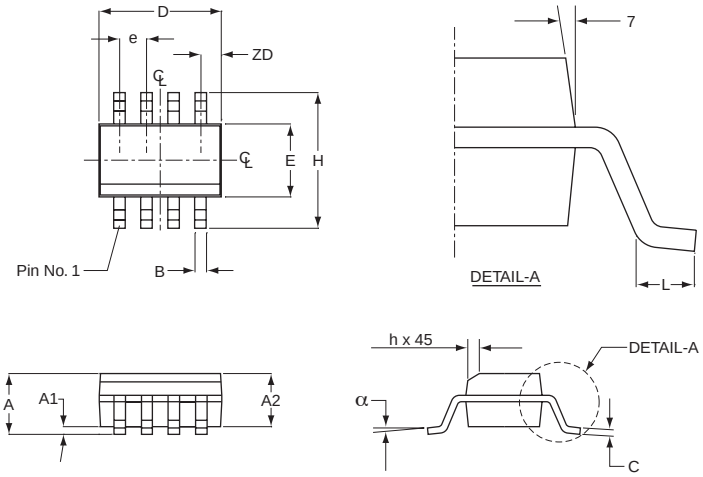
Figure 44. FHP3430 KEB012 (bottom side)

Figure 45. FHP3430 KEB018 (top side)

Figure 46. FHP3430 KEB018 (bottom side)

Mechanical Dimensions

8-Lead Outline Package (SOIC)

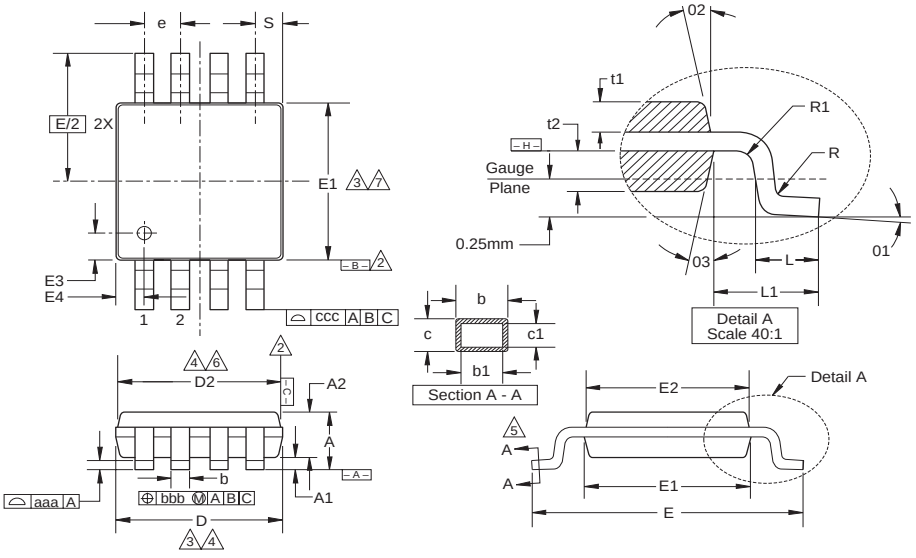


SOIC-8		
SYMBOL	**MIN**	**MAX**
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.53 ref	
A2	1.37	1.57

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.152mm (.006) per side (D).

8-Lead Outline Package (MSOP)



MSOP-8		
SYMBOL	**MIN**	**MAX**
A	1.10	–
A1	0.10	0.05
A2	0.86	0.08
D	3.00	0.10
D2	2.95	0.10
E	4.90	0.15
E1	3.00	0.10
E2	2.95	0.10
E3	0.51	0.13
E4	0.51	0.13
R	0.15	+0.15/-0.06
R1	0.15	+0.15/-0.06
t1	0.31	0.08
t2	0.41	0.08
b	0.33	+0.07/-0.08
b1	0.30	0.05
c	0.18	0.05
c1	0.15	+0.03/-0.02
01	3.0	3.0
02	12.0	3.0
03	12.0	3.0
L	0.55	0.15
L1	0.95 BSC	–
aaa	0.10	–
bbb	0.08	–
ccc	0.25	–
e	0.65 BSC	–
S	0.525 BSC	–

NOTE:

1 All dimensions are in millimeters (angle in degrees), unless otherwise specified.

2 Datums – B – and – C – to be determined at datum plane – H –.

3 Dimensions "D" and "E1" are to be determined at datum – H –.

4 Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.

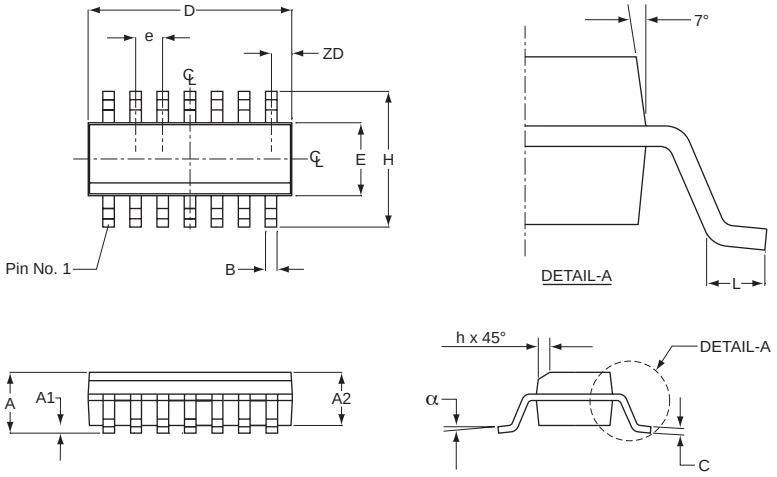
5 Cross sections A – A to be determined at 0.13 to 0.25mm from the leadtip.

6 Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.

7 Dimension "E1" and "E2" does not include interlead flash or protrusion.

Mechanical Dimensions

14-Lead Outline Package (SOIC)

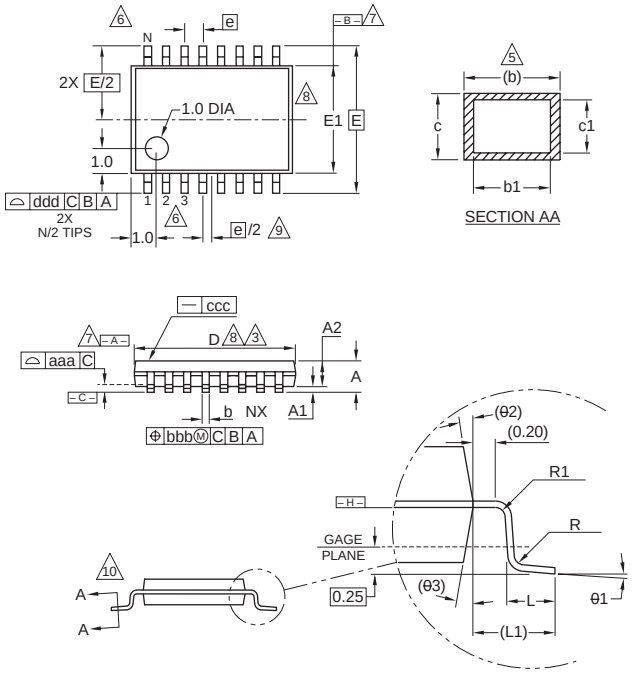


SOIC-14		
SYMBOL	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.337	.344
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
	0°	8°
ZD	0.20 ref	
A2	.054	.062

NOTE:

1. All dimensions are in inches.
2. Lead coplanarity should be 0 to 0.10mm (.004") n
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~3(
4. All dimensions excluding mold flashes and end fla from the package body shall not exceed o.152mn per side (d).

14-Lead Outline Package (TSSOP)



TSSOP-14			
SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0.05	–	0.15
A2	0.85	0.90	0.95
L	0.50	0.60	0.75
R	0.09	–	–
R1	0.09	–	–
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	–	0.16
θ1	0°	–	8°
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
θ2	12° REF		
θ3	12° REF		
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	14		

NOTES:

1 All dimensions are in millimeters (angle in degrees).

2 Dimensioning and tolerancing per ASME Y14.5–1994.

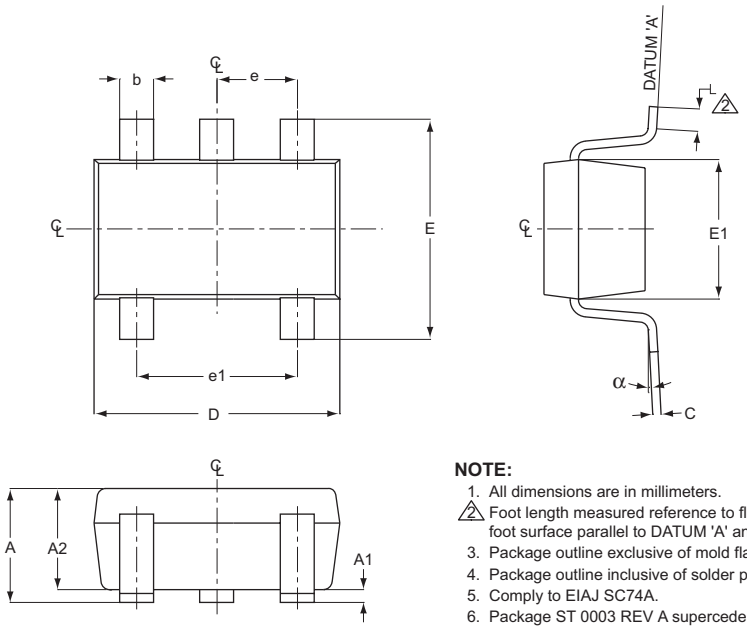
3 Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .

4 Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.

5 Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar connot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.

Mechanical Dimensions

5-Lead Outline Package (SOT23)



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.25	0.50
C	0.09	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 ref	
e1	1.90 ref	
α	0°	10°

NOTE:

1. All dimensions are in millimeters.
2. Foot length measured reference to flat foot surface parallel to DATUM 'A' and lead surface.
3. Package outline exclusive of mold flash & metal burr.
4. Package outline inclusive of solder plating.
5. Comply to EIAJ SC74A.
6. Package ST 0003 REV A supercedes SOT-D-2005 REV C.

Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty
FHP3130	FHP3130IS5X*	Yes	SOT23-5	Reel	3000
FHP3130	FHP3130IM8X*	Yes	SOIC-8	Reel	2500
FHP3230	FHP3230IMU8X*	Yes	MSOP-8	Reel	3000
FHP3230	FHP3230IM8X	Yes	SOIC-8	Reel	2500
FHP3430	FHP3430IMTC14X*	Yes	TSSOP-14	Reel	2500
FHP3430	FHP3430IM14X*	Yes	SOIC-14	Reel	2500

Temperature range for all parts: -40˚C to +85˚C.

Moisture sensitivity level for all parts is MSL-1.

* Preliminary

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
ActiveArray™
Bottomless™
Build it Now™
CoolFET™
CROSSVOLT™
DOME™
EcoSPARK™
E^2CMOS™
EnSigna™
FACT™
FACT Quiet Series™
FAST®
FASTr™
FPS™
FRFET™
GlobalOptoisolator™
GTO™
HiSeC™
I^2C™
i-Lo™
ImpliedDisconnect™
IntelliMAX™
ISOPLANAR™
LittleFET™
MICROCOUPLER™
MicroFET™
MicroPak™
MICROWIRE™
MSX™
MSXPro™
OCX™
OCXPro™
OPTOLOGIC®
OPTOPLANAR™
PACMAN™
POP™
Power247™
PowerEdge™
PowerSaver™
PowerTrench®
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
µSerDes™
SILENT SWITCHER®
SMART START™
SPM™
Stealth™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
TinyLogic®
TINYOPTO™
TruTranslation™
UHC™
UltraFET®
UniFET™
VCX™
Wire™

Across the board. Around the world.™
The Power Franchise®
Programmable Active Droop™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I16

