System Power Supply LSI Series for Use in Automotive Electronics

DMOS System Power Supply ICs with low current consumption

BD4912/BD4912-V4

●Description

The BD4912/BD4912-V4 provides multiple supply voltage outputs for use in car audio and satellite navigation systems with CD player, radio, antenna, lighting, and other components. In addition to overcurrent, overvoltage, and thermal shutdown circuits, it incorporates circuitry for reacting to sudden BATTERY power failures and is ideal for car audio and satellite navigation systems. With its 110 μA (max.) standby current, the BD4912/BD4912-V4 delivers low current consumption when the BATTERY is off.

●Features

1) Built-in power supplies for car audio and satellite navigation systems
   - 5.0 V microcontroller power supply
   - 8.12 V audio power supply
   - 7.9 V radio power supply
   - 10.3 V lighting power supply
   - 1 V_{DD}-linked high side switch
   - 2 V_{CC}-linked high side switches
2) Compatible with 0.1 μF output load ceramic capacitors. (Note: Select the adequate capacitance values for each particular application)
3) The ability to operate V_{DD} using the charge stored in a backup capacitor, prevents the IC from malfunctioning in the event of a sudden BATTERY power failure.
4) Output pins use low-dropout P-channel POWER MOS FETs
5) Built-in overcurrent protection circuits
6) Built-in overvoltage protection circuits
7) Built-in thermal shutdown circuit
8) A 12-pin power package gives the IC large power dissipation capabilities and is ideal for space-saving designs.

● Applications

Car audio and satellite navigation systems

●**Absolute maximum ratings** (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage 1	$V_{CC}1$	36	V
Supply Voltage 2	$V_{CC}2$	36	V
SEL1 Supply Voltage	SEL1	12	V
SEL2 Supply Voltage	SEL2	12	V
Power Dissipation	Pd	3400	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
Peak Supply Voltage 1	$V_{CC}1$ PEAK	50 (*1)	V
Peak Supply Voltage 2	$V_{CC}2$ PEAK	50 (*1)	V

*1 tr ≥ 1 ms; Bias voltage is applied for less than 200 ms.

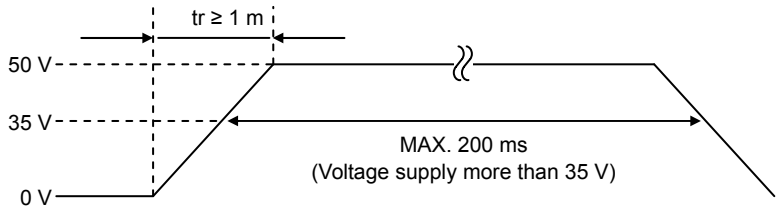


Fig.1 Peak Supply Voltage Waveform

●**Recommended operating ranges** (Ta = 25°C)

Parameter	Limits	Unit	Comment
Recommended Supply Voltage Range1	10 to 18	V	Except V_{DD} and ILM output
Recommended Supply Voltage Range 2	11.5 to 18	V	ILM output
Recommended Supply Voltage Range 3	6.3 to 18	V	V_{DD} output

●**Electrical characteristics** (Unless otherwise specified, Ta = 25°C; $V_{CC}1$ = $V_{CC}2$ = 14.4 V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Standby Circuit Current	Ist	—	—	110	μA	
Output Voltage (V_{DD}) 1	V_O1	4.80	5.00	5.20	V	I_O = 300 mA, $V_{CC}2$ = 10 V to 18 V
Dropout Voltage	ΔV_O1	—	0.8	1.1	V	I_O = 300 mA, $V_{CC}2$-V_O1
Peak Output Current	I_O1	400	—	—	mA	V_O1 ≥ 4.8 V
Ripple Rejection Ratio	R.R1	50	55	—	dB	f = 100 Hz, VRR = -10 dBV, I_O = 300 mA
Low Vcc Output Voltage	V_O1'	4.8	—	—	V	$V_{CC}2$ = 5 V, I_O = 10 mA
Output Voltage (AUDIO) 2	V_O2	7.8	8.12	8.3	V	I_O2 = 200 mA, $V_{CC}1$ = 10 V to 18 V
Dropout Voltage	ΔV_O2	—	0.4	0.7	V	I_O2 = 200 mA, $V_{CC}1$-V_O2
Peak Output Current	I_O2	200	—	—	mA	V_O2 ≥ 7.8 V
Ripple Rejection Ratio	R.R2	45	55	—	dB	f = 100 Hz, VRR = -10 dBV, I_O = 200 mA

⦿ This product is not designed for protection against radioactive rays.

⦿ Use Peak Output Current less than Limits Min. values.

●**Electrical characteristics** (Unless otherwise specified, Ta = 25°C; $V_{CC}1 = V_{CC}2 = 14.4$ V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
(SEL1 > 3.5 V)						
Dropout Voltage (P.CON) 3	ΔV_O3	—	0.4	0.7	V	I_O3 = 350 mA, $V_{CC}1$-V_O3
Peak Output Current	I_O3	350	—	—	mA	$V_O3 \geq 13.7$ V
(SEL1 > 7.0 V)						
Dropout Voltage (P.ANT) 4	ΔV_O4	—	0.4	0.7	V	I_O4 = 300 mA, $V_{CC}1$-V_O4
Peak Output Current	I_O4	300	—	—	mA	$V_O4 \geq 13.7$ V
(SEL2 > 3.5 V)						
Output voltage (AM) 5	V_O5	7.5	7.9	8.3	V	I_O5 = 25 mA, $V_{CC}1$ = 10 V to 18 V
Dropout Voltage	ΔV_O5	—	0.4	0.7	V	I_O5 = 25 mA, $V_{CC}1$-V_O5
Peak Output Current	I_O5	25	—	—	mA	$V_O5 \geq 7.5$ V
Ripple Rejection Ratio	R.R5	45	55	—	dB	f = 100 Hz, VRR = -10 dBV, I_O = 25 mA
(SEL2 > 2.0 V)						
Dropout Voltage (SW5V)	ΔV_O6	—	0.15	0.3	V	I_O6 = 30 mA, V_{DD}-V_O6
Peak Output Current	I_O6	30	—	—	mA	$V_O6 \geq V_{DD}$-0.2V
(SEL1 > 1.5 V)						
Output voltage (ILM) 7	V_O7	9.9	10.3	10.7	V	I_O7 = 200 mA, $V_{CC}1$ = 12 V to 18 V
Dropout Voltage	ΔV_O7	—	0.5	0.8	V	I_O7 = 200 mA, $V_{CC}1$-V_O7
Peak Output Current	I_O7	200	—	—	mA	$V_O7 \geq 9.9$ V
Ripple Rejection Ratio	R.R7	40	50	—	dB	f = 100 Hz, VRR = -10 dBV, I_O = 200 mA
Input (SEL1)						
Standby Level	Vth1-1	—	—	1.0	V	
ILM ON	Vth1-2	1.5	—	3.0	V	
ILM, P-CON ON	Vth1-3	3.5	—	5.0	V	
ILM, P-CON, P-ANT ON	Vth1-4	7.0	—	12.0	V	
SEL1 Input Impedance	Rin1	100	—	—	kΩ	
Input (SEL2)						
Standby Level	Vth2-1	—	—	1.0	V	
AUDIO, SW5V ON	Vth2-2	2.0	—	3.0	V	
AUDIO, SW5V, AM ON	Vth2-3	3.5	—	V_{DD}	V	
SEL2 Input Impedance	Rin2	100	—	—	kΩ	
Overvoltage Protection Threshold	Vovp	27	30	33	V	

⦿ This product is not designed for protection against radioactive rays.

⦿ Use Peak Output Current less than Limits Min. values.

● **Reference data** (Unless otherwise specified, $V_{CC}1 = V_{CC}2 = 14.4$ V)

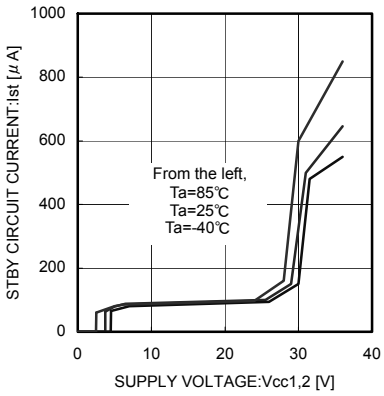


Fig.2 Standby Circuit Current

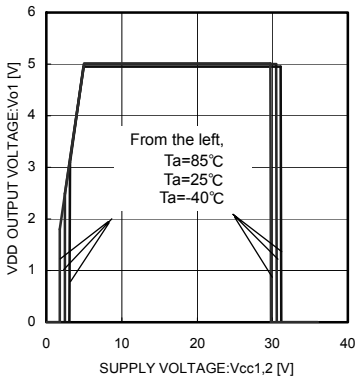


Fig.3 VDD Line Regulation
(I_O = No load)

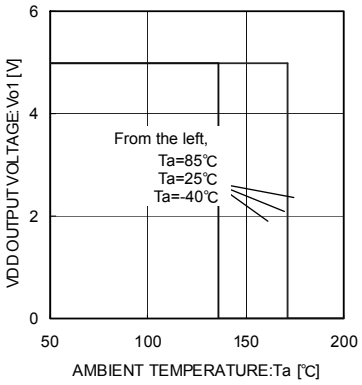


Fig.4 VDD Load Regulation

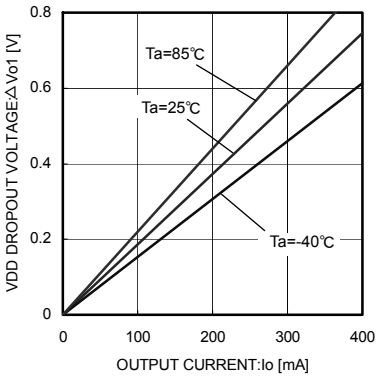


Fig.5 V_{DD} Dropout Voltage
($V_{CC}1 = V_{CC}2 = 4.8$ V)

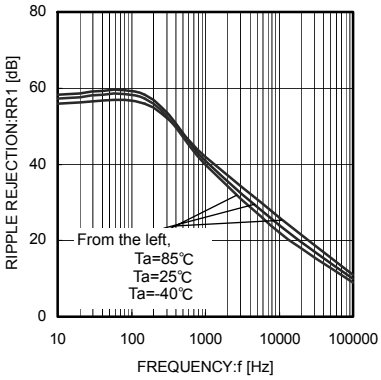


Fig.6 V_{DD} Ripple Rejection Ratio
(I_O = 300 mA)

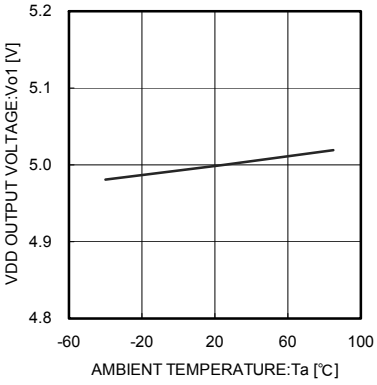


Fig.7 V_{DD} Output Voltage vs Temperature

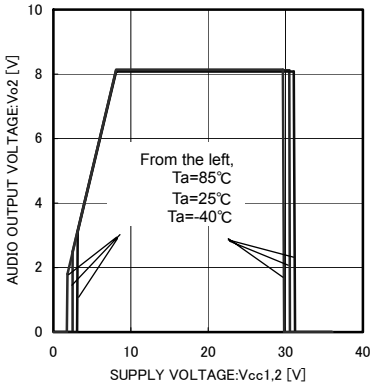


Fig.8 AUDIO Line Regulation
(I_O = No load)

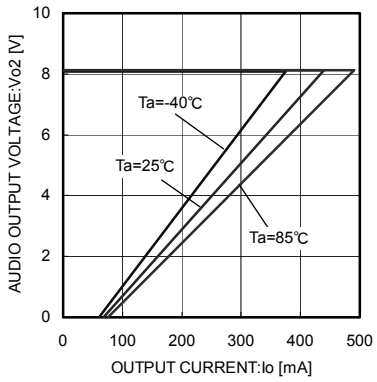


Fig.9 AUDIO Load Regulation

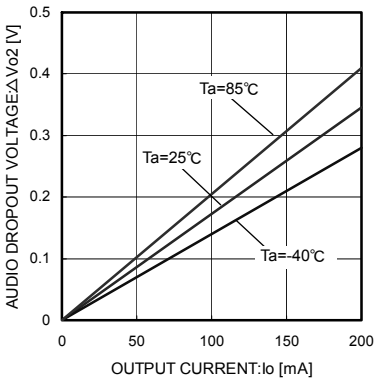


Fig.10 AUDIO Dropout Voltage
($V_{CC}1 = V_{CC}2 = 7.8$ V)

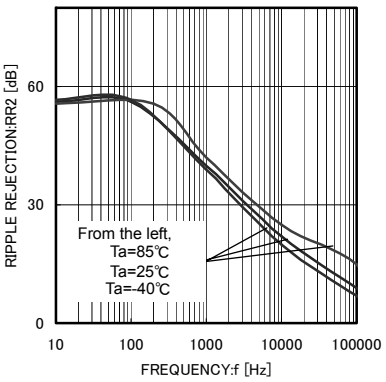


Fig.11 AUDIO Ripple Rejection Ratio
(I_O = 200 mA)

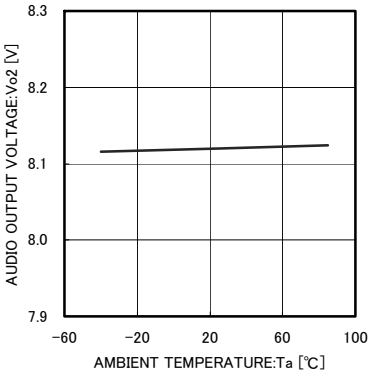


Fig.12 AUDIO Output Voltage vs Temperature

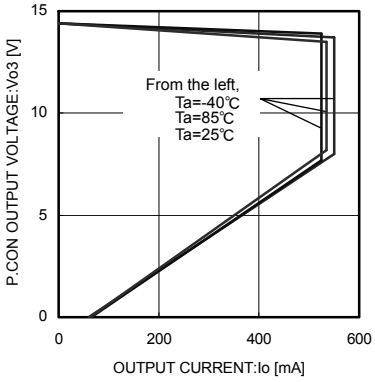


Fig.13 P.CON Load Regulation

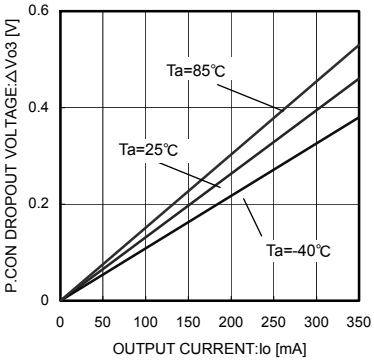


Fig.14 P.CON Dropout Voltage

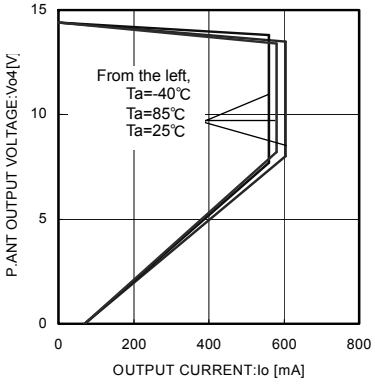


Fig.15 P.ANT Load Regulation

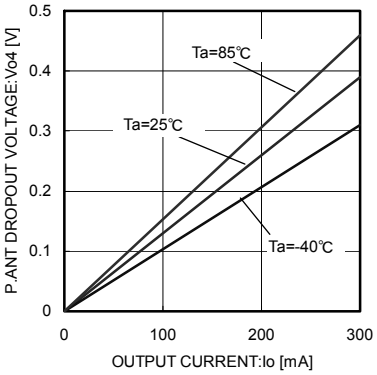


Fig.16 P.ANT Dropout Voltage

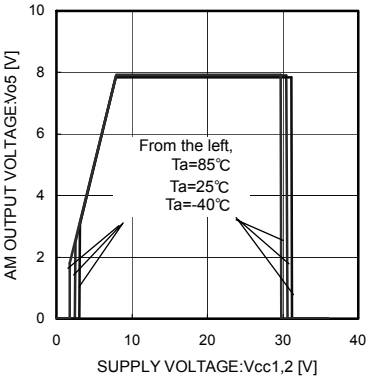


Fig.17 AM Line Regulation
(I_O = No load)

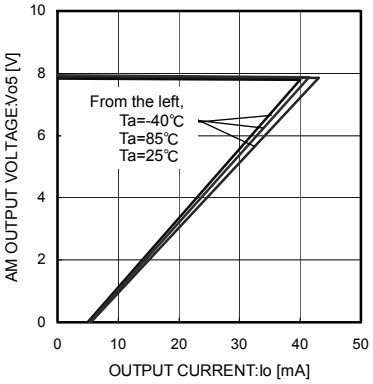


Fig.18 AM Load Regulation

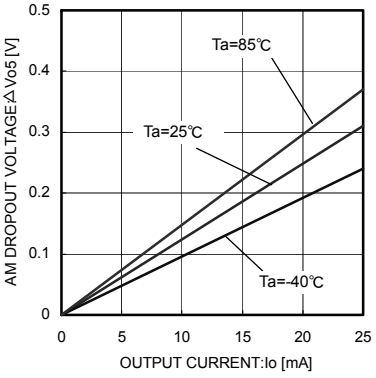


Fig.19 AM Dropout Voltage
($V_{CC}1$ = $V_{CC}2$ = 7.5 V)

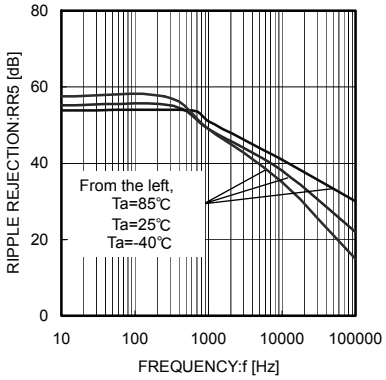


Fig.20 AM Ripple Rejection Ratio
(I_O = 25 mA)

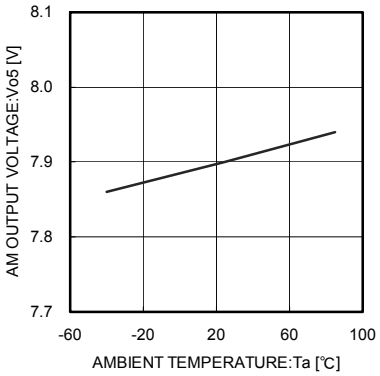


Fig.21 AM Output Voltage
vs Temperature

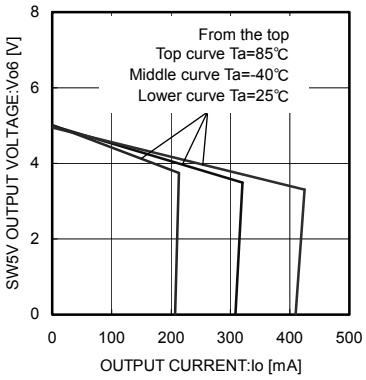


Fig.22 SW5V Load
Regulation

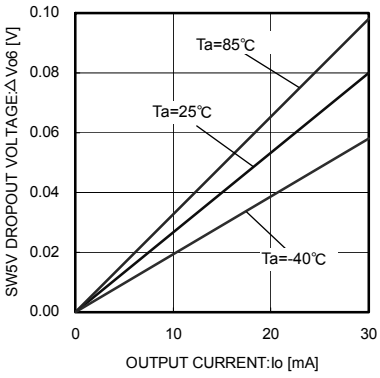


Fig.23 SW5V Dropout Voltage
($V_{CC}1$ = $V_{CC}2$ = 10 V)

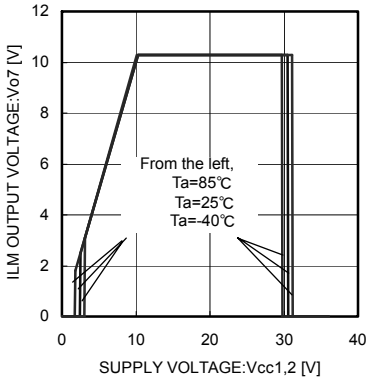


Fig.24 ILM Line Regulation
(I_O = No load)

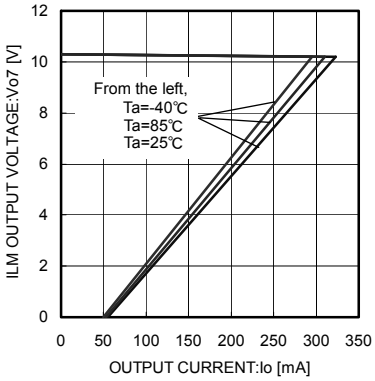


Fig.25 ILM Load Regulation

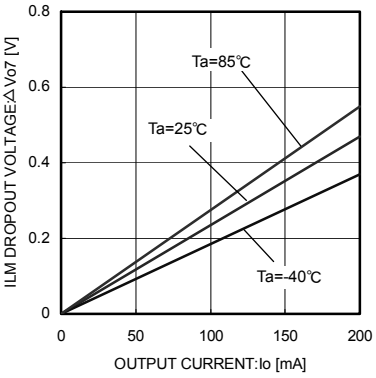


Fig.26 ILM Dropout Voltage
($V_{CC}1$ = $V_{CC}2$ = 9.9 V)

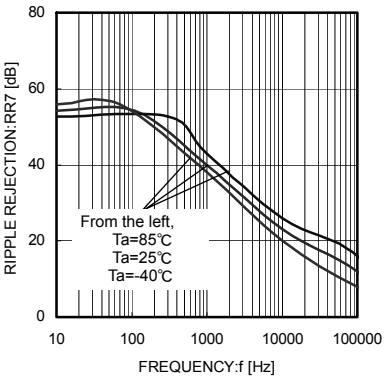


Fig.27 ILM Ripple Rejection Ratio
(I_O = 200 mA)

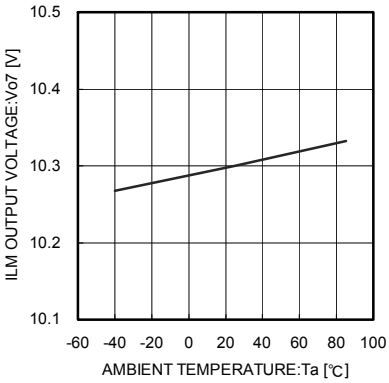


Fig.28 ILM Output Voltage
vs Temperature

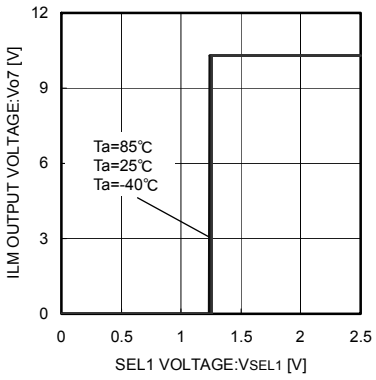


Fig.29 ILM Input Threshold Voltage

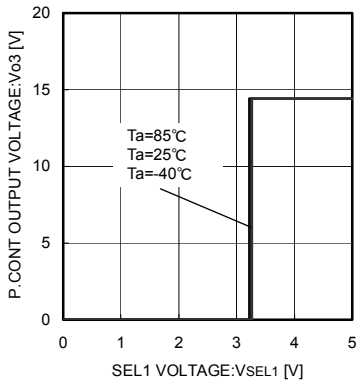


Fig.30 P.CON Input Threshold Voltage

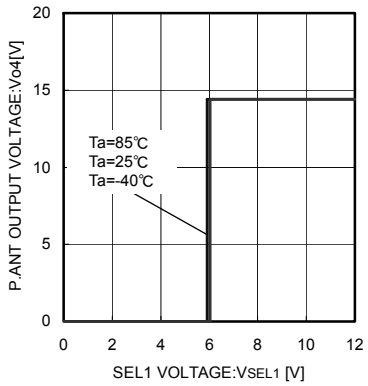


Fig.31 P.ANT Input Threshold Voltage

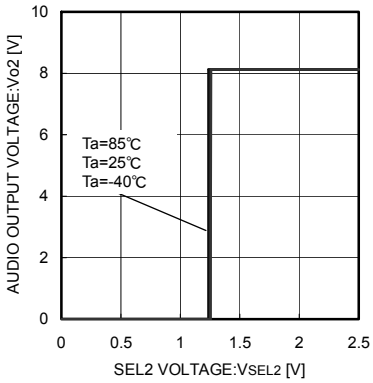


Fig.32 AUDIO Input Threshold Voltage

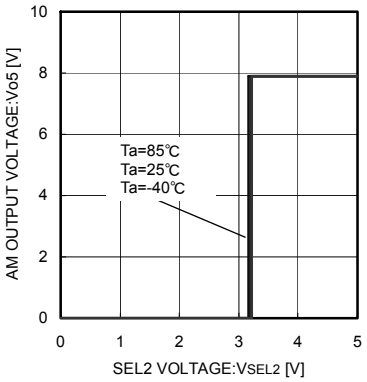


Fig.33 AM Input Threshold Voltage

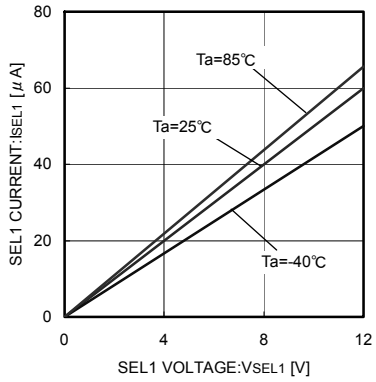


Fig.34 SEL1 Input Current

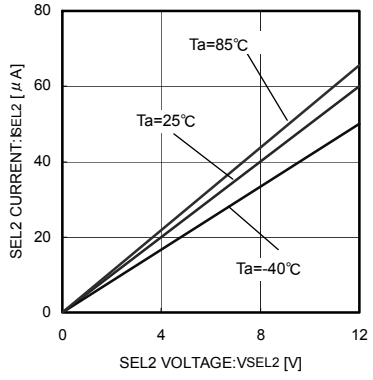


Fig.35 SEL2 Input Current

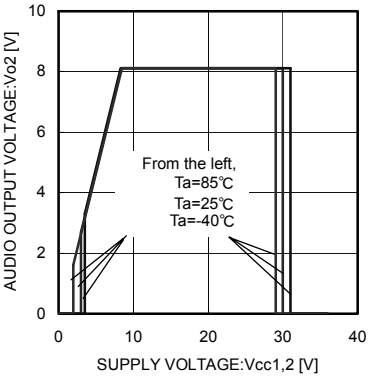


Fig.36 Overvoltage Operation

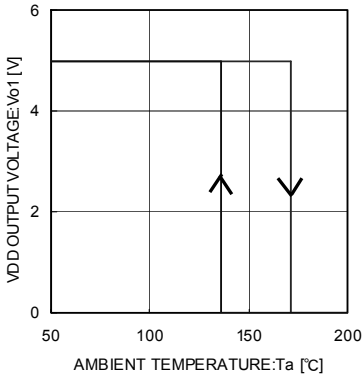


Fig.37 Thermal Shutdown Operation

●Block diagram

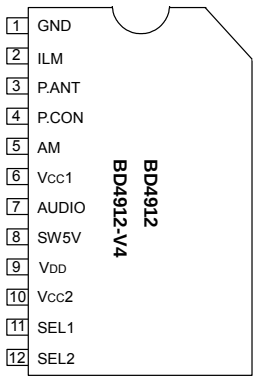


Fig.38 Pin Assignment Diagram

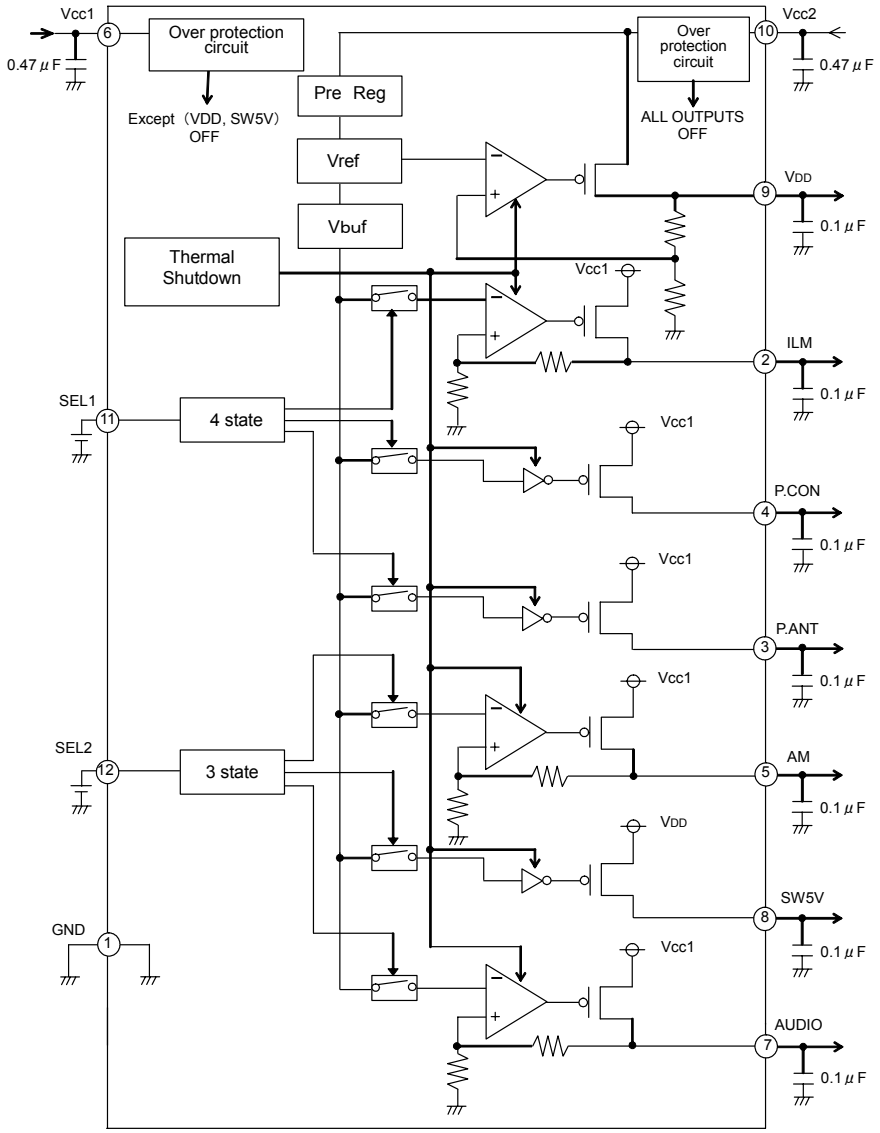


Fig.39 Block Diagram

●Pin descriptions

1	GND	This pin is connected to the IC's substrate.
2	ILM	This pin serves as the lighting power supply (10.3 V; Peak output current: 200 mA).
3	P.ANT	This pin outputs a voltage that is approximately 0.4 V (TYP) lower than the VCC1 pin voltage, and the peak output current is 300 mA.
4	P.CON	This pin outputs a voltage that is approximately 0.4 V (TYP) lower than the VCC1 pin voltage, and the peak output current is 350 mA.
5	AM	This pin serves as the AM receiver power supply (7.9 V; Peak output current: 25 mA).
6	VCC1	This pin is connected to the car's backup and ACC power supplies.
7	AUDIO	This pin serves as the common system power supply for volume and sound control (8.12 V, Peak output current: 200 mA), as well as the power supply for variable capacitance diodes and other components used for electronic tuning and cassette player features, such as the equalizer.
8	SW5V	This pin serves as the microcontroller power supply (5.0 V; Peak output current: 30 mA).
9	VDD	This pin serves as the microcontroller power supply (5.0 V; Peak output current: 400 mA).
10	VCC2	This pin serves as the VDD power supply pin.
11	SEL1	ILM, P.CON, and P.ANT output can be switched on or off by applying a 2.25 V, 4.25 V, or 9.5 V signal to this pin.
12	SEL2	AUDIO, SW5V, and AM output can be switched on or off by applying a 2.5 V or 4.25 V signal to this pin.

●I/O Equivalent circuit diagrams

3 PIN (P.ANT), 4 PIN (P.CON)

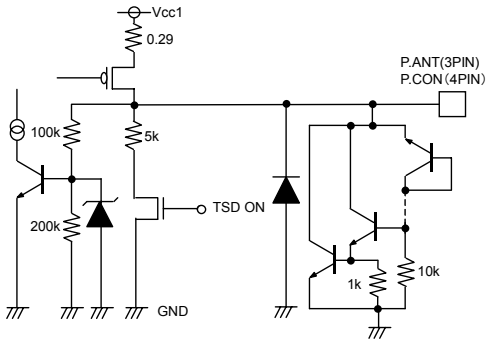


Fig.40

11 PIN (SEL1)

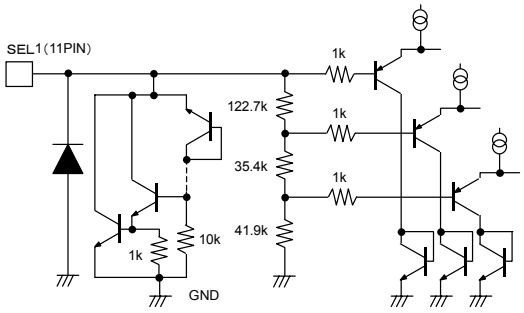
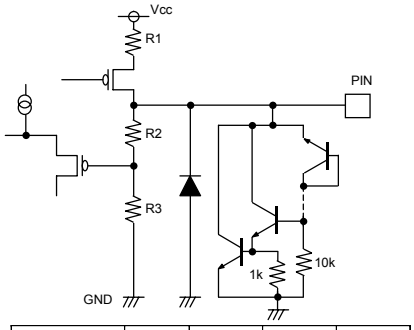


Fig.41

2, 5, 7, 9 PIN (ILM, AM, AUDIO, VDD)



PIN	Vcc	R1[Ω]	R2[kΩ]	R3[kΩ]
ILM (2PIN)	Vcc1	0.50	448.5	61.9
AM (5PIN)	Vcc1	4.00	445.4	80.7
AUDIO (7PIN)	Vcc1	0.43	437.7	78.5
VDD(9PIN)	Vcc2	0.25	381.3	125.0

Fig.42

12 PIN (SEL2)

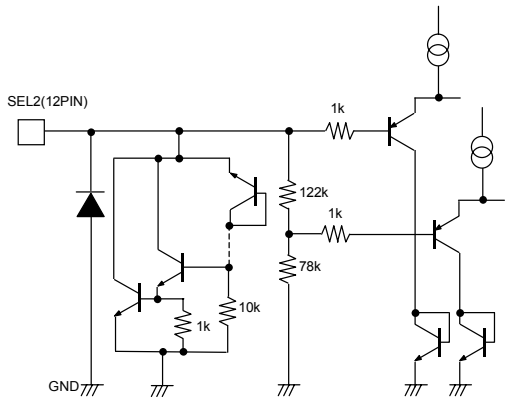


Fig.43

●Timing Chart

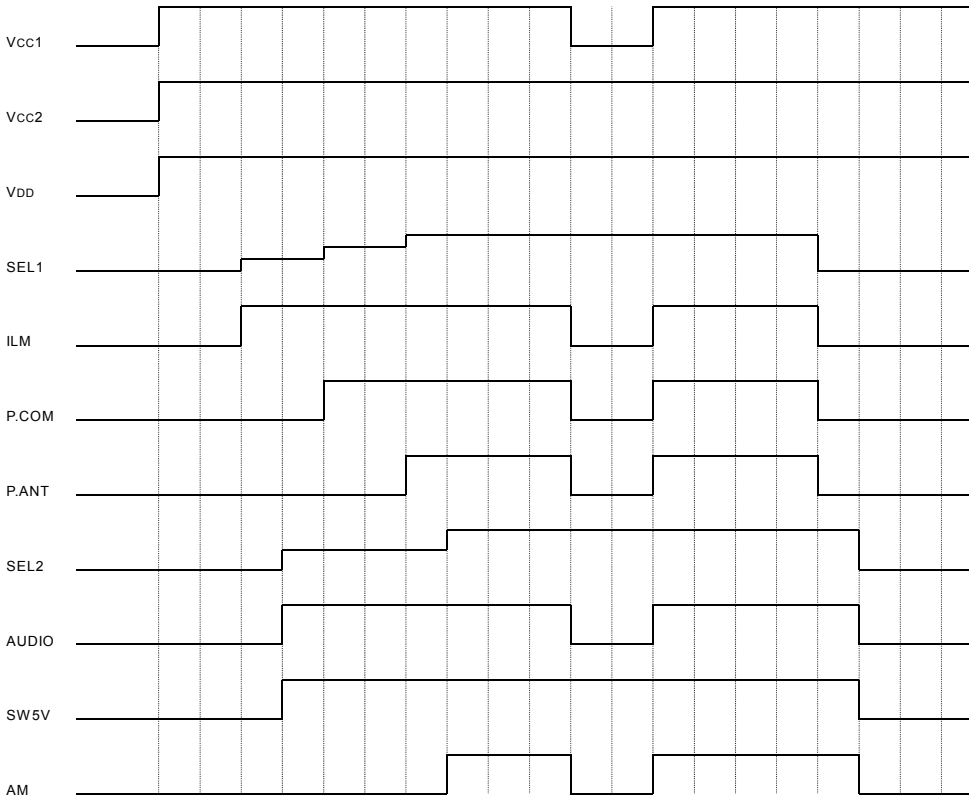
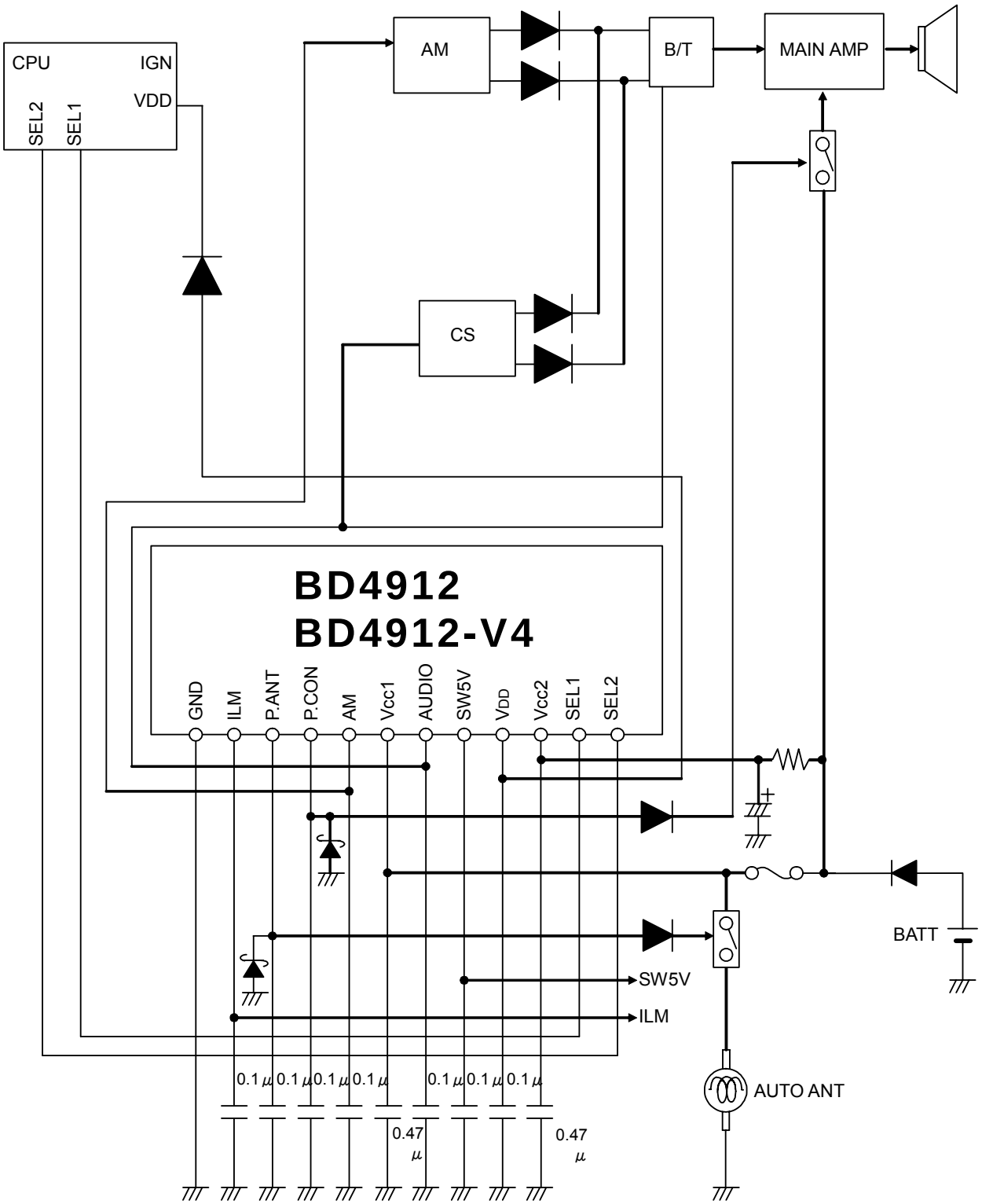


Fig.44 Timing Chart

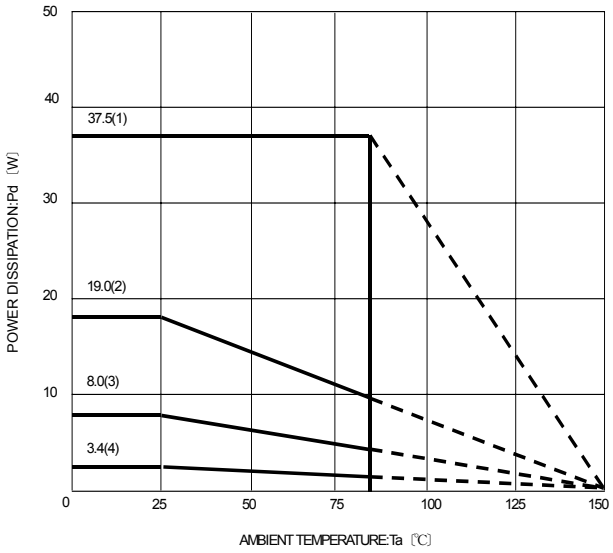
●**Application circuit**



(Unit R: Ω, C: F)

Fig.45 Application Circuits Example

●Thermal design



(1) When using an infinite heat sink θj-c = 2.0 (°C/W)
(2) 100 × 100 × 2 (mm^3) (when using an aluminum heat sink)
(3) 50 × 50 × 2 (mm^3) (when using an aluminum heat sink)
(4) IC without heat sink operation. θj-a = 36.8 (°C /W)
Note: When using an aluminum heat sink, use a tightening torque of 6 (Kg・cm) and apply silicon grease.

Fig.46 Power Dissipation Characteristics

Refer to the heat reduction characteristics illustrated in Fig. 46 when using the IC in an environment where Ta ≥ 25°C. The characteristics of the IC are greatly influenced by the operating temperature. If the temperature is in excess of the maximum junction temperature Tjmax, the elements of the IC may be deteriorated or damaged. It is necessary to give sufficient consideration to the heat of the IC in view of two points; First, the protection of the IC from instantaneous damage and second, the maintenance of the reliability of the IC in long-time operation.
In order to protect the IC from thermal destruction, it is necessary to operate the IC below the maximum junction temperature Tjmax. The chip's (junction area) temperature Tj may rise considerably even when the IC is being used at room temperature (25°C). Always operate the IC within the power dissipation Pd.

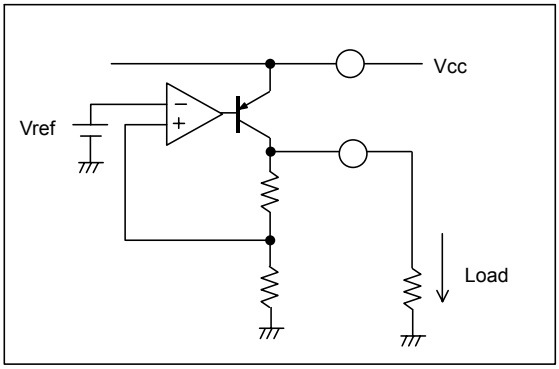


Fig.47

The maximum power consumption P_{MAX} (W) can be calculated as described below, where A denotes the maximum $V_{CC}1$ input voltage and B denotes the maximum $V_{CC}2$ input voltage:

I_1 = Max. V_{DD} output current
I_2 = Max. AUDIO output current
I_3 = Max. P.CON output current
I_4 = Max. P.ANT output current
I_5 = Max. AM output current
I_6 = Max. SW5V output current
I_7 = Max. ILM output current

- Power consumed by V_{DD} — $P1 = (B-5.0\ V) \times I_1$
- Power consumed by AUDIO — $P2 = (A-8.12\ V) \times I_2$
- Power consumed by P.CON — $P3 = 0.7\ V \times I_3$
- Power consumed by P.ANT — $P4 = 0.7\ V \times I_4$
- Power consumed by AM — $P5 = (A-7.9\ V) \times I_5$
- Power consumed by SW5V — $P6 = 0.7\ V \times I_6$
- Power consumed by ILM — $P7 = (A-10.3\ V) \times I_7$
- Power consumed by each circuit's current — P8 = A × Circuit current (circuit current is approximately 2 mA)

$P_{MAX} = P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 + P_8$

● **Operation Notes**

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.

3. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

7. Regarding input pin of the IC
   This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
   When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
   When GND > Pin B, the P-N junction operates as a parasitic transistor.
   Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.
   .

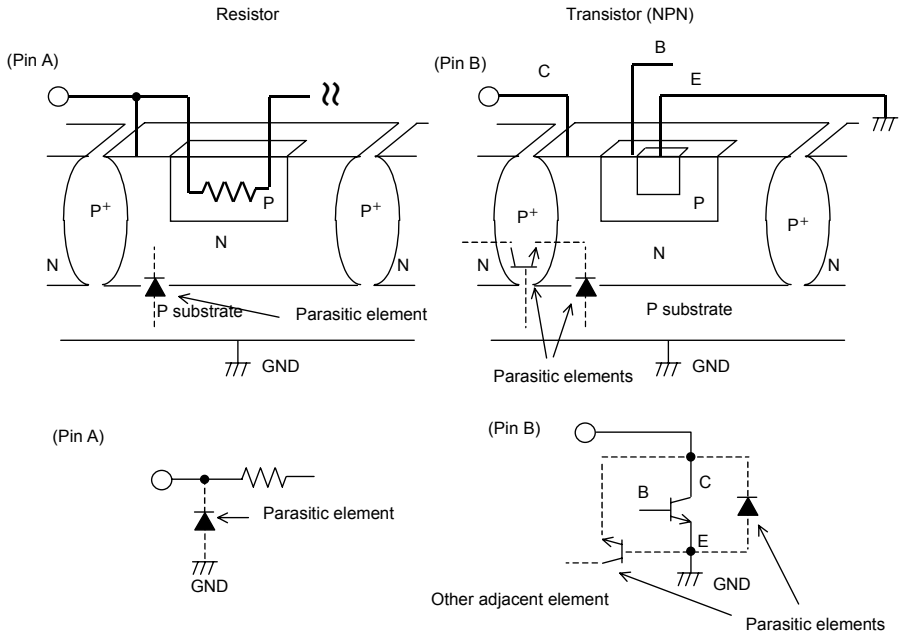


Fig.48 Example of a Simple Monolithic IC Architecture

8. Ground Wiring Pattern
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

9. Recommended operating ranges
The circuit functional operations are guaranteed within the Operating Voltage Range and Operating Temperature Range. Although standard electrical characteristics values are not guaranteed, characteristics values will not vary suddenly within these ranges. However, careful consideration must be taken in designing the circuit.

10. Output capacitors
Capacitors used to eliminate oscillation must be placed between the V_{DD} (pin 9), AUDIO (pin 7), AM (pin 5), ILM (pin 2), P.CON (pin 4), P.ANT (pin 3), and SW5V (pin 8) output pins and the GND pin.
Connect a capacitance of at least 0.1 μF. Ceramic capacitors can be used. Abrupt input voltage and load fluctuations can affect output voltages. Output capacitor capacitance values should be determined after sufficient testing using the actual application.

11. Applications or inspection processes with modes where the potentials of the V_{CC} pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. For example, such damage might occur when V_{CC} is shorted with the GND pin while an external capacitor is charged. Use capacitors that fall within the range listed for each pin in Table 1. It is recommended to insert a diode to prevent back current flow in series with V_{CC}, or bypass diodes between V_{CC} and each pin. If the V_{CC} pin carries a lower voltage than the GND pin, insert a protective diode between the V_{CC} and GND pins.

Output pin	Output capacitor
V_{DD}	0.1 μF to 2200 μF
SW5V	0.1 μF to 2200 μF
AUDIO	0.1 μF to 220 μF
AM	0.1 μF to 2200 μF
P.CON	0.1 μF to 10 μF
P.ANT	0.1 μF to 10 μF
ILM	0.1 μF to 47 μF

Table 1

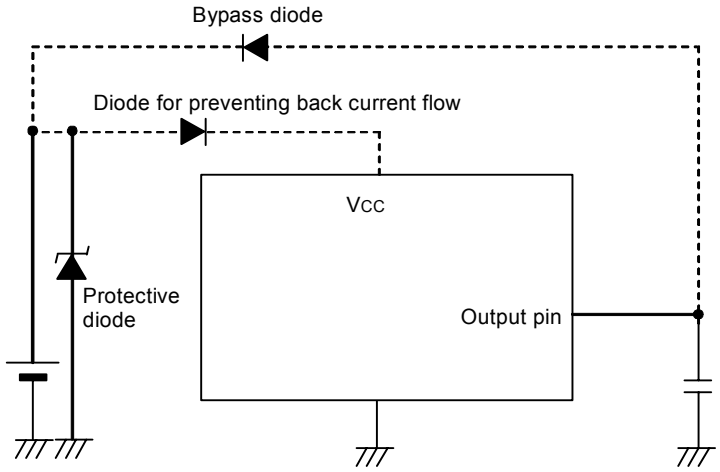


Fig.49 Example of Bypass Diode Insertion to Prevent Back Current Flow

12. Overcurrent protection circuits
The IC incorporates built-in overcurrent protection circuits for the V_{DD} (pin 9), AUDIO (pin 7), AM (pin 5), ILM (pin 2), P.CON (pin 4), P.ANT (pin 3), and SW5V (pin 8) output pins. Each circuit is specifically designed for the current capacity of the corresponding pin and acts to prevent damage to the IC when an overcurrent flows. The protection circuits use dropping fold-back type current limiting and are designed to limit current flow by not latching up in the event of a large and instantaneous current flow, originating from a large capacitor or other component. Their design allows for sufficient safety margins.
These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits (for example, applications where the IC is continuously connected to a load that significantly exceeds the output current capacity). Use caution regarding thermal design, as the output current capacity varies negatively with the temperature characteristics.

13. Overvoltage protection circuit
The overvoltage protection circuit is designed to turn off all output other than V_{DD} and SW5V output when the voltage differential between the $V_{CC}1$ (pin 6) and GND (pin 1) pins exceeds approximately 30 V (at room temperature). V_{DD} and SW5V output are turned off when the voltage differential between the $V_{CC}2$ (pin 10) and GND (pin 1) pins exceeds approximately 30 V (at room temperature).

Use caution when determining the supply voltage range to use.

14. Thermal shutdown circuit (TSD circuit)
    The IC incorporates a built-in thermal shutdown circuit (TSD circuit). However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature Tj will trigger the thermal shutdown circuit to turn off all output power elements. The circuit will automatically reset once the chip's temperature Tj drops. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

15. Ground patterns
    Pattern routes connecting the ground points, indicated in application circuits example, to the GND pin (pin 1) should be sufficiently short and should be positioned to avoid electrical interference.

16. Bypass capacitors between the VCC1/VCC2 and GND pins
    It is recommended to insert a bypass capacitor from 0.47 μF to 10 mF between the VCC1/VCC2 and GND pins, positioning it as close as possible to the pins.

17. Grounding the P.CON and P.ANT pins
    When the IC's GND pin (pin 1) is open and the P.CON (pin 4) and P.ANT (pin 3) pins are connected to a negative battery terminal (are grounded), a parasitic element may occur inside the IC, resulting in damage. To prevent such damage, it is recommended to insert a schottky diode between the P.CON and P.ANT pins and the GND pin. (See Fig. 50.)

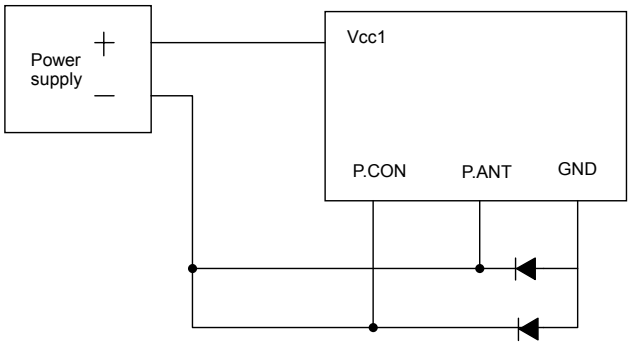


Fig.50 Ground Prevention Circuit Diagram

18. Applications with modes where the potentials of the input (VCC1) and GND pins and other output pins may be reversed from their normal states may cause damage to the IC's internal circuitry. In particular, it is recommended to create a bypass route with diodes or other components when loads including large inductance components are connected as with the P.ANT and P.CON pins in applications, where BEMF may be generated during startup or when output is turned off.

(Example)

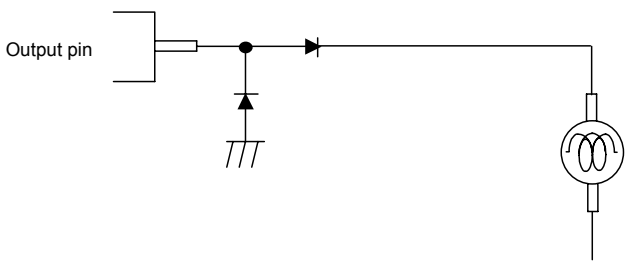


Fig.51 Example of Protective Diode Insertion

19. Always verify the characteristics of example application circuits prior to their use. When changing other external circuit constants, allow for sufficient margins after considering the variability of both the ROHM IC and external components, including both static and transient characteristics.

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Packaging specifications:
Noting: Tube container

SIP-M12

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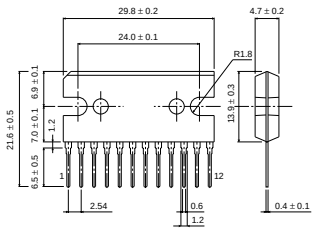

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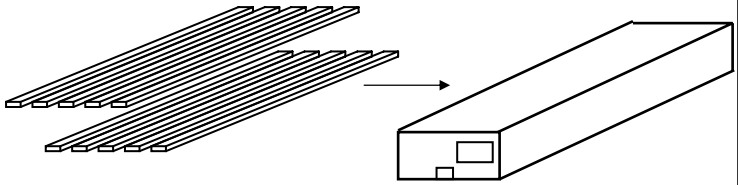

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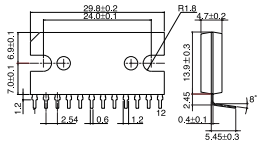

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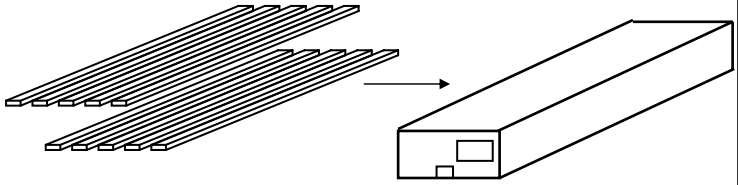

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