

SG6901A

FEATURES OVERVIEW

- Interleaved PFC/PWM switching
- Low start-up and operating current
- Innovative switching charge multiplier-divider
- Multi-vector control for improved PFC output transient response
- Average-current-mode control for PFC
- Programmable two-level PFC output voltage
- PFC over-voltage and under-voltage protections
- PFC and PWM feedback open-loop protection
- Cycle-by-cycle current limiting for PFC/PWM
- Slope compensation for PWM
- Constant power limit for PWM
- Brownout protection
- Over-temperature protection (OTP)

APPLICATIONS

- Switching Power Supplies with Active PFC and Standby Power
- High-Power Adaptors

DESCRIPTION

The highly integrated SG6901A is designed for power supplies with boost PFC and flyback PWM. It requires

very few external components to achieve versatile protections. It is available in a 20-pin SOP package.

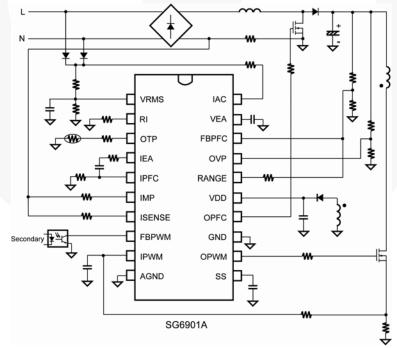
The patented interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6901A shuts off PFC to prevent extra-high voltage on output. Programmable two-level output voltage control reduces the PFC output voltage at low line input to increase the efficiency of the power supply.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6901A provides protection functions, such as brownout and RI pin open/short protection.

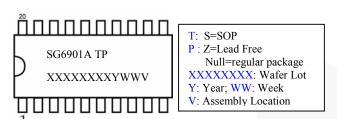
Typical Application



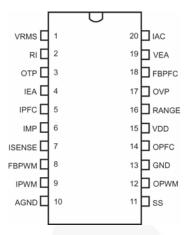


SG6901A

MARKING DIAGRAMS



PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6901ASZ		20-pin SOP

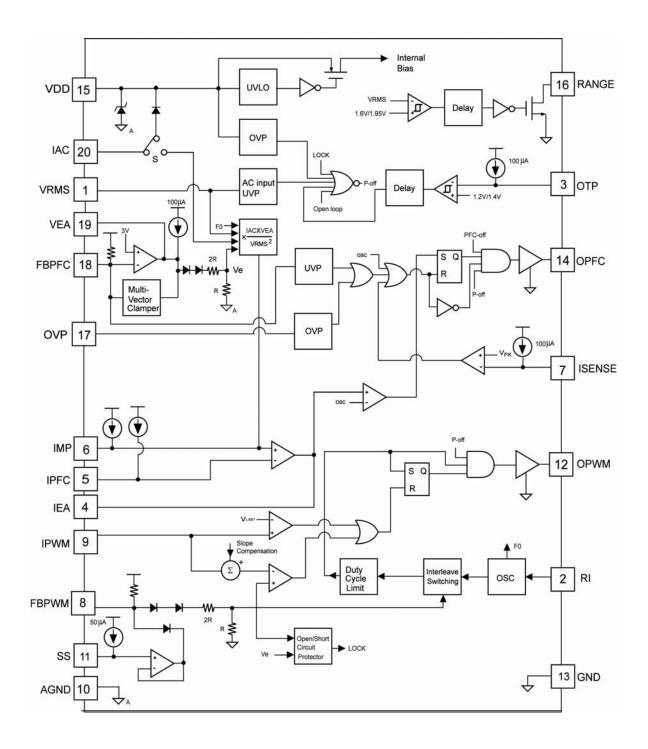


SG6901A

PIN DESCRIPTIONS

Name	Pin No.	Туре	Function
VRMS	1	Line-Voltage Detection	Line voltage detection. The pin is used for PFC multiplier, RANGE control of PFC output voltage, and brownout protection. For brownout protection, the controller is disabled after a delay time when the VRMS voltage drops below a threshold.
RI	2	Oscillator Setting	Reference setting. One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / RI] KHz, where RI is in $K\Omega$. For example, if R_I is equal to $24K\Omega$, the switching frequency is $65KHz$.
ОТР	3	Over Temperature Protection	This pin supplies an over-temperature protection signal. A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6901A is disabled.
IEA	4	Output for PFC Current Amplifier	This is the output of the PFC current amplifier. The signal from this pin is compared with an internal sawtooth and determines the pulse width for PFC gate drive.
IPFC	5	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current amplifier. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
IMP	6	Non-inverting Input for PFC Current Amplifier	The non-inverting input of the PFC current amplifier and the output of multiplier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
ISENS E	7	Peak Current Limit Setting for PFC	The peak-current setting for PFC.
FBPW M	8	PWM Feedback Input	The control input for voltage-loop feedback of PWM stage. It is internally pulled high through a $6.5 \mathrm{k}\Omega$ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
IPWM	9	PWM Current Sense	The current-sense input for the flyback PWM. Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
AGND	10	Ground	Signal ground.
SS	11	PWM Soft-Start	During startup, the SS pin will charge an external capacitor with a $50\mu\text{A}$ (RI= $24K\Omega$) constant current source. The voltage on FBPWM will be clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin will be quickly discharged.
OPWM	12	PWM Gate Drive	The totem-pole output drive for the Flyback PWM MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
GND	13	Ground	Power ground.
OPFC	14	PFC Gate Drive	The totem-pole output drive for the PFC MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
VDD	15	Supply	The power supply pin.
RANGE	16	PFC Output Voltage Control	Two-level output voltage setting for PFC. The PFC output voltage at low line can be reduced to improve efficiency. The RANGE pin has high impedance whenever the V_{RMS} voltage is lower than a threshold.
OVP	17	PFC Over-Voltage Input	The PFC stage over voltage input. The comparator disables the PFC output driver if the voltage at this input exceeds a threshold. This pin can be connected to FBPFC or it can be connected to the PFC boost output through a divider network.
FBPFC	18	Voltage Feedback Input for PFC	The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
VEA	19	Error Amplifier Output for PFC Voltage Feedback Loop	The error amplifier output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
IAC	20	Input AC Current	This input is used to provide current reference for the multiplier.

BLOCK DIAGRAM



SG6901A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{VDD}	DC Supply Voltage*	25	V
I _{AC}	Input AC Current	2	mA
V_{High}	OPWM, OPFC, IAC	-0.3 to +25.0	V
V_{Low}	Others	-0.3 to +7.0	V
P_D	Power Dissipation at T _A < 50°C	1.15	W
$T_{\rm J}$	Operating Junction Temperature	-40 to +125	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C
$R_{\theta JC}$	Thermal Resistance (Junction-to-Case)	23.64	°C/W
T _L	Lead Temperature (Wave Soldering or Infrared, 10 Seconds)	260	°C
$V_{ESD,HBM}$	Electrostatic Discharge Capability, Human Body Model	4.5	KV
V _{ESD,MM}	Electrostatic Discharge Capability, Machine model	250	V

^{*}All voltage values, except differential voltages, are given with respect to GND pin.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
T _A	Operating Ambient Temperature*	-20 to +85	°C

^{*}For proper operation.

ELECTRICAL CHARACTERISTICS

V_{DD}=15V, T_A=25°C unless otherwise noted.

V_{DD} Section

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{DD-OP}	Continuously Operating Voltage				20	V
I _{DD-ST}	Start-up Current	$0V < V_{DD} < V_{DD-ON}$		10	25	μΑ
I _{DD-OP}	Operating Current	V_{DD} =15V; OPFC, OPWM open; R_i =24K Ω		6	10	mA
V_{DD-ON}	Start Threshold Voltage		11	12	13	V
$V_{DD\text{-}OFF}$	Minimum Operating Voltage		9	10	11	V
$V_{\text{DD-OVP}}$	V _{DD} OVP Threshold		23.5	24.5	25.5	V
t _{D-VDDOVP}	Debounce Time of V _{DD} OVP		8		25	μs

Oscillator Section

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Fosc	PWM Frequency	R _i =24KΩ	62	65	68	KHz
Rı	RI Pin Resistance Range		15.6		47.0	ΚΩ
RI _{OPEN}	RI Pin Open Protection If R _I > RI _{open} , SG6901A Turns Off			200		ΚΩ
RI _{SHORT}	RI Pin Short Protection If R _I < RI _{short} , SG6901A Turns Off			2		ΚΩ

^{*}Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

SG6901A

VRMS for UVP and RANGE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{RMS-UVP-1}	RMS AC Voltage Under-Voltage Protection Threshold (with t _{UVP} delay)		0.75	0.8	0.85	V
V _{RMS-UVP-2}	Recovery Level on V _{RMS}		V _{RMS-UVP-1} + 0.16V	V _{RMS-UVP-1} + 0.18V	V _{RMS-UVP-1} + 0.2V	V
t _{D-PWM}	When UVP Occurs, Interval from PFC Off to PWM Off		t _{UVP-Min} +9		t _{UVP-Min} +1	ms
t _{UVP}	Under-Voltage Protection Delay Time*		150	195	240	ms
V _{RMS-H}	High V _{RMS} Threshold for RANGE Comparator		1.90	1.95	2.00	V
V _{RMS-L}	Low V _{RMS} Threshold for RANGE Comparator		1.55	1.60	1.65	V
t _{RANGE}	Range-Enable Delay Time		140	170	200	ms
V _{OL}	Output Low Voltage of RANGE Pin	I₀=1mA		4	0.5	V
I _{он}	Output High Leakage Current of RANGE Pin	RANGE=5V			50	nA

^{*} No delay for start-up.

PFC Stage

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
Av	Open-Loop Gain			60		dB
Z _o	Output Impedance			110		ΚΩ
OVP_{PFC}	PFC Over-Voltage Protection (OVP Pin)		3.20	3.25	3.30	V
\triangle OVP _{PFC}	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
t _{OVP-PFC}	Debounce Time of PFC OVP		40	70	120	μs
V _{FBPFC-H}	Clamp-High Feedback Voltage		3.10	3.15	3.20	V
G _{FBPFC-H}	Clamp-High Gain			0.5		μA/mV
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.90	V
G _{FBPFC-L}	Clamp-Low Gain			6.5		mA/mV
I _{FBPFC-L}	Maximum Source Current		1.5	2.0		mA
I _{FBPFC-H}	Maximum Sink Current		70	110		μΑ
UVP _{FBPFC}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
t _{UVP-FBPFC}	Debounce Time of PFC UVP		40	70	120	μs

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
Aı	Open-Loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common Mode Rejection Ratio	V _{CM} =0 to +1.5V		70		dB
V _{OUT-HIGH}	Output High Voltage		3.2			V
V _{OUT-LOW}	Output Low Voltage				0.2	V
I _{MR1} , I _{MR2}	Reference Current Source	R _i =24KΩ (I _{MR} =20+I _{Ri} •0.8)	50		70	μA
I L	Maximum Source Current		3			mA
I _H	Maximum Sink Current			0.25		mA

SG6901A

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _P	Constant Current Output	R _I =24KΩ	90	100	110	μΑ
V_{PK}	Peak Current Limit Threshold Voltage	V _{RMS} =1.05V	0.15	0.20	0.25	>
VPK	Cycle-by-Cycle Limit (V _{SENSE} < V _{PK})	V _{RMS} =3V	0.35	0.40	0.45	V
t _{PD-PFC}	Propagation Delay				200	ns
t _{LEB-PFC}	Leading-Edge Blanking Time		270	350	450	ns

Multiplier

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{AC}	Input AC Current	Multiplier Linear Range	0		360	μΑ
I _{MO-max}	Maximum Multiplier Current Output	R _i =24KΩ		250		μΑ
I _{MO-1}	Multiplier Current Output (Low-line, High-power)	V_{RMS} =1.05V; I_{AC} =90 μ A; V_{EA} =7.5V; R_{I} =24K Ω	200	250	280	μΑ
I _{MO-2}	Multiplier Current Output (High-line, High-power)	V_{RMS} =3V; I_{AC} =264 μ A; V_{EA} =7.5V; R_{I} =24K Ω	65	85		μΑ
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Vz	Output Voltage Maximum (Clamp)	V _{DD} =20V		16	18	V
$V_{OL\text{-PFC}}$	Output Voltage Low	V _{DD} =15V; I _O =100mA			1.5	V
t _{PFC}	Interval OPFC Lags Behind OPWM at Start-up		9.0	11.5	14.0	ms
V _{OH-PFC}	Output Voltage High	V _{DD} =13V; I _O =100mA	8			V
t _{R-PFC}	Rising Time	V_{DD} =15V; C_L =5nF; O/P =2V to 9V	40	70	120	ns
t _{F-PFC}	Falling Time	V_{DD} =15V; C_L =5nF; O/P =9V to 2V	40	60	110	ns
DCY _{MAX}	Maximum Duty Cycle		93		98	%

PWM Stage

FBPWM

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
A _{v-PWM}	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance		4	5	7	ΚΩ
I _{FB}	Maximum Source Current		0.8	1.2	1.5	mA
FB _{OPEN-LOOP}	PWM Open-Loop Protection voltage		4.2	4.5	4.8	V
t _{OPEN-PWM}	PWM Open-Loop Protection Delay Time		45	56	70	ms
	Interval of PWM Open-Loop Protection		450	600	750	Ī
TOPEN-PWM-Hiccup	Reset		450		750	ms

SG6901A

PWM-Current Sense

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{PD-PWM}	Propagation Delay to Output	VDD=15V,OPWM<=9V	60		120	ns
V _{LIMIT-1}	Peak Current Limit Threshold Voltage1	RANGE=Open	0.65	0.70	0.75	V
V _{LIMIT-2}	Peak Current Limit Threshold Voltage2	RANGE=Ground	0.60	0.65	0.70	V
t _{LEB-PWM}	Leading-Edge Blanking Time		270	350	450	ns
$\triangle V_{ ext{SLOPE}}$	Slope Compensation	$\triangle V_S = \triangle V_{SLOPE} \times (T_{on}/T)$ $\triangle V_S$: Compensation Voltage Added to Current Sense	0.45	0.50	0.55	V

PWM Output Driver

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{Z-PWM}	Output Voltage Maximum (Clamp)	V _{DD} =20V		16	18	V
V_{OL-PWM}	Output Voltage Low	V _{DD} =15V; I _O =100mA			1.5	V
V _{OH-PWM}	Output Voltage High	V _{DD} =13V; I _O =100mA	8			V
t _{R-PWM}	Rising Time	V_{DD} =15V; C_L =5nF; O/P=2V to 9V	30	60	120	ns
t _{F-PWM}	Falling Time	V_{DD} =15V; C_L =5nF; O/P=9V to 2V	30	50	110	ns
DCY _{MAXPWM}	Maximum Duty Cycle		73	78	83	%

OTP Section

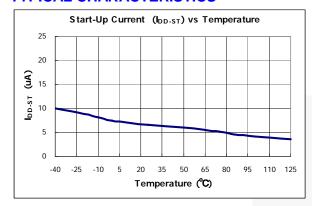
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{OTP}	OTP Pin Output Current	$R_i=24K\Omega$	90	100	110	μΑ
V _{OTP-ON}	Recovery Level on OTP		1.35	1.40	1.45	V
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
t _{OTP}	OTP Debounce Time		8		25	μs

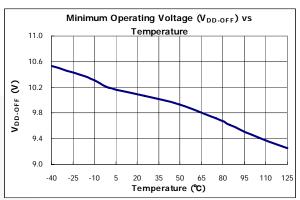
Soft-Start Section

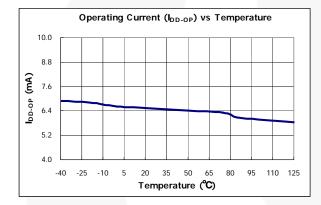
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I _{SS}	Constant Current Output for Soft-Start	R _T =24KΩ	44	50	56	μΑ
R_D	Discharge R _{DSON}			470		Ω

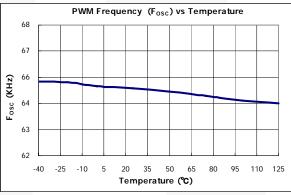


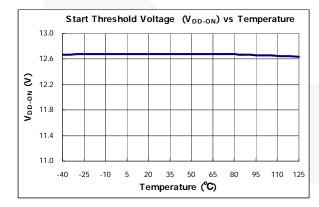
TYPICAL CHARACTERISTICS

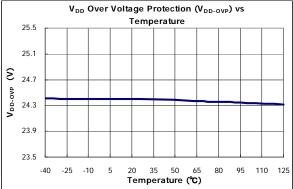




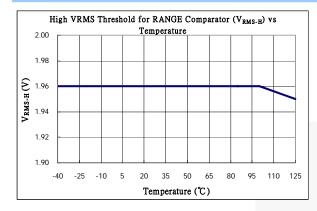


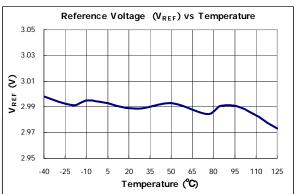


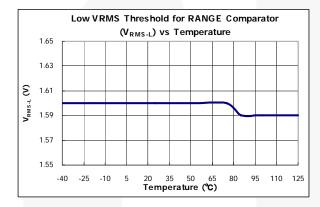


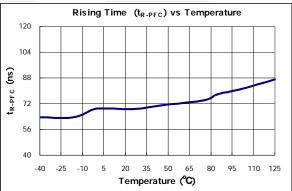


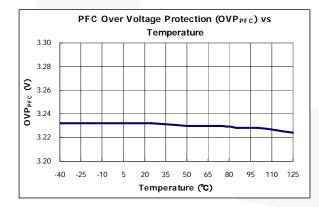
SG6901A

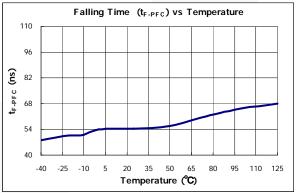




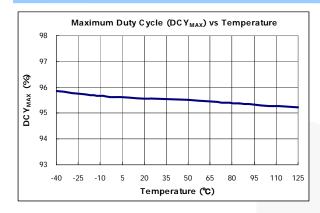


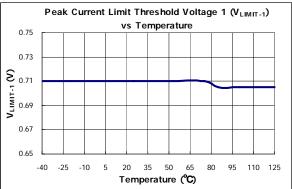


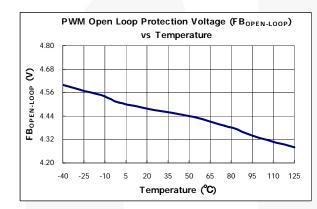


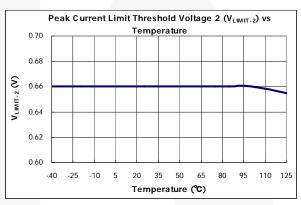


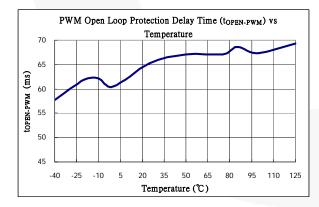
SG6901A

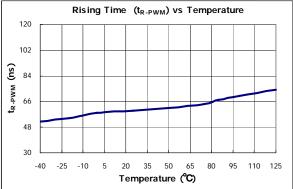




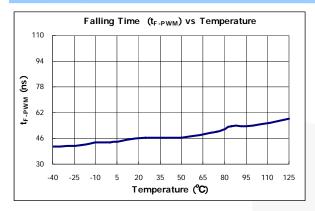


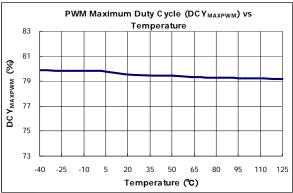


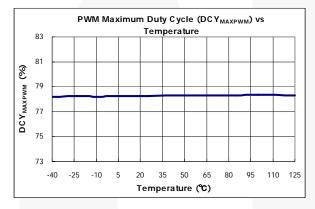


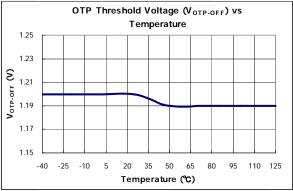


SG6901A









OPERATION DESCRIPTION

SG6901A is a highly integrated PFC/PWM combination controller. Many functions and protections are built in to provide a compact design. The following sections describe the operation and function.

Switching Frequency and Current Sources

The switching frequency of SG6901A can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$F_{OSC} = \frac{1560}{R_1 (k\Omega)} (kHz) \dots (1)$$

For example, a $24K\Omega$ resistor R_I results in a 65KHz switching frequency. Accordingly, a constant current, I_T , flows through R_I :

$$I_T = \frac{1.2V}{R_1 (k\Omega)} (mA)$$
(2)

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 1 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, and range control.

For brownout protection, the SG6901A is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and range control, refer to section below for more details.

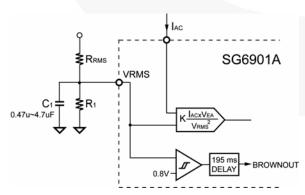


FIG.1 Line Voltage Detection Circuit

PFC Output Voltage Control (RANGE)

For an universal input (90 $\sim 264V_{AC}$) power supply applying active boost PFC and flyback as a second stage, the output voltage of PFC is usually designed around 250V at low line and 390V at high line. This can improve the efficiency at low-line input. The RANGE pin (open-drain structure) is used for the two-level output voltage setting.

Figure 2 shows the RANGE output that programs the PFC output voltage. The RANGE output is shorted to ground when the V_{RMS} voltage exceeds V_{RMS-H} (1.95V) while it is of high impedance (open) whenever the V_{RMS} voltage drops below V_{RMS-L} (1.6V). The output voltages can be designed using equations:

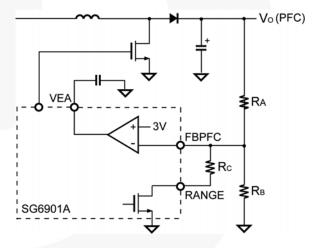


FIG.2 Range Control Two-Level Output Voltage

Interleave Switching

The SG6901A uses interleaved switching to synchronize the PFC and flyback stages, which reduces switching noise and spreads the EMI emissions. Figure 3 shows off-time, T_{OFF}, inserted between the turn-off of the PFC gate drive and the turn-on of the PWM.

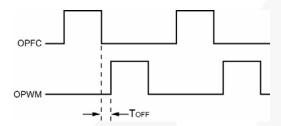


FIG.3 Interleaved Switching Pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 4 shows the total control loop for the average-current-mode control circuit of SG6901A.

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \qquad (4)$$

As shown in Figure 4, the current output from IMP pin, I_{MP} , is the summation of I_{MO} and I_{MR1} . I_{MR1} and I_{MR2} are identical fixed-current sources used to pull high the operating point of the IMP and IPFC pins since the voltage across R_S goes negative with respect to ground. Constant current sources I_{MR1} and I_{MR2} are typically $60\mu A$.

Through the differential amplification of the signal across R_S , better noise immunity is achieved. The output of $I_{\rm IEA}$ is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current I_S is proportional to $I_{\rm MO}$:

$$I_{MO} \times R_2 = I_S \times R_S - \dots$$
 (5)

According to Equation 5, the minimum value of R_2 and maximum of R_S can be determined since I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor R_S . The value of R_S should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) may be used to improve efficiency of high-power converters.

To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as constant as possible, according to Equation 4. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance Z_O and a capacitor C_{EA} ($1\mu F \sim 10\mu F$) should be connected to ground. This establishes a dominant pole f1 for the voltage loop:

$$f_1 = \frac{1}{2\pi \times Z_{O} \times C_{EA}} \qquad ----- \qquad (6)$$

The average total input power can be expressed as:

From Equation 7, V_{EA} , the output of the voltage error amplifier, controls the total input power and the power delivered to the load.

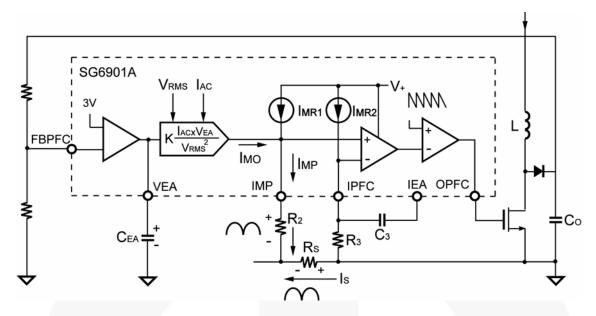


FIG.4 Average-Current-Mode Control Loop

Multi-Vector Error Amplifier

Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

Figure 5 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ±5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response.

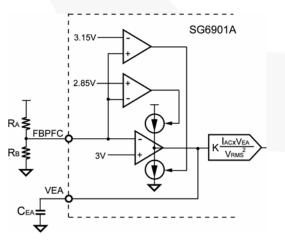


FIG. 5 Multi-Vector Error Amplifier

PFC Over-Voltage Protection

Using a voltage divider from the output of PFC to the OVP pin, the PFC output voltage can be safely protected.

Once the voltage on the OVP pin is over OVP_{PFC}, the OPFC is disabled. THE OPFC is not enabled again until the OVP voltage falls below OVP_{PFC}.

Cycle-by-Cycle Current Limiting

SG6901A provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 6 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below V_{PK} .

The voltage of V_{RMS} determines the voltage of V_{PK} . The relationship between V_{PK} and V_{RMS} is shown in Figure 6.

The amplitude of the constant current, I_P , is determined by the internal current reference according to the equation:

$$I_P = 2 \times \frac{1.2V}{R_I}$$
 -----(8)

SG6901A

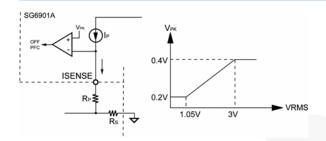


FIG. 6 V_{RMS} Controlled Current Limiting

The peak current of the I_{SENSE} is given by $(V_{RMS} < 1.05V)$:

$$I_{SENSE_peak} = \frac{(I_p \times R_p) - 0.2V}{R_s} \qquad (9)$$

Flyback PWM and Slope Compensation

As shown in Figure 7, peak-current-mode control is utilized for flyback PWM. The SG6901A inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous current-mode operation.

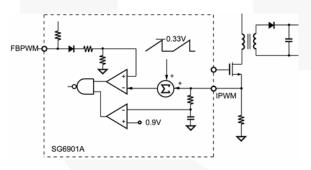


FIG. 7 Peak Current Control Loop

When the IPWM voltage, across the sense resistor, reaches the threshold voltage (0.9V), the OPWM is turned off after a small propagation delay t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp is inserted at every switching cycle.

Limited Power Control

Every time the output of power supply is shorted or overloaded, the FBPWM voltage increases. If the FBPWM voltage is higher than a designed threshold, FB_{OPEN-LOOP} (4.5V) for longer than t_{OPEN-PWM} (56ms), the OPWM is turned off.

As long as the voltage on the VDD pin is larger than $V_{\text{DD-OFF}}$ (minimum operating voltage), the OPWM is not enabled. This protection is reset every $t_{\text{OPEN-PWM-Hiccup}}$ interval. A low-frequency hiccup mode protection prevents the power supply from being overheated under overloading conditions.

Over-Temperature Protection

SG6901A provides an OTP pin for over-temperature protection. A constant current is output from this pin. If $R_{\rm I}$ is equal to $24 {\rm K}\Omega,$ the magnitude of the constant current is $100 \mu A.$ An external NTC thermistor must be connected from this pin to ground, as shown as Figure 8. When the OTP voltage drops below $V_{\rm OTP-OFF}$ (1.2V), SG6901A is disabled and does not recover until OTP voltage exceeds $V_{\rm OTP-ON}$ (1.4V).

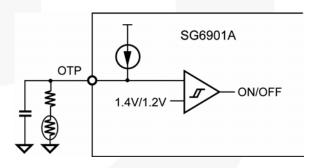


FIG. 8 OTP Function

Soft-Start

During start-up of PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by the SS voltage during start-up. In the event of a protected condition and/or PWM disabled, the SS pin quickly discharges.

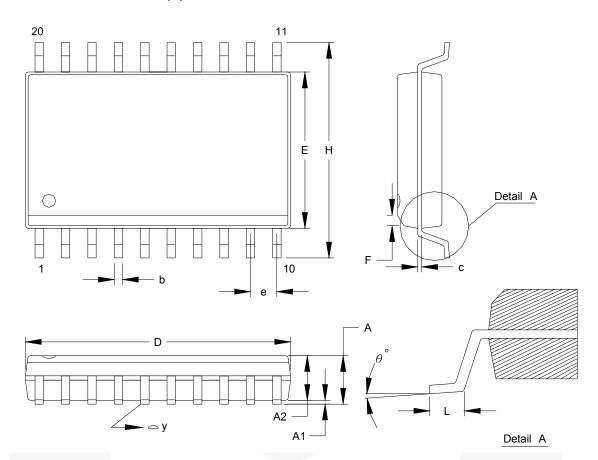
Gate Drivers

SG6901A output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode to protect the external power MOSFET.



SG6901A

PACKAGE INFORMATION 20 PINS – PLASTIC SOP (S)



Dimensions:

Cumabal	Millimeter			Inch		
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.
Α	2.362		2.642	0.093		0.104
A1	0.101		0.305	0.004		0.012
A2	2.260		2.337	0.089		0.092
b		0.406			0.016	
С		0.203			0.008	
D	12.598		12.903	0.496		0.508
E	7.391		7.595	0.291		0.299
е		1.270			0.050	
Н	10.007		10.643	0.394		0.419
L	0.406		1.270	0.016		0.050
F		0.508X45°			0.020X45°	
у			0.101			0.004
θ ullet	0°		8°	0°		8°







TRADEMARKS

The following are registered and unregistered trademarks and service marks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx[®]
Build it Now™
CorePLUS™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
Fairchild®

Ecospark®

Fairchild®

Fairchild Semiconductor®

FACT Quiet Series™

FACT®

FAST®

FastvCore™

FPS™

FRFET®

Global Power Resource®

Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MilerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®

PDP-SPM™
Power220®

Green FPS™

Power247[®] POWEREDGE[®] Power-SPM[™] PowerTrench[®]

Programmable Active Droop™ QFET[®] QS™ QT Optoelectronics™ Quiet Series™

RapidConfigureTM
SMART STARTTM
SPM[®]
STEALTHTM
SuperFETTM
SuperSOTTM-3
SuperSOTTM-6

SuperSOT™-8 SvncFET™

The Power Franchise®

TinyBoost™
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyPWM™
TinyPWT®
UHC®
UniFET™

VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I31