



General Description

The MAX17119 includes a 10-channel, high-voltage, level-shifting scan driver with a gate-pulse modulation (GPM) feature to shape the corner of the scan-driver output to reduce flicker. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The high-voltage level-shifting scan driver is designed to drive the TFT panel gate logic. Its 10 outputs swing from +38V (maximum) to -12V (minimum) and can swiftly drive capacitive loads. There are two positive supply inputs that provide flexibility for system design.

The GPM feature is employed to shape the corner of the falling edge of the clock channels. This reduces flicker, and therefore improves the display quality.

The MAX17119 also features a dedicated discharge channel and an integrated voltage detector. When the system shuts down, the voltage detector commands the discharge channel to swing its output to positive supply voltage so as to remove any residual image on the display quickly.

The MAX17119 is available in a 28-pin, 5mm x 5mm, thin QFN package with a maximum thickness of 0.8mm for thin LCD panels.

Applications

LCD Monitors I CD TVs

Features

- ♦ High-Voltage Level-Shifting Scan Drivers **Logic-Level Inputs** +38V to -12V Outputs **GPM Feature Discharge Channel**
- **♦ Thermal-Overload Protection**
- ♦ 28-Pin. 5mm x 5mm Thin QFN Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17119ETI+	-40°C to +85°C	28 TQFN

+Denotes lead(Pb)-free/RoHS-compliant package.

ABSOLUTE MAXIMUM RATINGS

A1-A9, VSENSE, FLK1, FLK2,	FLK3 to GND0.3V to +6V
GON1, GON2 to GND	0.3V to +40V
GOFF to GND	14V to +0.3V
Y1-Y7, YDCHG to GND(V_{GOFF} - 0.3V) to $(V_{GON1} + 0.3V)$
Y8, Y9 to GND(V_{GOFF} - 0.3V) to $(V_{GON2} + 0.3V)$
RE to GND	0.3V to (VGON1 + 0.3V)
Y1-Y6 to RE(V_{GOFF} - 0.3V) to $(V_{GON1} + 0.3V)$
Y1-Y6, YDCHG Load RMS Cu	rrent350mA
GON1 RMS Current	600mA

GON2 RMS Current	380mA
GOFF RMS Current	600mA
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
28-Pin, 5mm x 5mm TQFN	
(derate 34.5mW/°C above +70°C)	2758.6mW
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{GON} = 30V, V_{GOFF} = -6.2V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE DRIVER BLOCK	K				
GON_ Input-Voltage Range		12		38	V
GOFF Input-Voltage Range		-12		-2	V
GOFF Supply Current	A1-A9 = 3.3V, VSENSE = GND, no load		100	200	μΑ
GON_ Total Supply Current	A1-A9 = 3.3V, VSENSE = GND, no load		450	750	μΑ
Output Voltage Low (Y1-Y9, YDCHG)	IOUT = 10mA		GOFF + 0.08	GOFF + 0.16	V
Output Voltage High (Y1-Y7, YDCHG)	IOUT = 10mA	GON1 - 0.16	GON1 - 0.08		V
Output Voltage High (Y8, Y9)	I _{OUT} = 10mA	GON2 - 0.16	GON2 - 0.08		V
Rise Time (Y1-Y7, YDCHG)	$T_A = +25^{\circ}C$, $V_{GON1} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)		50	200	ns
Fall Time (Y1-Y7, YDCHG)	$T_A = +25^{\circ}C$, $V_{GON1} = 30$ V and $V_{GOFF} = -6.2$ V (Note 1)		40	120	ns
Rise Time (Y8, Y9)	$T_A = +25^{\circ}C$, $V_{GON2} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)		50	200	ns
Fall Time (Y8, Y9)	$T_A = +25^{\circ}C$, $V_{GON2} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)		40	120	ns
Propagation Delay A_ Rising to Y_ Rising, VSENSE Falling to YDCHG Rising	With V _{GON} __ = 30V and V _{GOFF} = -6.2V (Note 1)		50		ns
Propagation Delay A_ Falling to Y_ Falling, VSENSE Rising to YDCHG Falling	With VGON_= 30V and VGOFF = -6.2V (Note 1)		50		ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{GON} = 30V, V_{GOFF} = -6.2V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay FLK_ Falling			50		200
to Y_ Discharge			50		ns
Y_ to RE Switch On-Resistance			50	100	Ω
CONTROL INPUTS					
Logic Input-Voltage Range (A1–A9)				5.5	V
Logic Input Voltage Low (A1–A9)				0.8	V
Logic Input Voltage High (A1–A9, VSENSE)		2			V
Logic Input-Leakage Current (A1-A9)	0V < A_, VSENSE < 5.5V, T _A = +25°C	-1		+1	μΑ
VOLTAGE DETECTOR					
VSENSE Voltage Range				5.5	V
VSENSE Bias Current	VSENSE = 1.5V	2.3	4.6	8	μΑ
VSENSE Threshold Voltage	Falling edge	1.158	1.218	1.278	V
THERMAL PROTECTION					
Thermal Shutdown	Rising edge, hysteresis = 15°C		+160		°C

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{GON} = 30V, V_{GOFF} = -6.2V, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-VOLTAGE DRIVER BLOCK					
GON_ Input-Voltage Range		12		38	V
GOFF Input-Voltage Range		-12		-2	V
GOFF Supply Current	A1-A9 = 3.3V, VSENSE = GND, no load			200	μΑ
GON_ Total Supply Current	A1-A9 = 3.3V, VSENSE = GND, no load			750	μΑ
Output Voltage Low (Y1-Y9, YDCHG)	IOUT = 10mA			GOFF + 0.16	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{GON} = 30V, V_{GOFF} = -6.2V, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage High (Y1–Y7, YDCHG)	I _{OUT} = 10mA	GON1 - 0.16			V
Output Voltage High (Y8, Y9)	I _{OUT} = 10mA	GON2 - 0.16			V
Rise Time (Y1-Y7, YDCHG)	T _A = +25°C, V _{GON1} = 30V and V _{GOFF} = -6.2V (Note 1)			200	ns
Fall Time (Y1-Y7, YDCHG)	T _A = +25°C, V _{GON1} = 30V and V _{GOFF} = -6.2V (Note 1)			120	ns
Rise Time (Y8, Y9)	T _A = +25°C, V _{GON2} = 30V and V _{GOFF} = -6.2V (Note 1)			200	ns
Fall Time (Y8, Y9)	$T_A = +25^{\circ}C$, $V_{GON2} = 30V$ and $V_{GOFF} = -6.2V$ (Note 1)			120	ns
Y_ to RE Switch On-Resistance				100	Ω
CONTROL INPUTS					
Logic Input-Voltage Range (A1-A9)				5.5	V
Logic Input Voltage Low (A1-A9)				0.8	V
Logic Input Voltage High (A1-A9)		2			V
VOLTAGE DETECTOR					
VSENSE Voltage Range				5.5	V
VSENSE Threshold Voltage	Falling edge	1.158		1.278	V
VSENSE Pullup Current	VSENSE = 1.5V	2.3		8	μΑ

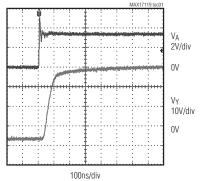
Note 1: The panel models for different channels are illustrated in Figure 4.

Note 2: -40°C specs are guaranteed by design, not production tested.

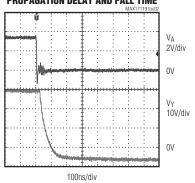
Typical Operating Characteristics

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$

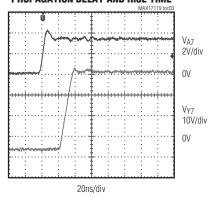
SCAN-DRIVER OUTPUT RISING EDGE (Y1-Y6) PROPAGATION DELAY AND RISE TIME



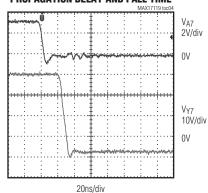
SCAN-DRIVER OUTPUT FALLING EDGE (Y1-Y6) PROPAGATION DELAY AND FALL TIME



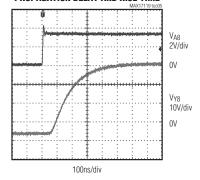
SCAN-DRIVER OUTPUT RISING EDGE (Y7) PROPAGATION DELAY AND RISE TIME



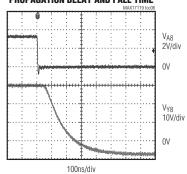
SCAN-DRIVER OUTPUT FALLING EDGE (Y7) PROPAGATION DELAY AND FALL TIME



SCAN-DRIVER OUTPUT RISING EDGE (Y8 AND Y9) PROPAGATION DELAY AND RISE TIME



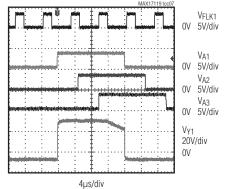
SCAN-DRIVER OUTPUT FALLING EDGE (Y8 AND Y9) PROPAGATION DELAY AND FALL TIME



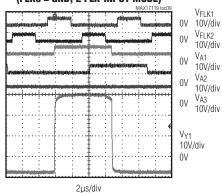
Typical Operating Characteristics (continued)

 $(T_A = +25^{\circ}C, \text{ unless otherwise noted.})$

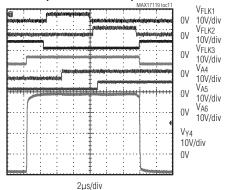




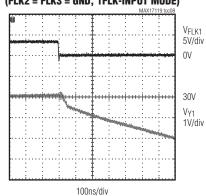
SCAN-DRIVER OUTPUT WITH GPM (FLK3 = GND, 2 FLK-INPUT MODE)



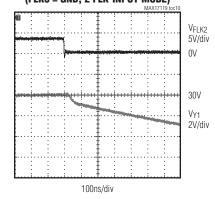
SCAN-DRIVER OUTPUT WITH GPM (3 FLK-INPUT MODE)



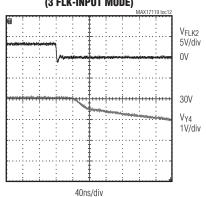
GPM PROPAGATION DELAY-FLK_ FALLING TO Y_ FALLING (FLK2 = FLK3 = GND, 1FLK-INPUT MODE)



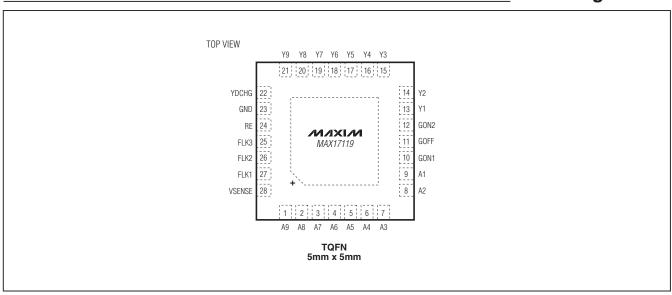
GPM PROPAGATION DELAY-FLK_ FALLING TO Y_ FALLING (FLK3 = GND, 2 FLK-INPUT MODE)



GPM PROPAGATION DELAY-FLK_ Falling to Y_ Falling (3 Flk-input mode)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1–9	A9-A1	Level-Shifter Logic-Level Input
10	GON1	Gate-On Supply Input 1. GON1 is the positive supply for the Y1–Y7 and YDCHG level shifters. Bypass GON1 to ground with a minimum of 1µF ceramic capacitor.
11	GOFF	Gate-Off Supply Input. GOFF is the negative supply for the Y1–Y9 and YDCHG. Bypass GOFF to ground with a minimum of 1µF ceramic capacitor.
12	GON2	Gate-On Supply Input 2. GON2 is the positive supply for the Y8 and Y9 level shifters. Bypass GON2 to ground with a minimum of 1µF ceramic capacitor.
13–21	Y1-Y9	Level-Shifter Outputs
22	YDCHG	Level-Shifter Output for Discharge Function
23	GND	Ground
24	RE	Resistor Connection Input for GPM Function
25	FLK3	GPM Control Input for Level-Shifter Outputs Y3 and Y6
26	FLK2	GPM Control Input for Level-Shifter Outputs Y2 and Y5
27	FLK1	GPM Control Input for Level-Shifter Outputs Y1 and Y4
28	VSENSE	Input Voltage Sense for Voltage Detector. This pin is usually connected to V_{LOGIC} in the system through a resistor-divider (R1 and R2). When V_{VSENSE} is below its threshold, the discharge channel of the level-shifter channel is turned on and YDCHG is connected to GON1 internally. There is a 4.6µA internal pullup current on VSENSE and both R1 and R2 should be less than $50k\Omega$.
_	EP	Exposed Backside Pad. Connect to GOFF . Copper area should be maximized for thermal performance.

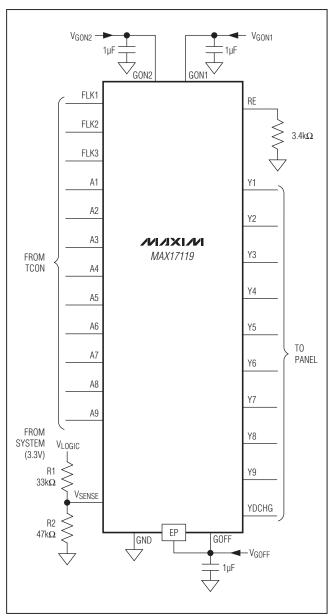


Figure 1. Typical Operating Circuit

Typical Operating Circuit

The MAX17119 typical operating circuit is shown in Figure 1. The positive supply voltage for GON1 and GON2 is 30V (typ) and negative supply voltage for GOFF is -6.2V (typ).

Detailed Description

The MAX17119 includes a 10-channel, high-voltage, level-shifting scan driver with a GPM feature. The device is optimized for TFT-LCD applications. The GPM feature is employed to shape the corner of the falling edge of the clock channels. This reduces flicker, and therefore improves the display quality. There is a dedicated discharge channel. It works with the integrated voltage detector to swing its output to VGON1 when the system shuts down so as to remove any residual image on the display quickly. Figure 2 shows the MAX17119 functional diagram.

High-Voltage Level-Shifting Scan Driver

The MAX17119 includes 10-channel, high-voltage, level-shifting buffers that can buffer logic inputs and shift them to a desired level to drive TFT-LCD row logic. The driver outputs swing between their power-supply rails, according to the input-logic level. The driver output is VGOFF when its respective input is logic-low, and is VGON_ when its respective input is logic-high. These 10 driver channels are grouped for different GON supplies. Y1–Y7 and YDCHG are supplied from GON1; Y8 and Y9 are supplied from GON2. The high-voltage, level-shifting scan drivers can swing from +38V to -12V and can swiftly drive capacitive loads.

GPM Function

The six clock channels of Y1–Y6 support the GPM function, which shaves the corner of the scan-driver outputs' falling edge depends on FLK_. The corner shaving is achieved by turning off the scan-driver switches, and turning on the GPM switches to let the panel load capacitance discharge through the resistor at the RE pin as the functional diagram shows (Figure 2).

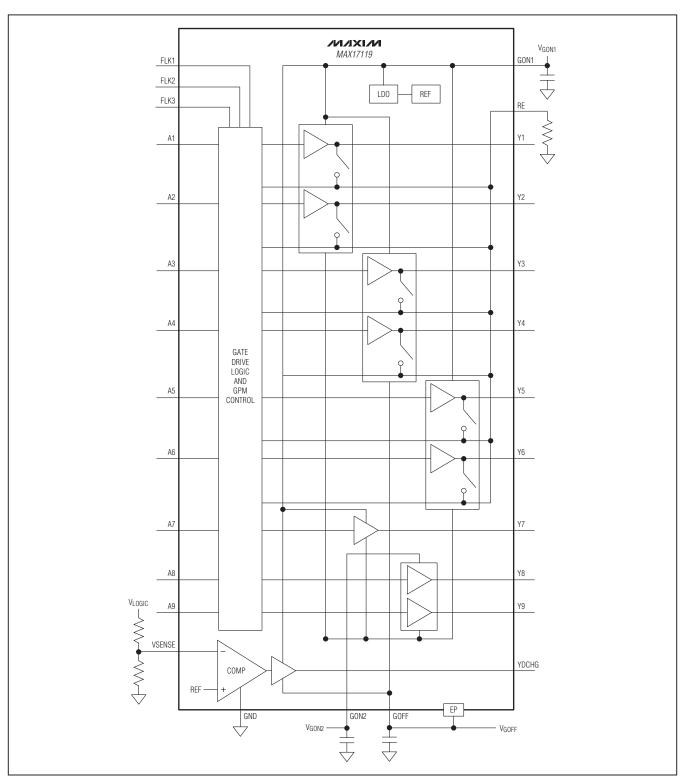


Figure 2. MAX17119 Functional Diagram

A simple timing sequence of GPM is shown in Figure 3. The scan-driver outputs (Y1-Y6) follow their respective inputs (A1-A6). On the falling edge of VFLK_, the corner shaving on VY_ is implemented until VY_ is driven to VGOFF (VA_ goes low).

The GPM function has three operating modes. Table 1 shows the detailed configurations of FLK1, 2, 3 and A1–A9 input signals for these modes.

Discharge Function

One scan-driver output (YDCHG) is a dedicated discharge channel for removing residual image on display during power-down. The integrated voltage detector monitors system supplies, such as 3.3V logic supply. Through a resistor-divider, the MAX17119 commands the discharge channel to swing its output to VGON1 once the input to the voltage detector (VSENSE) is lower than threshold.

Load Models for Different Channels

Figure 4 shows the test load.

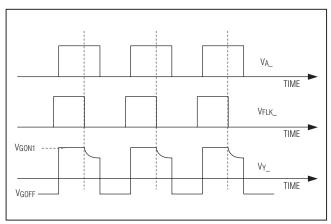


Figure 3. GPM Function Timing Sequence

Power-On and -Off Sequence

Figure 5 shows the power-on and power-off sequence for the application. In general, the supply voltage for the timing controller (VLOGIC) is ready first. The timing controller should send input A_ to the scan drivers after VGON_ and VGOFF_ are ready. Since the MAX17119 uses VGOFF_ as substrate instead of GND, VGOFF should go below -2V at least before VGON_ starts to build up, as in Figure 5.

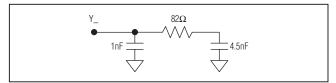


Figure 4. Test Load

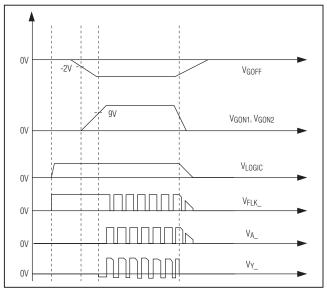


Figure 5. MAX17119 Power-On and -Off Sequence

Table 1. GPM Operating Modes

-	_												
	FLK1	FLK2	FLK3	A1	A2	А3	A 4	A 5	A 6	A 7	A8	A9	Y1-Y9
Typical HDTV application (1-FLK line)	T(*)	L	L	Т	Т	Т	Т	Т	Т	Т	Т	Т	All connected to panel
Typical monitor application (2-FLK lines)	Т	Т	L	Т	Т	Н	Т	Т	Н	Т	Т	Т	Y3 and Y6 high impedance
Typical full HDTV application (3-FLK lines)	Т	Т	Т	Т	Т	Т	Т	Т	Т	Т	Т	Т	All connected to panel

T(*) means from TCON; L: logic-low; H: logic-high

Thermal Protection

The MAX17119 includes a thermal-protection circuit. Thermal-overload protection prevents excessive power dissipation from overheating the MAX17119. When the junction temperature exceeds $T_J = +160^{\circ}C$ (typ), the device shuts down and all the outputs are put into high-impedance mode. The thermal protection is not latched and the device recovers once the temperature drops below the hysteretic threshold (+15°C typ).

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major component of power dissipation is the power dissipated in the high-voltage scan drivers.

When driving a pure capacitive load, the power dissipated by the scan-driver outputs depends on the scan frequency, the capacitive load, and the difference between the GON_ and GOFF supply voltages. Assuming only

A7, A8, and A9 drive a very light load and that the power loss associated is negligible, the power loss is:

PDSCAN = 6 x CPANEL x (VGON1 - VGOFF)² x fSCAN If the six scan drivers (A1–A6) operate at a frequency of 50kHz, the load of the six outputs is 5nF, and the supply voltage difference is 30V, then the power dissipated is 1.35W.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a GOFF plane and connect it to EP.
- Create a ground island (GND) consisting of the supply capacitors' grounds and GND pin.
- Connect all these together with short, wide traces or a small ground plane.
- Place the capacitors as close as possible to the respective supply voltage pins (GON1, GON2, and GOFF).

Refer to the MAX17119 Evaluation Kit for an example of proper board layout.

Chip Information

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TQFN	T2855+6	<u>21-0139</u>

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