LMV112 40 MHz Dual Clock Buffer

Check for Samples: LMV112

FEATURES

- **(Typical Values are: V_{SUPPLY} = 2.7V and C_L = 20 pF, Unless Otherwise Specified.)**
- **Small Signal Bandwidth 40 MHz**
- **Supply Voltage Range 2.4V to 5V**
- **Slew Rate 110 V/µs**
- **Total Supply Current 1.6 mA**
- **Shutdown Current 59 µA**
- **Rail-to-Rail Input and Output**
- **Individual Buffer Enable Pins**
- **Rapid T_{on} Technology**
- **Crosstalk Rejection Circuitry**
- **8-pin WSON, Pin Access Packaging**
- **Temperature Range −40°C to 85°C**

APPLICATIONS

- **3G Mobile Applications**
- **WLAN-WiMAX Modules**
- **TD_SCDMA Multi-Mode MP3 and Camera**
- **GSM Modules**
- **Oscillator Modules**

DESCRIPTION

The LMV112 is a high speed dual clock buffer designed for portable communications and accurate multi-clock systems. The LMV112 integrates two 40 MHz low noise buffers which optimizes application and out performs large discrete solutions. This device enables superb system operation between the base band and the oscillator signal path while eliminating crosstalk.

Texas Instruments' unique technology and design deliver accuracy, capacitance and load resistance while increasing the drive capability of the device. The low power consumption makes the LMV112 perfect for battery applications.

The robust, independent, and flexible buffers are designed to provide the customer with the ability to manage complex clock signals in the latest wireless applications. The buffers deliver 110 V/µs internal slew rate with independent shutdown and duty cycle precision. The patented analog circuit drives capacitive loads beyond 20 pF. Texas Instruments' proven biasing technique has 1V centering, rail-to-rail input/output unity gain, and AC coupled convenient inputs. These integrated cells save space and require no external bias resistors. Texas Instruments' rapid recovery after disable optimizes performance and current consumption. The LMV112 offers individual enable pin controls and since there is no internal ground reference either single or split supply configurations offer additional system flexibility and power choices.

The LMV112 is a proven replacement for any discrete circuitry and simplifies board layout while minimizing related parasitic components.

The LMV112 is produced in the small WSON package which offers high quality while minimizing its use of PCB space. Texas Instruments' advanced packaging offers direct PCB-IC evaluation via pin access.

TYPICAL APPLICATION

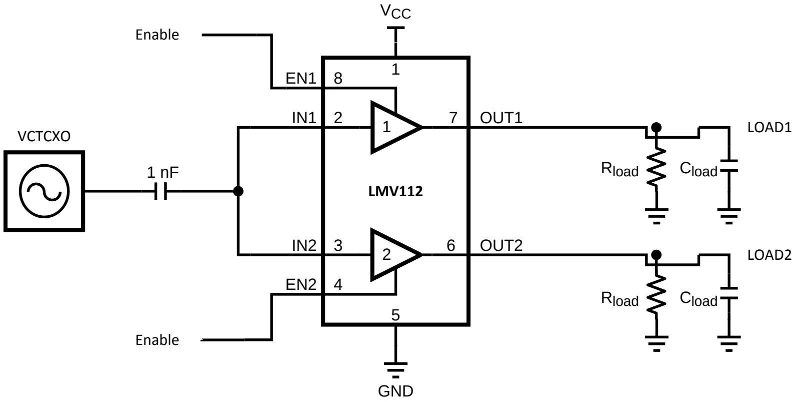

Figure 1.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltages ($V^+ – V^-$)	5.5V
ESD Tolerance (3)	
Human Body	2000V
Machine Model	200V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (4)	+150°C
Soldering Information	
Infrared or Convection (35 sec.)	235°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human Body Model: 1.5 kΩ in series with 100 pF. Machine Model: 0Ω in series with 200 pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

OPERATING RATINGS(1)

Supply Voltage ($V^+ – V^-$)	2.4V to 5.0V
Temperature Range (2) (3)	−40°C to +85°C
Package Thermal Resistance (2) (3)	
WSON-8 (θ_{JA})	217°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} − T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.
(3) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$.

2.7V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (1).

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 0.63 V_{PP}; −3 dB		40		MHz
FPBW	Full Power Bandwidth	V_{IN} = 1.6 V_{PP}; −3 dB		28		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		3.4		MHz
Distortion and Noise Performance						
e_n	Input-Referred Voltage Noise	f = 1 MHz		26		$nV/\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz		91		dB
CT	Crosstalk Rejection	f = 26 MHz, P_{IN} = 0 dBm		54		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%), f = 1 MHz		7		ns
t_f	Fall Time			6		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step, f = 1 MHz		118		ns
OS	Overshoot	0.1 V_{PP} Step, f = 1 MHz		41		%
SR	Slew Rate (4)	V_{IN} = 1.6 V_{PP}, f = 26 MHz		110		V/µs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2}$ = V_{DD} ; No Load		1.6	2.0 **2.1**	mA
		$Enable_{1,2}$ = V_{SS} ; No Load		59	72 **78**	µA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	58 **57**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{OUT} = 0.1 V_{PP}	0.97 **0.95**	1.01	1.05 **1.07**	V/V
V_{OS}	Output Offset Voltage			0.4	16 **17**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (5)			4		µV/°C
R_{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 26 MHz		140		
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		141		kΩ
		Enable = V_{SS}		141		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		2.3		pF
		Enable = V_{SS}		2.3		
Z_{IN}	Input Impedance	f = 26 MHz, Enable = V_{DD}		10.4		kΩ
		f = 26 MHz, Enable = V_{SS}		10.9		
V_O	Output Swing Positive	V_{IN} = V_{DD}	2.65 **2.63**	2.69		V
	Output Swing Negative	V_{IN} = V_{SS}		10	50 **65**	mV

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(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A .
(2) All limits are specified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the average of the positive and negative slew rate.
(5) Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

2.7V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
I_{SC}	Output Short-Circuit Current (6)	Sourcing	−18 **−13**	−27		mA
		Sinking	20 **16**	30		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

(6) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

5V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{DD} = 5V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 0.63 V_{PP}; −3 dB		42		MHz
FPBW	Full Power Bandwidth	V_{IN} = 1.6 V_{PP}; −3 dB		31		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		4.9		MHz
Distortion and Noise Performance						
e_n	Input-Referred Voltage Noise	f = 1 MHz		27		$nV/\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz		90		dB
CT	Crosstalk Rejection	f = 26 MHz, P_{IN} = 0 dBm		61		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%), f = 1 MHz		7		ns
t_f	Fall Time			6		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step, f = 1 MHz		80		ns
OS	Overshoot	0.1V_{PP} Step, f = 1 MHz		20		%
SR	Slew Rate (4)	V_{IN} = 1.6 V_{PP}, f = 26 MHz		120		V/µs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2}$ = V_{DD} ; No Load		2.5	3.5 **3.8**	mA
		$Enable_{1,2}$ = V_{SS} ; No Load		62	80 **89**	µA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	58 **57**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{OUT} = 0.1 V_{PP}	0.99 **0.97**	1.00	1.01 **1.03**	V/V
V_{OS}	Output Offset Voltage			1.3	16 **17**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (5)			3		µV/°C
R_{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 26 MHz		118		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$.
(2) All limits are specified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the average of the positive and negative slew rate.
(5) Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

5V ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits are specified for T_J = 25°C, V_{DD} = 5V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ, $C_{COUPLING}$ = 1 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		134		kΩ
		Enable = V_{SS}		134		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		2.0		pF
		Enable = V_{SS}		2.0		
Z_{IN}	Input Impedance	f = 26 MHz, Enable = V_{DD}		7.2		kΩ
		f = 26 MHz, Enable = V_{SS}		8.0		
V_O	Output Swing Positive	V_{IN} = V_{DD}	4.96 **4.94**	4.99		V
	Output Swing Negative	V_{IN} = V_{SS}		10	40 **55**	mV
I_{SC}	Output Short-Circuit Current (6)	Sourcing	-40 **-28**	-68		mA
		Sinking	70 **50**	98		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

(6) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

BLOCK DIAGRAM

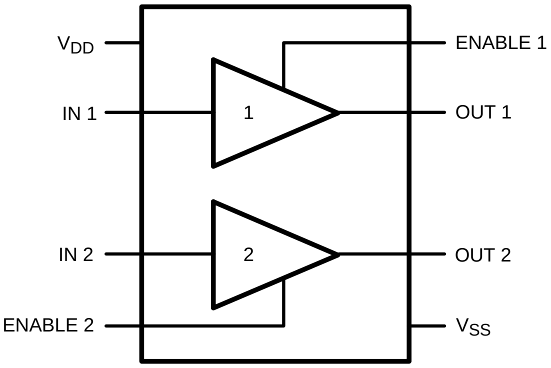

Figure 2.

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	V_{DD}	Voltage supply connection
2	IN 1	Input 1
3	IN 2	Input 2
4	ENABLE 2	Enable buffer 2
5	V_{SS}	Ground connection
6	OUT 2	Output 2
7	OUT 1	Output 1
8	ENABLE 1	Enable buffer 1

CONNECTION DIAGRAM

Top View

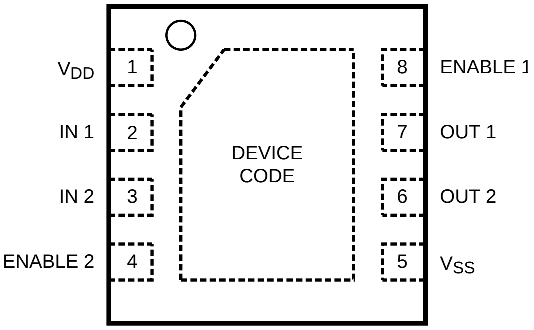

Figure 3. 8-Pin WSON (NGQ Package)

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

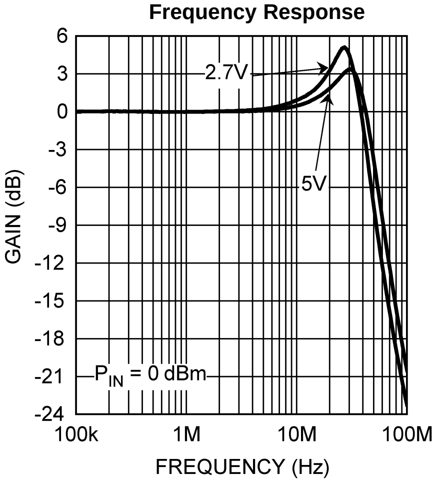

Figure 4.

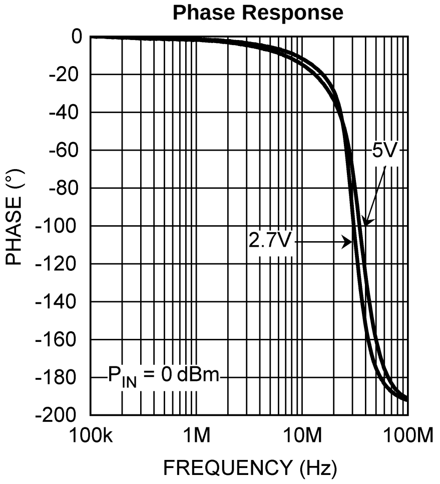

Figure 5.

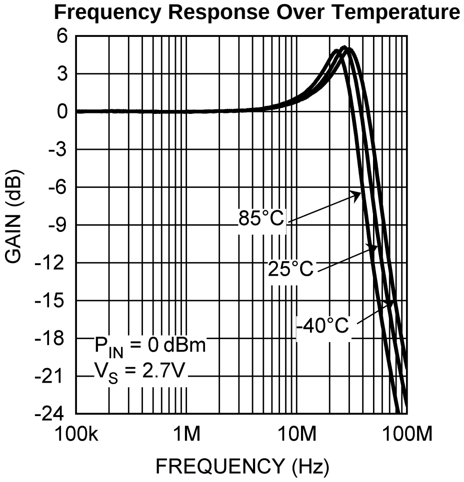

Figure 6.

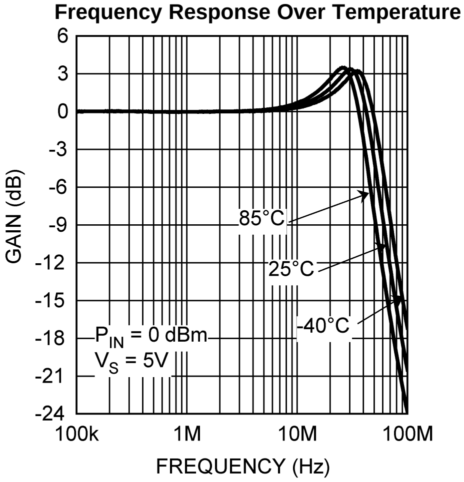

Figure 7.

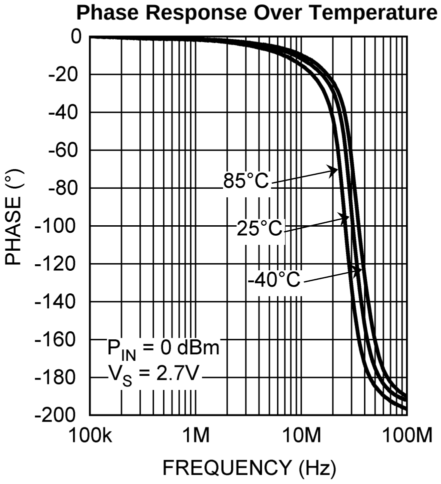

Figure 8.

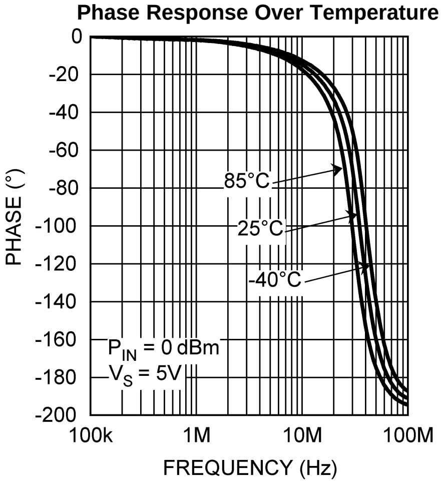

Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

Full Power Bandwidth

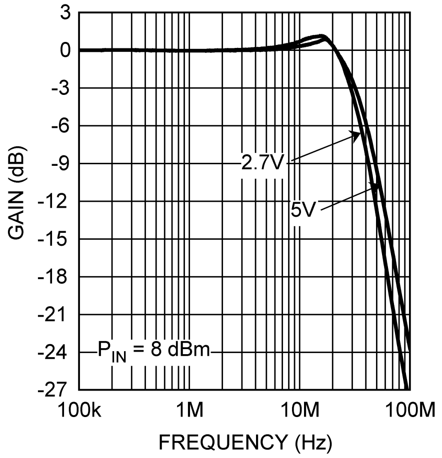

Figure 10.

Gain Flatness 0.1 dB (GFN)

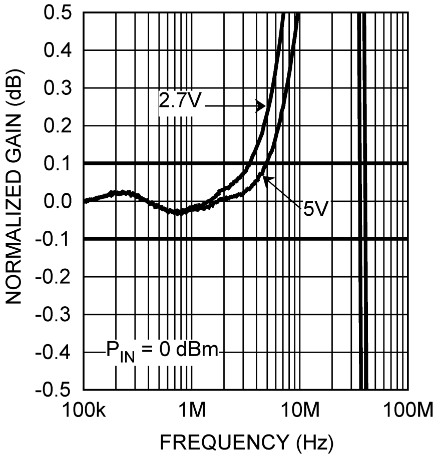

Figure 11.

Voltage Noise

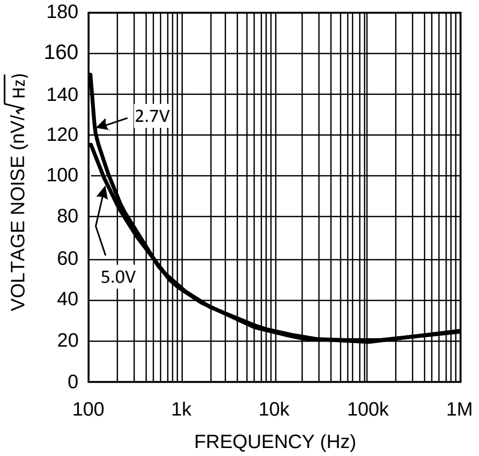

Figure 12.

Isolation Output to Input vs. Frequency

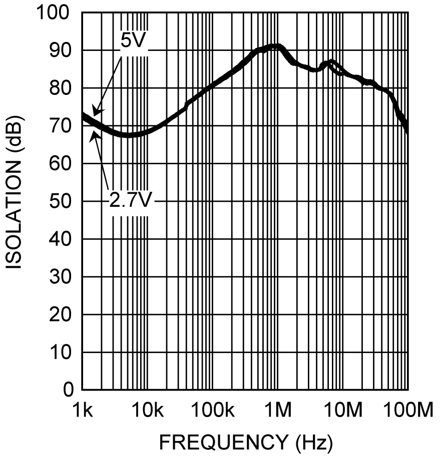

Figure 13.

Crosstalk Rejection vs. Frequency

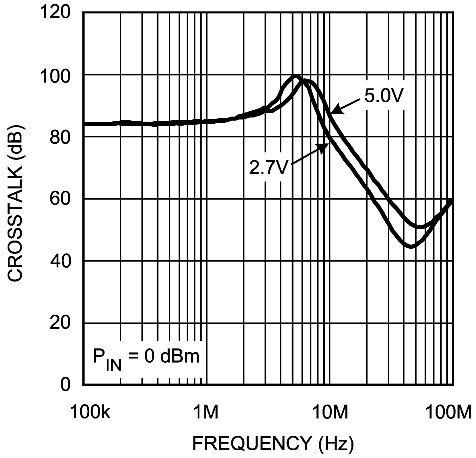

Figure 14.

Transient Response Positive

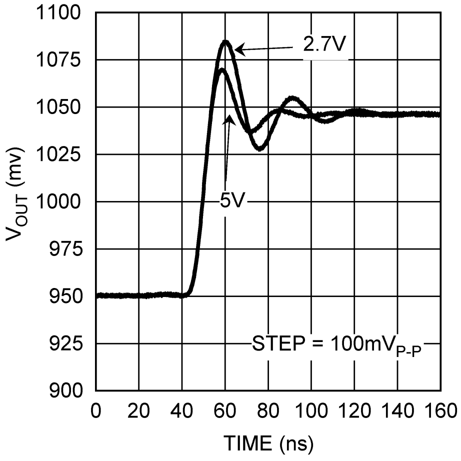

Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $\text{Enable}_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

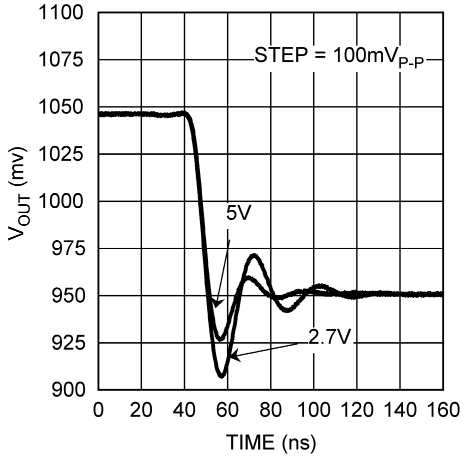
Transient Response Negative

Figure 16.

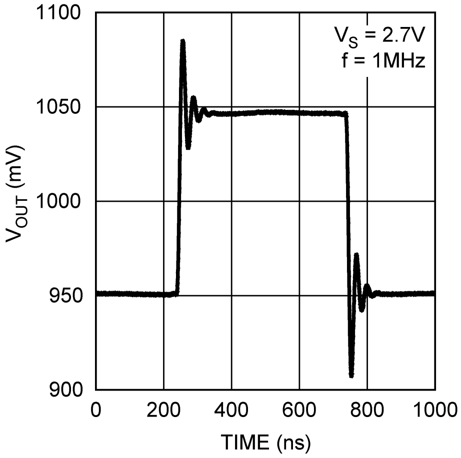
Small Signal Pulse Response

Figure 17.

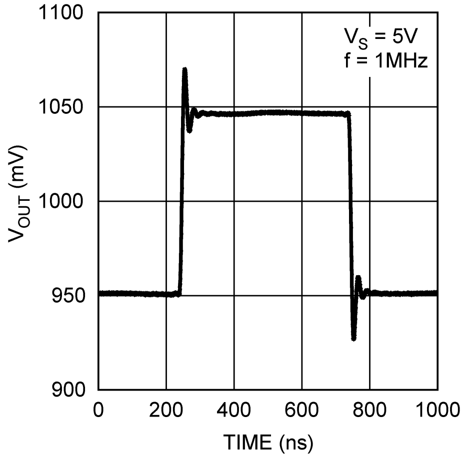
Small Signal Pulse Response

Figure 18.

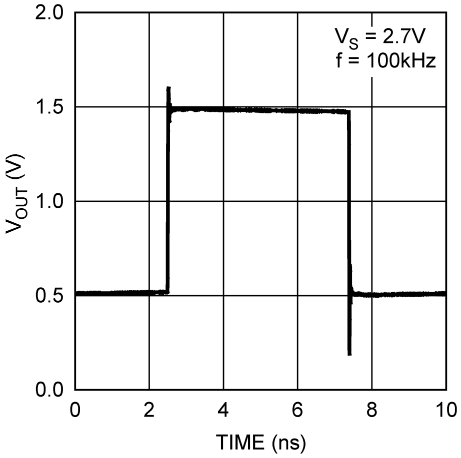
Large Signal Pulse Response

Figure 19.

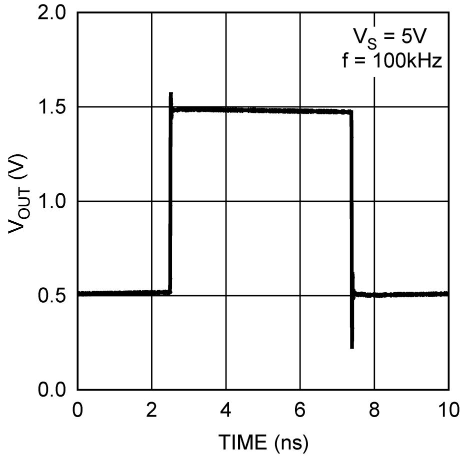
Large Signal Pulse Response

Figure 20.

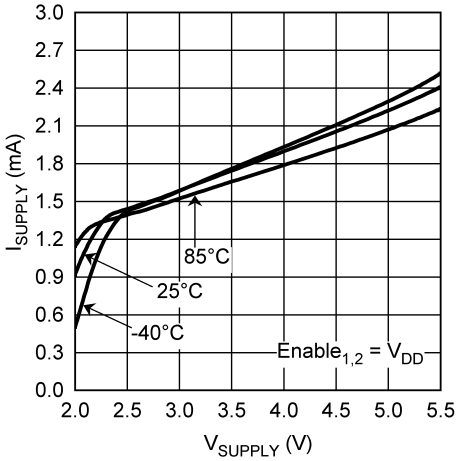
I_{SUPPLY} vs. V_{SUPPLY}

Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $\text{Enable}_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

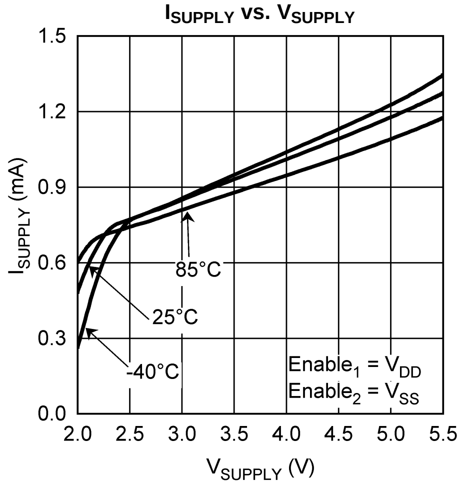
I_{SUPPLY} vs. V_{SUPPLY}

Figure 22.

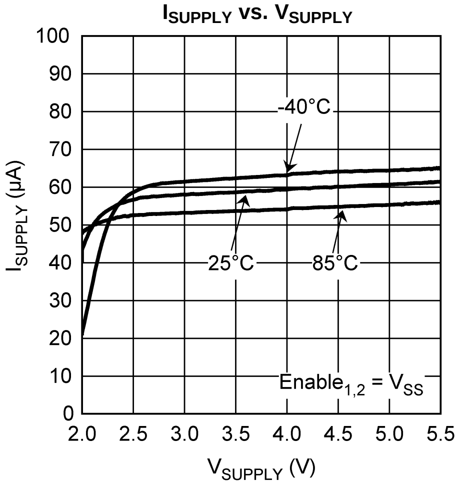
I_{SUPPLY} vs. V_{SUPPLY}

Figure 23.

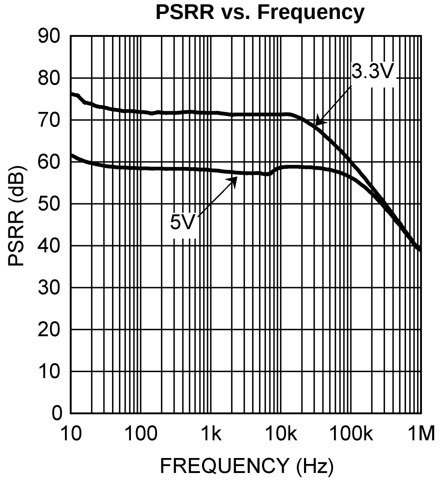
PSRR vs. Frequency

Figure 24.

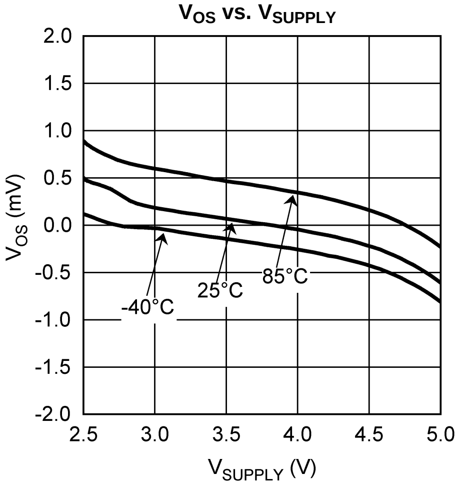
V_{OS} vs. V_{SUPPLY}

Figure 25.

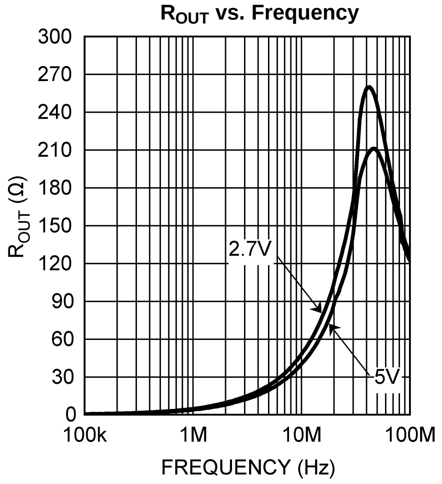
R_{OUT} vs. Frequency

Figure 26.

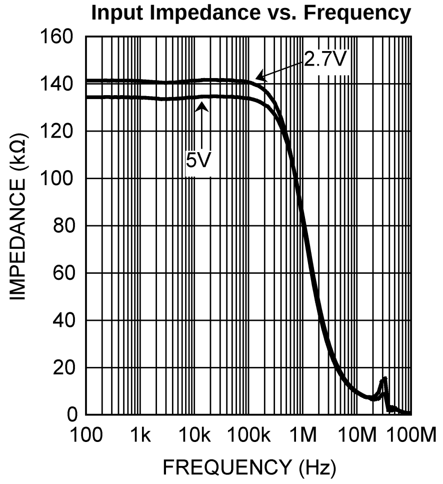
Input Impedance vs. Frequency

Figure 27.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

V_{OUT} vs. I_{OUT} (Sourcing)

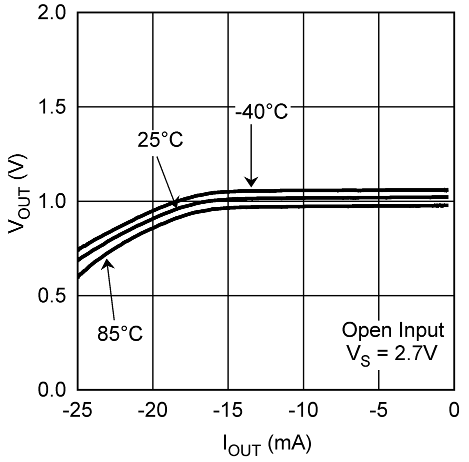

Figure 28.

V_{OUT} vs. I_{OUT} (Sourcing)

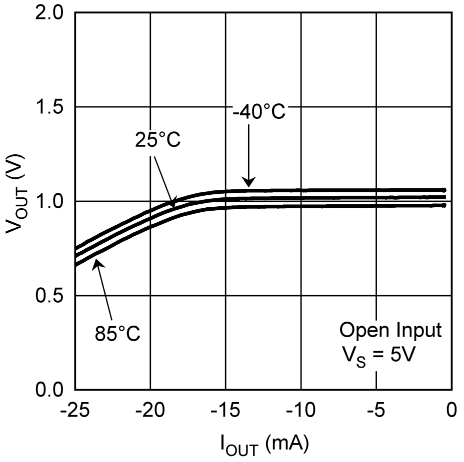

Figure 29.

V_{OUT} vs. I_{OUT} (Sinking)

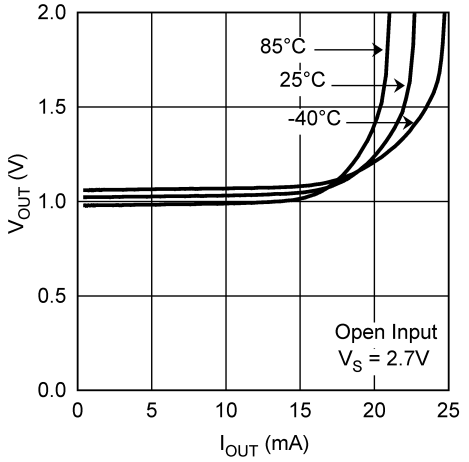

Figure 30.

V_{OUT} vs. I_{OUT} (Sinking)

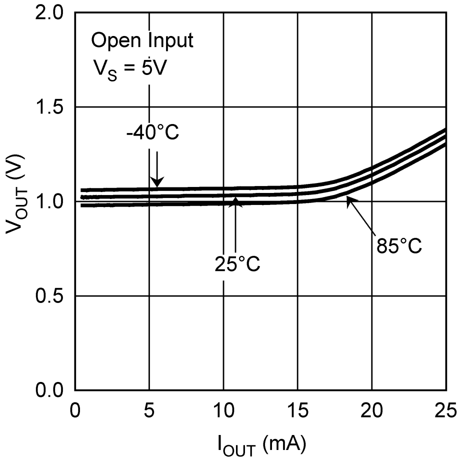

Figure 31.

I_{SC} Sourcing vs. V_{SUPPLY} over Temperature

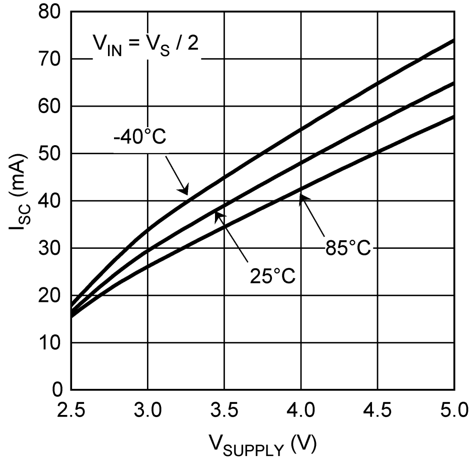

Figure 32.

I_{SC} Sinking vs. V_{SUPPLY} over Temperature

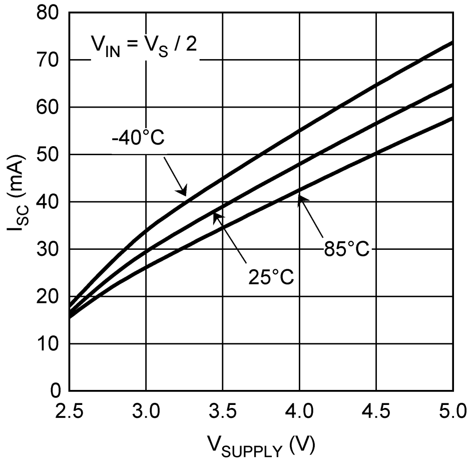

Figure 33.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 20 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 1 nF, unless otherwise specified.

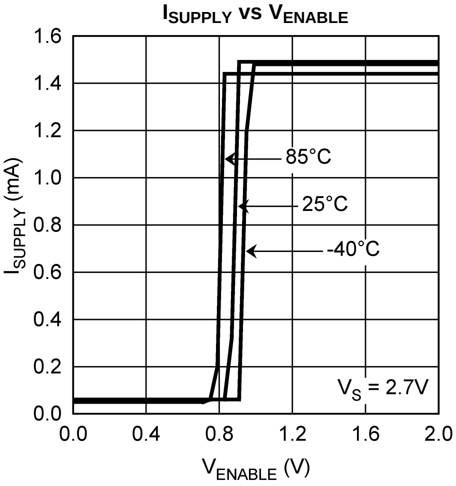

Figure 34.

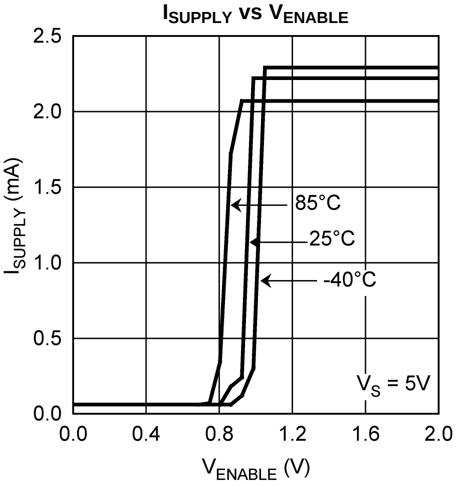

Figure 35.

APPLICATION INFORMATION

GENERAL

The LMV112 is designed to minimize the effects of spurious signals from the base band chip to the oscillator. Also the influence of varying load resistance and capacitance to the oscillator is minimized, while the drive capability is increased.

The inputs of the LMV112 are internally biased at 1V, making AC coupling possible without external bias resistors.

To optimize current consumption, the buffer not in use can be disabled by connecting the enable pin to V_{SS}.

The LMV112 has no internal ground reference; therefore, either single or split supply configurations can be used.

The LMV112 is an easy replacement for discrete circuitry. It simplifies board layout and minimizes the effect of layout related parasitic components.

INPUT CONFIGURATION

AC coupling is made possible by biasing the input. A large DC load at the oscillator input could change the load impedance and therefore it's oscillating frequency. To avoid external resistors the inputs are internally biased. This biasing is set at 1V as depicted in Figure 36. Because this biasing is set at 1V, the maximum amplitude of the AC signal is 2 V_{PP}.

The coupling capacitance should be large enough to let the AC signal pass. This is a unity gain buffer with rail-to-rail inputs and outputs.

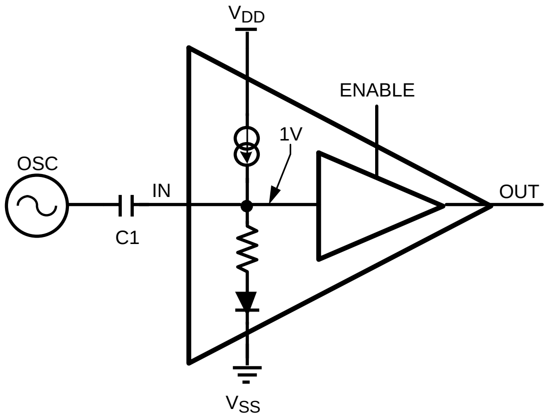

Figure 36. Input Configuration

FREQUENCY PULLING

Frequency pulling is the frequency variation of an oscillator caused by a varying load. In the typical application, the load of the oscillator is a fixed capacitor (C1) and the input impedance of the buffer.

To keep the input impedance as constant as possible, the input is biased at 1V, even when the part is disabled. A simplified schematic of the input configuration is shown in Figure 36.

ISOLATION AND CROSSTALK

Output to input isolation prevents the clock from being affected by spurious signals generated by the digital blocks at the output buffer. See the characteristic graphic entitled “Isolation Output to Input vs. Frequency” in the TYPICAL PERFORMANCE CHARACTERISTICS section.

A block diagram of the isolation is shown in Figure 37. Crosstalk rejection between buffers prevents signals from affecting each other. Figure 37 shows a Base band IC and a Bluetooth module as examples of this. For more information, see the characteristic graphic labeled “Crosstalk Rejection vs. Frequency” in the TYPICAL PERFORMANCE CHARACTERISTICS section.

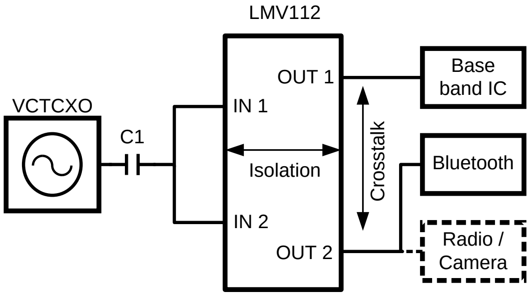

Figure 37. Isolation Block Diagram

DRIVING CAPACITIVE LOADS

Each buffer can drive a capacitive load. Be aware that every capacitor directly connected to the output becomes part of the loop of the buffer. In most applications the load consists of the capacitance of copper tracks and the input capacitance of the application blocks. Capacitance reduces the gain/phase margin and increases the instability. It leads to peaking in the frequency response and in extreme situations oscillations can occur. To drive a large capacitive load it is recommended that a series resistor is included between the buffer and the load capacitor. The best value for this isolation resistance is often found by experimentation.

The LMV112 datasheet reflects measurements with capacitance loads of 20 pF at the output of the buffers. Most common applications will probably use a lower capacitance load, which will result in lower peaking and significantly greater bandwidth, see Figure 38.

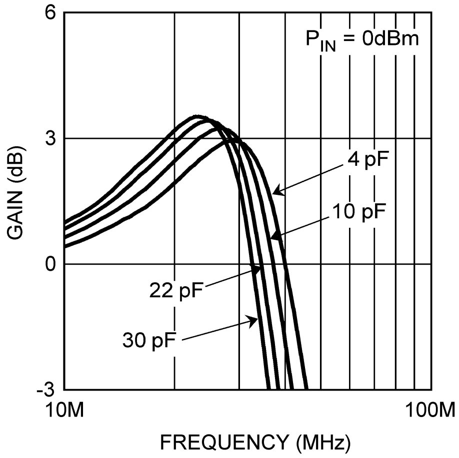

Figure 38. Bandwidth and Peaking

LAYOUT DESIGN RECOMMENDATION

Careful consideration for circuitry design and PCB layout will eliminate problems and will optimize the performance of the LMV112. It is best to have the same ground plane on the PCB for all power supply lines. This gives a low impedance return path for all decoupling and other ground connections.

To ensure a clean supply voltage it is best to place decoupling capacitors close to the LMV112, between V_{CC} and ground. The output of the VCO must be correctly terminated with proper load impedance.

Another important issue is the value of the components, which also determines the sensitivity to disturbances. Resistor value's should be but avoid using values that cause a significant increase in power consumption while loading inputs or outputs to heavily.

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV112SD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	112SD	Samples
LMV112SDX/NOPB	ACTIVE	WSON	NGQ	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	112SD	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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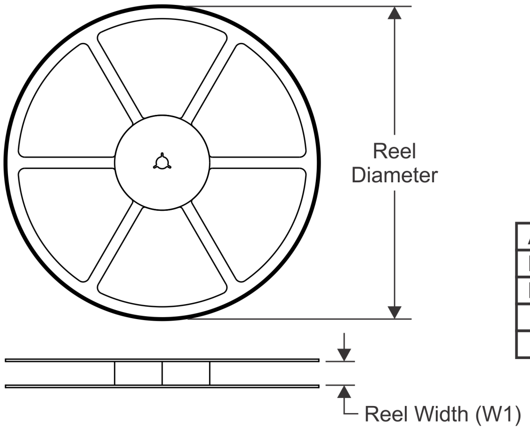
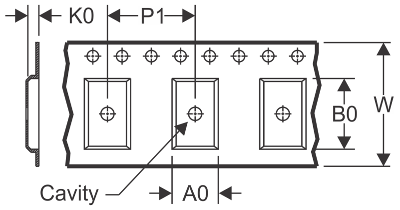
TAPE AND REEL INFORMATION

REEL DIMENSIONS

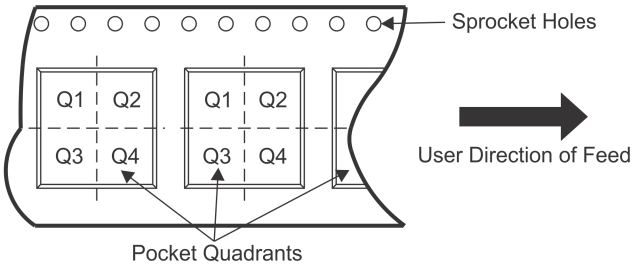


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

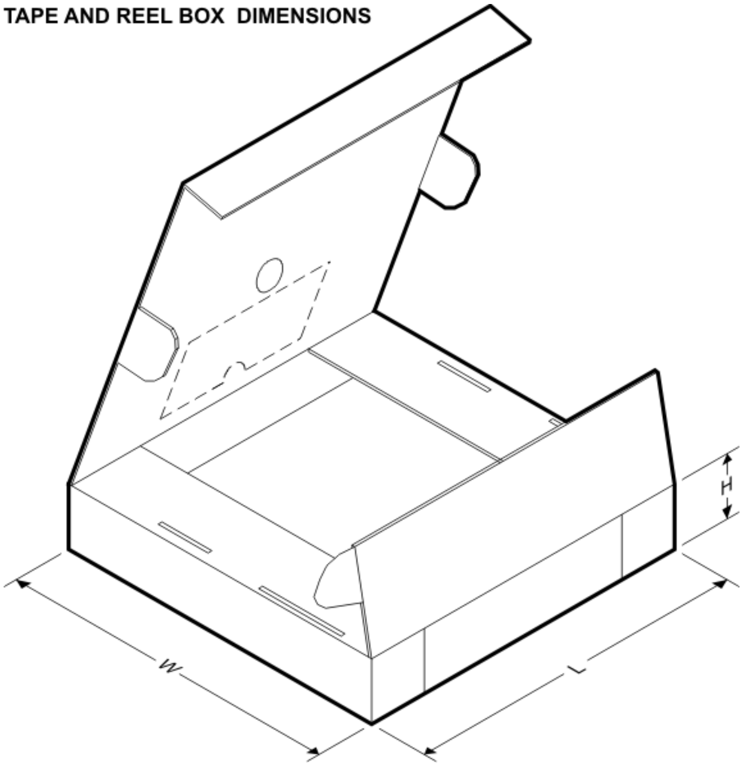
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

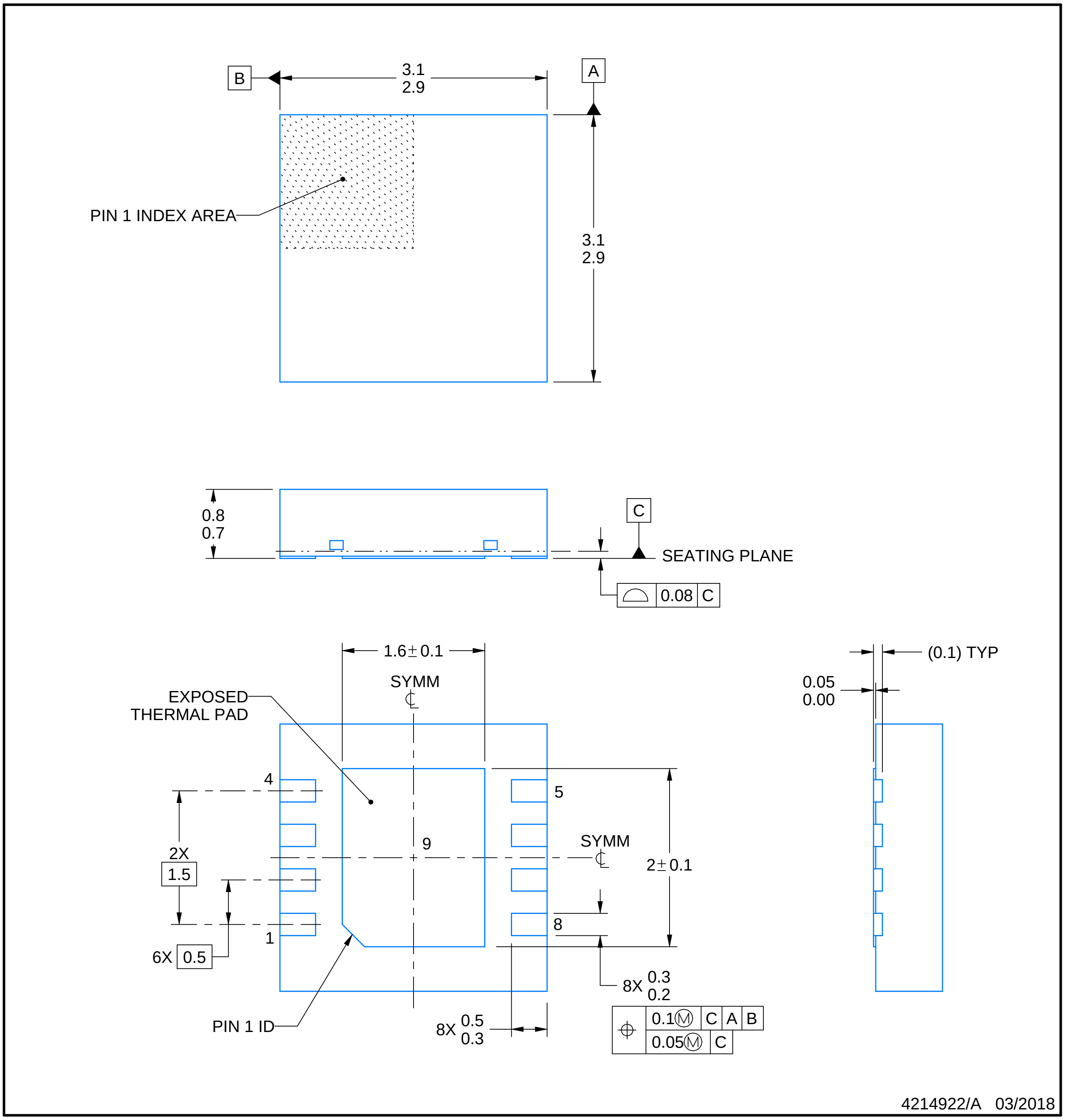
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV112SD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LMV112SDX/NOPB	WSON	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



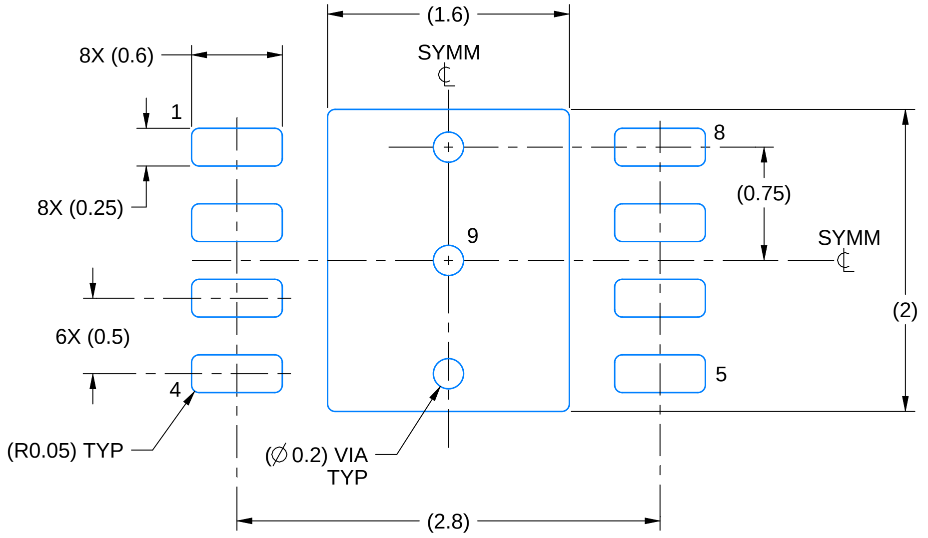
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV112SD/NOPB	WSON	NGQ	8	1000	210.0	185.0	35.0
LMV112SDX/NOPB	WSON	NGQ	8	4500	367.0	367.0	35.0

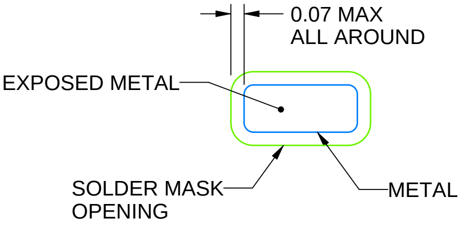


NOTES:

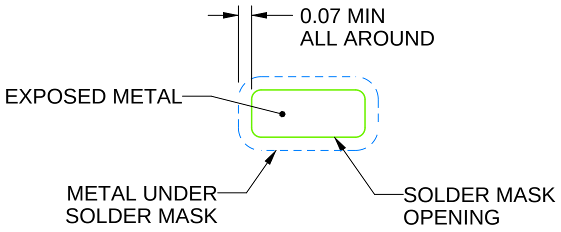
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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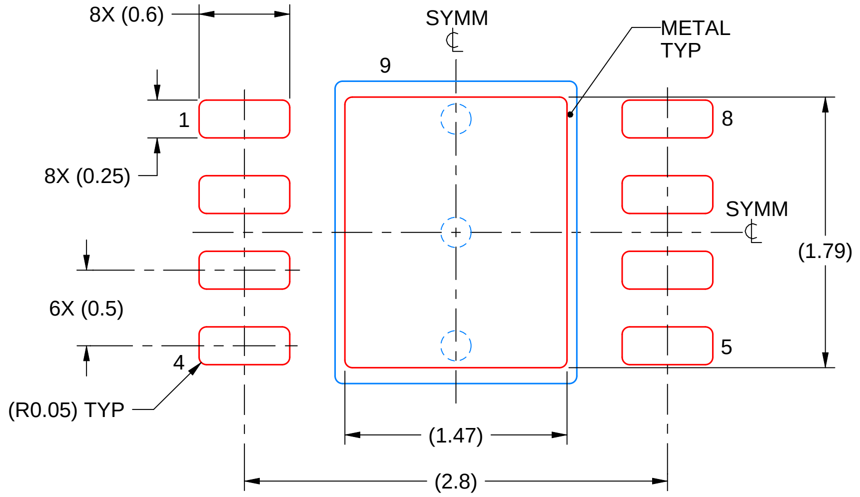
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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