Remote Control Transmitter Keyfob Application Example for TDA7110F

Application Note

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Table 1

Revision History 1st edition (no previous revisions)	
Page or Item	**Subjects (major changes since previous revision)**
V1.0, June 2012	

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1 Introduction

This Application Note gives a systematic overview about the steps taken by design and prototype build of a keyfob, based on a TDA7110F transmitter chip and a low power, yet very efficient RISC-type microcontroller manufactured by Microchip Technology Inc.

The design is compliant with the recent ETSI regulations for the 433 MHz ISM-band (EN300-220).

The approach stays close to the RF-Designer's viewpoint. Project details, including the choice of topology and layout decisions, are explained in-depth.

Firmware implementation and code debug topics are approached in a dedicated chapter.

The implementation of the required transmission parameters is done in a flexible manner (based on formal parameters) suitable to be adopted by applications with significant differences in protocol formats and requirements. This framework may be used as project draft for customer-specific designs, enhancing cost efficiency and shortening the time-to-market time.

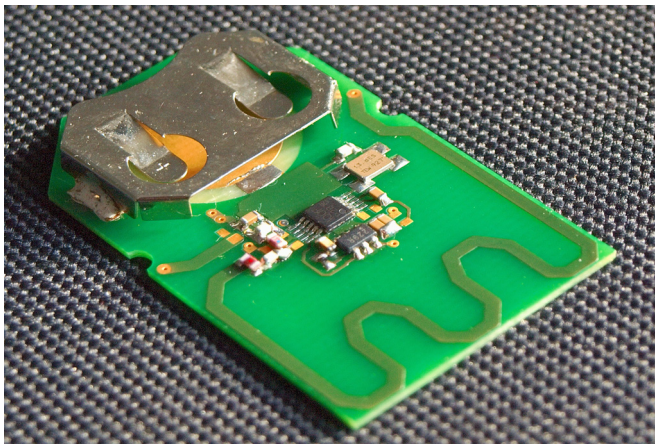


Figure 1 Top side view of Keyfob, battery and cover removed

Explanations on the interdependencies between modulation (signal) parameters and their influence on the generated RF-signal spectrum are dealt with in the **Chapter 3 Modulation parameters and their influence on signal spectrum**. This is an important aspect as far as the radiated signals must comply with regulatory standards on frequency stability, maxima of radiated power level, occupied bandwidth, maxima of unwanted radiations (i.e. harmonics of the carrier, intermodulation products, RF power leaking into adjacent channels) and so on.

Beyond regulatory aspects these parameters (of the transmitter) have comparable importance for a well performing RF link as receiver parameters and performance.

A subchapter deals with antenna topology choices, with an overview of monopole and magnetic loop antennas, bearing in mind that the usage of both types has been widespread by sub-gigahertz handheld devices. Antenna gain and radiation efficiency as well as radiated power and global power efficiency (of the full keyfob, as a system) are closely related factors.

The final part of the material contains an assembly code example for programming the PIC10F220 / 10F222 microcontroller and implementing an intelligent keyfob for FSK/ASK modulation scheme and Manchester encoding with additional functions of supply voltage monitoring and power management.

1.1 TDA7110F transmitter overview and features

The ICs of the TDK51xx/ TDA71xx family offer a high level of integration and need only a few external components in order to implement a fully functional transmitter. The device contains an integrated PLL synthesizer and a high efficiency power amplifier, which drives the load - which is in most cases a radiator (antenna). A special circuit design and a unique power amplifier design are used for reduced current consumption thus extending battery life. Additional features are a power down mode (with very low quiescent current) and a divided clock output.

Main features

- Transmit frequency range 433..435 MHz
- User selectable ASK and FSK modulation modes
- High efficiency RF power amplifier (typically +10 dBm RF output power)
- Low supply current
- Power down mode with low quiescent current (typical 0.3 nA @ +25°C current consumption in this mode)
- Crystal oscillator for accurate reference frequency generation ($f_{crystal}$ = $f_{TX\_Nominal}$ / 32)
- Fully integrated PLL frequency synthesizer
- Clock output for µC clocking / synchronisation (clock output frequency is $f_{crystal}$ /16)
- On-chip VCO without any external components
- Chip-internal f_{TX_LOW} / f_{TX_HIGH} switch for FSK modulation mode
- Low external component count
- Supply voltage range 2.1.. 4.0 V
- Operating temperature range -40.. +85 °C

1.2 Microchip PIC10F220 / 222 microcontroller family overview and features

The PIC10F220 / 222 devices from Microchip Technology Inc. are low-cost, high-performance, 8-bit, fully static Flash-memory based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word / single-cycle instructions. All instructions are single cycle (1 µs) except for program branches, which take two cycles.
The 12-bit wide instructions are highly symmetrical, resulting in code compression over CISC type architecture.

The PIC10F220 / 222 products depend over special features like Power-on Reset (POR) and Device Reset Timer (DRT), which eliminates the need for external Reset circuitry.
Internal Oscillator mode is provided (INTOSC), thereby preserving the limited number of I/O pins available for GPIO functions (no need for external crystal).
Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power consumption and reliability.

Main features

- 12 bit wide single-cycle instructions, except for program branches which are two cycle
- 8-bit wide data path
- 4 or 8 MHz precision internal oscillator (factory calibrated to ±1%) resulting in 500 ns / 1µs instruction cycle
- Direct, indirect and relative addressing modes for data and instructions
- Watchdog Timer (WDT) with dedicated on-chip RC oscillator
- Power saving sleep mode and wake-up from sleep on GPIO pin change
- Low operating current:< 175µA @ 2V / 4 MHz and 100 nA @ 2V typical standby current (sleep mode)
- Supply voltage range 2.0V..5.5 V
- Programmable weak pull-ups on GPIO pins
- 8-bit Real-Time Clock / Counter (TMR0) with 8-bit programmable prescaler
- Analog-to-Digital (A/D) Converter with 8-bit resolution and two external input channels

2 Keyfob implementation

The Keyfob Demonstrator described in this material is based on a TDA7110F transmitter and a low power yet very efficient RISC-type microcontroller of the PIC10F2xxx family, the latter manufactured by Microchip Technology Inc.
The example code listed in **Appendix** is suitable to be run either on PIC10F220 with 256 words of code memory and 16 bytes of SRAM for general purpose usage, or - if some encryption algorithms are demanded (probably of medium strength) then the PIC10F222 with 512 words of code memory and 23 bytes of SRAM may be a viable alternative. For applications demanding strong encryption algorithms, which may yield code size in excess of 512 words and usually are also more computation intensive as “plain” encoding, an upscaled member of the PIC microcontroller family (with 13 or 14 bit code width) might be a good choice.

Note: There are, of course, no limitations in choosing another microcontroller type (and supplier), as long as the selected host device can cope with the targeted supply voltage range (2.1..4 V for TDA7110F) and its architecture is suitable to support the application (the features should at best include an energy saving sleep / standby mode and a wake-up mechanism triggered by state change of GPIO lines for sensing key depressions).

2.1 Hardware

Relevant parts of the Keyfob Demonstrator schematics are shown in **Figure 4** and the full schematic in **Figure 13**. The unit operates in the 433 MHz band and the modulation mode is configured (per Firmware and component placement) either for ASK or for FSK.

Note: implementation of mixed mode modulation schemes based on this project are also possible (for instance synchronization bits transmitted with ASK modulation, followed by payload transmitted with FSK). The solution is drafted at the end of this chapter.

For reference frequency generation a crystal of nominal frequency equal with 1/32 of the desired transmit frequency is required (i.e. 1/32 of nominal carrier- or channel frequency). The chip-internal synthesizer in TDA7110F transmitter is of integer-N type. The VCO’s output frequency in stationary mode (i.e after the VCO pulls in and the PLL achieves phase-lock) is an integer multiple (***N***) of the reference frequency (f_{ref}), which is derived from the crystal oscillator.

$$\mathbf{f}_{\mathrm{carrier}} = \mathbf{N} \times \mathbf{f}_{\mathrm{ref}} \quad (1)$$

Note: the division ratio of the chip-internal divider (between VCO and phase detector of TDA7110F) is 64, but as the frequency of the signal delivered by VCO is also divided by two before applied to the RF power amplifier, the effective division ratio, relative to transmit frequency is 32 (64:2).
For example to generate a carrier of 433.920 MHz frequency will require a crystal of 13.560 MHz.
*A general Block Diagram of the chip, including the synthesizer unit is shown by **Figure 27**.*

To ensure maximum flexibility in system design and during evaluation, the Keyfob Demonstrator has been designed to be configured for:

- ASK modulation scheme or
- FSK modulation scheme

by choice of proper Firmware version, with conditional directives embedded in source code (for details refer to **Appendix**).

The antenna type is configured by board assembly (i.e. by component placement) either for:

- On-board electrical antenna (monopole), or for
- On-board magnetic loop antenna

If the coil *L4* is placed but the components annotated as *R4* and *C8* left unplaced, the resulting radiator will be a monopole (E-field antenna), as shown in **Figure 2**.

Attention: *unplaced components R4 and C8 are not shown in* ***Figure 2****, whereas* ***Figure 13*** *shows all of the components (i.e. for all versions) no matter if placed or left unplaced for a given configuration.*

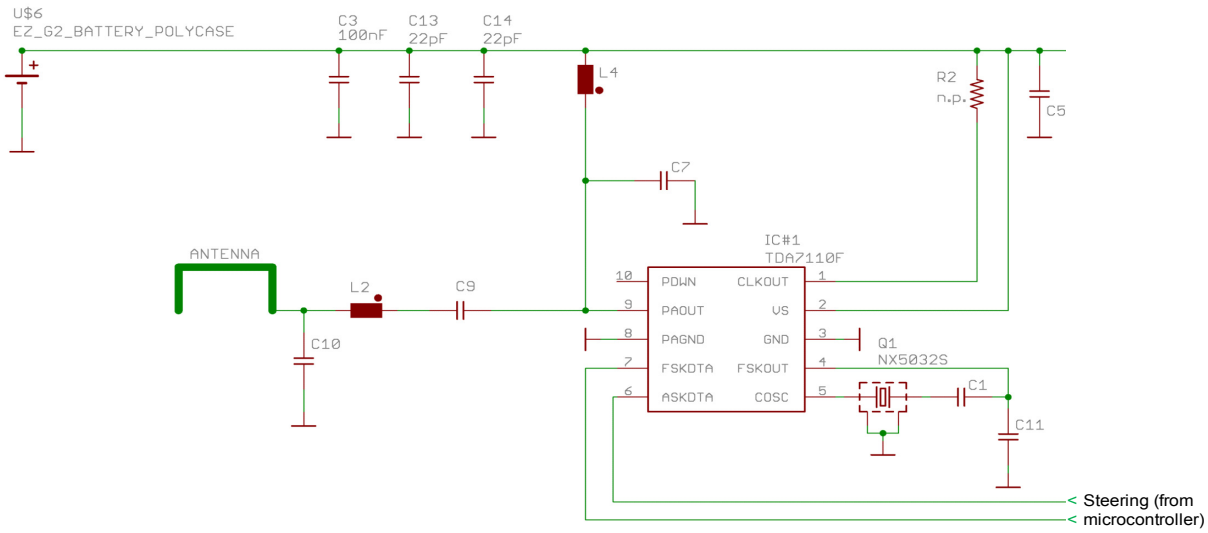


Figure 2 Board configuration for electrical antenna version. Unplaced components are hidden.

Provided a magnetic loop antenna setup, the RF-current component will flow through the entire antenna structure. By this setup *L4* will be left unplaced and the RF power amplifier will be fed with supply voltage over the current limiting resistor *R4*, resulting in a topology as shown in **Figure 3**.

If the capacitor C8 is of low value or unplaced (below 10..12 pF for the Keyfob operating in the 433 MHz band), R4 will introduce some degree for damping in the antenna circuit, a useful feature for suppression of parasitic resonances or attenuation of harmonics.

On the other hand, if *C8* has a high value (of around 100 pF or above) then the common node of *R4; C8* and the loop antenna are practically grounded, and *R4* acts like a current limiting resistor for the DC component flowing through the collector of the RF power amplifier transistor.

As such the current consumption of the RF end-stage can be reduced, and the amount of RF power delivered by the power amplifier shall decrease simultaneously.
This solution of RF power reduction may be an option for low power, short-range radio links.

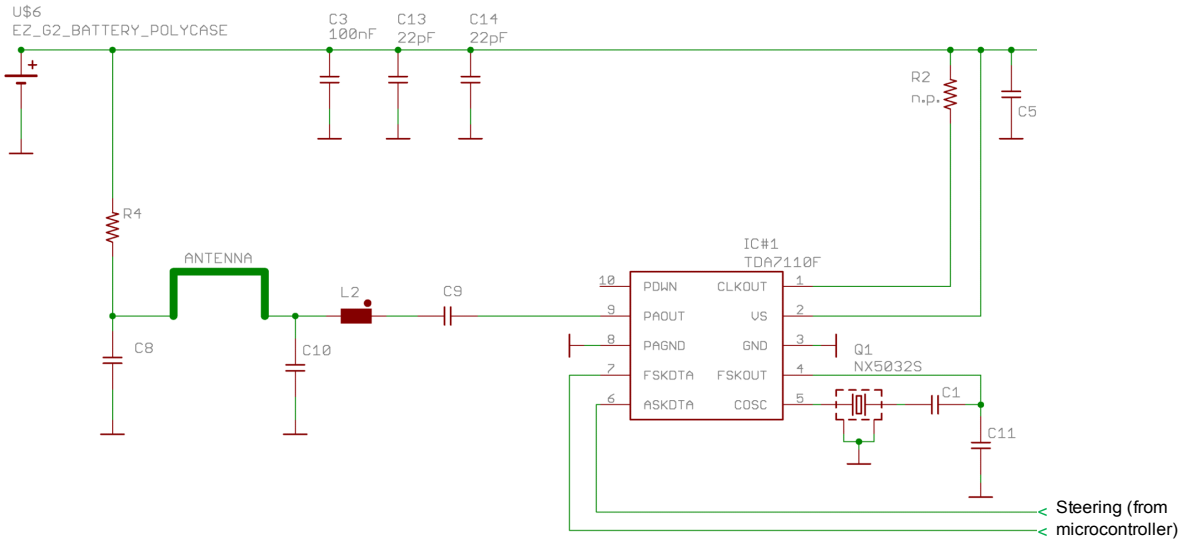


Figure 3 Configuration for magnetic loop antenna version. Unplaced components are not represented.

The microcontroller embedded in the keyfob unit (a RISC type PIC10F220 / 222) scans the key matrix (seeking also for states like multiple, simultaneously depressed keys). A unique representation of code is associated to each depressed key and this information is encoded by the Firmware, according to the used encoding scheme. Additionally a scrambling or encryption algorithm may be applied. The encoded data becomes part of the payload. Depending on the requested ruggedness of the link, supplementary to the data field some error detection or detection and correction information may be inserted into the payload.

Based on the frame content to be transmitted, the microcontroller assembles the frame (which apart from the previously mentioned payload part may also contain other fields, meant for signaling and synchronization), applying the frame bit by bit (or chip by chip) to the modulator.

At the same time the microcontroller generates the control signal(s) for the TDA7110F RF transmitter.

Note: by usage of NRZ (Non Return to Zero) encoding scheme the datastream which is applied to modulator is a 1:1 copy of the bits, composing the frame (and in this respect is not encoded, just a copy of the bitstream). If for instance Manchester encoding is used, each bit is composed of two elements, referred also as "chips". This encoding method is explained in Subchapter 2.3.2 ***Example for implementation of key scan and Manchester encoding****.*

The power management is also part of the microcontroller's tasks, the device putting itself and the TDA7110F in sleep mode (power down) after transmission of the frame, provided the scan does not identify any other depressed key.
The microcontroller will commence code execution at the entry point following the SLEEP instruction on subsequent key activation, assuming that before entering the sleep mode the "*wakeup on pin state change*" function have been activated (as in the recent firmware versions, see the **Appendix**).

As part of the power management, another task of the microcontroller is the supervision of the supply voltage level. This is accomplished by sampling the supply voltage value over the microcontroller's internal A/D converter (at best before starting an RF-transmission).

In order to prevent transmissions on erroneous frequencies systematic check of supply voltage value is an appropriate method (and associated with high confidence level) if performed before the ongoing frame transmission.

Attention: *Operating the RF transmitter below the* ***minima*** *of allowed supply voltage (of 2.1 V according to TDA7110F Datasheet) may result in PLL unlock. This may yield frequency error of the transmitted signal beyond the regulatory (legal) limits.The reason for this is that even if the phase detector, the VCO and the RF power amplifier are still working by "forced" operation below supply voltage minima, the tuning range of the VCO may slide out of the nominal range, thus frequency error may occur.*

Attention: *Operating the RF transmitter beyond the* ***maxima*** *of allowed supply voltage (of 4 V according to TDA7110F Datasheet) may result in irrecoverable damage to the chip.*

During idle time (i.e. no key is depressed and there is no ongoing transmission) the microcontroller switches the transmitter in power down mode by pulling low the following lines

- PDWN (Pin 10; TDA7110F)
- ASKDTA (Pin 6; TDA7110F)
- FSKDTA (Pin 7; TDA7110F)

followed by execution of a SLEEP instruction, thus placing itself also in low power mode.

If set in sleep mode typical current consumption of the respective microcontroller is below 100 nA and of around 0.3 nA for the TDA7110F, if powered down (PDWN pulled Low).
If a key is depressed (U$3 or U$4 in schematics **Figure 13**) the microcontroller is awaken from sleep mode and code execution commences.

The antenna feedpoint impedance and that of the chip internal RF power amplifier in the TDA7110F are matched, by the impedance matching network comprising the following elements

C9; L2; C10; C8 and *R4* if a loop antenna configuration is used (*L2* and *C7* are unplaced in this case)

- *C7; L4; C9; L2;* and *C10* if a monopole antenna configuration is used (*C8* and *R4* are unplaced in this case)

Obviously the component values in those impedance matching networks are determined by

- output impedance of the RF power amplifier and
- the radiation impedance of the antenna.

The latter is strongly influenced by antenna type (monopole or magnetic loop) even if the physical length of the conductive structures (striplines) on the printed circuit board is the same for both antenna versions.

The two antenna types may have very different radiation impedances for the same operating frequency.

Meanwhile radiation impedance of antennas is frequency dependent, which means that any antenna performing well in another (and distant) frequency band cannot be simply “imported” without performance loss, unless retuned for the new band.

For all the above reasons the component values in the impedance matching network are listed in **Table 3** for two antenna configurations (electrical antenna, also referred to as *monopole* and magnetic loop antenna, also referred to as *loop antenna*).

Once the design has been settled for a given target performance (RF carrier power, efficiency point of RF power amplifier and spurious rejection profile) even though after “freeze” of component values the Keyfob’s transmit frequency is slightly changed (but still inside the allowed limits of the respective ISM band) it is not mandatory to readjust the values of the components in the matching network.

However a change in type (technology) and / or manufacturer of the reactive elements (coils and capacitors) may have a noticeable influence on the effective impedance of the matching network due to the fact that the effective ***Q*** of the reactive elements on the operating frequency may differ significantly from the nominal ***Q*** value of that particular component, as specified by manufacturer.
Usually component manufacturers test the components at significantly lower frequencies as the frequencies allocated for VHF/UHF ISM bands, but the trend is going toward full coverage of the sub-gigahertz bands.

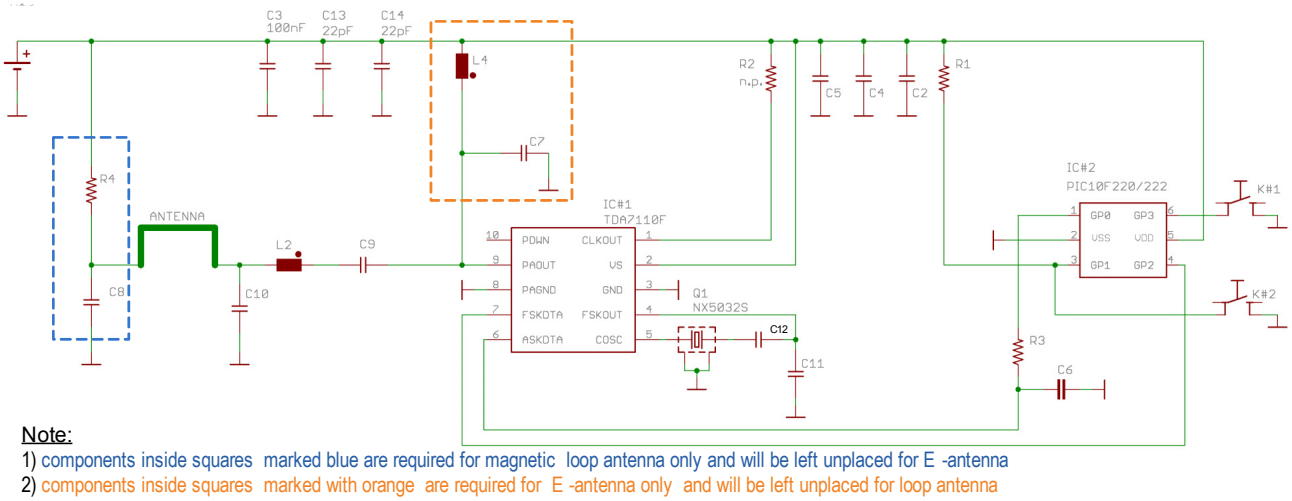
It is common knowledge that the ***Q*** parameter of coils may severely depend on technology, type and provider (manufacturer), especially in the upper ISM bands (of 868 MHz and 915 MHz).

The spread in terms of ***Q*** parameter is not so severe by capacitors, but the temperature coefficient may exhibit significant variations over type and manufacturer.

During the whole design process (from prototype to productive version) it is therefore wise and time-saving (but not mandatory) to use components of the same type (technology) and originating from the same manufacturer, even if the values are retuned several times during any subsequent iterations.

Tools from several manufacturers are able to deliver accurate forecast regarding the component impedance versus frequency behavior over a wide frequency range.

For details on simulation software please refer to **[7]** and **[9]** in **References**.



Note:
1) components inside squares marked blue are required for magnetic loop antenna only and will be left unplaced for E -antenna
2) components inside squares marked with orange are required for E -antenna only and will be left unplaced for loop antenna

Figure 4 TDA7110F Keyfob Demonstrator schematics, configured for FSK modulation. Unplaced components are hidden. Placed 0R bridges shown as continuos wire segments for ease of signal tracking in this drawing.

In order to minimize spectral splatter and perturbation of adjacent channels it is recommended to proceed according as per the sequence below:

- at the beginning of a transmission (e.g. frame) the PLL is activated for around 1..3 msec, yet without activating the RF power amplifier
  This time is sufficient for the reliable start of crystal oscillator. Actually the crystal begins to swing well earlier, but according to definition, startup time equals the time elapsed from powering the oscillator until to the oscillation amplitude shall have reached 90% of the stationary value.
  In order for the phase comparator (which is part of the on-chip synthesizer) to operate properly, it requires a certain level of signal at both inputs (i.e. inputs from reference oscillator and from the integer-N divider). Levels below limit are usually associated with erroneous comparator output or at least with a noticeable increase of the jitter at the output. This jitter cannot be eliminated entirely by the loop filter, and it may thus degrade the phase noise figure of the transmitter.
  Transmitters of the TDA71xx family are designed to operate with low phase noise and jitter. After the startup time has been elapsed the drive level required for proper operation of the phase comparator shall be duly reached, and the issue mentioned in the above paragraph shall only apply to the transient mode of the oscillator. Thus if the RF power amplifier is activated too early, or if the reference oscillator is driven by an external signal with insufficient level (for instance a TCXO, with too low drive level) frequency error may occur or degradation of the output signal's phase noise ratio may result.
  The oscillator startup is followed by the active transmission phase. At this stage there are differences between ASK and FSK operation mode, details being explained below:

  – For transmissions using **ASK** modulation scheme (whereas the transmitter schematics matches the simplified version as shown in **Figure 5**), the **FSKDTA** line shall be held high (to keep the PLL in active state) while the **ASKDTA** pin is pulsed according to the data stream and the implemented encoding scheme. Thus the RF power amplifier is switched ON and OFF, as shown in **Figure 25**. Meanwhile the reference oscillator and synthesizer part - VCO included - will stay all the time ON during the ongoing transmission and switched OFF at the end of transmission.
    In other words the amplitude shift keying (ASK) is accomplished at the RF power amplifier level.[1)]

1) As the VCO is always ON during active transmission, there may be a minor level of RF energy leaking from VCO toward the output of the RF power amplifier, even if this amplifier is OFF. The level of leakage is well below the admitted regulatory threshold (usually by around -70 dBm, measured at RF PA pin) and depends at large extent from the quality of the (external) decoupling capacitors.

– If **FSK** modulation scheme is used (whereas the transmitter schematics matches the simplified version as shown in **Figure 4**,) the timing diagram shall be similar to that shown in **Figure 26**.
During oscillator startup and PLL acquisition time the **FSKDTA** line shall be held high (to set and keep the PLL in active state) and **ASKDTA** shall be pulled low, thus holding the RF power amplifier in inactive state thus avoiding transmission with unlocked PLL.
This phase is shown by the mid-portion (of time axis) in **Figure 26**, marked with PLL-Enable.
After the startup time have been elapsed the active transmission part follows, realized by pulsing the **FSKDTA** pin in accordance with the data stream and the used encoding scheme, while keeping the **ASKDTA** pin high, thus enabling the RF power amplifier.
As a consequence an RF carrier with practically constant envelope but variable frequency will be output by the RF power amplifier.

Both timing procedures as listed above (associated with **ASK** and **FSK** modulation) will render a margin that shall be suffice for the reference oscillator to start up and it will just as well grant the PLL the necessary time to pull in (on reference frequency) and achieve phase-lock.

Note: The startup time of the Reference Oscillator is imposed mainly by

1. *the gain of the NIC type oscillator itself (negative resistance **-R** of the **N**egative **I**mpedance **C**onverter) and*
2. *the equivalent R; L; C parameters of the used crystal, major influence being derived from equivalent R_s of the crystal (see the **TDA7110F Datasheet** for computation of Startup Time and Oscillator Margin)*

- It is recommended to choose a time constant of the mentioned RC group of around 1/6 of the bit cell time for NRZ modulation and 1/6..1/10 part of the bit duration if a DC-free encoding scheme is used (like Manchester). The benefits of the procedure (power ramping and modulation signal shaping) are explained in detail in **Chapter 3 Modulation parameters and their influence on signal spectrum**.

Another efficient measure aiming minimization of spectral splatter consists of steering the AM modulator of the TDA7110F (in fact the RF-power amplifier block) using a ramped signal with moderate slew-rate on both, the leading and the trailing edge instead of a fast-rising digital signal (i.e. with high slew-rate).

The group *R3* and *C6* (schematics **Figure 4**) is implementing this function, acting as a low-pass filter with moderate cut-off frequency. The RF-transients generated by moderately “rounded” modulation signals, alike the ones shown in the mid and right side of **Figure 21**, contain less high order harmonics energy thus causing less perturbation in the adjacent channels and less spectral splatter as the high slew-rate signal, shown on the left-hand side of the same figure.

It is recommended to choose a time-constant parameter for the mentioned RC group of around 1/6 of the bit duration if NRZ modulation is employed or 1/6..1/10 part of the bit duration if a DC-free encoding scheme is used (for example Manchester).

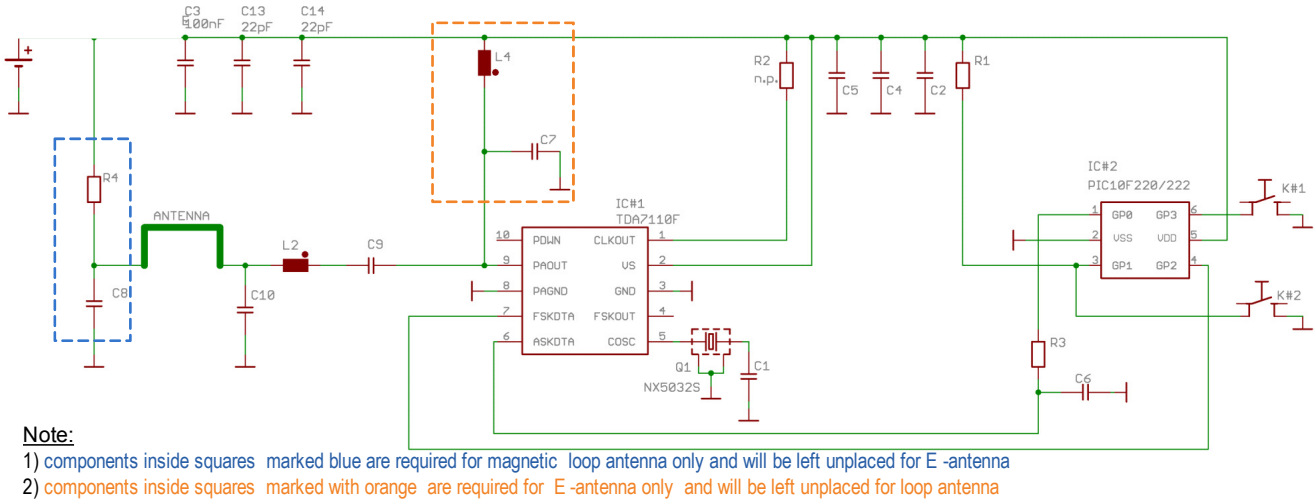
Detailed explanation on the procedure’s benefits (i.e. power ramping and modulation signal shaping) shall be provided in **Chapter 3 Modulation parameters and their influence on signal spectrum**.

In order to ease up firmware debugging during development phase and firmware update of already assembled boards, connections to in-circuit programmer / debugger (*ICD*) are provided on the PCB (upper-right corner region in **Figure 13**).

Attention: *To avoid voltages which may exceed the reliable limits of TDA7110F during ICD-steered operations, (in circuit programming and debugging) and to keep the ICD-tool safely isolated from ASKDATA input, resistor R3 should have a minimum value of 470 Ohms or it should be temporarily de-soldered for the time the ICD is connected with the Keyfob*

The keyfob is energized by a 3V lithium cell. Low internal resistance battery types are preferred for this design as the total current drain from battery is of around 12 mA during transmit bursts.

In order to detect supply voltage drops below the allowed minimum supply voltage level of the TDA7110F, duly accurate monitoring of the battery voltage can be performed by the microcontroller's on-chip 8 bit A/D converter.



Note:
1) components inside squares marked blue are required for magnetic loop antenna only and will be left unplaced for E -antenna
2) components inside squares marked with orange are required for E -antenna only and will be left unplaced for loop antenna

Figure 5 TDA7110F Keyfob Demonstrator schematics, configured for ASK modulation scheme. Unplaced components are hidden. Placed 0R bridges shown as continuos wire segments for ease of signal tracking in this drawing.

The modulation mode dependent assembly versions are listed below.
If the Keyfob is intended solely for ASK modulation, a single load capacitor, *C1*, connected in series with the crystal shell be required, as shown in **Figure 5**. The value of this capacitor shall be in accordance with the load capacitor range, as indicated in the data sheet of the particular crystal by its manufacturer.

Fine tuning of the channel frequency is possible by means of changing the value of *C1* as long as this variation complies with the range of load capacitance, specified in the data sheet.

Table 2 Modulation mode (ASK / FSK) dependent assembly versions

Part designator	Modulation scheme Component value		Unit	Type/ size	Note
	FSK	ASK)			
C1	not placed	10	pF	0402 (R07S)	Johanson Technology, NP0 type
C11	6.8	not placed	pF	0402 (R07S)	Johanson Technology, NP0 type
C12	10	not placed	pF	0402 (R07S)	Johanson Technology, NP0 type
Q1	13 560		kHz	TSS5032A/B[3)]	Reference,1/32 of RF carrier frequency ($f_{crystal}$=1/32 f_c);Manufacurer Tokyo Denpa Co. Ltd **weblink**

2.2 Antenna and matching network design and performance evaluation

This chapter provides a brief description of the steps taken to design an antenna, suitable for mobile operation in the 434 MHz ISM band, and, in conjunction with this antenna, a network, matching the output impedance of the RF power amplifier to the footpoint impedance of that particular antenna.

2.2.1 Design of the RF power amplifier to antenna matching network

The RF power amplifier in the TDA7110F transmitter is built around a bipolar junction transistor (BJT) stage, operating in class-C mode. The clear advantages of this solution are:

- good efficiency
- simplicity and reliability (no need for thermal compensation of bias voltage value, like by class-A amplifiers)
- flexibility

As shown in **Figure 6**, the RF power amplifier is terminated in a load, which is, in most cases, a radiator (antenna or antenna array), either connected to the amplifier over a matching network (the most frequently used solution) or directly. Latter is a seldom used solution, as wire antennas or structures realized on printed circuit board (stripline or patch antenna) with footpoint impedance value close to the conjugate complex of the power amplifier's impedance (which is a condition for maximum power transfer) would have mostly an impractical size (at least for mobile or handheld applications) in the 433 MHz band.

Due to this fact, solely the solution of connecting the radiator over a matching network to the power amplifier shall be analyzed below.

The large signal equivalent model of the RF power amplifier found in TDA7110F is shown in the left side block of **Figure 6**. It is worth to note that this is a simplified and linearized model, valid for the impedance of the power amplifier in the maximum output power region. It does not take in account the nonlinearity due to compression and the output impedance may differ significantly from the values which are based on small signal model.

The optimum load for the RF power amplifier could be easily determined by the substitution method.

Attention: in addition to the PA's internal capacitance the method, as described below takes in account also the on-board stray capacitance and the losses in striplines. Therefore the resulting equivalent power amplifier impedance (as shown in Figure 6) is different from the de-embedded impedance value listed in the TDA7110F Datasheet.

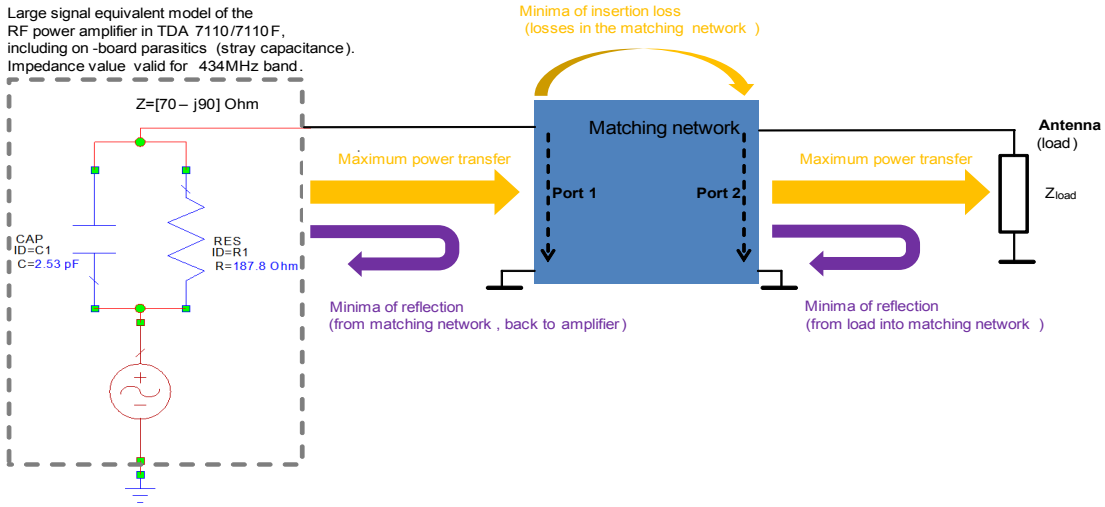


Figure 6 Large signal model of the TDA7110's RF power amplifier (simplified version)

A laboratory setup, based on the substitution method for measurement of large-signal impedance of RF power amplifiers is shown in **Figure 8**. Basically it is the implementation of the setup drafted in **Figure 7**, but instead of a load with fixed impedance a tuner with variable impedance is used.

The measurement assumes the following steps:

- the RF power amplifier is connected over a bias-T and port $\mathbf{P_2}$ of a double-throw coaxial relay to a tuner. Port $\mathbf{P_3}$ of the tuner is terminated in a 50 Ohms load, usually an RF power meter or a spectrum analyzer
- by variation of the tuner's impedance such points are searched (based on impedance predictions derived from simulation or simply by random variation of tuner impedance) where either the output power of the RF power amplifier is close to the theoretical peak, allowed by the supply voltage or the power added efficiency of the power amplifier stage is close to maximum.
  The efficiency of the power amplifier is the ratio of the RF output power and the DC input power. The RF output power is recorded by the power meter (or spectrum analyzer) and the DC input power is the product of the supply voltage multiplied with the current drained by the amplifier.

- the coaxial relay is then switched over to port P_1 and the load's impedance is measured. After de-embedding of the measurement data the optimum load trend curves will result (or contours if drawn in a Smith-diagram).

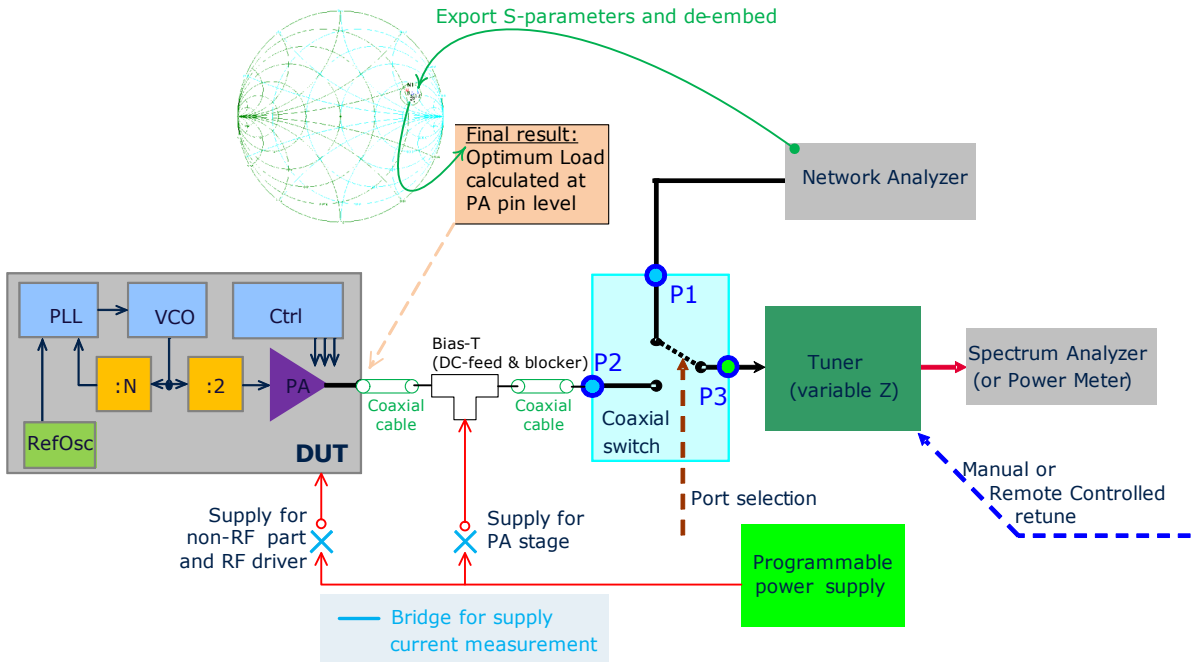


Figure 7 Block diagram of an RF power amplifier measurement bench.

A laboratory setup for impedance measurements based on substitution method is shown in **Figure 8**.

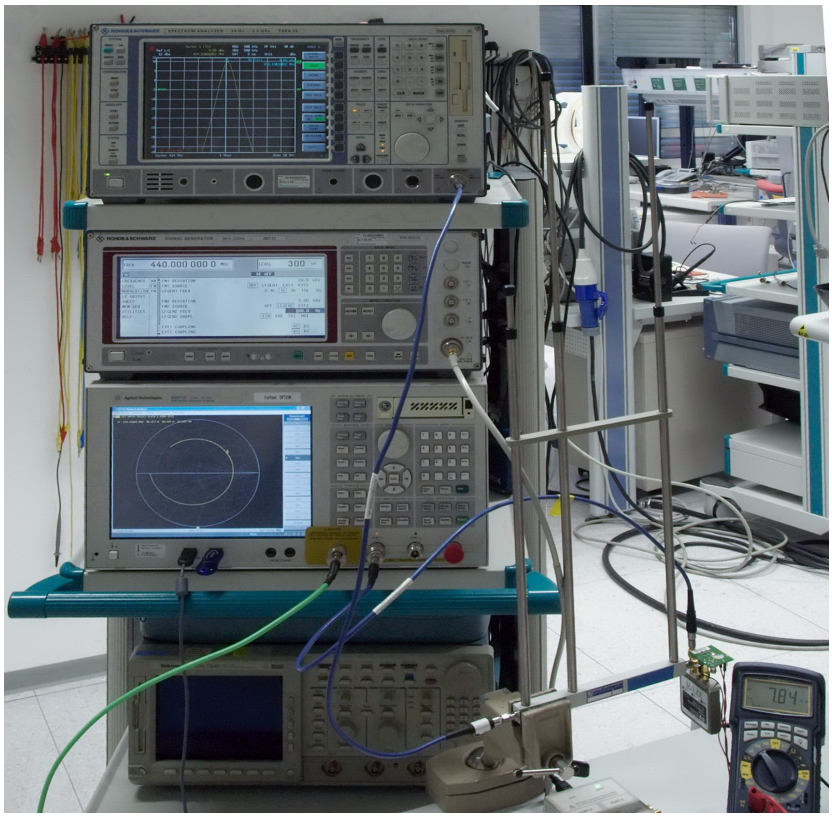


Figure 8 RF power amplifier optimum load measurement setup. The tuner is held by a wise, the coaxial switch, used to switch between spectrum- and network analyzer is left to multimeter.

2.2.2 Antenna design considerations

Following part is just a short overview of the steps taken in order to

- design
- build, evaluate, optimize
- and finally to qualify

antennas for mobile applications.

The main tool for design of small antennas in the sub-gigahertz frequency domain is usually an EM-solver, embedded in a simulator, which serves as GUI, either of general application coverage or one specialized, dedicated for design of radiators and antennas.

In the particular case of keyfobs, there are usually

- hard constrains regarding the available space for antenna. Quite often the shape of PCB is already imposed by the shape of the external shell - in most cases some sort of molded plastics. The position of keys, pushbuttons and display underwent ergonomy considerations and the board design (PCB) is subdued to those initial conditions.
- the on-board electronics is exposed to medium- or high intensity EM fields, as the components are in the immediate vicinity of the radiator
- constrains in term of cost, size and weight limit or restrict the usage of shielding
- strong coupling with the operator's hand is expected, as the normal operation mode of such a device is held in hand and keys are pushed by fingers.
  The strong capacitive coupling leads to
  – absorption of a part of the radiated RF energy in the human tissues
    (however as the total available power delivered by the transmitter is low, usually not exceeding 10 mW, the operator is exposed to RF radiation levels well below the safe limits, specified by Specific Absorption Rate (SAR) recommendations and regulations.
  – medium grade- or even strong detuning of the antenna, which at its turn translates into load pulling

As it may be seen in **Figure 9**, the environment may have a considerable influence on antenna impedance, at the fundamental frequency (transmit channel) and at harmonics as well. The antenna design process have to cope with all the above listed limitations and still deliver - as a final result, antenna devices which have good radiation efficiency in the operating frequency band, acceptable rejection of the harmonics (i.e. low gain on harmonics frequencies) and are less prone in terms of performance degradation to detuning. As a final conclusion it is recommended to design and evaluate the antenna in conjunction with a Human Hand Model.

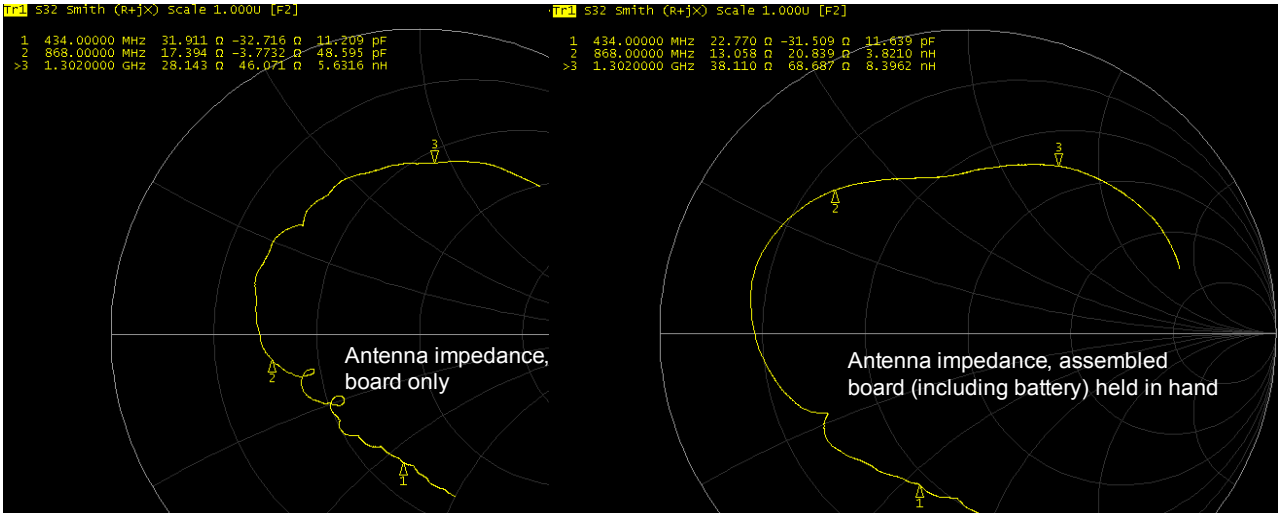


Figure 9 Keyfob antenna impedance. Left side - measurement on a bare board, right side - impedance measurement on assembled board, held in hand. Notice the change of impedance.

2.3 Firmware and encoding scheme

In order to reduce the energy consumption and extend the battery life-cycle, the example code (listed in **Appendix**) is laid out so that the PIC10F22x microcontroller enters Sleep mode during the idle time thus significantly decreasing the current drain from the battery. While in Sleep mode, if the state of input pins *GP1* or *GP3* changes, the wake-up on pin-state change mechanism is triggered and the microcontroller resumes the code execution.

As the microcontroller incorporates weak pull-ups on the inputs, which can be activated or deactivated by means of clearing or setting the $\overline{\text{GPPU}}$ bit in OPTION register, it is practical to use those internal weak pull-ups instead of external resistors.

Within the recent implementation, the monitored inputs are *GP1* and *GP3* (i.e. monitoring of two keys).

If there are any requirements for monitoring of more than 2 keys, a 2*2 scanning matrix could be implemented as shown in **Figure 18**.
The maximum size of the scan matrix is imposed by the number of available GPIO pins and is limited to 4 keys (2*2 matrix) if microcontrollers of the PIC10F2xxx family are used. For extended keyboard functionality (and thus a higher number of GPIO lines used for keyboard scanning) the PIC12Cxxx or PIC16Fxx family members are more suitable.

If the 4-key extended scan matrix solution is implemented (with PIC10F2xxx), proper care is needed to avoid the short glitches (resulting from the scan procedure) intruding the PDWN and ASKDATA pins of the TDA7110F transmitter at a level which may trigger false Tx-activation and transmission.
Therefore:

- RC low pass filters are used between the keyboard matrix and the transmitter's inputs, which are able to reject (filter out) the short glitches
- The keyboard scanning routines have to be set up so that to minimize the pulse width resulting from scanning. Implementing such routines is not bound to major efforts as most of the instructions of the PIC10F22x family execute quite fast, in one cycle (yielding 500 ns / 1 µs instruction execution time by 4 / 8MHz clock).

Entering the "wake-up from sleep" state is signalled by "1" state of $\overline{\text{GPWUF}}$ flag in STATUS register (0x03.7).
All other reset types keep this flag in "0", and is set "1" only by the *wake-up from sleep* event.

In order to activate the "wake-up from sleep on pin change" feature, in advance of execution of a SLEEP instruction the $\overline{\text{GPWU}}$ bit of OPTION register (0x.na.7) have to be cleared.
For detailed description of the wake-up mechanism, please refer to ***PIC10F220 / 222 Datasheet***.

Subsequent to a wake-up from sleep event, the depressed key is identified (if there are still any active ones), a corresponding code is inserted in the frame (as payload) and then frame shall be transmitted.
Once the end of frame is reached, the transmitter shall be deactivated by pulling low the PDWN; ASKDTA and FSKDTA lines, or if PDWN is floating (i.e. left not connected, as in **Figure 4** and **Figure 5**), then by pulling low the ASKDTA and FSKDTA lines.

*Note: the power-up function of the TDA7110F chip is the equivalent of a hard-wired OR between the **PDWN**; **ASKDTA** and **FSKDTA** lines.*

After execution of a SLEEP instruction, the microcontroller enters sleep mode. This shall produce a significantly reduced current consumption for both devices, the TDA7110F chip (which is powered down) and the microcontroller, until the sleep mode is maintained.

2.3.1 Basic example with 2 bytes of payload and NRZ encoding

The frame structure of the application listed in **Appendix Section 5.1** consists of:

- A run-in portion of 4 bits, required by the RSSI block of the counter side (receiver) for recognition and to pull in and, but the duration can be shortened if the receiver's RSSI (and AGC if any) is fast enough.

- Two synchronization bytes (0x55) and (0xAA).
- A payload of two bytes.

In this example no explicit encoding is applied (i.e. the bits are transmitted in transparent mode, equivalent with non inverted NRZ encoding) but any simple encoding scheme like Manchester, Miller or Biphase can be easily implemented in the available code space of a 10F22x microcontroller.

The example code is set up for 1200 bit/s transmission speed, assuming the internal oscillator of the PIC 10F22x is set for 4 MHz nominal frequency. For transmissions clocked with 8MHz internal oscillator frequency the timing variables have to be adjusted accordingly.
The timing parameters are listed and their effects explained in the relevant source code part.

For each byte the most significant bit (MSB) is transmitted first and LSB as the last one.

A screenshot of the data stream, as generated by example code (listed in **Section 5.1** is shown in **Figure 10**.

The basic-line PIC10F22x microcontrollers have a 2-level hardware stack, allowing of the storage of 2-program counter words.

Programmers shall consider that the “chaining” of subsequent subroutine calls must be considered and tracked carefully due to this limitation, otherwise stack overflow may occur and there are no indications (flags) whatsoever for any stack under- or overflow situations.

The above limitation is the main reason for the “mixed” appearance of the example code - partially it may look like macro expansions, without- or with seldom call of subroutines, and partially (with special regard to data transmission routines) it may rely on short loops and timing subroutine calls, thus using lower level subroutines embedded / called by higher level routines. As emphasized before, in order to avoid stack overflow, proper care needs to be taken not to exceed the number of two simultaneous calls.

During the code development and verification phase, the flash memory (code and configuration) of the PIC10F22x microcontrollers may be rewritten with new content by means of an in-circuit programmer /debugger (ICD), as described in the previous part (**Chapter 2.1**), without removing the microcontroller from the application board.

Detailed description of the in-circuit serial programming procedure is provided in the technical documentations related to the PIC 10F22x microcontroller family, published by Microchip Technology Inc.

Attention: *proper care is required throughout any operations under control of in-circuit programmer or debugger (for instance flash programming, read, write, verify) as the battery-delivered supply voltage may be conflictive with the signals forced by the in-circuit programmer / debugger.*
Therefore it is highly recommended the removal of the battery while the ICD-tool is connected.

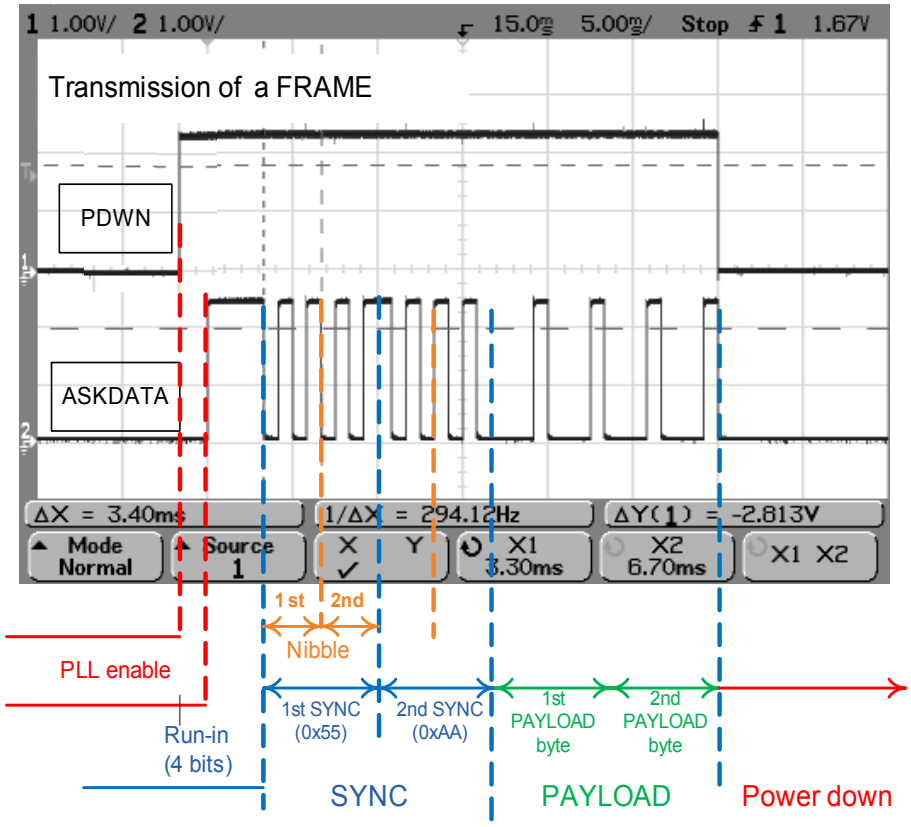


Figure 10 Data transmission with 1200 bit/s, as implemented in the example code (listed in Section 5.1). 1st SYNC byte is 0x55, 2nd 0xAA followed by two bytes of payload. Observe the run-in (4 bits) at the lead portion of the frame and that the PLL is activated ~2 msec before SYNC transmission begins to allow for crystal oscillator startup and PLL settling time.

2.3.2 Example for implementation of key scan and Manchester encoding

In this subchapter the details of a more complex implementation, in terms of frame structure are explained.

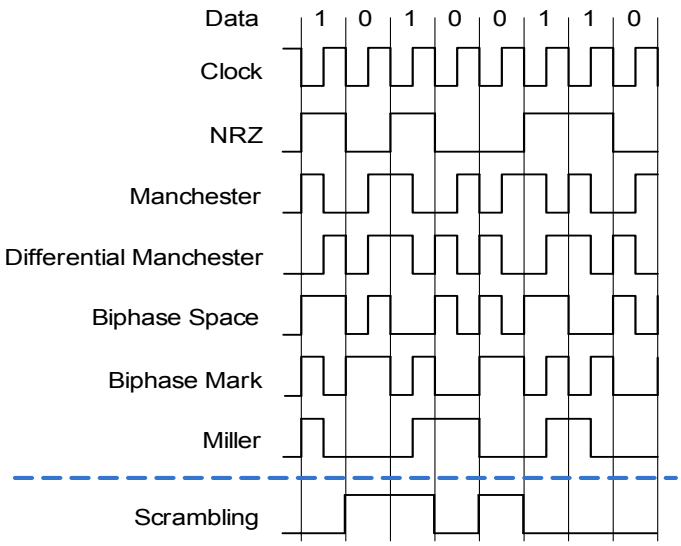


Figure 11 A graphical overview of several, widespread encoding schemes.

The implementation, is compatible, in terms of frame structure, encoding and transmission speed with the *TDA7210V Remote Control Receiver Board*, described in **References [6]** and with the *PMAfob*, a project built around the transmitters of TDA51xx/TDA71xx SmartLEWIS™ MCU family. Complete project files, containing detailed description of hardware, code and frame structure are to be found in **References [3]**.

Figure 11 is a graphical overview of the most widespread encoding modes, used in RF remote controls and telemetry systems. However for detailed comparison of the listed encoding methods the reader is advised to refer to dedicated materials, dealing with Code Theory and encoding algorithms.

To maintain compatibility with the receiver project, as described in **References [6]** then same framing and data structure is used as by the KeyFob project described in **References [3]**.

The main transmission parameters are listed below:

- transmission speed 9600 bit/sec
- Manchester encoding
- emulation of AES encryption
- RF channel frequency 433.920 MHz

The source code is contained in the downloadable **TDA7110F_Keyfob_Design_Package.zip** file.

2.4 Finetuning and possible alignments

Timing routines, which are under the control of the 10F22x microcontroller rely on the frequency accuracy of the on-chip oscillator. The initial accuracy is rather good (around 1% according to **PIC 10F220 / 222 Datasheet**) but if the user does wish so, the onboard oscillator frequency may be verified and adjusted within a reasonable range.

To align the oscillator and timing routines in the software, proceed according to the following sequence:

- Verify the accuracy of the onboard oscillator. This can be achieved easily, if the FOSC4 bit in the OSCCAL register is set (0x05.0). In this case a signal with 1/4 frequency of the on-board oscillator will be output on *GP2* port, overriding other port functions.
  The initial frequency error should be measured and if necessary the oscillator will be trimmed.
- In order to trim the oscillator, a frequency correction factor has to be determined and stored in memory, respectively loaded into the OSCCAL register at power-up. The correction factor is a 7 bit, signed integer, with standard representation (i.e. the number is positive and will increase the frequency if the most significant bit of OSCCAL register is “0” and vice-versa, the frequency will be decreased if this sign bit is “1” as then the rest of the string represents a negative integer).
- Subsequent to the trimming of the on-chip oscillator within the desired accuracy range, the timing accuracy of bitrate generation routines shall be checked. This can be accomplished either by counting the total number of execution cycles (most instructions execute in one cycle, except *call, retlw, goto* (jump) and conditional branch instructions) or by running a small program-loop that shall output a known bit pattern (for instance a symmetrical ..101010.. sequence).
  Timing errors can thus be easily visualized on oscilloscope and corrected in the corresponding code segment. An example is shown in **Figure 12**.
  As the timing error tends to multiply (with increasing bit number), it is more reasonable to measure the duration of an N-bit string instead of a single bit. It may also happen that a timing error with positive deviation, say for the “1” and a negative deviation (of error) for “0” annihilate each other or at least the sum is less than each one apart, this leading to a partial compensation, as long as the number of “1”s and of “0”s is roughly equal in a frame.
  But for a pattern consisting in majority of - say “1”s the individual errors will add up. Such an asymmetrical error type may not be obvious in a symmetrical bit pattern (like the previously mentioned..101010.. sequence) but it may, nevertheless, produce adverse effects if a long string of identical bits is transmitted with a non DC-free encoding, duly leading to error multiplication.
  Therefore it is recommended to use during the test and calibration of the timing routines not only patterns with binomial distribution, but also several patterns containing more, identical subsequent bits, especially if such a pattern may appear later in the application, as part of a frame.

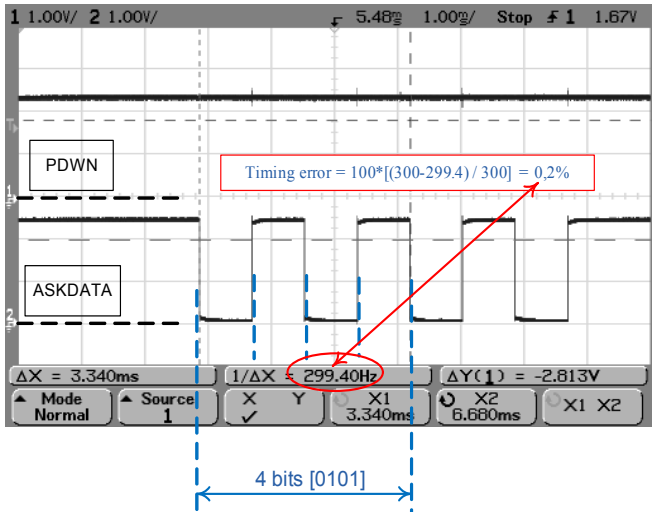


Figure 12 Check for timing errors.
By this transmission of test pattern (1200 bit/s) the nominal duration of 4 bits corresponds to 300Hz and the effective duration, measured with X-cursors indicates an absolute error of 0.6 Hz, yielding a relative error of 0.2%.

The RF transmit frequency of the keyfob is imposed by the reference frequency (f_{TX} = 32 * $f_{crystal}$). The crystal's oscillation frequency can be fine-tuned (in a narrow range) by variation of *C1* capacitor's value.

For calculations of feasible load capacitor value range (*C1* in this design) please consult the Chapter dedicated to reference oscillator in the **TDA7110F Datasheet**.

The transmit frequency can be monitored and measured either with a spectrum analyzer (a frequency marker option may ease the reading) or with an RF frequency counter.

Another option to perform the oscillator frequency check is to measure the subdivided reference frequency signal on Pin 1 (CLKOUT) of the TDA7110F chip.

As the built-in synthesizer of the transmitter is of integer-N type, the VCO frequency, as well as the transmit frequency shall be an integer multiple of the reference frequency
f_{TX} = 32 * $f_{crystal}$.
On the other hand, the signal frequency on CLKOUT pin of TDA7110F equals $f_{crystal}$ /16. This pin is driven by an open-collector stage (as described in **TDA7110F Datasheet**). Therefore to reach a reasonable signal swing (on CLKOUT pin) a pull-up resistor shall be connected between the CLKOUT pin and the positive supply voltage line.
A placeholder for the pull-up resistor is provided on the PCB, designated as component *R2*.
After the alignments are completed, it is recommended to remove this resistor or at least not to load it with excessive capacitive loads (for instance a low pass filter with large capacitor value may appear for this output as a significant capacitive load).
Current glitches generated by loading- and discharging the capacitor (connected to pin 1, CLKOUT) may interfere with the PLL's charge pump current and appear as parasitic sidebands of [K * f_{CLKOUT}] frequency, grouped around the RF carrier.

Therefore, considering the above frequency division- and multiplication relations f_{TX} = 32 * 16* f_{CLKOUT} or in other words

$$f_{TX} = 512 \times f_{CLKOUT} \quad (2)$$

Using the above relation, the carrier frequency can be determined even without an RF-frequency counter or spectrum analyzer, by simply measuring the signal frequency on CLKOUT pin and multiplying it with 512, provided the frequency counter instrument used for the test has a good accuracy for signals below 1 MHz.

Note: If using this procedure for transmit frequency check, take care to use an AC-coupled high impedance probe at the frequency counter input (instead of direct DC-coupling, which would inject a DC-current from the supply line over the pull-up resistor and into the probe).
Such a high impedance probe can be reliably driven by the respective CLKOUT pin's driver stage, maintaining DC-isolation of the frequency counter's input port from the power supply of the Keyfob.

2.5 Keyfob Demonstrator schematics, layout and version-specific eBOM

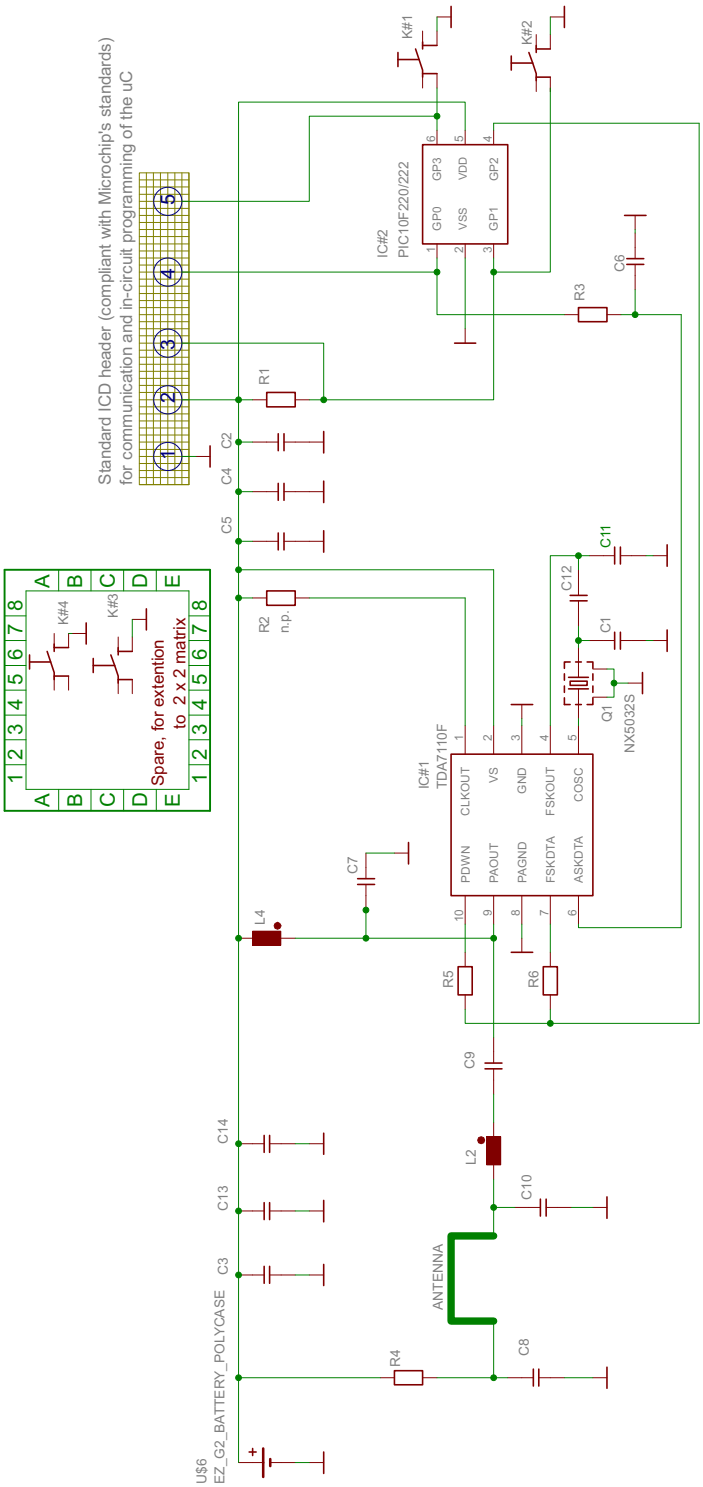


Figure 13 Keyfob Demonstrator schematics

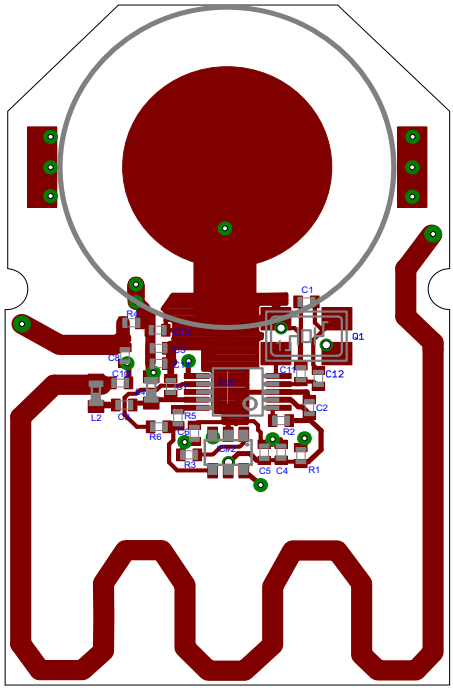


Figure 14 PCB, component placement, top view

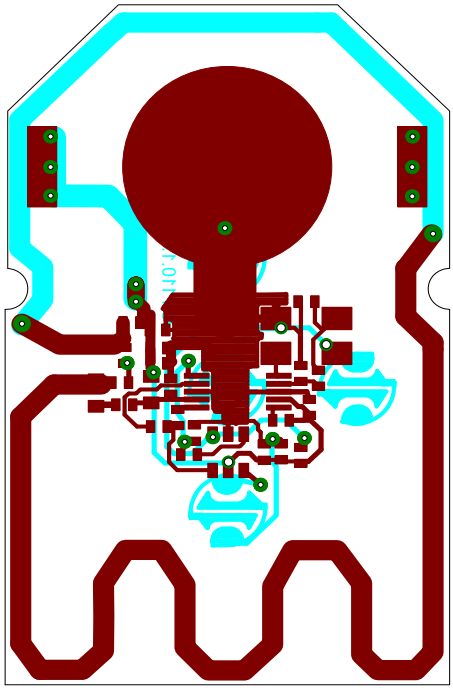


Figure 15 PCB, top and bottom copper

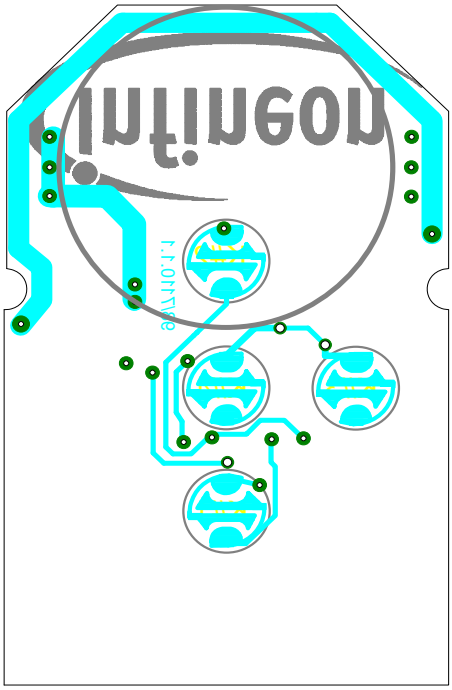


Figure 16 Component placement, bottom layer with silk mask

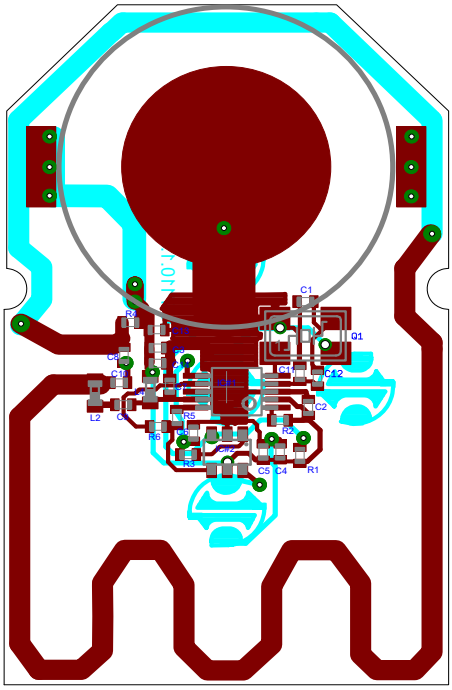


Figure 17 PCB, top placed components with top and bottom copper layers visible

Table 3 eBOM TDA7110F Keyfob Demonstrator

Antenna version dependent component values					
Part designator	Value Antenna Type		Unit	Type/ size	Note
	E-434 [1]	M-434 [2]			
C7	1,5	n.p.	pF	0402 (R07S)	Johanson Technology; NP0 type
C8	n.p.	3,3	pF	0402 (R07S)	Johanson Technology; NP0 type
C9	6,8	10	pF	0402 (R07S)	Johanson Technology; NP0 type
C10	4,7	3,9	pF	0402 (R07S)	Johanson Technology; NP0 type
L2	27	27	nH	0402Q	Johanson Technology; cer. chip inductor
L4	82	n.p.	nH	0402Q	Johanson Technology; cer. chip inductor
R4	n.p.	0R	Ohm	0402	may be increased up to 47 Ohms
Components common for both antenna versions.					
C1	see **Table 2**		pF	0402 (R07S)	
C2	100		pF	0402	
C3	100		nF	0402	
C4	100		nF	0402	
C5	100		pF	0402	
C6	4,7		nF	0402	adjust for low pass filter cutoff frequency
C11	see **Table 2**		pF	0402 (R07S)	set FSK frequency shift
C12	see **Table 2**		pF	0402 (R07S)	set center frequency in FSK mode
C13	100		pF	0402	
C14	100		pF	0402	
R1	not placed / 330		kOhm	0402	only for versions with battery voltage monitoring option in FW, otherwise n.p.
R2	not placed		kOhm	0402	only for test 0.68..1 kOhm
R3	2K2		kOhm	0402	adjust for lowpass filter cutoff frequency
R5	n.p. / 0R		Ohm	0402	n.p for FSK/ASK transmitter 0R for ASK-only transmitters
R6	0R / n.p.		Ohm	0402	0R for FSK/ASK transmitter n.p. for ASK-only transmitter
IC#1	TDA7110F			TSSOP-10	Infineon Technologies AG **weblink**
IC#2	PIC 10F22x			SOT23	Microchip Technology Inc. **weblink**
Q1	13.560		MHz	TSS5032A/B[3]	Tokyo Denpa Co. Ltd **weblink**

Note:

1) E-xxx designator for version(s) with electrical antenna, xxx is the frequency band (expressed in MHz)
2) M-xxx designator for version(s) with magnetic loop antenna, xxx is the frequency band (expressed in MHz)
*3) For other crystal type or manufacturer recommendation, consult the Infineon Technologies web page (search for sorted list of manufacturers and tested crystal versions) **weblink***
4) all capacitors used within Keyfob project are of 0402 size, manufactured by Johanson Technology
5) all inductors used with Keyfob project are ceramics chip inductors (of 0402Q size), manufactured by Johanson Technology

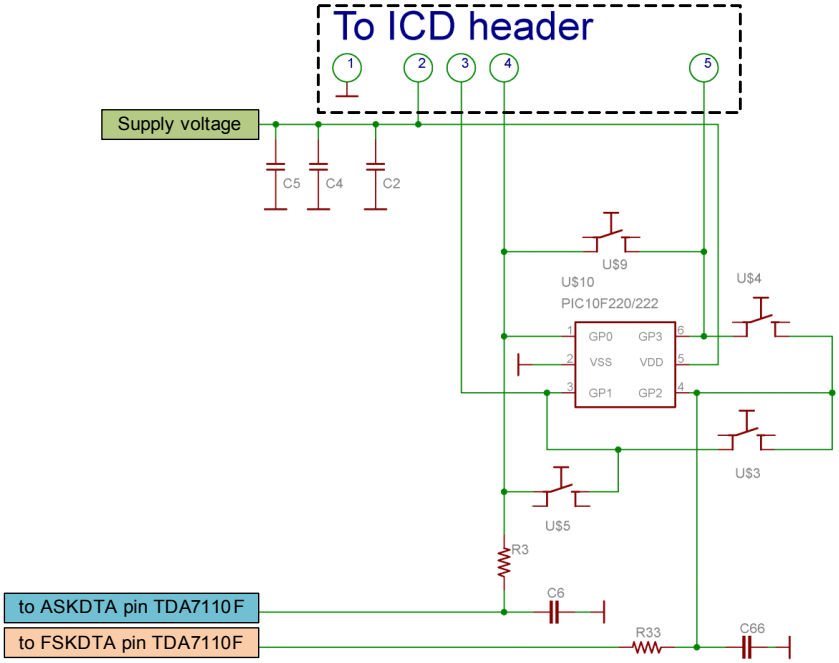


Figure 18 Version of a keyfob with 2 x 2 key scan matrix (RF transmitter not shown in this diagram) The ICD-Header can be used for in-circuit programming and debugging.

3 Modulation parameters and their influence on signal spectrum

Below is an overview on the factors which have major influence on RF performance and spectrum, with emphasis on the parameters which are under the control of the System Designer and Programming Expert. Any knowledge on the relations between parameters which are influencing the signal quality, spectrum and resulting occupied bandwidth may be helpful when performing system design and during firmware development.

If the transmitter is part of an already given system (with predefined transmission parameters as it is the case in this Keyfob project), the modulation and timing parameters are usually given (a priori) and there is little room for change. Nevertheless, even if the modulation type is imposed (ASK or FSK), certain parameters, which can potentially be influenced by design including circuit topology, layout and component value, may have a major impact on regulatory compliance by means of signal spectrum and occupied bandwidth.

3.1 Amplitude shift keying (ASK)

An amplitude modulated signal can be described in time domain as:

$$f(t) = A_c \sin(\omega_c t + \varphi) \times \left(\sum_j A_{mj} \sin(\omega_m t + \theta_m) \right) \quad (3)$$

where A_c is the amplitude of the carrier signal and A_{mj} the amplitude of the modulation signal components.

The modulated signal contains frequency components (denoted tones) which are grouped at multiples of the modulation frequency and centered relative to (around) the f_c carrier frequency as shown in **Figure 19**.
The frequency of those tones, grouped around the carrier is $f_{tj} = (f_c \pm j*f_m)$ where f_m is the modulation frequency and j is the order of the tone. These f_{tj} components are denoted also as sideband components, respectively upper- and lower sideband (USB; LSB), relative to the carrier's frequency (upper sideband if $f_{tj} > f_c$ and lower sideband if $f_{tj} < f_c$).

If the modulating signal is a symmetrical one (for instance a square wave with 50% duty cycle) and if the RF power amplifier is switched on- and off to achieve amplitude modulation of the carrier (i.e. ON/OFF keying, referred also as OOK sometimes) the spectrum of the modulated carrier contains the odd-order modulation tones, as dominants in the upper and lower sidebands.
In other words the energy of the modulated RF-signal is expected to be grouped mainly around the $f_{tj} = [f_c \pm (2j+1)*f_m]$ spectral lines and significantly lower energy in the region of the even-order tones of $f_{tj} = [f_c \pm 2j*f_m]$ frequency shall be expected.

Actually, as both the upper- and lower sidebands are included, this means that the occupied bandwidth (OBW) of an amplitude modulated signal, with modulation depth close to 100% (i.e. generated by switching the RF power amplifier itself or its driver stage ON and OFF) will always be at least twice the equivalent modulation frequency ($OBW > 2\ f_m$).

Note: it is also possible to transmit only one "half" of the spectrum, either the upper- or the lower sideband, if a modulator with special architecture is set up for generation of single-sideband (SSB) signals. Either the upper- or the lower sideband is applied to the RF power amplifier (which shall have a reasonably linear transfer function) whereas the other sideband is rejected. The result is a reduction of the occupied bandwidth and, at the same time, an increase of the energy density in the radiated sideband.
The only drawback of the method is that at the Rx side the regeneration of the suppressed carrier is required for demodulation, which leads to a more complex demodulator structure of the receiver.

If the occupied bandwidth is computed on the inclusion criteria of all the spectral components -20dB below the carrier power (or in-band peak), the 3rd order sideband tones of OOK modulated signal will also be part of this range. Thus, for a given f_m equivalent modulation frequency, the expected value of the occupied bandwidth (OBW) will be as follows:

$$OBW \geq 6 \times f_m \quad (4)$$

As an exemplification for above statements, two spectral plots are represented in **Figure 19**. The blue trace matches a signal spectrum generated by a square-wave modulating signal and a modulation depth close to 100% (i.e. similar to the ON / OFF keying method, referred also as OOK).

The green plot corresponds to the same modulating signal, but with modulation depth reduced to 30%. The signals shown in this example have been generated by a highly accurate RF-signal generator with programmable AM modulation depth, and not a TDA7110F transmitter. The demonstration has been accomplished in order to emphasize the theoretical limitations bound to the occurrence of sidetones and occupied bandwidth.

By comparing the two plots, following conclusions are worth to be remembered:

- if the modulation signal is of a symmetrical waveform, then besides the carrier (f_c) the spectrum is dominated by the odd order sidetones $(2n+1)*f_m$ of the modulating frequency (f_m)
- the even order sidetones $(2n)*f_m$ of the modulating frequency (f_m) decrease rapidly by decreasing modulation depth (observe the blue vs. green plot, especially in the region of the 2nd sidetones)
- if the *-20 dB below peak* criteria is applied and if the modulation method is the ON /OFF keying, then the 3rd order sidetone will fall into the occupied bandwidth
  (observe the two horizontal red lines, one set to carrier peak power and the other -20 dB below)

Note: the other main factor influencing the occupied bandwidth (OBW) is the modulation frequency (f_m), but this, respectively the datarate and encoding method are usually fixed per system definition.

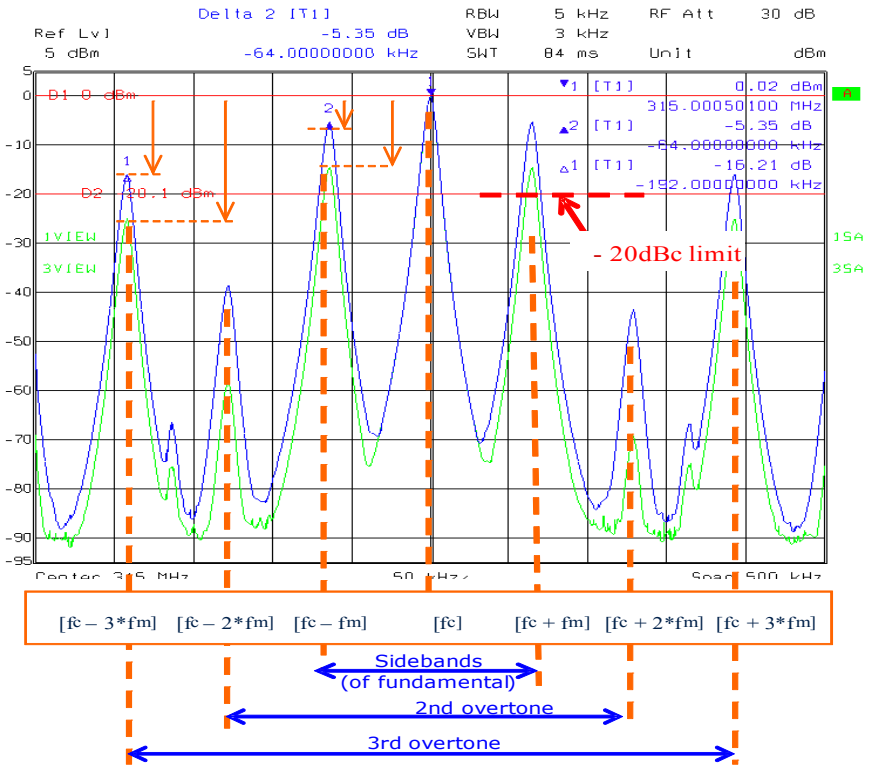


Figure 19 Sideband tones of an AM signal

The AM-modulator in TDA7110F uses the ON / OFF keying method (at RF power amplifier level), yielding a modulation depth of almost 100%. Assuming that ASK modulation is used, the only way to influence the bandwidth and spectrum of the generated RF signal is the ramping of the modulating signal (i.e. a slight decrease of slew-rate and the “rounding” of the leading and trailing edges of the waveform applied to the ASKDATA pin).

The states of the AM modulator are summarized below:

Table 4 ASKDTA - RF power amplifier

ASKDTA (Pin6)	RF power amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

Conclusion

- Judging solely on the usage of the occupied bandwidth criteria of a moderate modulation depth, it seems to have a clear advantage versus the ON/OFF keying method. However, it is worthwhile remembering that if the modulation depth is reduced, the RF-power amplifier will be never be switched off during transmission, thus reducing the efficiency of the DC power usage of the transmitter. Meanwhile, on the receive side, decrease of the peak-to-peak voltage swing on the detector will produce detrimental effects on the data slicer, with potential degradation of the signal-to-noise ratio (S/N).
- However if there is a strong demand for reduction of occupied bandwidth, and the modulation method is AM (ASK) then consider setting the modulation depth to around 70..80%, which might reduce the 3rd order sidetone below the -20 dBc threshold, without significant efficiency degradation.
  Hints regarding this solution are contained in **Reference [4]**.

An efficient way of reducing the spectral splatter caused by the transients (mainly during off-on switching transitions of the RF power amplifier) is the ASK sloping capability.This means that a ramped signal, with moderate slew-rate shall be applied to the modulator (ASKDATA pin) instead of switching ON of the PA by a step-like, digital signal. **Figure 20** illustrates the spectral energy distribution difference between two signals with same nominal power and datarate, both of the aforementioned being generated by ASK modulation. It is clearly visible that provided the use of the power sloping option, the power leaking into adjacent channels shall be significantly lower for the sloped signal towards the 5th order sidetone. In other words, the power sloped ASK signal will generate less interference at frequency offsets larger than [$f_c \pm 3*f_m$] than the unsloped signal.

In order to reduce spectral splatter, it is recommended to implement power sloping in ASK applications, especially if higher data rates are used.

Please consider the items enlisted below:

- A steep rise of the RF power does cause spectral splatter. This is not a chip issue, it is merely a consequence of physical laws.
  The steeper the transition (i.e. as shorter the rise time) the wider the expected bandwidth of the transient.
- Controlled rise of the signal power with moderate slew-rate in case of AM modulation may lead to a moderate increase of jitter by edge detection (in receiver). However, provided the edge detection and window positioning of expected phase transition are handled properly (by Firmware in Host, which will process the received raw data) there will be no sensitivity loss (or just an insignificant degree) on the receive side and, at the same time out-of-band signals (spectral splatter, due to transients) are efficiently minimized on the transmit side.
- As rule of thumb, a moderate ratio (of around 10%) of power sloping is recommended.

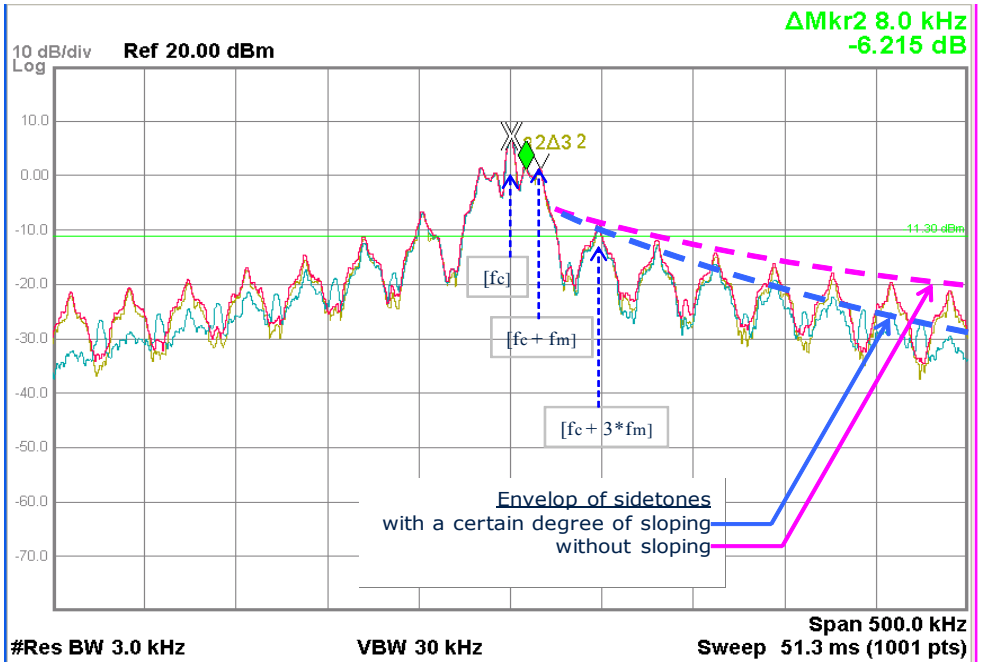


Figure 20 Level of sidebands, ASK signal with and without power ramping

The example shown in **Figure 21** depicts (from left to right) the time domain plot of an unsloped signal, generated by TDA7110F in ASK mode (left side plot), a signal sloped with 10% of bit duration (middle), and a signal sloped with 30% on the right side.

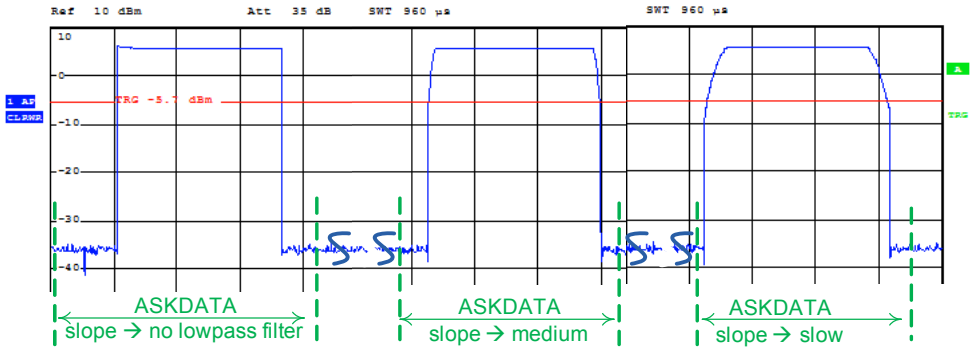


Figure 21 Effect of sloping on signal power (RF-power vs. time)

A simple method for checking the effectiveness of RF-power sloping in terms of spectral splatter is the following:

- Set the center frequency of a spectrum analyzer to carrier frequency of the investigated transmitter.
- Set the frequency span to around 10..15MHz (or both the *Start* and *Stop* frequencies, as their difference yields the *Span*)
- Set the resolution bandwidth (RBW) of the instrument to around 100 kHz (100 kHz is fine for low and medium datarates, higher transmission speeds may require wider RBW)
- Set the video bandwidth to at least 3 times the RBW, to avoid distortion of the detected pulses
- Set a reasonably long sweep time, peak detector mode and maximum hold for the respective trace (MaxHold).
- Observe the “spikes” left and right of the carrier, caused by the RF-power transients (mainly caused by the OFF-->ON transition of the RF carrier). As long as the instrument is in MaxHold mode, from time to time start a new Clear & Record (Write) operation may prove useful, to clear the recorded trace and start a new acquisition.

Recording more traces with the method described and at the same time varying the sloping ratio (the time constant, given by *C6* and *R3*) can deliver fast (but coarse) indication about the effectiveness of a particular setup on the maxima of the expected transients.

The procedure is exemplified in **Figure 22**. In this example the transients in the signal with 10% slope ratio are associated, obviously, with lower amount of spectral splatter as signal generated without sloping control.
For accurate measurements instead of the quick-check described above the method described in the particular *Regulatory Specification* should be used, of course (as per ETSI EN 220-300 for instance).

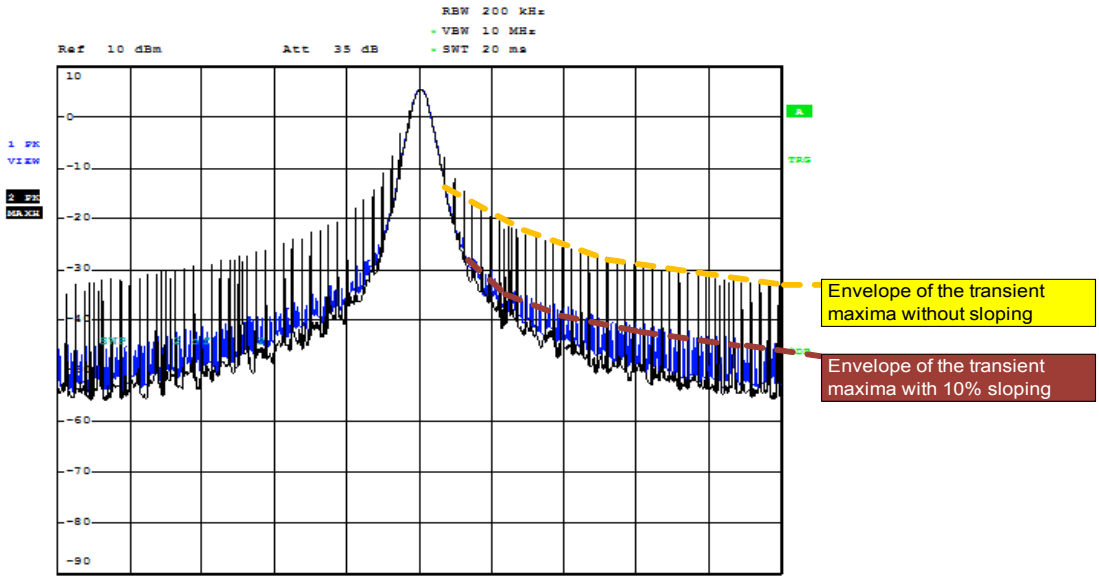


Figure 22 Effect of RF-power sloping on the transients

3.2 Frequency shift keying (FSK)

FSK modulation is achieved by detuning the reference oscillator frequency by a fixed amount. As shown in **Figure 27**, an external capacitor, connected in series with the crystal is either grounded by a chip- internal switch, or if the switch is left open, then the capacitor appears as connected in series with the crystal.

As it can be observed in this figure, the common node of the crystal and frequency-tuning external capacitor is connected over the FSKOUT pin to an internal switch, which at its turn is controlled by the state of the FSK modulator input (i.e. the signal level applied to FSKDTA pin).

The states of the FSK switch are summarized below:

Table 5 FSKDTA - FSK switch

FSKDTA (Pin7)	FSK switch
Low[1)]	CLOSED
Open[2)], High[3)]	OPEN

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

The crystal oscillator operates at around 13.56 MHz, as the crystal frequency is 1/32 of the carrier frequency f_c. The signal generated by the reference oscillator is applied over buffers to the phase comparator and to a 1:16 divider chain. The output of the latter is available at CLKOUT (Pin1), and may be used for synchronization or to drive the clock input of a micro controller (with nominal 847.5 kHz clock frequency, resulting from 13 560 kHz /16).

In FSK modulation mode, the subdivided 847.5 kHz clock is also FM-modulated (in accordance with the bit stream applied to FSKDTA modulator input) but the frequency shift is small and for most applications can be simply disregarded. Assuming ± 44kHz frequency shift for the generated RF signal (in 434 MHz ISM band) the relative "timing- jitter" as it appears at the CLKOUT pin is in magnitude of 2*10(exp -5).

.

If frequency modulation is used (FSK) Carson's bandwidth rule can be applied to define the approximate bandwidth requirements.

This rule is valid for communications system components using frequency modulated carriers modulated by signals which can be regarded as continuous in time domain and having a broader spectrum of frequencies (in frequency domain) rather than a single frequency component. The rule delivers accurate results for occupied bandwidth calculation if the modulating components are sine waves with a well defined upper frequency limit. However, there are certain limitations in bandwidth prediction accuracy if the modulating signal exhibits discontinuities (in time domain) such as a square wave or pulse (i.e. the equivalent Fourier series has a large number of components, or, theoretically speaking, an infinite number).
Nonetheless, due to the simplicity of Carson's bandwidth rule method, it is worthwhile using it for a first, even though coarse approximation of the occupied bandwidth estimate.

More elaborate methods, which take into account the discontinuities in the signal shape, deliver accurate results (i.e. the overtones are being considered, the signal is decomposed in Fourier series for analysis) but the background mathematical apparatus is a more complex one, and as for the computations, it usually requires a dedicated environment (software).

Carson's bandwidth rule is expressed by the relation

$$\mathrm{BWR} = 2 \times (\Delta \mathrm{f} + \mathrm{fm}) \tag{5}$$

where *BWR* is the bandwidth requirement, *Δf* is the peak frequency deviation, and f_m is the highest frequency component in the modulating signal.

For example, an FM signal with 50 kHz peak deviation, and a maximum modulating frequency of 4kHz, would require an approximate bandwidth of 2*(50+4) = 108 kHz as predicted by this estimate.
The maximum modulating frequency shall be computed according to the used encoding scheme.
For instance by NRZ encoding the fundamental frequency is half of the nominal datarate, by Manchester encoding it equals the datarate.

Note: theoretically speaking any frequency modulated signal, generated by an ideal modulator, and steered by a squarewave signal at input shall have an infinite number of sidebands and hence an infinite bandwidth but in practice all significant sideband energy (98% or more) is concentrated within the bandwidth defined by Carson's rule. This may be regarded as a useful approximation, but setting the threshold at 98% (of in-band power) by definition of occupied bandwidth still means that the power outside the band is only about 17 dB less than inside. Therefore Carson's Rule is of little use in spectrum planning, as the limit (maxima) of power falling into adjacent channel(s), allowed by most regulatory standards is well below -17 dBc.

3.3 Comparison of ASK versus FSK signal spectrum. A practical viewpoint.

As emphasized in the introductory part, quite often compatibility with already existing systems is one of the-demands during the design of a new application. In this case practically all the main transmission parameters are set and fixed in advance and there is little room for change.
In contrary, by design of new applications a certain freedom in the transmission parameter choice is given, at least as long as the main criteria are:

- system cost
- reliability
- compliance with regulatory standards (usually region or country specific)

The system designer may face the question -Which is the best datarate choice and the suitable modulation type for the particular application?

As regarded form transmitter side, following aspects shell be taken in account:

- Transmission with low datarate yields narrower occupied bandwidth versus a high datarate transmission, for the same modulation mode. This saves a valuable resource - frequency band occupancy, and yields more margin by compliance with regulatory standards.
- Calculated for the same transmission capacity (expressed in bits/sec) transmission with lower datarate takes longer time, as with high datarate. Consequently, if the transmitter is operating with the same power (assumed not to depending on datarate) the total power consumption of the transmitter is higher for a low datarate system, as it shall stay active for longer time to achieve the same output.
- If several transmitters, with overlapping coverage area are transmitting packets without a time-domain synchronization protocol between the units (as they may belong to different networks or operate in stand-alone mode), the collision probability will increase by increase of transmission time of each individual transmitter

If the transmission parameters are analyzed from the receive site's viewpoint, the following aspects shall be considered

- As a low datarate transmission yields narrower occupied bandwidth (versus a high datarate one), the bandwidth of the intermediate frequency stage (IF) and post-detection filter (or data-filter, at demodulator output) may be reduced as well. Thus a reduction of the in-band noise power will be achieved, leading to better receiver sensitivity (versus a receiver with same gain and noise figure, but wider IF bandwidth).
- As already mentioned by the transmitter analysis, increased datarate would require a shorter active (receive) time for the same transmission capacity (expressed in bits/sec) versus a low-datarate system. Thus the power consumption of the receiver can be reduced by increasing the transmission speed, as the current consumption in active mode is usually much higher (by magnitudes) as the standby or sleep-mode current, drawn by receiver in idle mode.
- Receivers for frequency modulation (FSK) have a clear advantage over those built for amplitude modulation (ASK) in terms of noise immunity (and demodulator gain), as long as the RF or IF carrier to noise power ratio (C/N) does not drop below 6 dB. Below this threshold the peak detector of an AM system performs better (i.e. with better signal-to-noise ratio at the demodulator output) as the ratio detector or discriminator and even the PLL demodulator of an FM receiver.

Clearly, some of the above points are conflicting and a trade-off shell be met, therefore system designers are advised to set clear goals by project definition in terms of

- Link budget (including required or targeted range, Tx power, Rx sensitivity and antenna gain of both sides)
- Energy budget (resulting from weighted sum of active and standby mode currents in the system)
- In case of battery operated applications (as this Keyfob project) the decrease of available voltage over the battery lifetime and an increase of the internal resistance, this latter limiting the maximum current, which can be drained from battery before the minima of the system's supply voltage is reached. It is worth to note that the battery voltage is also temperature dependent. The documents **[1]** and **[10]** in **References** give a detailed description of different battery types and ageing dependent behavior.

As regarding the choice weather ASK or FSK may suite better a particular application, it is worth to note that there are significant differences in the spectrum of two carriers, one generated by AM modulator and the other by FM, even if the power of the unmodulated carrier would be the same.

In **Figure 23** the spectral plots of three signals are shown

- unmodulated carrier (CW) represented by the yellow plot
- the same carrier, but frequency modulated, with + 65 kHz frequency shift by an unshaped (square-wave) signal corresponding to Manchester encoded 9600 bit/sec data stream is plotted in light-blue
- again the same carrier, but amplitude modulated, with 100% modulation depth, by an unshaped (square-wave) signal corresponding to Manchester encoded 9600 bit/sec data stream is plotted in magenta

The plots have been recorded with the detector of the spectrum analyzer set to maximum hold mode (MaxHold) and a resolution bandwidth (RBW) wide enough not to show the individual spectral components, but sufficiently narrow to avoid significant distortion of the envelope's shape.

*Note: the fundamental frequency, equivalent with a Manchester-encoded signal of 9600 bit/sec is of 9.6 kHz. As the waveform is symmetrical (50% duty-cycle), sidetones with significant energy are expected at + (2n+1) * 9.6 kHz frequency offset, relative to the carrier.*

Measurements with the above listed instrument settings (trace MaxHold and 20 kHz RBW) yield envelope curves tangent to the peak values of the individual spectral components, in other words a worst case scenario, but close to the method the two widespread regulatory systems (ETSI EN 220-300 and FCC Part 15D) do use for measurement of out of band emissions.

Note: An instrument-grade RF generator have been used as signal source during the test, to keep distortions and intermodulation products at low level.

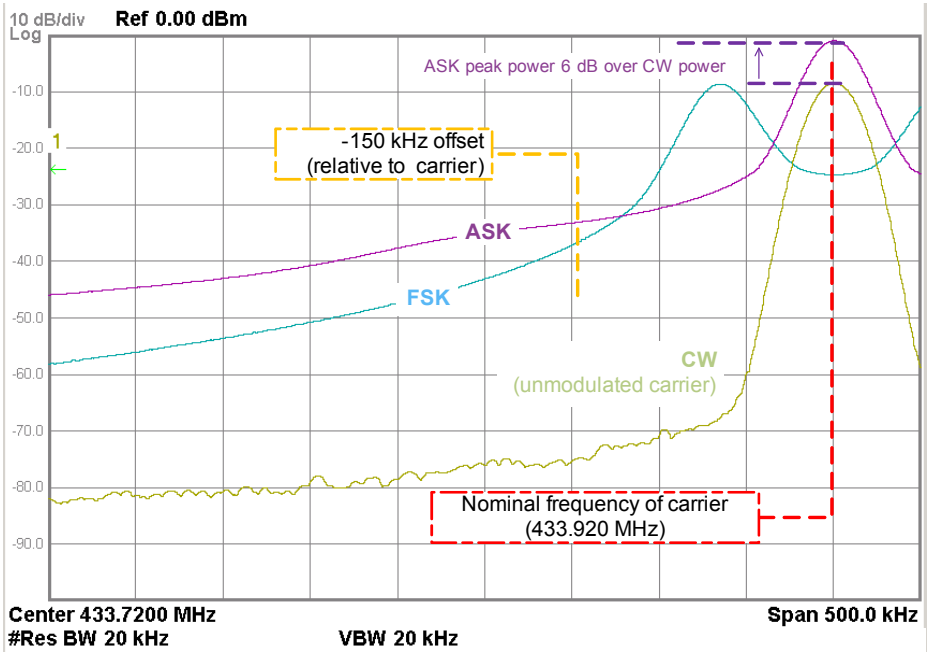


Figure 23 Occupied bandwidth of ASK and FSK signals for the same encoding scheme and equal datarate. Only the lower sideband is shown in this figure (as the two sidebands are expected to be symmetrical relative to carrier frequency).

Considering the results of above described test, following conclusions may be drawn:

- amplitude shift keying (ASK) concentrates significant amount of energy close to the carrier (i.e in the low order sidetones). The peak power of the ASK signal is exceeding by +6dB the power of the CW carrier.
- the amplitude of the high-order sidetones decreases by increasing frequency offset (relative to carrier), but the steepness of sidetone peak amplitude vs. frequency offset function is moderate above the 7th sidetone, assuming the modulation depth is 100% or close to this value (i.e. if ON-OFF keying is used). However, if the modulation depth is reduced to around 70..80%, the amplitude of high-order sidetones decreases faster (see **Figure 19** for relevant data) but the price for this enhancement is a certain increase in current consumption (mainly for the RF power amplifier).
- In conclusion ASK is at best suitable for low- or moderate speed transmissions.
  Power "leaking" into adjacent channels have to be considered, and if required, signal shaping applied.

- frequency shift keying (FSK) is characterized by two power peaks, placed under- and over the carrier frequency, at offsets equaling the positive and negative frequency shift values.

- if the modulation index is of a moderate value (3..5), by frequency offsets (relative to carrier) exceeding the double of the frequency shift value, the envelope, tangent to peak of the individual spectral lines decreases faster as by ASK modulation (for instance on left side of **Figure 23**, by frequency offsets exceeding 150 kHz). Assuming that the transmitter is modulated by a Manchester-encoded, 20 kbit/sec data stream and that the frequency shift, measured on RF carrier is 65 kHz yield a modulation index of 3,25 (65 / 20).
- In conclusion FSK modulation is more efficient, in terms of spectrum usage for medium and high datarates, but there are no other disadvantages (beyond a wider occupied bandwidth) to be used for low datarate transmissions as well.

Attention: at first glance the reduction of modulation index may appear as a straightforward way toward reduction of the occupied bandwidth. However, low modulation index values have an adverse effect on demodulator gain (in receiver), therefore users are advised to keep the value between 3 and 5.

*Note: assuming the crystal's parameters are known in advance, the amount of frequency shift, at reference frequency level can be set by proper choice of the load capacitors value (C11 and C12, see **Figure 4**). As explained in **Chapter 2.1**, the frequency of the RF carrier is 32 times the reference frequency. Due to the inherent nature of the PLL, the frequency shift of the reference is also multiplied by 32 (as long as the bitrate of the modulation signal does not exceed the maxima specified in the TDA7110F Datasheet). Consequently the effective frequency shift, referred to RF carrier is 32 times the shift of the reference frequency.*

The results of occupied bandwidth measurement (OBW) are summarized below for the following test cases:

- two different bitrates, 2400 bit/sec, respectively 9600 bit/sec
- ASK and FSK modulation modes
- Manchester encoding (by all test cases)

*Note: for occupied bandwidth calculation the 99% in-band energy (of the total power) criteria have been used during the tests summarized in **Table 6**. As previously emphasized, different regulatory specifications may use other (usually more restrictive) maxima values for out of band and unwanted emissions. The compliance test shell be done as imposed by the specific regulation(s).*

Table 6 Modulation Modes and Occupied Bandwidth summary

Datarate [bit/sec]	Modulation mode	Occupied bandwidth [kHz]	Note
2400[1)]	ASK	70	Modulation depth 100%
	FSK	140	Frequency shift ±40 kHz
9600[2)]	ASK	105	Modulation depth 100%
	FSK	210	Frequency shift ±65 kHz

1) Manchester encoded stream, 50% duty cycle symmetrical waveform, no shaping (low pass filter) on modulator input

2) Manchester encoded, 50% duty cycle symmetrical waveform, no shaping /power ramping

3.4 ASK/FSK modulator and power control in TDA7110F

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin10).

If the bias circuitry is powered up, the ASKDTA pin is pulled up internally.

Forcing the voltage at the pins low overrides the internally set state.

The block diagram of the modulator is shown in **Figure 24**.

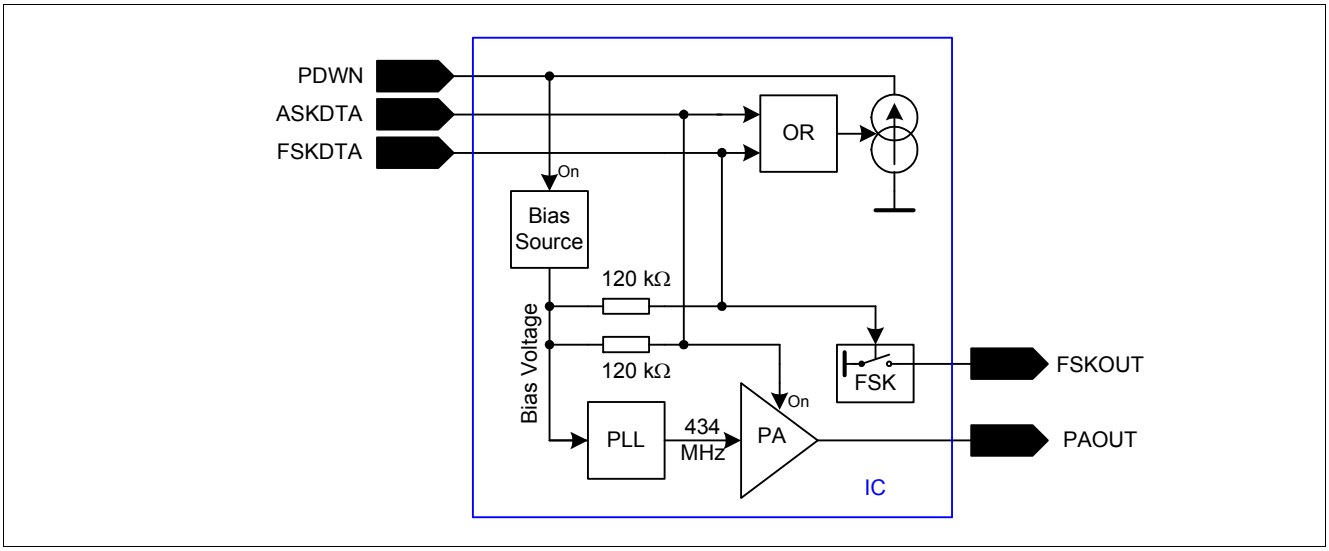


Figure 24 TDA7110F modulator and power control, block diagram

Table 7 provides a listing of TDA7110F's powering states.

Table 7 Power Modes

PDWN	FSKDTA	ASKDTA	MODE
Low[1)]	Low, Open	Low, Open	POWER DOWN
Open[2)]	Low	Low	
High[3)]	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low: Voltage at pin < 0.7 V (PDWN),
Voltage at pin < 0.5 V (ASKDTA; FSKDATA)

2) Open: Pin open

3) High: Voltage at pin > 1.5 V

Attention: Other combinations for the state of the control pins PDWN; FSKDATA; ASKDTA are not recommended

To avoid spurious radiation and spectral splatter it is strongly recommended to switch not directly from PDWN-mode to TRANSMIT-mode, but first to PLL-ENABLE-mode and start the transmission with a small delay, to make sure that

- the reference oscillator's startup time and
- PLL settling time (i.e. the time needed by PLL to "lock" on the reference oscillator's frequency)

elapsed, either like shown in **Figure 25** for ASK transmissions or, if FSK transmission mode shall be used, than according to a timing diagram similar to that shown in **Figure 26**.

Note: the oscillator startup time is expected in the 0.6..2msec range, the PLL lock time is typical below 0.1 msec

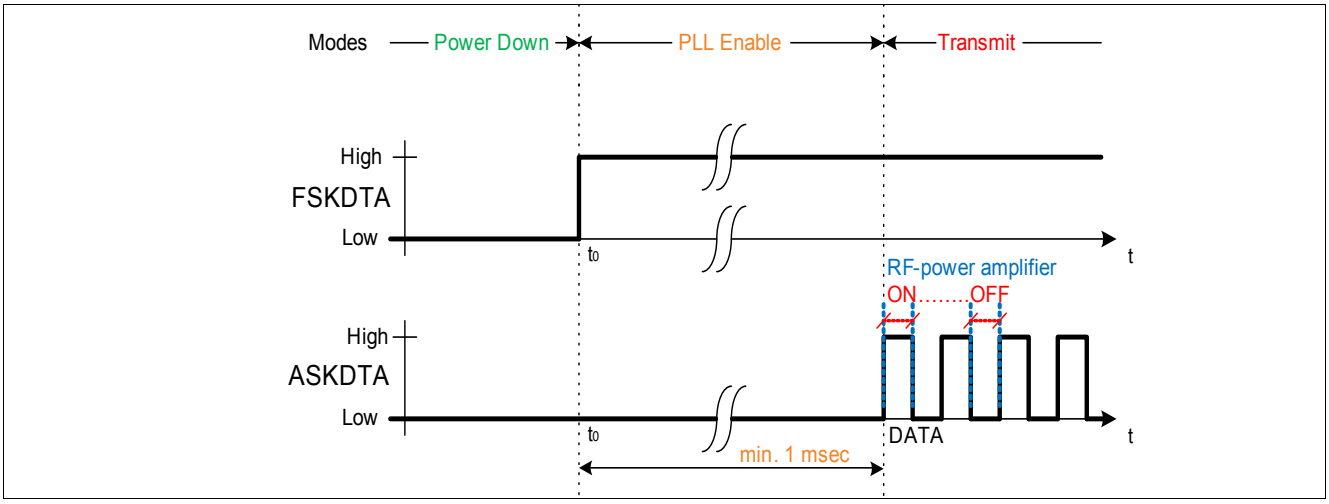


Figure 25 Timing of PLL activation and starting a transmission in ASK Mode

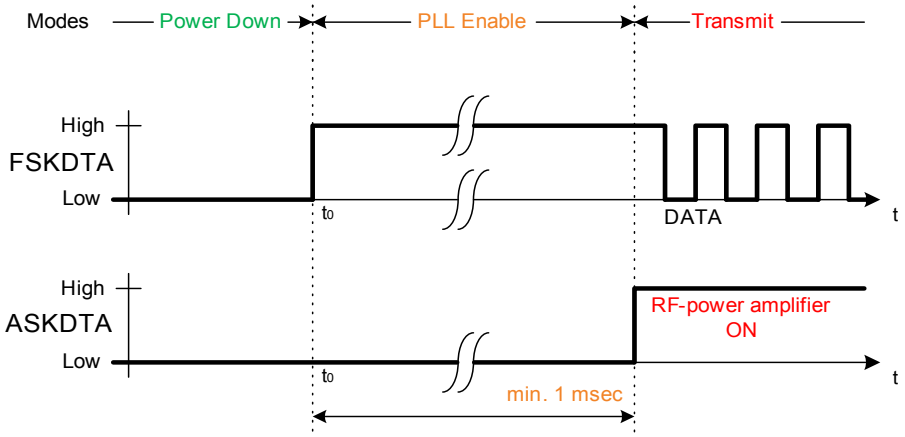


Figure 26 Timing of PLL activation and transmission in FSK Mode

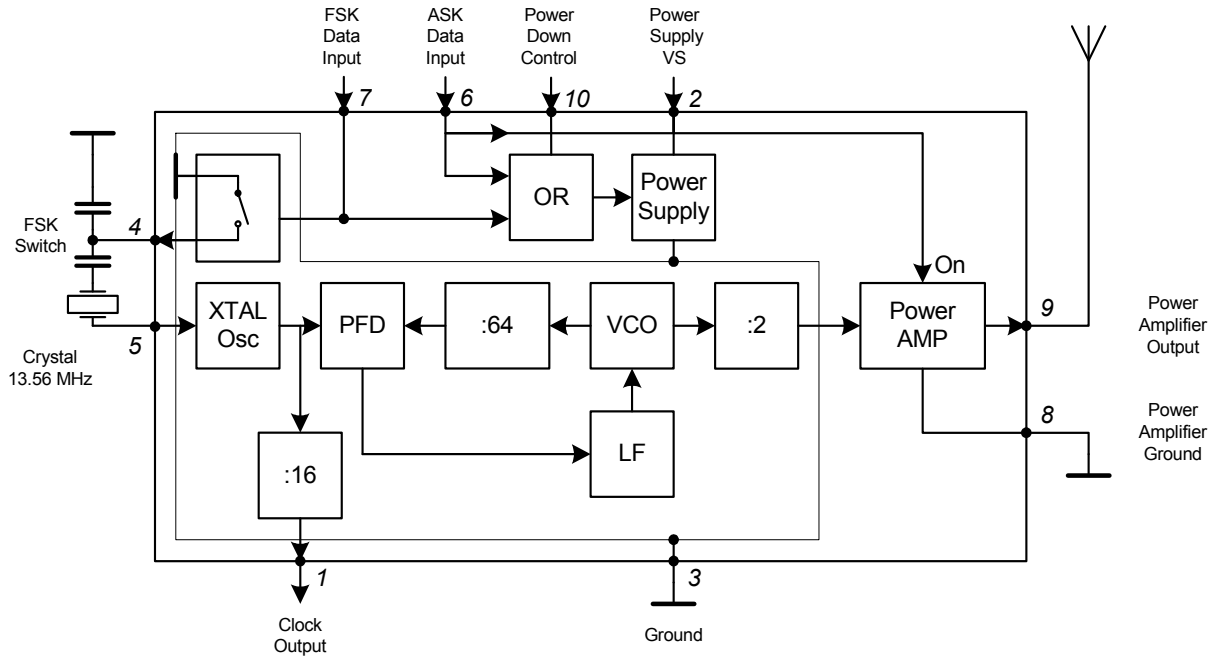


Figure 27 Block diagram of the TDA7110F transmitter

4 Debug techniques

Please, find below some hints for system verification, as well as suggestions for an efficient code debugging sequence. If the code (executed by µC) malfunctions or the transmitter does not work as expected, at first try to identify and understand the root cause. Some of the most frequent reasons are as follows:

- Inconsistent code
- Some “gaps” in understanding and / or interpretation of transmitter’s functions or microcontroller instruction set.

The µC code itself can be quickly debugged if established (and well-known) procedures are used. Debugging usually begins by setting breakpoint(s) and allocation of trace files to code segments (tracking of I/O pin state changes and register values). This is more efficient and less time consuming as a series of “crash and relaunch” trials.

For a better understanding of the TDA7110F transmitter structure (at least at block diagram level) and control functions, please refer to ***TDA7110F Datasheet***.

If systematic code malfunction occurs, an efficient method, especially for those familiar with hardware debugging methods is to “watch” the microcontroller’s special function registers (SFRs) and backtrace the transferred data.

This procedure is especially useful if there are doubts about data integrity, or there are suspicions that glitches (which are short on absolute scale and random, but long enough to be interpreted by the microcontroller as pin-change transitions) have falsely triggered the system. Usually glitches occur due to crosstalk in the host system or as a consequence of insufficient supply line decoupling.

To trace the transmitted data over an RF-link a receiver tuned on the TX-channel frequency is sufficient or a spectrum analyzer, with center frequency set properly (to Tx-channel nominal value), resolution bandwidth (RBW) and video bandwidth (VBW) of the instrument set to 100..500 kHz and frequency span vernier to Zero Span.
If the analyzer is triggered on the RF-carrier level (-50 dBm in example below) the signal looks like in **Figure 28**.

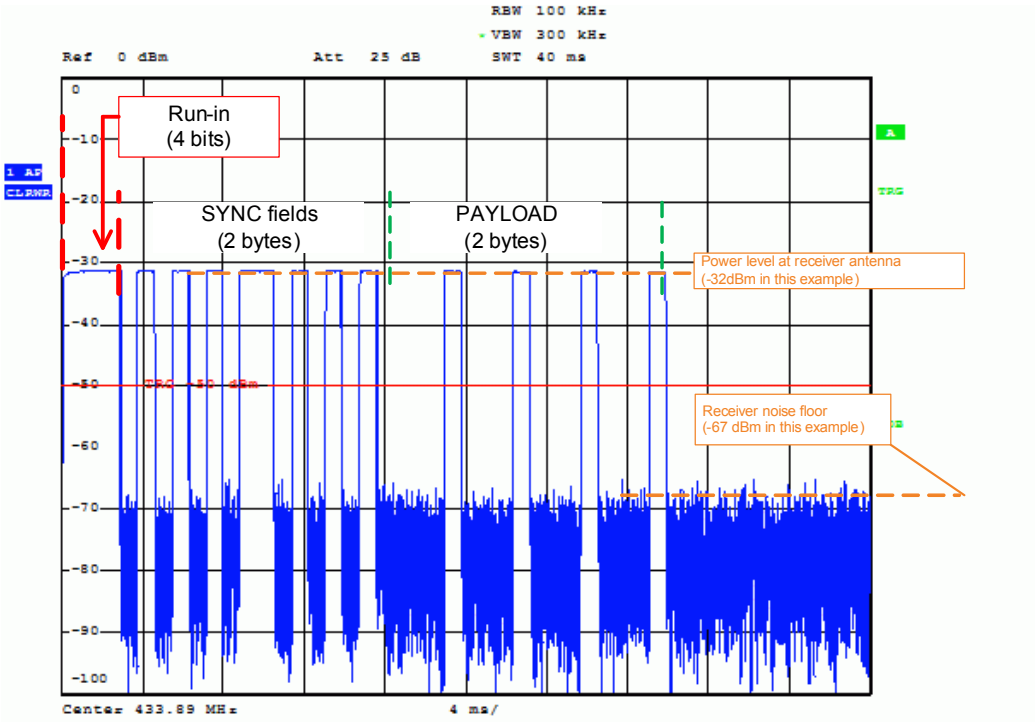


Figure 28 ASK frame, as received and demodulated by a Spectrum Analyzer.As the frequency span is set to zero (during this test), thus the signal is displayed in time-domain (instead of frequency domain representation - the “default” operating mode of Spectrum Analyzers).

5 Appendix

5.1 Simple example code implementing Keyfob functions

The example listed below serves as example for the implementation of a 2-key simple Keyfob, based on TDA7110F transmitter and a PIC10F220 /10F222 microcontroller. The frame and payload structure could be easily adapted to other, customer specific formats.

Transmission parameters are:

- NRZ encoding
- ASK modulation scheme
- Datarate 1200 sym/sec
- Frame with 4 bits lead-in, 2 bytes preamble and 2 bytes payload
- Transmitter is powered down after frame transmission, the uC put in sleep mode, waiting for key activation

```
;(C) Infineon Technologies AG, 2012
;             LIST   P=10F222
#include <P10F222.inc> ; processor specific variable definitions
errorlevel  -302 ; suppress message 302 from list file
__CONFIG   _CP_OFF & _MCLRE_OFF & _WDT_OFF & _IOSCFS_4MHZ
; '__CONFIG' directive is used to embed configuration word within .asm file.
; The lables following the directive are located in the respective .inc file.
; See data sheet for additional information on configuration word settings.

;(C) Infineon Technologies AG, 2010
;************************** DEFINE STATEMENTS *********************************
;; pin definitions
#define ASKDATA        GPIO,0
#define POWERON         GPIO,2
#define KEY1        GPIO,1 ;keyboard switch #1
#define KEY2        GPIO,3 ;keyboard switch #

;registers
#define PORTCONFIG b'00001010'; mask for configuring I/O ports, GPIO1 & 3 input,
GPIO2 &0 output
#define ADCONFIG 0x00 ; A/D converter config. bits and STOP/GO ctrl.

;flags
#define WAKEUP STATUS,GPWUF ;Wakeup flag set if wakeup from SLEEP due to pin change

;parameters
#define DCOUNT 10xaa ;delay #1, only for test phase
#define DCOUNT2 0x02;delay #2,  only for test phase
```

```
#define BT 0xCD ;bit cell duration for 1200 bit/sec  (may need adjustment if the
oscillator is trimmed !)

#define SYNC#1 0x55 ;sync pattern #1
#define SYNC#2 0xAA ;sync pattern #2

;General Puropse Registers (GPR) used for parameter/variable storage
#define PAYLOAD1 0x10 ;gen. register for payload storage,  address of 1st GPR
#define PAYLOAD2 PAYLOAD1 + 1 ;gen. register for payload storage
#define TEMP PAYLOAD2 + 1 ;temp. storage for transmitted byte

#define COUNTER1 TEMP + 1 ;delay counter #1 (inner loop)
#define COUNTER2 COUNTER1 + 1 ;delay counter #2 (outer loop)
#define BITTIME COUNTER2 + 1 ;bit cell duration

;#define SHUTDOWNACTIVE Flag,0
;#define POTSTATE Flag,1

;****************************** START OF CODE *********************************
        org 0x00
        movlw 0x12 ;****** REMOVE THIS LINE FOR PRODUCTION ******
; movlw 0x01 ; use for measurement of oscillator center frequency,
; pin GP2 will output a signal with  f_osc/4 frequency if LSB in OSCCAL is set
        movwf OSCCAL ;load the factory oscillator calibration value
;******************************************************************************
; Check if power-on Reset or Wakeup event?
        btfsc WAKEUP
        goto SCAN ;Flag set --> wakeup event --> find out which key is depressed?
;******************************************************************************
; InitializeSFRs - Initialize Special Function Registers
;
;******************************************************************************
InitializeSFRs
        movlw 0x07 ; OPTION register configuration, wakeup on pin-change enabled
;weak pullups enebled (GP1 & GP3)
;0xC7 for no pullups, no weakup on pin change
        option

        movlw PORTCONFIG ;configure GPIO1 & 3 input, GPIO2 &0 output
        tris GPIO        ;validate GPIO configuration
```

```
        movlw ADCONFIG ;configure A/D inputs and converter
        movwf ADCON0 ;stop A/D

        movlw b'00000000' ; set for no-transmit, both outputs LOW
        movwf GPIO

;*****************************************************************************
; Initialize Program Variables
;
;*****************************************************************************
        movlw 0x11 ;0x11 is just  a dummy value, for test
        movwf PAYLOAD1 ;just  for test, delete in final version
        movwf PAYLOAD2 ;just  for test,  delete in final version
;*****************************************************************************
; Initialization done, read the keyboard input buffer and go to SLEEP Mode

;*****************************************************************************
        movf        GPIO,0 ;read the input keys, update the input latch content
        sleep


;*****************************************************************************
; Main program loop
;
;*****************************************************************************
SCAN        bcf WAKEUP ;clear the wakeup event flag
        movf GPIO,0 ;read the input keys, update the input latch content

        movlw 0x11 ;0x11 is just  a dummy value, for test
        movwf PAYLOAD1 ;just  for test, delete in final version
        movwf PAYLOAD2 ;just  for test,  delete in final version

;transmit the full frame
FRAME        bsf POWERON ;switch ON  the transmitter
        call GAP ;send a short CW signal allowing receiver RSSI to pull in
        movlw SYNC#1 ;send SYNC byte #1
        movwf TEMP
        call SEND

        movlw SYNC#2 ;send SYNC byte #2
        movwf TEMP
        call SEND
```

```
        movf PAYLOAD1,0 ;send PAYLOAD byte#1
        movwf TEMP
        call SEND

        movf PAYLOAD2,0 ;send PAYLOAD byte#2
        movwf TEMP
        call SEND

        bcf POWERON ;
        call LONGBRAKE ;JUST FOR TEST
;        goto FRAME ;JUST FOR TEST
;Frame transmitted, prepare for next keystroke and goto SLEEP
        movf GPIO,0 ;read the input keys, update the input latch content
        sleep

;_____________
;Subroutines, small chunks of code for test (see also flowchart in Firmware
Documentation)

SEND call BIT ;sends the byte stored in TEMP in the MSB...LSB sequence (1st MSB and
last LSB)
                call BIT ;send bit 6
                call BIT
                call BIT
                call BIT
                call BIT
                call BIT
                call BIT ;send bit 0
                retlw 0

GAP               movlw 0xf0 ;preamble, 4 bits of HIGH
                movwf TEMP ;stored in same register as "bytes to send"
                call BIT
                call BIT
                call BIT
                call BIT
                retlw 0
BIT               btfsc TEMP,7
                goto CONT1
                bcf ASKDATA
                goto CONT2
```

```
CONT1                bsf ASKDATA
CONT2                rlf TEMP,1 ;send MSB then shift toward LSB

                movlw BT ;ASKDATA level is set, now wait until end of bit cell
; (for  NRZ, or half cell for Manchester)
                movwf BITTIME
CONT3 nop ; a few NOPs to trim the delay loop
                decfsz BITTIME,1 ;decrease counter until 0
                goto CONT3
                retlw 0
; a long delay, just for test phase
LONGBRAKE clrf TEMP
                movlw DCOUNT2        ;initialize outer loop counter
                movwf COUNTER2
LG0 movlw DCOUNT1 ;initialize inner loop counter
                movwf COUNTER1
LG1 decfsz COUNTER2,1
                goto LG2 ;continue  if COUNTER2 <>0
                retlw 0
LG2 decfsz COUNTER1,1
                goto LG2
                goto LG0
END ; 'end of program'directive
```

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