

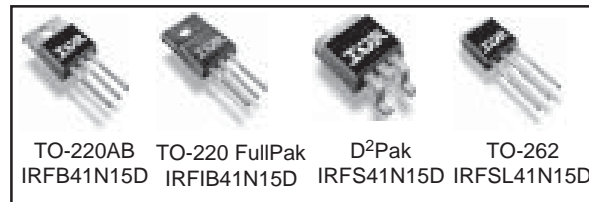
**Applications**

- High frequency DC-DC converters

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective  $C_{OSS}$  to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

<b><math>V_{DSS}</math></b>	<b><math>R_{DS(on)}</math> max</b>	<b><math>I_D</math></b>
<b>150V</b>	<b>0.045<math>\Omega</math></b>	<b>41A</b>



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	41	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	29	
$I_{DM}$	Pulsed Drain Current ①	164	
$P_D$ @ $T_A = 25^\circ\text{C}$	Power Dissipation, D <sup>2</sup> Pak	3.1	W
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation, TO-220	200	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation, Fullpak	48	
	Linear Derating Factor, TO-220	1.3	W/ $^\circ\text{C}$
	Linear Derating Factor, Fullpak	0.32	
$V_{GS}$	Gate-to-Source Voltage	$\pm 30$	V
dv/dt	Peak Diode Recovery dv/dt ③	2.7	V/ns
$T_J$	Operating Junction and	-55 to + 175	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lb•in)

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	$^\circ\text{C/W}$
$R_{\theta JC}$	Junction-to-Case, Fullpak	—	3.14	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑥	—	62	
$R_{\theta JA}$	Junction-to-Ambient, D <sup>2</sup> Pak ⑦	—	40	
$R_{\theta JA}$	Junction-to-Ambient, Fullpak	—	65	

Notes ① through ⑦ are on page 12

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# IRFB/IRFIB/IRFS/IRFSL41N15D

International  
IR Rectifier

## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.17	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.045	$\Omega$	$V_{GS} = 10V, I_D = 25A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 120V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

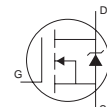
	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	18	—	—	S	$V_{DS} = 50V, I_D = 25A$
$Q_g$	Total Gate Charge	—	72	110	nC	$I_D = 25A$ $V_{DS} = 120V$ $V_{GS} = 10V$ ④
$Q_{gs}$	Gate-to-Source Charge	—	21	31		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	35	52		
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$V_{DD} = 75V$ $I_D = 25A$ $R_G = 2.5\Omega$ $V_{GS} = 10V$ ④
$t_r$	Rise Time	—	63	—		
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		
$t_f$	Fall Time	—	14	—		
$C_{iss}$	Input Capacitance	—	2520	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 120V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑤
$C_{oss}$	Output Capacitance	—	510	—		
$C_{rss}$	Reverse Transfer Capacitance	—	110	—		
$C_{oss}$	Output Capacitance	—	3090	—		
$C_{oss}$	Output Capacitance	—	230	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	250	—		

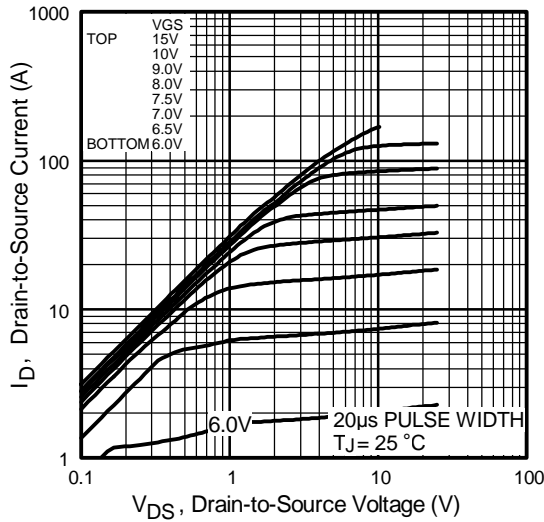
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	470	mJ
$I_{AR}$	Avalanche Current ①	—	25	A
$E_{AR}$	Repetitive Avalanche Energy ①	—	20	mJ

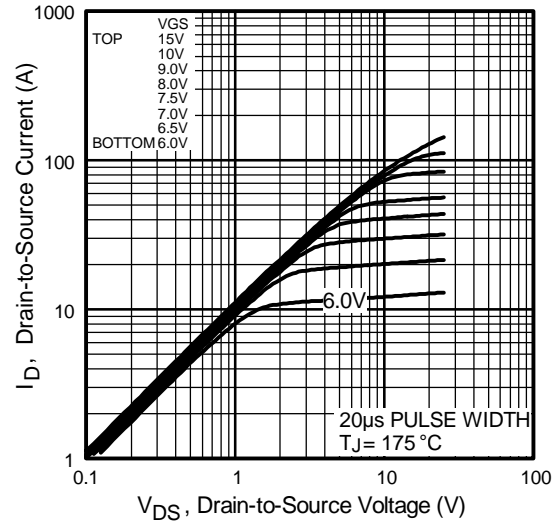
## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	41	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	164		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	170	260	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
$Q_{rr}$	Reverse Recovery Charge	—	1.3	1.9	$\mu C$	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

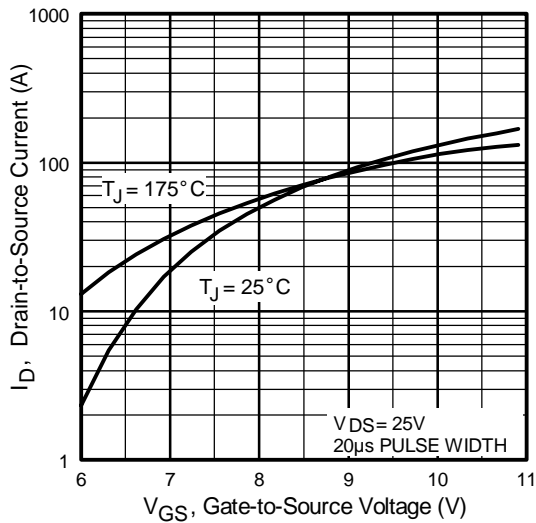




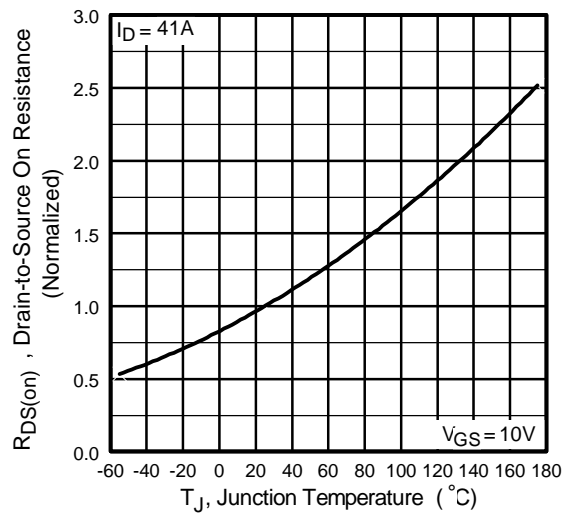
**Fig 1.** Typical Output Characteristics



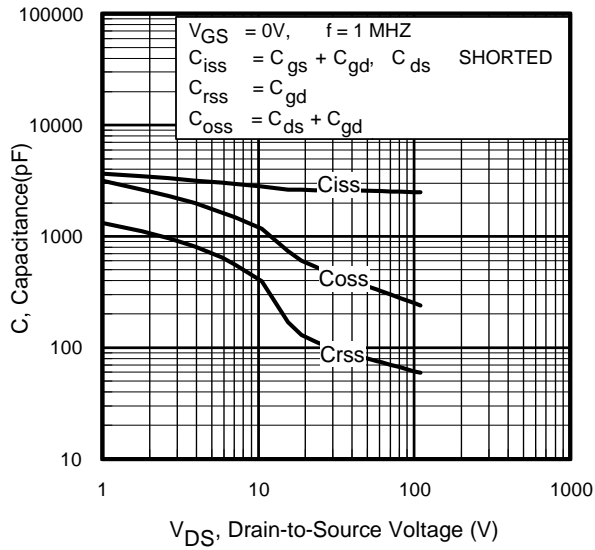
**Fig 2.** Typical Output Characteristics



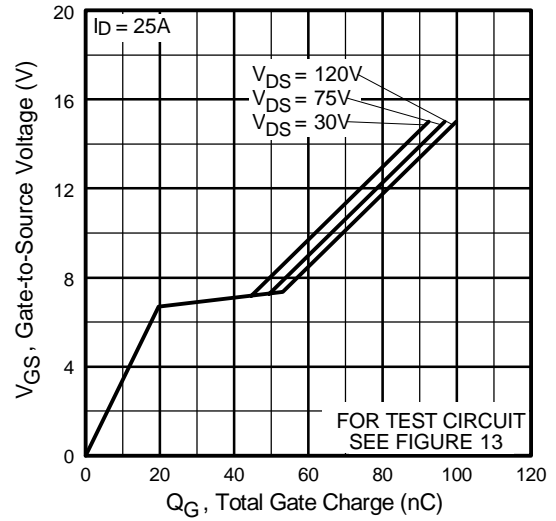
**Fig 3.** Typical Transfer Characteristics



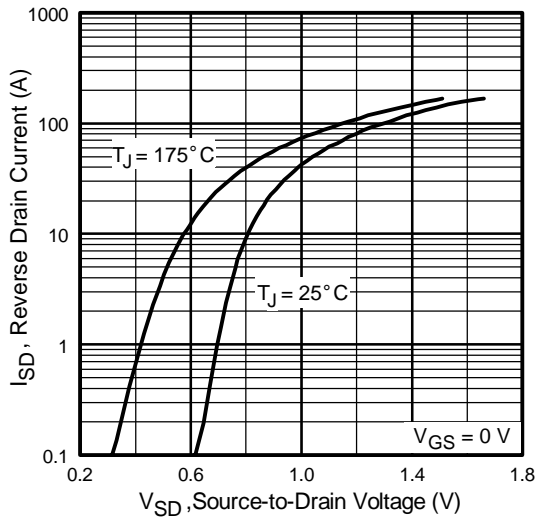
**Fig 4.** Normalized On-Resistance vs. Temperature



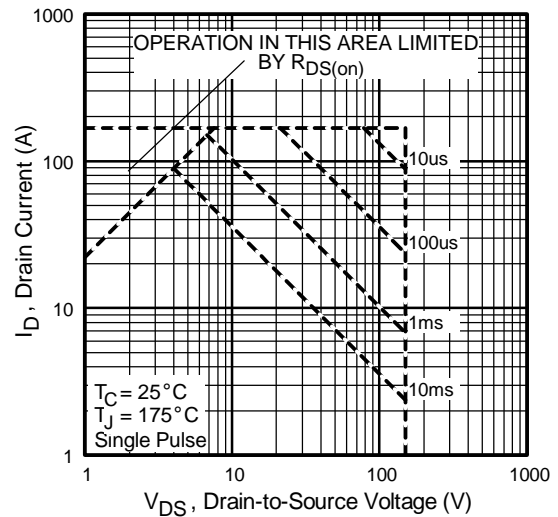
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



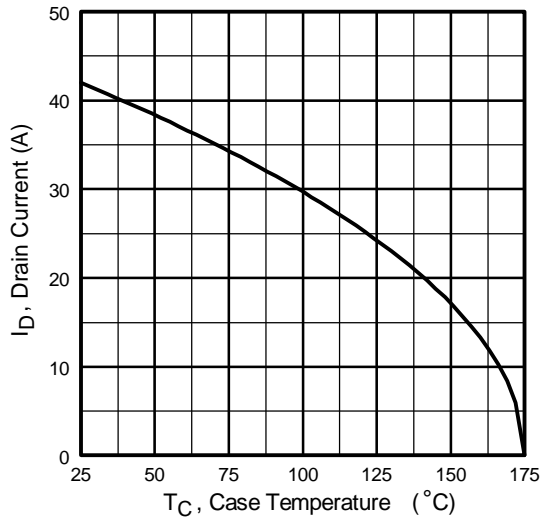
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



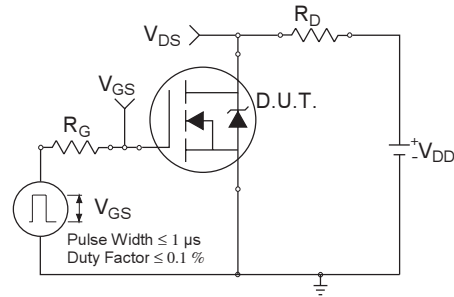
**Fig 7.** Typical Source-Drain Diode Forward Voltage



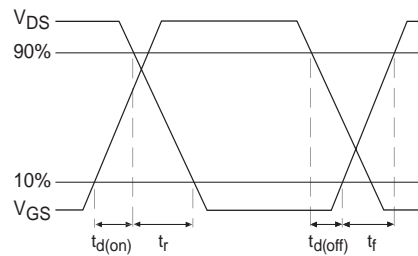
**Fig 8.** Maximum Safe Operating Area



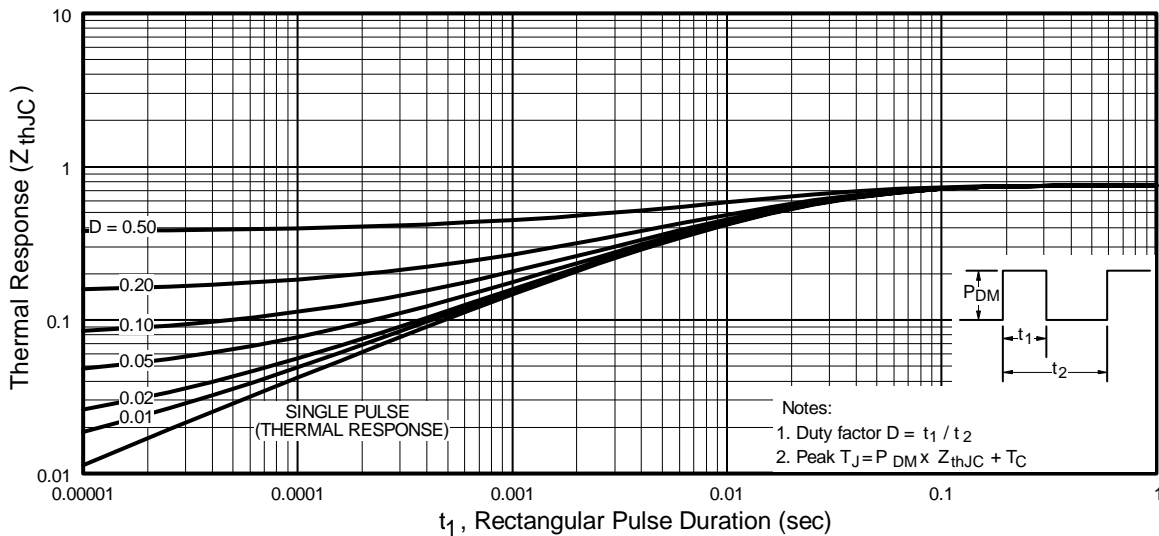
**Fig 9.** Maximum Drain Current Vs. Case Temperature



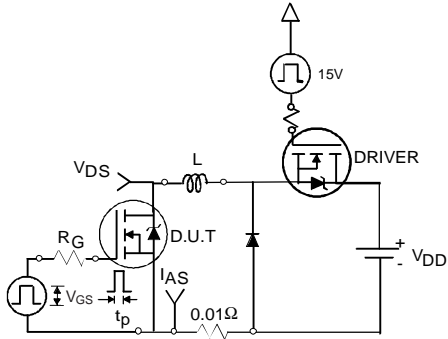
**Fig 10a.** Switching Time Test Circuit



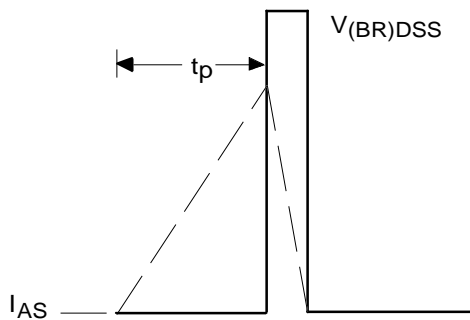
**Fig 10b.** Switching Time Waveforms



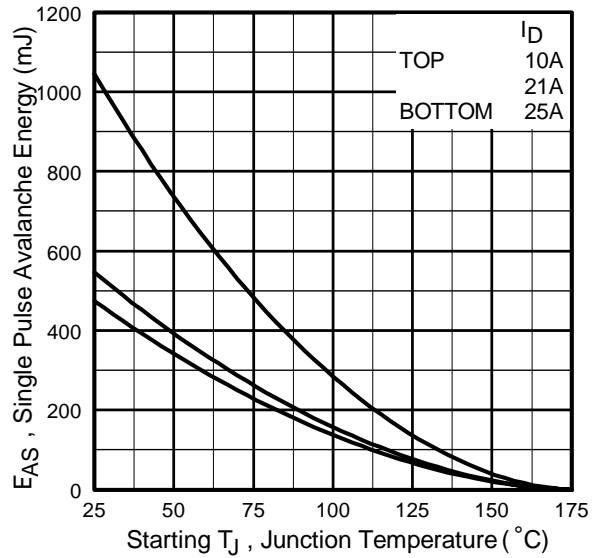
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



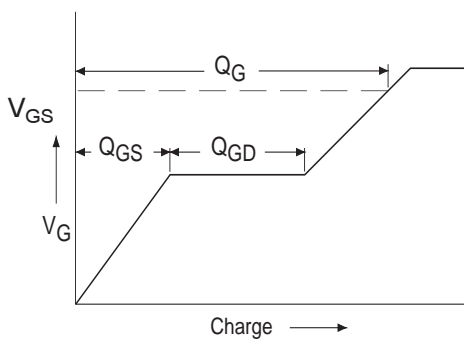
**Fig 12a.** Unclamped Inductive Test Circuit



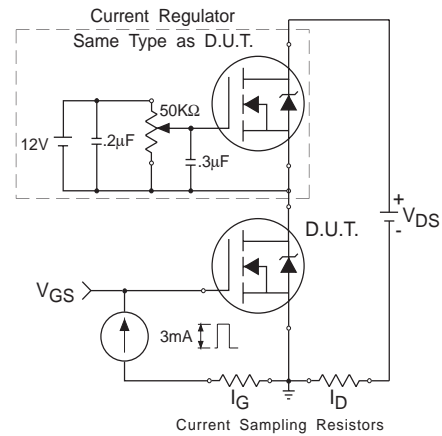
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

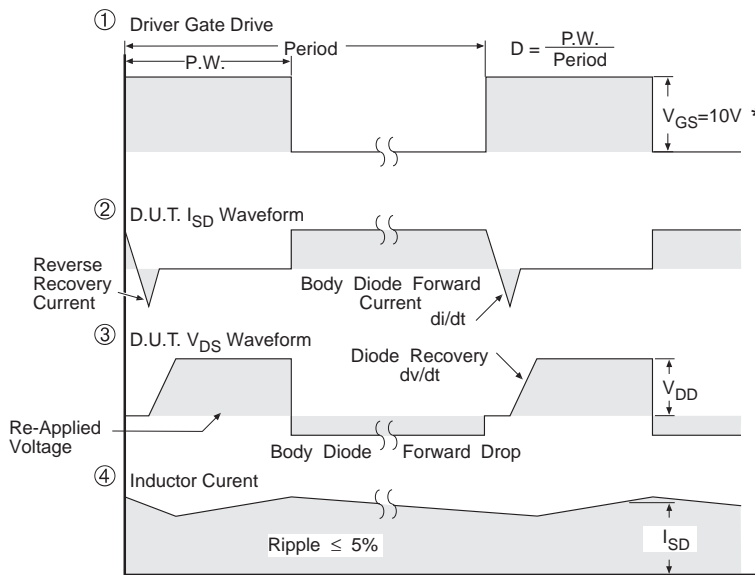
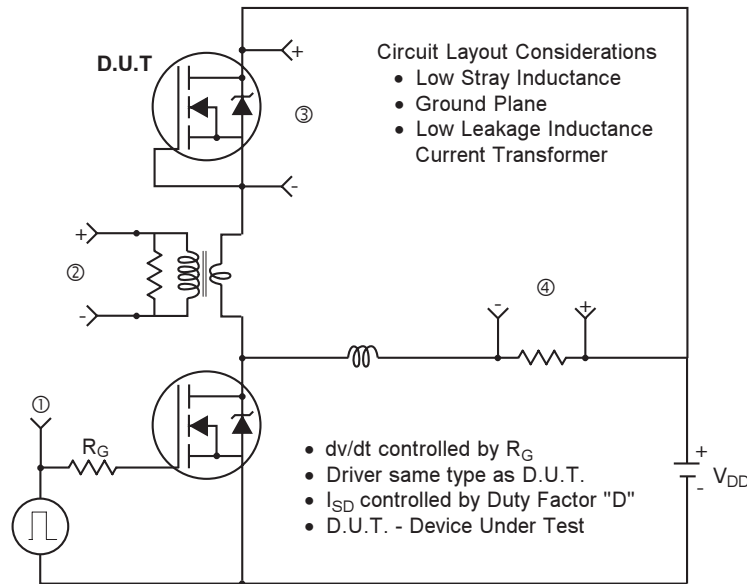


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

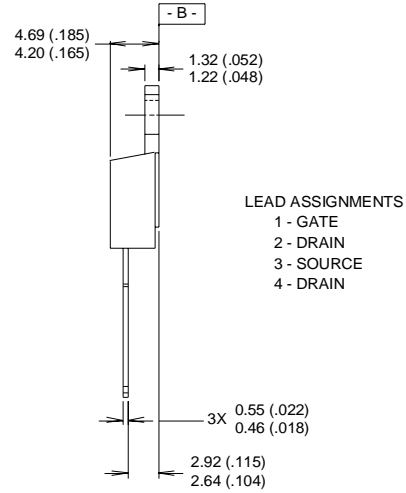
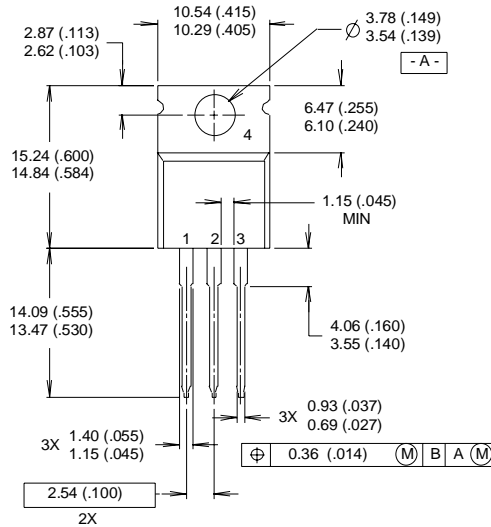
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRFB/IRFIB/IRFS/IRFSL41N15D

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## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



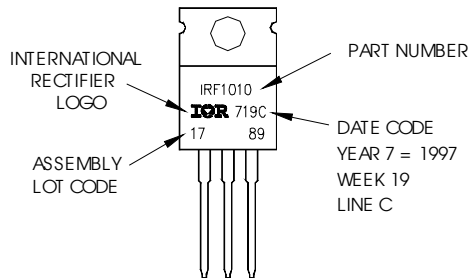
**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

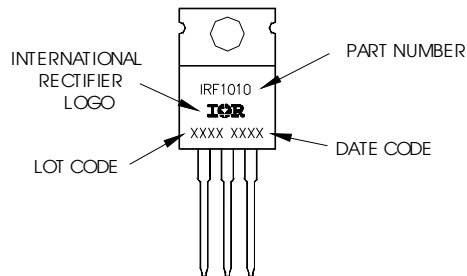
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



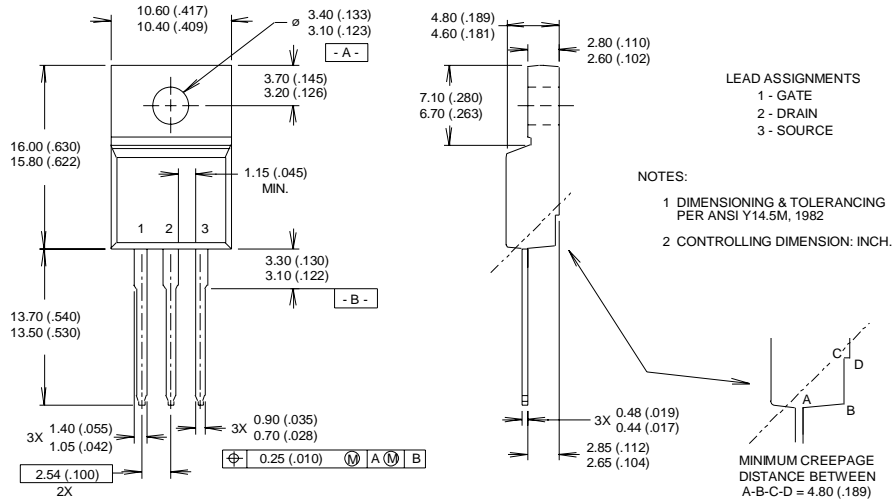
For GB Production  
 EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"





## TO-220 Full-Pak Package Outline

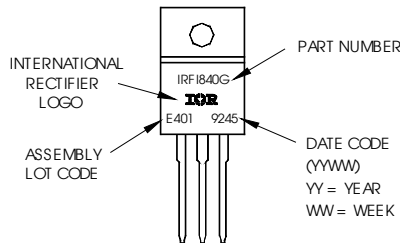
Dimensions are shown in millimeters (inches)



## TO-220 Full-Pak Part Marking Information

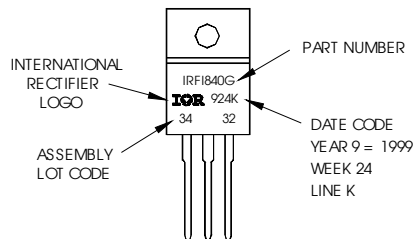
Notes: This part marking information applies to all devices produced before 02/26/2001 and currently for parts manufactured in GB.

EXAMPLE: THIS IS AN IRF1840G  
 WITH ASSEMBLY  
 LOT CODE E401



Notes: This part marking information applies to devices produced after 02/26/2001 in location other than GB.

EXAMPLE: THIS IS AN IRF1840G  
 WITH ASSEMBLY  
 LOT CODE 3432  
 ASSEMBLED ON WW 24 1999  
 IN THE ASSEMBLY LINE "K"

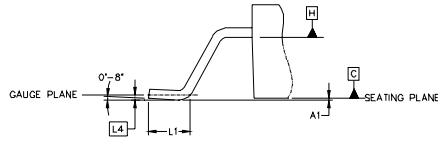


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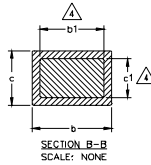
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## D<sup>2</sup>Pak Package Outline

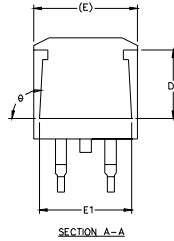
Dimensions are shown in millimeters (inches)



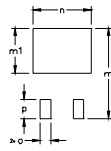
DETAIL "A"  
ROTATED 90°  
SCALE R:1



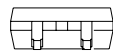
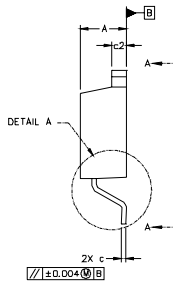
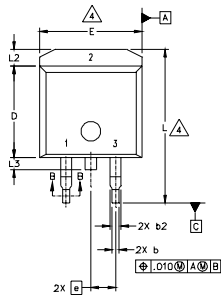
SECTION B-B  
SCALE: NONE



SECTION A-A



FOOT PRINT  
SCALE 2:1



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	3
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2			1.65	.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

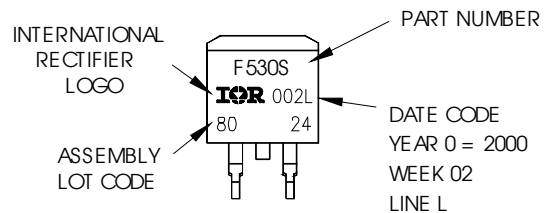
\* PART DEPENDENT.

### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCH.

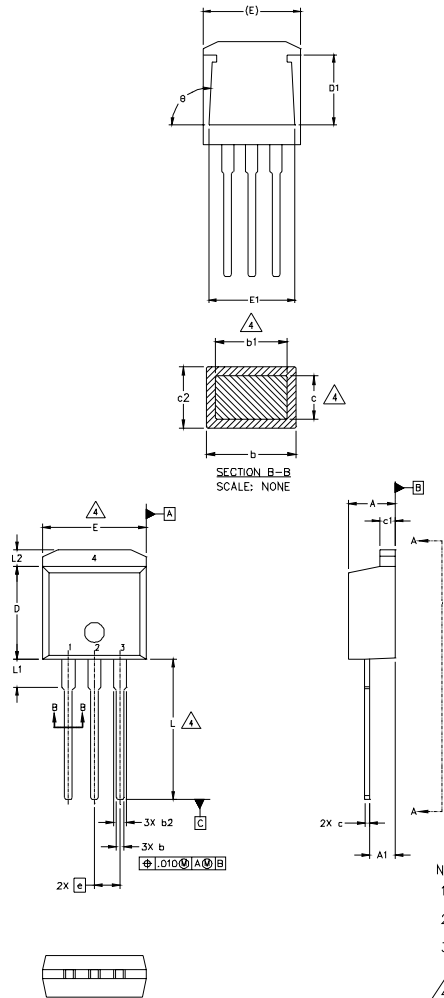
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW02, 2000  
IN THE ASSEMBLY LINE "L"



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.38	0.63	.015	.025	
c1	1.14	1.40	.045	.055	3
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### IGBT

- 1- GATE
- 2- COLLECTOR
- 3- EMITTER

#### NOTES:

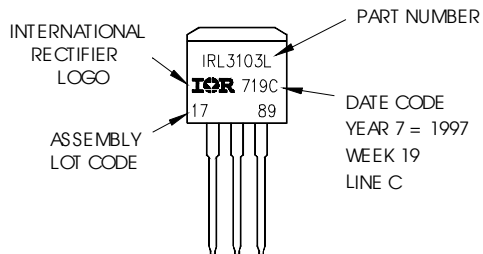
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

5. CONTROLLING DIMENSION: INCH.

## TO-262 Part Marking Information

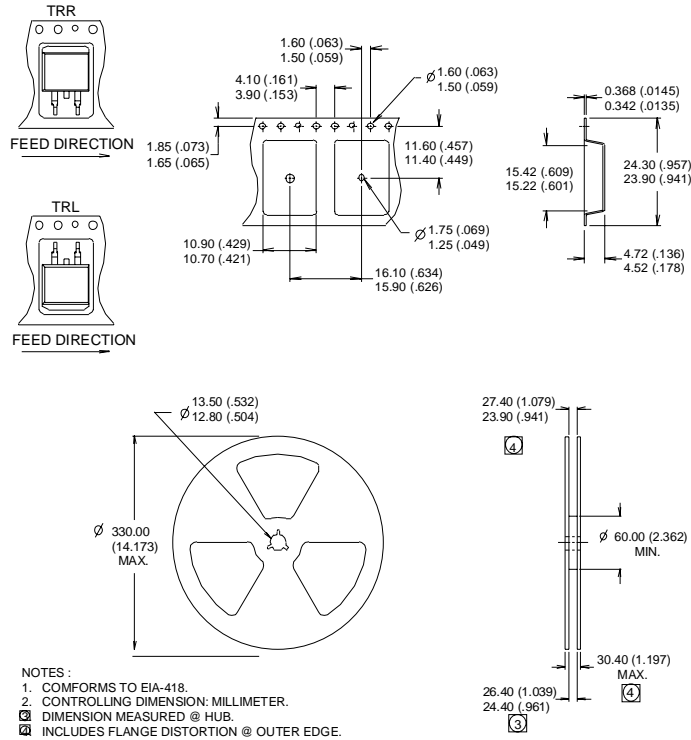
EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



# IRFB/IRFIB/IRFS/IRFSL41N15D

## D<sup>2</sup>Pak Tape & Reel Information

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**IR** Rectifier



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.5\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 25\text{A}$ .
- ③  $I_{SD} \leq 25\text{A}$ ,  $di/dt \leq 340\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ This is only applied to TO-220AB package.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

**TO-220AB & TO-220 FullPak packages are not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
TAC Fax: (310) 252-7903

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[www.irf.com](http://www.irf.com)