Data Sheet, Version1.3, July 2003

# TDA 16846

# TDA 16846-2

# TDA 16847

# TDA 16847-2

Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor

Power Management & Sup

Infineon technologies

**TDA 16846/TDA 16846-2**
**Revision History: Current Version: 2003-07-31**

Previous Version Data Sheet TDA 16846: 2000-01-14
Previous Version Data Sheet TDA 16846-2: 2002-07-30

| Page (in previous Version) | Page (in current Version) | Subjects (major changes since last revision) |
|---|---|---|
| | | The data sheets for TDA 16846 and TDA 16846-2 have been combined in this version. Some measuring values are updated: |
| 20 | 20 | Pin 1 basic value 1 $V_{1B1}$ and $V_{1B2}$ slightly changed.<br>Pin 2 discharge current $I_{2DC\ min}$ changed from 0.5 mA to 0.6 mA.<br>Pin 14 overvoltage $V_{14OVmax}$ threshold changed from 17.0 V to 17.1 V. |
| 21 | 21 | Pin 3 delay to switch on $t_{3d}$ slightly decreased.<br>Pin 4 charge current $I_{4ch}$ and discharge current $I_{4DCH}$ added.<br>Pull high resistor $R_{1min}$ changed from 18kOhm to 15 kOhm according to the data sheet for TDA 16846. |
| 22 | 22 | Pin 7 charge current $I_{7\ min}$ and upper threshold $V_{7Hmin}$ small changed. |
| 23 | 23 | Pin 13 rise and fall time adapted according to $C_{13}$= 1nF (prev. 10 nF).<br>$V_{13aclow}$ slightly decreased (only TDA 16846-2, TDA 16847-2). |

**TDA 16846-2/TDA 16847-2:**
**Improvements of TDA 16846-2/TDA16847-2 compared with TDA 16846/TDA16847**

| | | |
|---|---|---|
| Pin 5 | OCI | Expanded input voltage range down to zero, series resistor between pin 5 and ground is no longer necessary. |
| Pin 7 | SYN | Improved startup to prevent the transformer from saturation also in fixed frequency and synchronized mode. |
| Pin 11 | PVC | Noise-immunity improved by spike blanking. |
| Pin 13 | OUT | Reduced output voltage level for off state. |
| Pin 14 | VCC | Noise-immunity improved by spike blanking. |

**Edition 07.03**

**Published by Infineon Technologies AG**
**St.-Martin-Strasse 53**
**D-81541 München**

**© Infineon Technologies AG 2003**
**All Rights Reserved.**

**Attention please!**

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologiesis an approved CECC manufacturer.

**Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide.

**Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

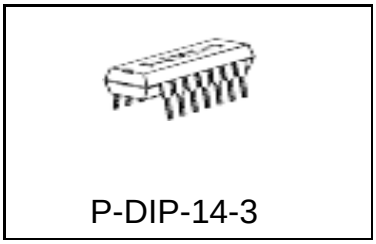
Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

**Controller for Switch Mode Power Supplies Supporting Low Power Standby and Power Factor Correction**

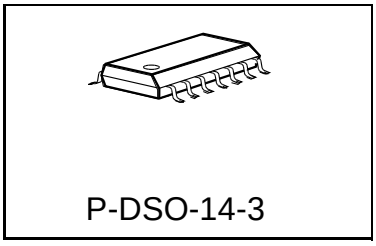
**TDA 16846**
**TDA 16846-2**

**Bipolar IC**

# 1 Overview



P-DIP-14-3



P-DSO-14-3

## 1.1 Features

- Line Current Consumption with PFC
- Low Power Consumption
- Stable and Adjustable Standby Frequency
- Very Low Start-up Current
- Soft-Start for Quiet Start-up
- Free usable Fault Comparators
- Synchronization and Fixed Frequency Circuits
- Over- and Undervoltage Lockout
- Switch Off at Mains Undervoltage
- Temporary High Power Circuit (only TDA 16847-2)
- Mains Voltage Dependent Fold Back Point Correction
- Continuous Frequency Reduction with Decreasing Load
- Adjustable and Voltage Dependent Ringing Suppression Time

| Type | Ordering Code | Package |
|---|---|---|
| TDA 16846 | Q67000-A9377 | P-DIP-14-3 |
| TDA 16847 | Q67000-A9378 | P-DIP-14-3 |
| TDA 16846G | Q67006-A9430 | P-DSO-14-3 |
| TDA 16847G | Q67006-A9412 | P-DSO-14-3 |
| TDA 16846-2 | Q67040-S4494 | P-DIP-14-3 |
| TDA 16847-2 | Q67040-S4496 | P-DIP-14-3 |
| TDA 16846-2G | Q67040-S4495 | P-DSO-14-3 |
| TDA 16847-2G | Q67040-S4497 | P-DSO-14-3 |

## 1.2 Description

The TDA 16846-2 (this name is used in the description for all types) is optimized to control free running or fixed frequency flyback converters with or without Power Factor Correction (Current Pump). To provide low power consumption at light loads, this device reduces the switching frequency in small steps with load, towards an adjustable minimum (e. g. 20 kHz in standby mode). Additionally, the startup current is very low. To avoid switching stress on the power devices, the power transistor is always switched on at minimum voltage. A special circuit is implemented to avoid jitter. The device has

several protection functions: $V_{CC}$ over- and undervoltage, mains undervoltage, current limiting and 2 free usable fault comparators. Regulation can be done by using the internal error amplifier or an opto coupler feedback (additional input). The output driver is ideally suited for driving a power MOSFET. Fixed frequency and synchronized operation are also possible.

The TDA 16846-2 is suited for TV-, VCR- sets, SAT receivers and other sets for consumer electronics. It also can be used in PC monitors.

The TDA 16847-2 is identical with TDA 16846-2 but has an additional power measurement output (pin 8) which can be used as a Temporary High Power Circuit.

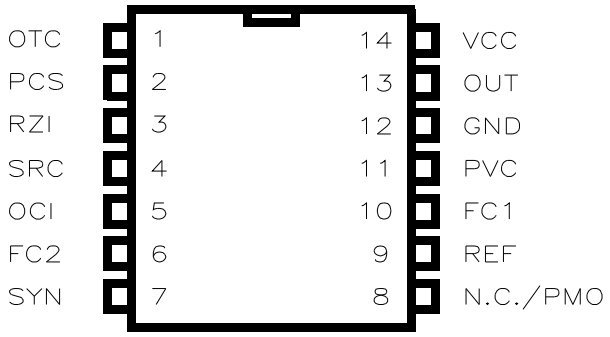



**Figure 1 Pin Configuration** (top view)

## 1.3 Pin Definitions and Functions

| Pin | Symbol | Function |
|---|---|---|
| 1 | OTC | Off Time Circuit |
| 2 | PCS | Primary Current Simulation |
| 3 | RZI | Regulation and Zero Crossing Input |
| 4 | SRC | Soft-Start and Regulation Capacitor |
| 5 | OCI | Opto Coupler Input |
| 6 | FC2 | Fault Comparator 2 |
| 7 | SYN | Synchronization Input |
| 8 | N.C./PMO | Not Connected (TDA 16846-2) / PMO (TDA 16847-2) |
| 9 | REF | Reference Voltage and Current |
| 10 | FC1 | Fault Comparator 1 |
| 11 | PVC | Primary Voltage Check |
| 12 | GND | Ground |
| 13 | OUT | Output |
| 14 | VCC | Supply Voltage |

## 1.4 Short Description of the Pin Functions

| Pin | Function |
|---|---|
| 1 | A parallel RC-circuit between this pin and ground determines the ringing suppression time and the standby-frequency. |
| 2 | A capacitor between this pin and ground and a resistor between this pin and the positive terminal of the primary electrolytic capacitor quantifies the max. possible output power of the SMPS. |
| 3 | This is the input of the error amplifier and the zero crossing input. The output of a voltage divider between the control winding and ground is connected to this input. If the pulses at pin 3 exceed a 5 V threshold, the control voltage at pin 4 is lowered. |
| 4 | This is the pin for the control voltage. A capacitor has to be connected between this pin and ground. The value of this capacitor determines the duration of the softstart and the speed of the control (primary regulation). |
| 5 | If an opto coupler for the control is used, its output has to be connected between this pin and ground. The voltage divider at pin 3 has then to be changed, so that the pulses at pin 3 are below 5 V. |
| 6 | Fault comparator 2: A voltage > 1.2 V at this pin stops the SMPS (v.also pin 9). |
| 7 | If fixed frequency mode is wanted, a parallel RC circuit has to be connected between this pin and ground. The RC-value determines the frequency. If synchronized mode is wanted, sync pulses have to be fed into this pin. |
| 8 | TDA 16846-2: Not connected. TDA 16847-2: This is the power measurement output of the Temporary High Power Circuit. A capacitor and a RC-circuit has to be connected between this pin and ground. |
| 9 | Output for the reference voltage (5 V). With a resistor between this pin and ground the fault comparator 2 (pin 6) is enabled. |
| 10 | Fault comparator 1: If a voltage > 1 V is applied to this pin, the SMPS stops. |
| 11 | This is the input of the primary voltage check. The voltage at the anode of the primary electrolytic capacitor has to be fed to this pin via a voltage divider. If the voltage of this pin falls below 1 V, the SMPS is switched off. A second function of this pin is the primary voltage dependent fold back point correction (only active in free running mode). |
| 12 | Common ground. |
| 13 | Output signal. This pin has to be connected via a series resistor to the gate of the power transistor. |
| 14 | Connection for supply voltage and startup capacitor. After startup, the supply voltage is produced by the control winding of the transformer and rectified by an external diode. |

## 1.5 Block Diagrams

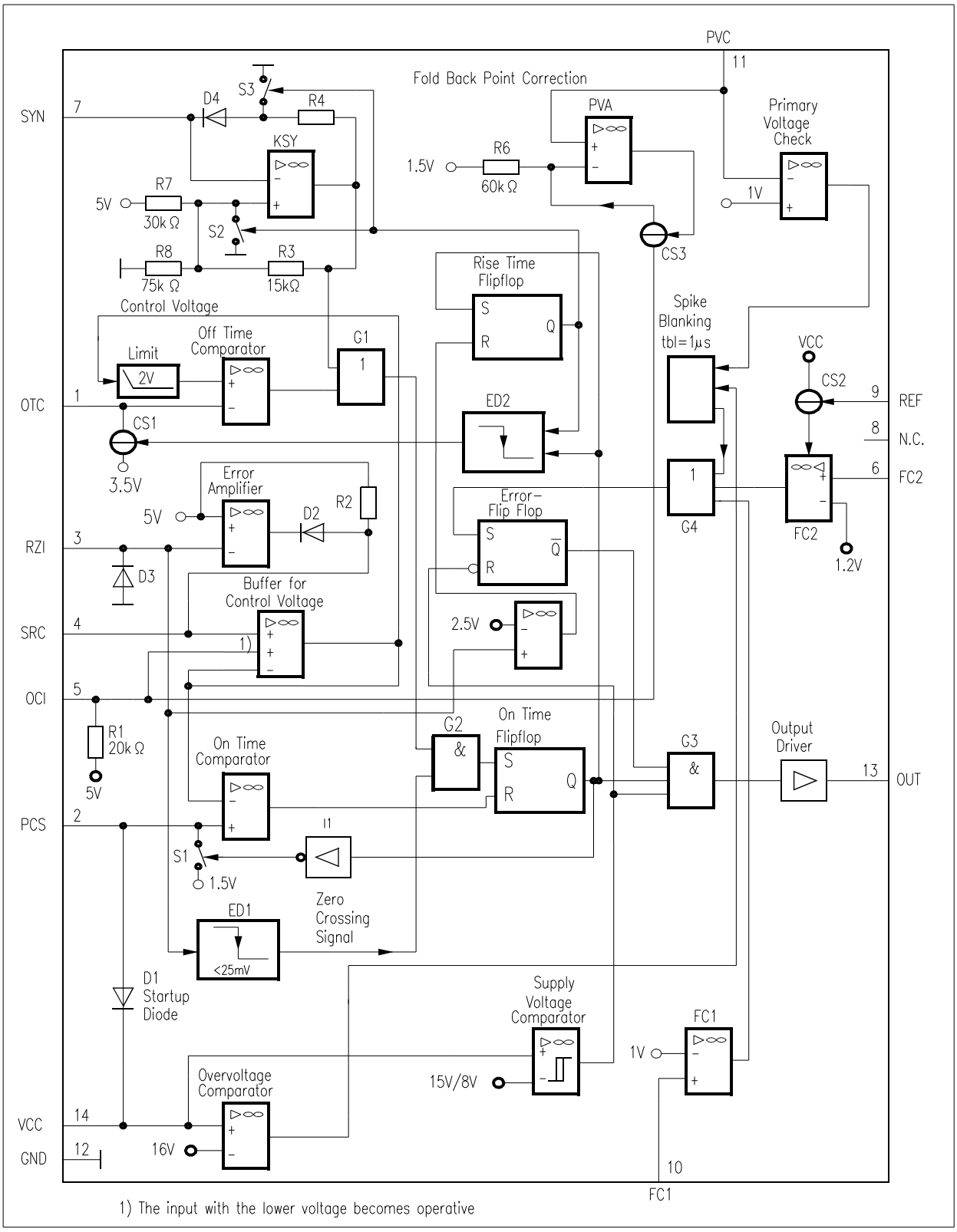



**Figure 2 TDA 16846-2**

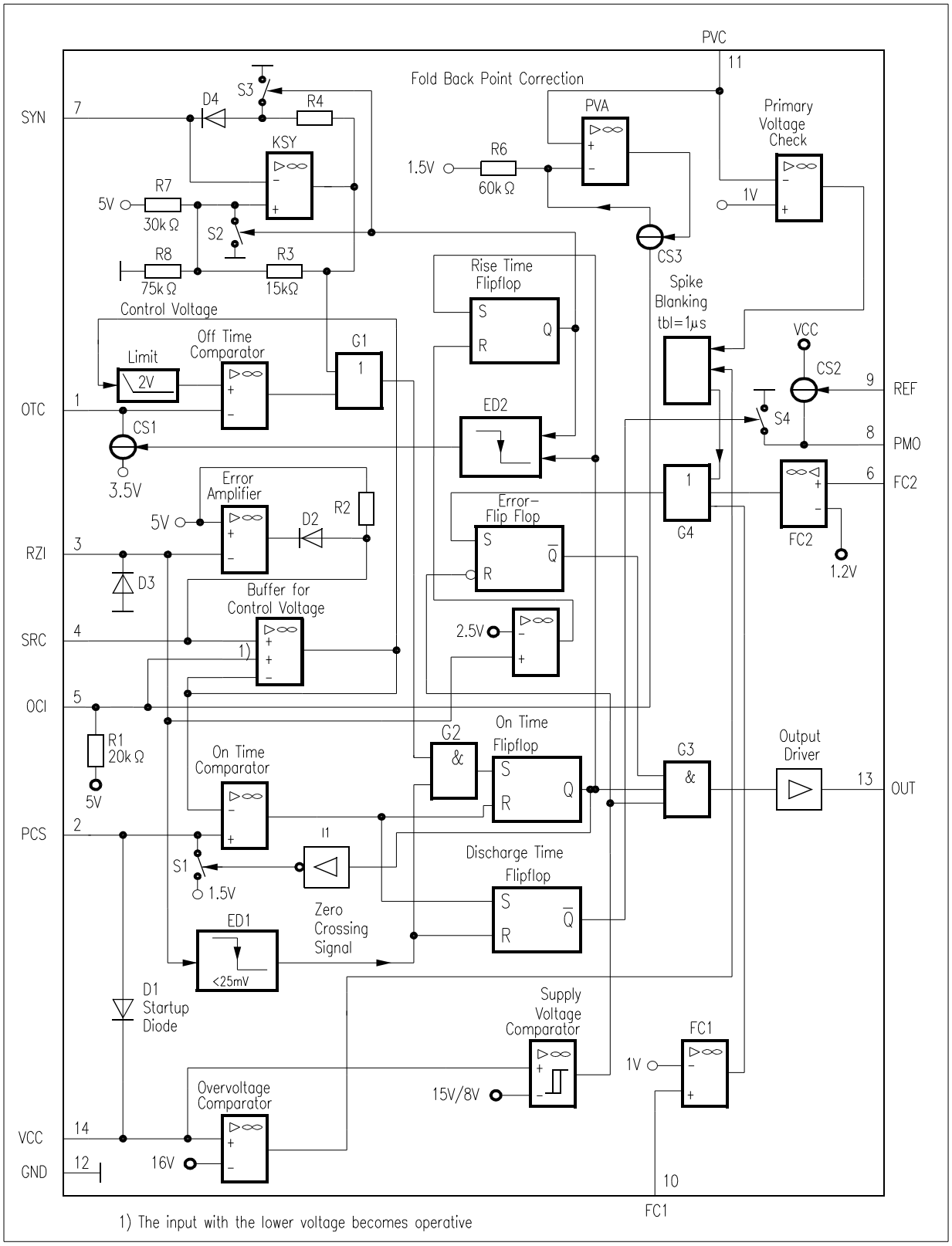



**Figure 3 TDA 16847-2**

# 2 Functional Description

### Start Up Behaviour (Pin 14)

When power is applied to the chip and the voltage $V_{14}$ at Pin 14 ($V_{CC}$) is less than the upper threshold ($V_{ON}$) of the Supply Voltage Comparator (SVC), then the input current $I_{14}$ will be less than 100 ∝A. The chip is not active (off state) and driver output (Pin 13) and control output (Pin 4) will be actively held low. When $V_{14}$ exceeds the upper SVC threshold ($V_{ON}$) the chip starts working and $I_{14}$ increases. When $V_{14}$ falls below the lower SVC threshold ($V_{OFF}$) the chip starts again from its initial condition. **Figure 4** shows the start-up circuit and **Figure 5** shows the voltage $V_{14}$ during start up. Charging of $C_{14}$ is done by resistor $R_2$ of the “Primary Current Simulation” (see later) and the internal diode D1, so no additional start up resistor is needed. The capacitor $C_{14}$ delivers the supply current until the auxiliary winding of the transformer supplies the chip with current through the external diode D14.

It is recommended to apply a small RF snubber capacitor of e.g. 100 nF parallel to the electrolytic capacitor at pin 14 as shown in the application circuits in Figures 15, 16 , and 17.

To avoid multiple pulses during start up in fixed frequency mode (danger of transformer saturation), the IC works in freerunning mode until the pulses at pin 3 (RZI) exceed the 2.5 V threshold (only TDA 16846-2, TDA 16847-2).

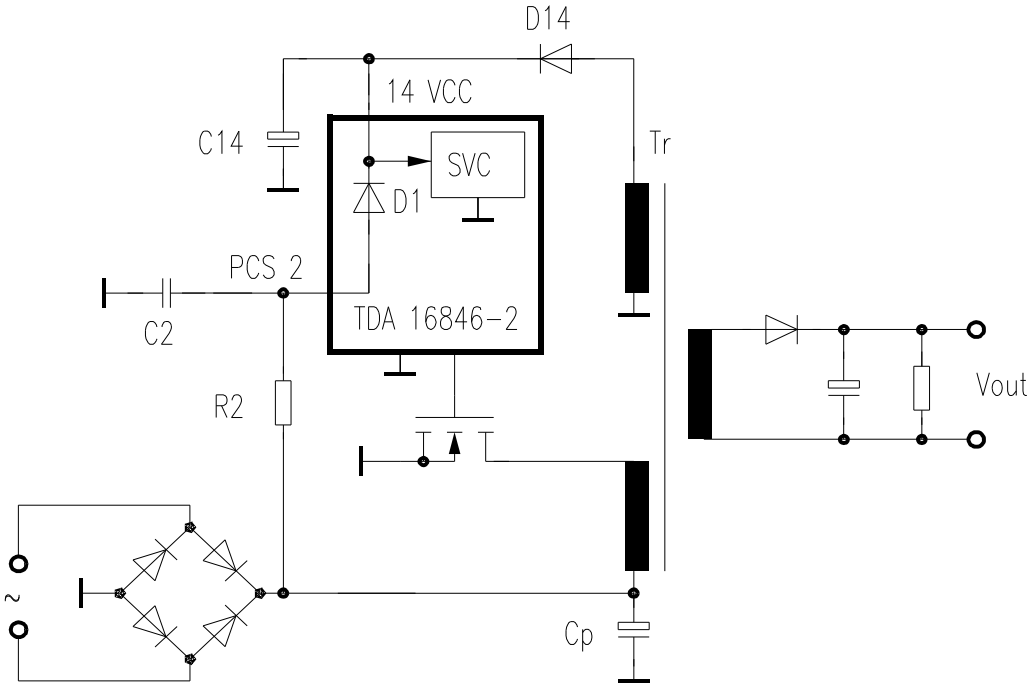



**Figure 4 Startup Circuit**

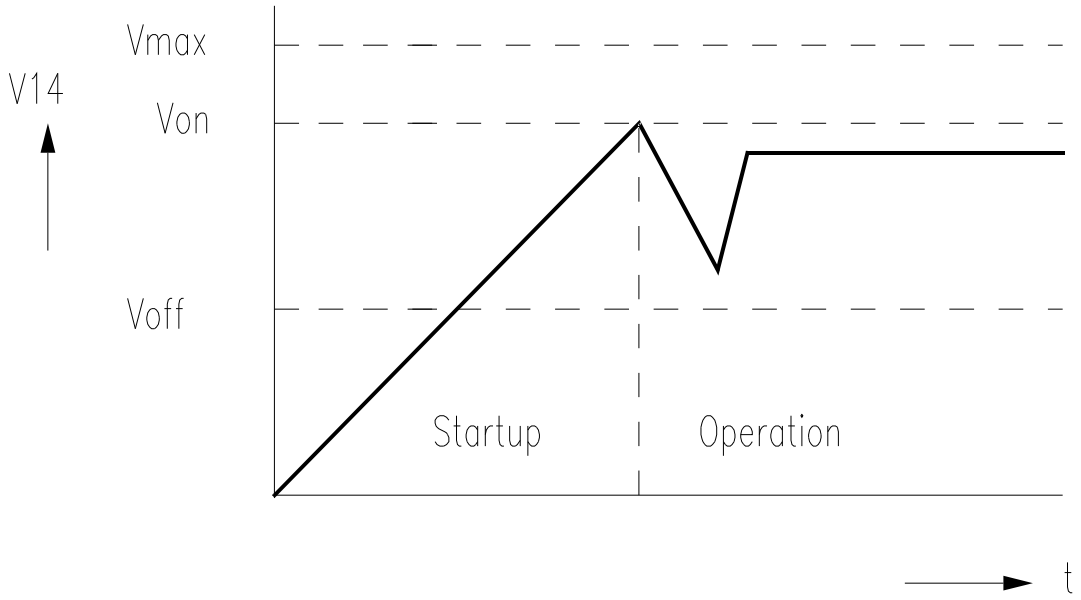



**Figure 5 Startup Voltage Diagram**

### Primary Current Simulation PCS (Pin 2) / Current Limiting

A voltage proportional to the current of the power transistor is generated at Pin 2 by the RC-combination $R_2$, $C_2$ (**Figure 4**). The voltage at Pin 2 is forced to 1.5 V when the power transistor is switched off and during its switch on time $C_2$ is charged by $R_2$ from the rectified mains. The equation of $V_2$ and the current in the power transistor ($I_{primary}$) is

$$V_2 = 1{,}5\ \text{V} + \frac{L_{primary} \cdot I_{primary}}{R_2 \cdot C_2}$$

$L_{primary}$: Primary inductance of the transformer

The voltage $V_2$ is applied to one input of the On Time Comparator ONTC (see **Figure 2**). The other input is the control voltage. If $V_2$ exceeds the control voltage, the driver switches off (current limiting). The maximum value of the control voltage is the internal reference voltage 5 V, so the maximum current in the power transistor ($I_{Mprimary}$) is

$$I_{Mprimary} = \frac{3{,}5\ \text{V} \cdot R_2 \cdot C_2}{L_{primary}}$$

The control voltage can be reduced by either the Error Amplifier EA (current mode regulation), or by an opto coupler at Pin 5 (regulation with opto coupler isolation) or by the voltage $V_{11}$ at Pin 11 (Fold Back Point Correction).

### Fold Back Point Correction PVC (Pin 11)

$V_{11}$ is derived from a voltage divider connected to the rectified mains and reduces the limit of the possible current maximum in the power transistor if the mains voltage increases. I.e. this limit is independent of the mains (only active in free running mode). The maximum current ($I_{Mprimary}$) depending on the voltage $V_{11}$ at Pin 11 is

$$I_{Mprimary} = \frac{(4\,V - V_{11}/3) \cdot R_2 \cdot C_2}{L_{primary}}$$

### Off-Time Circuit OTC (Pin 1)

**Figure 6** shows the Off-Time Circuit which determines the load dependent frequency curve. When the driver switches off (**Figure 7**) the capacitor $C_1$ is charged first by current $I_{1L}$ (approx. 0.5 mA, for extended ringing suppression time). As soon as the voltage at pin 3 reaches the level $V_{3L}$ (2.5 V), the charging current is switched to the higher value $I_{1H}$ (approx. 1 mA, for normal ringing suppression time). This current flows until the capacitor's voltage reaches 3.5 V. The charge time TC1 is

$$TC1 \approx \frac{C_1 \cdot 1{,}5\,V}{1mA}$$

For proper operation of the special internal anti- jitter circuit, TC1 (rising time for $I_{1H}$ only) should have the same value as the resonance time "tR" of the power circuit (**Figure 7**). After charging $C_1$ up to 3.5 V the current source is disconnected and $C_1$ is discharged by resistor $R_1$. The voltage $V_1$ at Pin 1 is applied to the Off-Time Comparator (OFTC). The other input of OFTC is the control voltage. The value of the control voltage at the input of OFTC is limited to a minimum of 2 V (for stable frequency at very light load). The On-Time Flip Flop (ONTF) is set, if the output of OFTC is high [1)] and the voltage $V_3$ at Pin 3 falls below 25 mV (zero crossing signal is high). This ensures switching on of the power transistor at minimum voltage. If no zero crossing signal is coming into pin 3, the power transistor is switched on after an additional delay until $V_1$ falls below 1.5 V (see **Figure 6**, OFTCD). As long as $V_1$ is higher than the limited control voltage, ONTF is disabled to suppress wrong zero crossings of $V_3$, due to parasitic oscillations from the transformer after switch-off. The discharge time of $C_1$ is a function of the control voltage.

[1)] i.e. $V_1$ is less than the limited control voltage.

| Control Voltage | Output Power | Off-time TD1 |
|---|---|---|
| 1.5 - 2 V | Low | Constant ($TD1_{MAX.}$), const. frequency stand by |
| 2 - 3.5 V | Medium | Decreasing |
| 3.5 - 5 V | High | Free running, switch-on at first minimum |

If the control voltage is below 2 V (at low output power) the “off-time” is maximum and constant

$$TD1_{max} \approx 0{,}56 \cdot R_1 \cdot C_1$$

During the discharge time tD1, V1 must not fall below the limit $V_{1L}$, otherwise the function is not guaranteed.

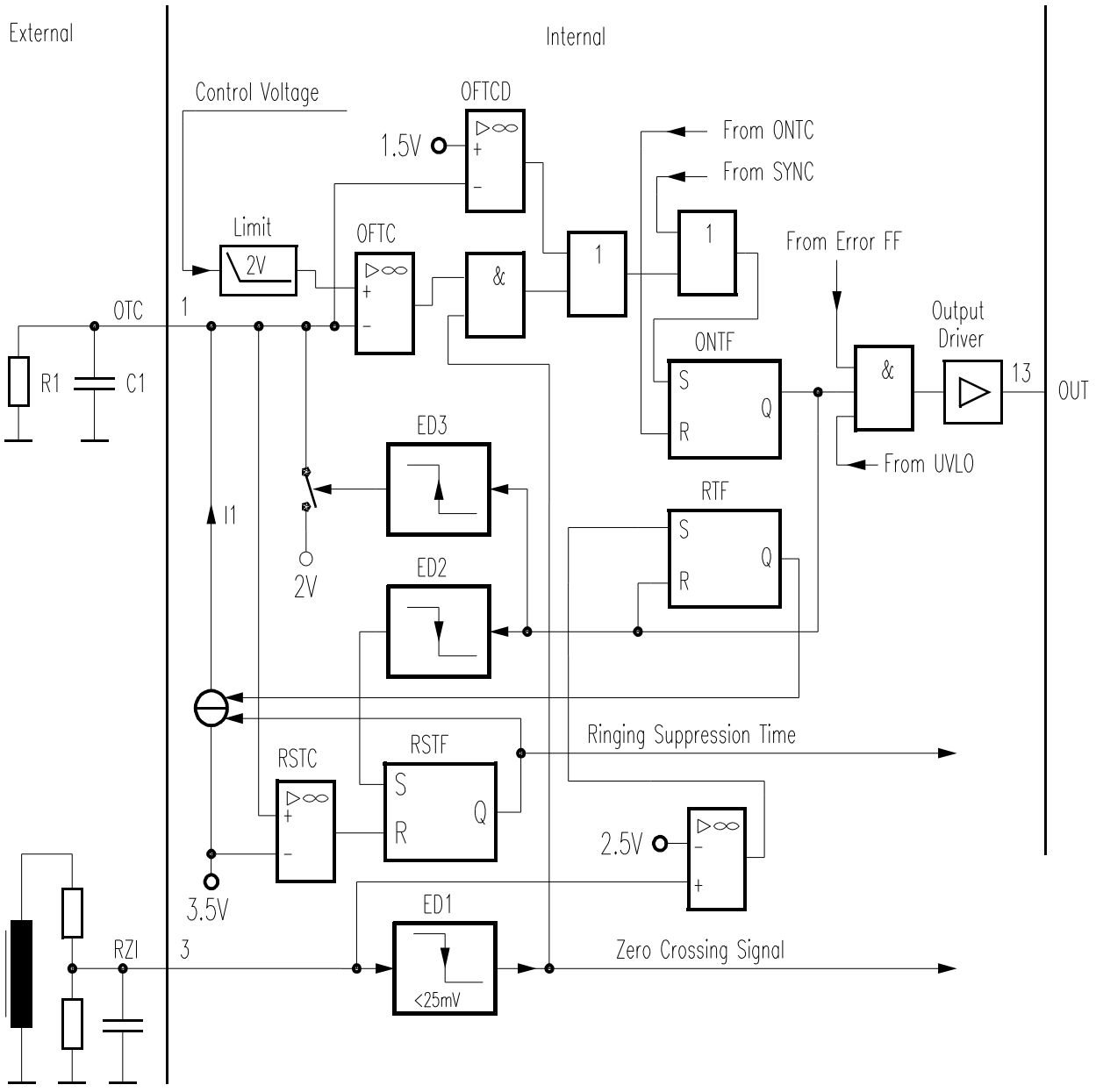



**Figure 6 Off-Time-Circuit**

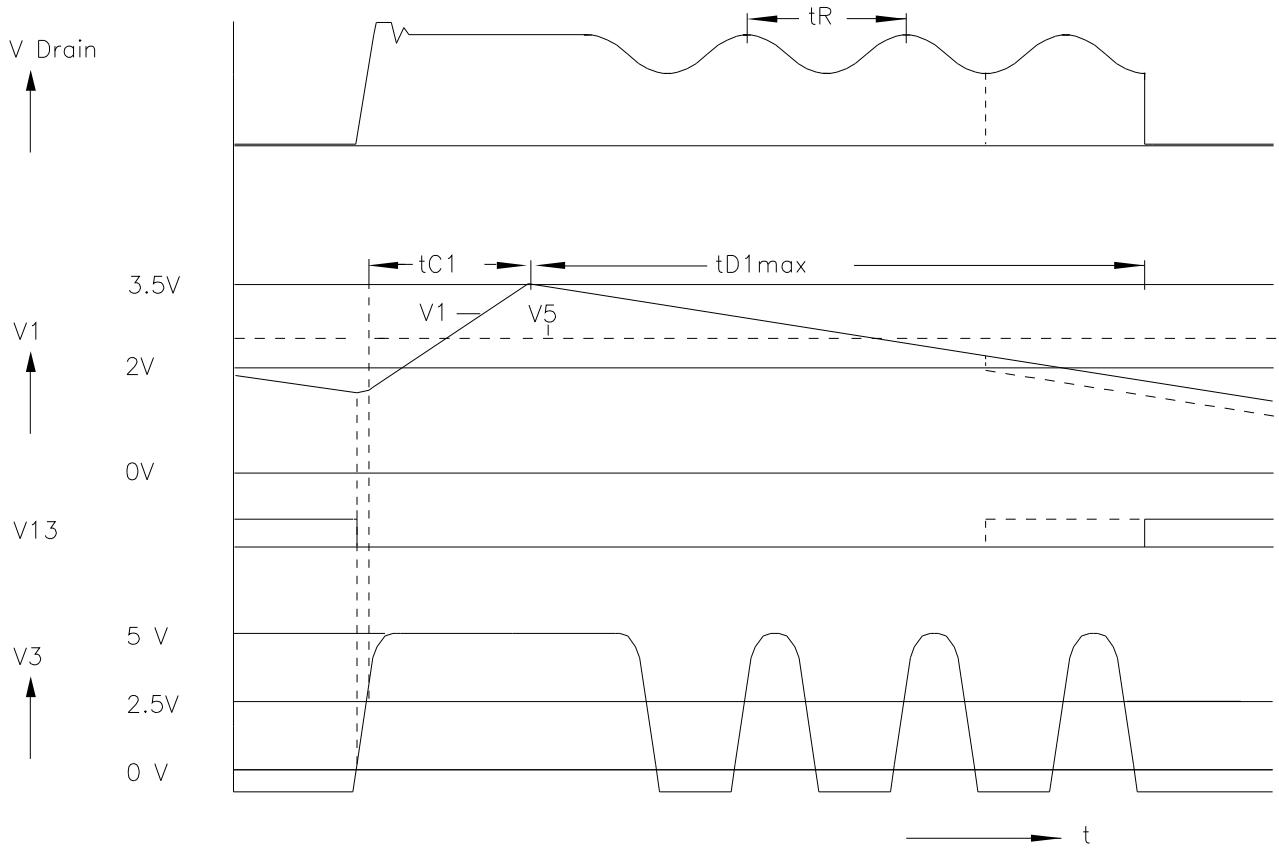



**Figure 7 Pulse Diagram of Off-Time-Circuit**

**Figure 8** shows the converters switching frequency as a function of the output power.

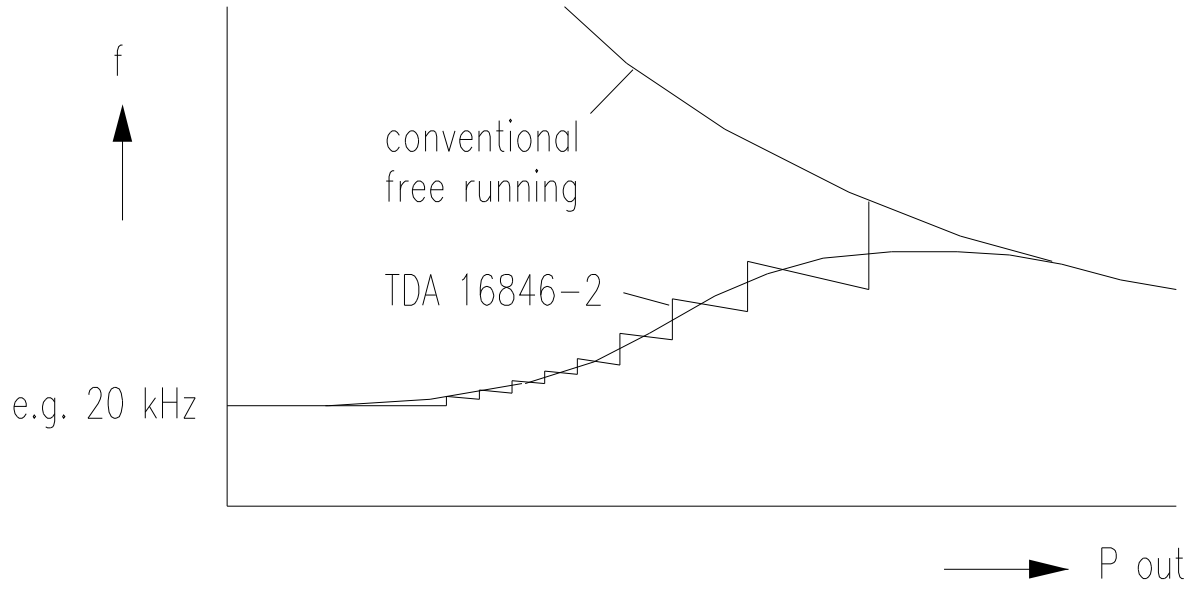



**Figure 8 Load Dependent Frequency Curve**

### Error Amplifier EA / Soft-Start (Pin 3, Pin 4)

**Figure 9** shows the simplified Error Amplifier circuit. The positive input of the Error Amplifier (EA) is the reference voltage 5 V. The negative input is the pulsed output voltage from the auxiliary winding, divided by $R_{31}$ and $R_{32}$. The capacitor $C_3$ is dimensioned only for delaying zero crossings and smoothing the first spike after switch-off. Smoothing of the regulation voltage is done with the soft start capacitor $C_4$ at Pin 4. During start up $C_4$ is charged with a current of approx. 2 ∝A (Soft Start). For primary regulation $C_4$ is charged and discharged with pulsed currents. **Figure 10** shows the voltage diagrams of the Error Amplifier circuit.

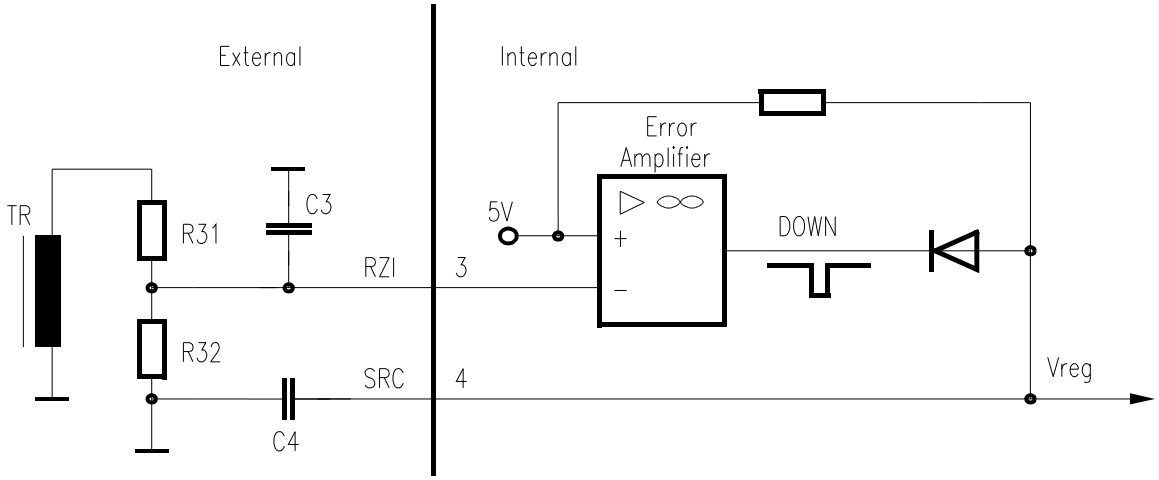



**Figure 9 Error Amplifier**

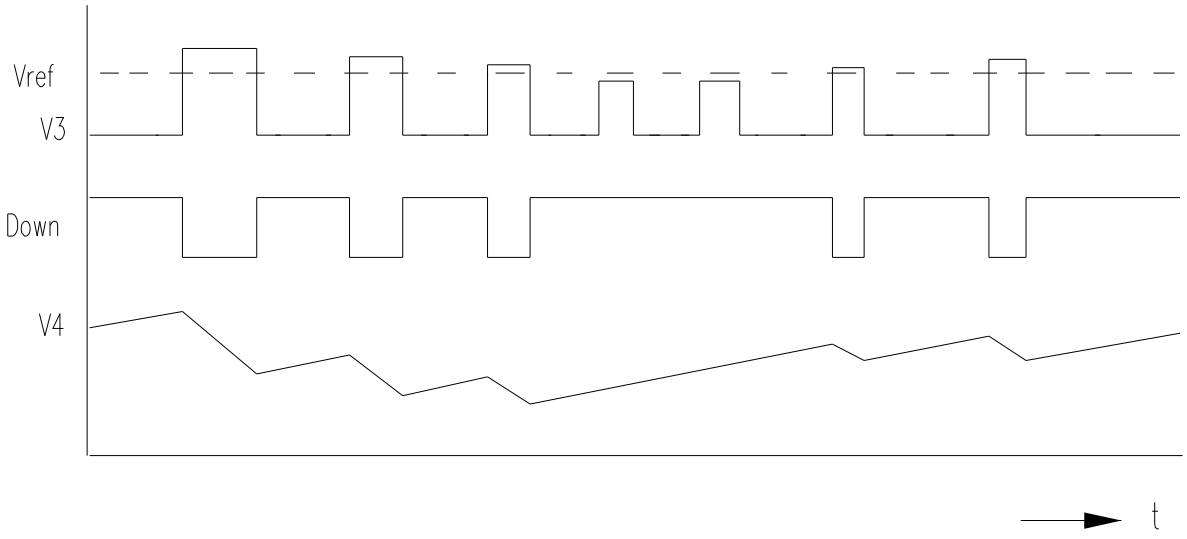



**Figure 10 Regulation Pulse Diagram**

### Fixed Frequency and Synchronization Circuit SYN (Pin 7)

**Figure 11** shows the Fixed Frequency and Synchronization Circuit. The circuit is disabled when Pin 7 is not connected or connected to pin 9 (Vref, to avoid noise sensitivity). With $R_7$ and $C_7$ at Pin 7 the circuit is working. $C_7$ is charged fast with approx. 1 mA and discharged slowly by $R_7$ (**Figure 11**). The power transistor is switched on at beginning of the charge phase. The switching frequency is (charge time ignored)

$$f \approx \frac{0{,}8}{R_7 \cdot C_7}$$

When the oscillator circuit is working the Fold Back Point Correction is disabled (not necessary in fixed frequency mode). “Switch on” is only possible when a “zero crossing” has occurred at Pin 3, otherwise “switch-on” will be delayed (**Figure 12**).

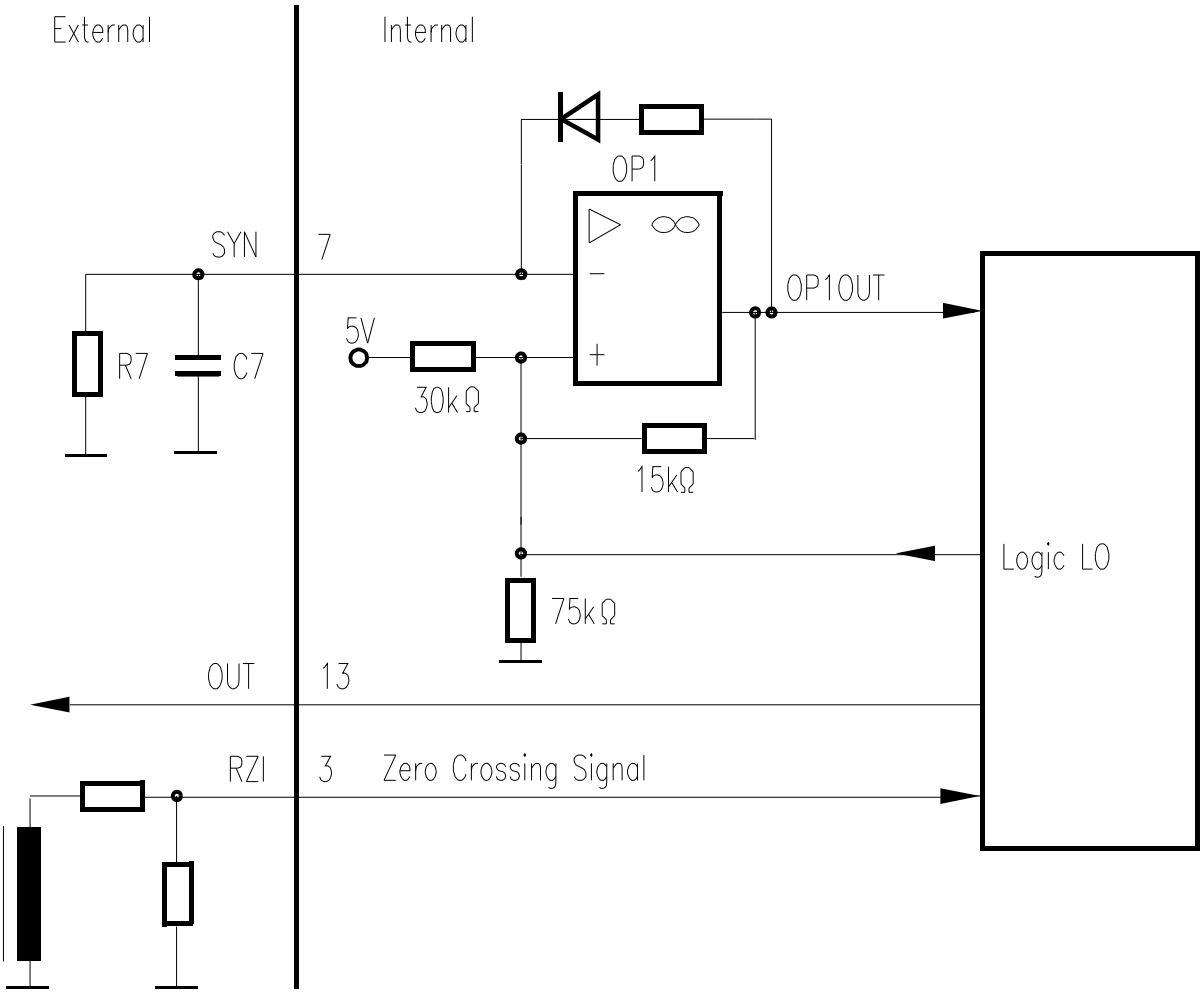



**Figure 11 Synchronization and Fixed Frequency Circuit**

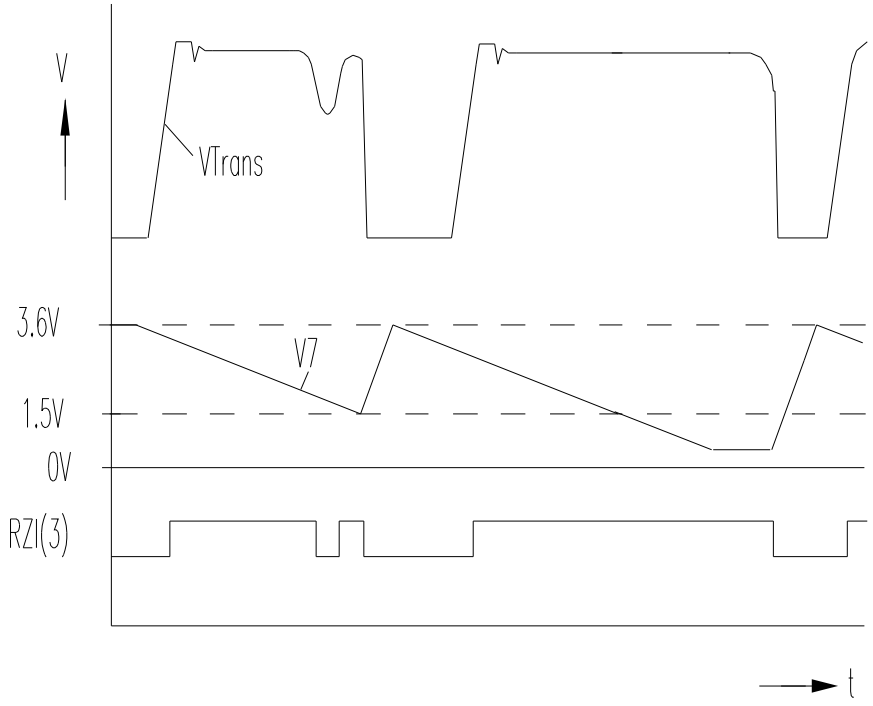



**Figure 12 Pulse Diagram for Fixed Frequency Circuit**

Synchronization mode is also possible. The synchronization frequency must be higher than the oscillator frequency.

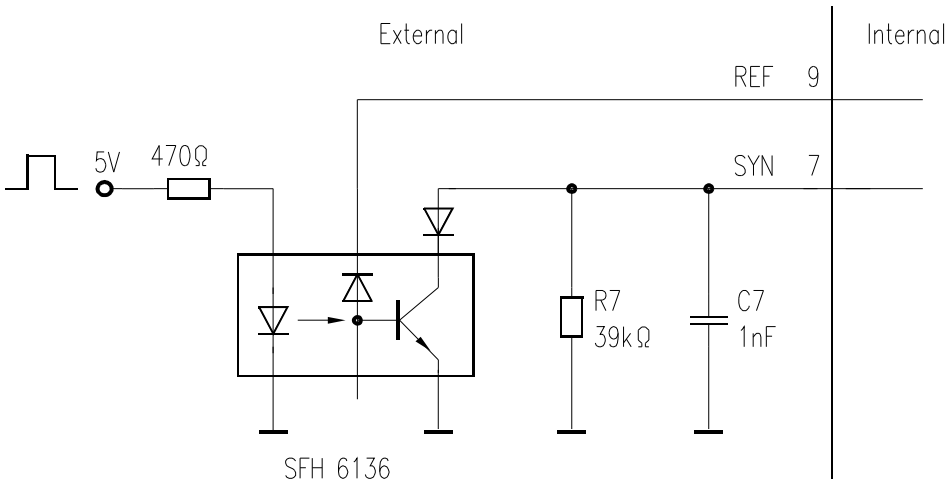



**Figure 13 Ext. Synchronization Circuit**

# 3 Protection Functions

The chip has several protection functions:

### Current Limiting

See “Primary Current Simulation PCS (Pin 2) / Current Limiting” and “Fold Back Point Correction PVC (Pin 11)”.

### Over- and Undervoltage Lockout OV/SVC (Pin 14)

When $V_{14}$ at Pin 14 exceeds 16.5 V, e. g. due to a fault in the regulation circuit, the Error Flip Flop ERR is set and the output driver is shut-down. When $V_{14}$ goes below the lower SVC threshold, ERR is reset and the driver output (Pin 13) and the soft-start (Pin 4) are shut down and actively held low.

### Primary Voltage Check PVC (Pin 11)

When the voltage $V_{11}$ at Pin 11 goes below 1 V the Error Flip Flop (ERR) is set. E.g. a voltage divider from the rectified mains at Pin 11 prevents high input currents at a too low input voltage.

### Free Usable Fault Comparator FC1 (Pin 10)

When the voltage at Pin 10 exceeds 1 V, the Error Flip Flop (ERR) is set. This can be used e. g. for mains overvoltage shutdown.

### Free Usable Fault Comparator FC2 (Pin 6)

When the voltage at Pin 6 exceeds 1.2 V, the Error Flip Flop (ERR) is set. A resistor between Pin 9 (REF) and ground is necessary to enable this fault comparator.

### Voltage dependent Ringing Suppression Time

During start-up and short-circuit operation, the output voltage of the converter is low and parasitic zero crossings are applied for a longer time at Pin 3. Therefore the Ringing Suppression Time TC1 (see “Off-Time Circuit OTC (Pin 1)”) is extended with a factor of 2.2 at a low output voltage. The voltage at pin 1 must not fall below the limit $V_{1L}$.

# 4 Temporary High Power Circuit FC2, PMO, REF (Pin 6, 8, 9, TDA 16847-2)

**Figure 14** shows the Temporary High Power Circuit:

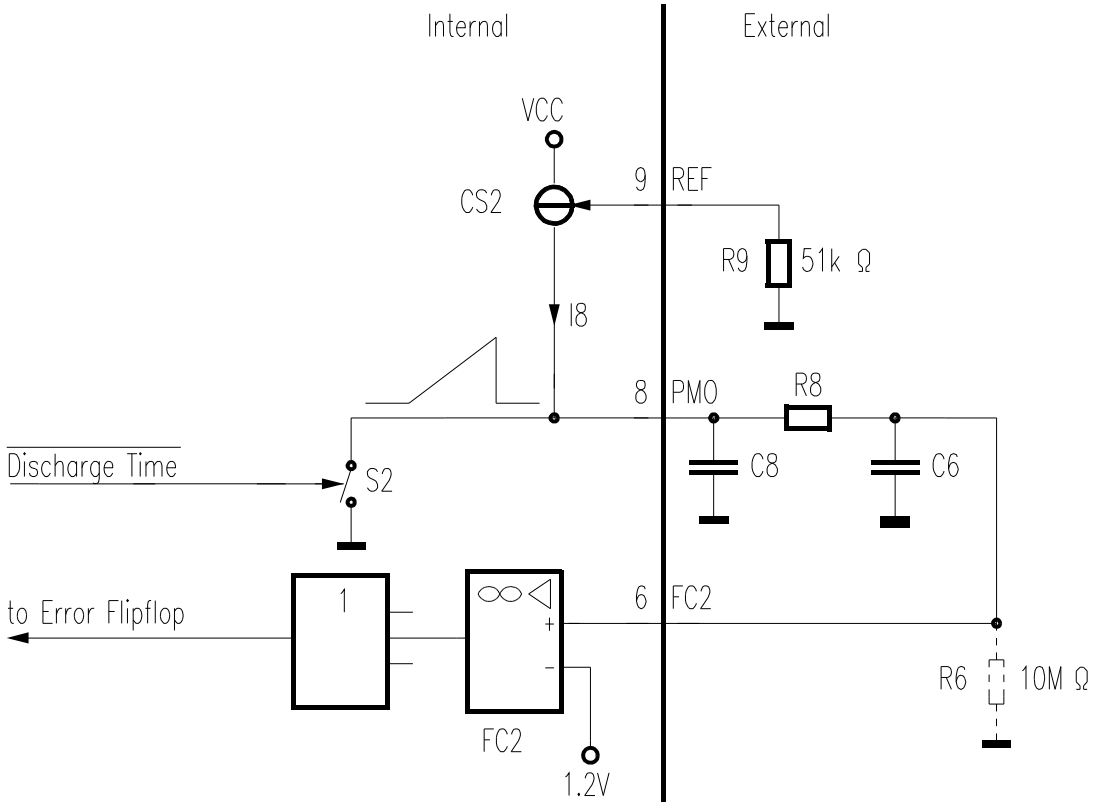



**Figure 14**

The Temporary High Power Circuit (THPC) consists of two parts:

Firstly, a power measurement circuit is implemented: The capacitor $C_8$ at Pin 8 is charged with a constant current $I_8$ during the discharge time of the flyback transformer and grounded the other time. Thus the average of the sawtooth voltage $V_8$ at Pin 8 is proportional to the converter´s output power (at constant output voltages). The charge current $I_8$ for $C_8$ is set by the resistor $R_9$ at Pin 9:

$$I_8 = 5\ \text{V}/R_9$$

Secondly, a High Power Shutdown Comparator (FC2) is implemented: When the voltage $V_6$ at Pin 6 exceeds 1.2 V the Error Flip Flop (ERR) is set. The output voltage of the power measurement circuit (Pin 8) is smoothed by $R_8/C_6$ and applied to the “high power shutdown” input at Pin 6. The relation between this voltage $V_6$ and the output power of the converter $P$ is approximately:

$$V_6 \approx (P \cdot L_{Secondary} \cdot 5\ V)/(V_{OUT}^2 \cdot C_8 \cdot R_9)$$

$L_{Secondary}$: The transformers secondary inductance

$V_{OUT}$: The converters output voltage

So the time constant of $R_9/C_8$ for a certain high power shutdown level $P_{SD}$ is:

$$R_9 \cdot C_8 \approx (P_{SD} \cdot L_{Secondary} \cdot 4.2)/V_{OUT}^2$$

The converters high power shutdown level can be adjusted lower (by $R_9$, $C_8$) than the current limit level (see “current limiting”). Thus because of the delay$R_8/C_6$, the converter can deliver maximum output power (current limit level) for a certain time (e. g. for power pulses like motor start current) and a power below the high power shutdown level for an unlimited time. This is of advantage because the thermal dimensioning of the power devices needs to be done for the lower power level only. Once the voltage $V_6$ exceeds 1.2 V no more charging or discharging happens at Pin 8. The voltage $V_6$ remains high due to the bias current out of FC2 and the converter remains switched-off. Reset can be done either by plugging-off the supply from the mains or by a high value resistor $R_6$ (**Figure 14**). $R_6$ causes a reset every few seconds. When Pin 9 is not connected or gets too little current (I9 < I9FC2), the temporary high power circuit is disabled.

# 5 Electrical Characteristics

## 5.1 Absolute Maximum Ratings

All voltages listed are referenced to ground (0 V, $V_{SS}$) except where noted.

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply Voltage at Pin 14 | $V_{CC}$ | – 0.3 | 17 | V | – |
| Voltage at Pin 1, 4, 5, 6, 7, 9, 10 | – | – 0.3 | 6 | V | – |
| Voltage at Pin 2, 8, 11 | – | – 0.3 | 17 | V | – |
| Startup current into Pin 2 | $I_2$ | | 1 | mA | |
| Voltage at Pin 3<br>Current into Pin 3 | RZI | <br>– 10 | 6 | V<br>mA | <br>$V_3$ < – 0.3 V |
| Current into Pin 9 | $I_{REF}$ | – 1 | – | mA | – |
| Current into Pin 13 | $I_{OUT}$ | <br>– 100 | 100 | mA<br>mA | $V_{13} > V_{CC}$<br>$V_{13}$ < 0 V |
| ESD Protection | – | – | 2 | kV | MIL STD 883C method 3015.6, 100 pF, 1500 Ω |
| Storage Temperature | $T_{stg}$ | – 65 | 125 | °C | – |
| Operating Junction Temperature | $T_J$ | – 25 | 125 | °C | – |
| Thermal Resistance Junction-Ambient | $R_{thJA}$ | – | 110 | K/W | P-DIP-14-3 |
| Soldering Temperature | – | – | 260 | °C | – |
| Soldering Time | – | – | 10 | s | – |

*Note: Stress beyond the above listed values may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.*

## 5.2 Characteristics

Unless otherwise stated, – 25 °C < $T_j$ < 125 °C, $V_{CC}$ = 12 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Supply Voltage and Startup Circuit VCC (Pin 14)** | | | | | | |
| Overvoltage threshold | $V_{14\ OV}$ | 15.7 | 16.5 | 17.1 | V | |
| Turn-ON threshold | $V_{14\ ON}$ | 14.5 | 15 | 15.5 | V | – |
| Turn-OFF threshold | $V_{14\ OFF}$ | 7.5 | 8 | 8.5 | V | – |
| Delta-OV-$V_{14\ ON}$ | – | 0.5 | – | – | V | – |
| Supply current, OFF | $I_{14OFF}$ | – | 40 | 100 | ∝A | $V_{CC} = V_{14\ ON}$ -100 mV |
| Supply current, ON | $I_{14ON}$ | – | 5 | 8 | mA | Output low |
| **Primary Current Simulation PCS (Pin 2) / Current Limiting** | | | | | | |
| Basic value | $V_2$ | 1.45 | 1.5 | 1.55 | V | $I_2$ = 100 ∝A |
| Peak value | $V_2$ | 4.85 | 5 | 5.15 | V | $V_{11}$ = 1.2 V |
| Discharge current | $I_{2DC}$ | 0.6 | 1.0 | 2.5 | mA | $V_2$ = 3 V |
| Bias current Pin 2 | – | – 1.0 | – 0.3 | – | ∝A | $V_2$ = 2 V |
| **Fold Back Point Correction PVC (Pin 11)** | | | | | | |
| Peak value | $V_5$ | 3.8 | 4.1 | 4.3 | V | $V_{11}$ = 4.5 V |
| Bias current Pin 11 | – | – 1.0 | – 0.3 | – | ∝A | $V_{11}$ = 1.5 V |
| **Off-Time Circuit OTC (Pin 1)** | | | | | | |
| Charge current | $I_{1H}$ | 0.9 | 1.1 | 1.4 | mA | $V_3 > V_{3L}$ |
| Charge current | $I_{1L}$ | 0.35 | 0.5 | 0.65 | mA | $V_3 < V_{3L}$ |
| Peak value | $V_{1P}$ | 3.38 | 3.5 | 3.62 | V | – |
| Basic value 1 | $V_{1B1}$ | 1.9 | 2 | 2.1 | V | – |
| Basic value 2 | $V_{1B2}$ | 1.44 | 1.5 | 1.58 | V | – |
| $V_1$ Lower limit | $V_{1L}$ | | 80 | 140 | mV | |
| Bias current Pin 1 | – | – 1.1 | – 0.4 | – | ∝A | $V_1$ = 2.2 V |

## 5.2 Characteristics (cont'd)

Unless otherwise stated, – 25 °C < $T_j$ < 125 °C, $V_{CC}$ = 12 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Zero Crossing Input RZI (Pin 3)** | | | | | | |
| Zero crossing threshold (Pin 3) | | 15 | 25 | 35 | mV | – |
| Delay to switch-on | $t_{3d}$ | 250 | 350 | 460 | ns | – |
| Bias current Pin 3 | – | –2 | – 1.2 | – | ∝A | $V_3$ = 0 V |
| **Error Amplifier Input RZI (Pin 3)** | | | | | | |
| Input threshold (Pin 3) | $V_{EATH}$ | 4.85 | 5 | 5.15 | V | – |
| Low voltage threshold (Pin 3) | $V_{3L}$ | 2.4 | 2.5 | 2.6 | V | – |
| Bias current Pin 3 | – | – | – 0.9 | – | ∝A | $V_3$ = 3 V |
| **Softstart and Regulation Voltage SRC (Pin 4)** | | | | | | |
| Soft-start charge current (Pin 4) | $I_{4CHS}$ | – 2.5 | – 1.8 | – 1.2 | ∝A | $V_4$ = 2 V |
| Charge current Pin 4 | $I_{4CH}$ | -0.9 | -0.7 | -0.5 | mA | |
| Discharge current Pin 4 | $I_{4DCH}$ | 0.9 | 1.4 | 1.9 | mA | |
| **Opto Coupler Input OCI (Pin 5)** | | | | | | |
| Input voltage range (TDA 16846, TDA 16847) | $V_5$ | 0.3 | – | 6 | V | – |
| Input voltage range (TDA 16846-2, TDA 16847-2) | $V_5$ | 0 | – | 6 | V | – |
| Pull high resistor to $V_{REF}$ | $R_1$ | 15 | 20 | 28 | kΩ | – |

## 5.2 Characteristics (cont'd)

Unless otherwise stated, – 25 °C < $T_j$ < 125 °C, $V_{CC}$ = 12 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Fixed Frequency and Synchronization Circuit SYN (Pin 7)** | | | | | | |
| Charge current | $I_7$ | -0.9 | -1.3 | -1.6 | mA | – |
| Upper threshold | $V_{7H}$ | 3.4 | 3.6 | 3.7 | V | – |
| Lower threshold | $V_{7L1}$ | 1.53 | 1.6 | 1.67 | V | – |
| Input voltage range | $V_{7L2}$ | 0.4 | | 6 | V | – |
| Bias current Pin 7 | – | – 2.4 | – 1.8 | – 1.1 | ∝A | $V_7$ = 4 V |
| **Primary Voltage Check PVC (Pin 11)** | | | | | | |
| Threshold | $V_{11}$ | 0.95 | 1 | 1.06 | V | – |
| **Reference Voltage REF (Pin 9)** | | | | | | |
| Voltage at Pin 9 | $V_9$ | 4.8 | 5 | 5.15 | V | $I_9$ = – 100 ∝A |
| Current to enable FC2 | $I_{9FC2}$ | – 18 | – 7 | | µA | |

## 5.2 Characteristics (cont'd)

Unless otherwise stated, – 25 °C < $T_j$ < 125 °C, $V_{CC}$ = 12 V

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Fault Comparator FC2 (Pin 6)** | | | | | | |
| HPC Threshold | $V_6$ | 1.12 | 1.2 | 1.28 | V | – |
| Bias Current Pin 6 | – | – 1.0 | – 0.3 | 0.1 | ∝A | $V_6$ = 0.8 V |
| **Fault Comparator FC1 (Pin 10)** | | | | | | |
| Threshold | $V_{10}$ | 0.95 | 1 | 1.06 | V | – |
| Bias current Pin 10 | – | 0.35 | 0.65 | 0.95 | ∝A | $V_{10}$ = 0.8 V |
| **Power Measurement Output PMO (Pin 8, only TDA 16847, TDA 16847-2)** | | | | | | |
| Charge current Pin 8 | $I_8$ | – 110 | – 100 | – 90 | ∝A | $I_9$ = – 100 ∝A |
| **Output Driver OUT (Pin 13)** | | | | | | |
| Output voltage low state | $V_{13\ low}$ | 1.1 | 1.8 | 2.4 | V | $I_{13}$ = 100 mA |
| Output voltage high state | $V_{13\ high}$ | 9.2 | 10 | 11 | V | $I_{13}$ = – 100 mA |
| Output voltage during low $V_{14}$ (TDA 16846, TDA 16847) | $V_{13\ aclow}$ | 0.8 | 1.8 | 2.5 | V | $I_{13}$ = 10 mA, $V_{14}$ = 7 V |
| Output voltage during low $V_{14}$ (TDA 16846-2, TDA 16847-2) | $V_{13\ aclow}$ | 0.5 | 1 | 1.5 | V | $I_{13}$ = 10 mA, $V_{14}$ = 7 V |
| Rise time | – | 30 | 50 | 100 | ns | $C_{13}$ = 1 nF, $V_{13}$ = 2 … 8 V |
| Fall time | – | 10 | 20 | 50 | ns | $C_{13}$ = 1 nF, $V_{13}$ = 2 … 8 V |

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A$ = 25 °C and the given supply voltage.*

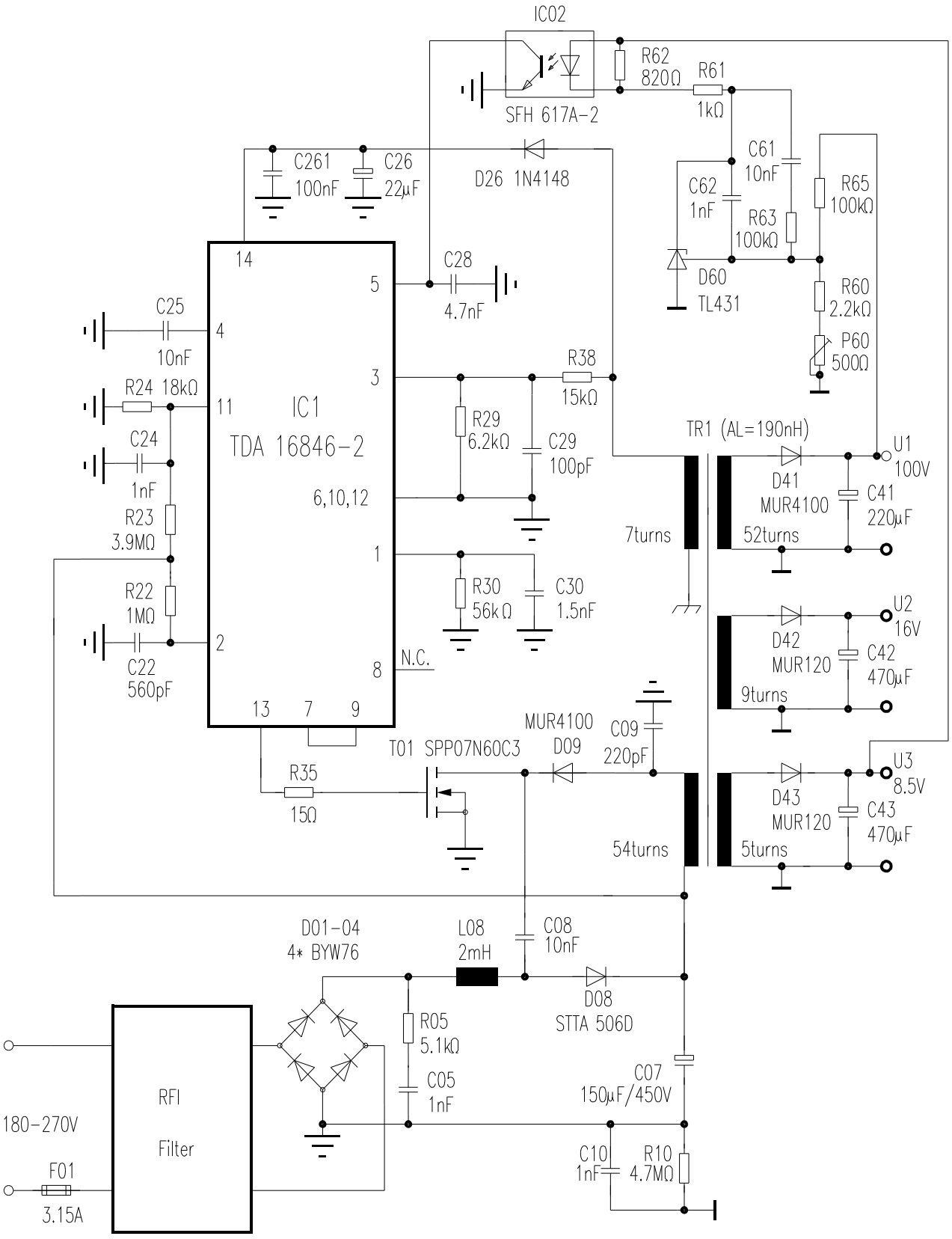



**Figure 15 Circuit Diagram for Application with PFC**

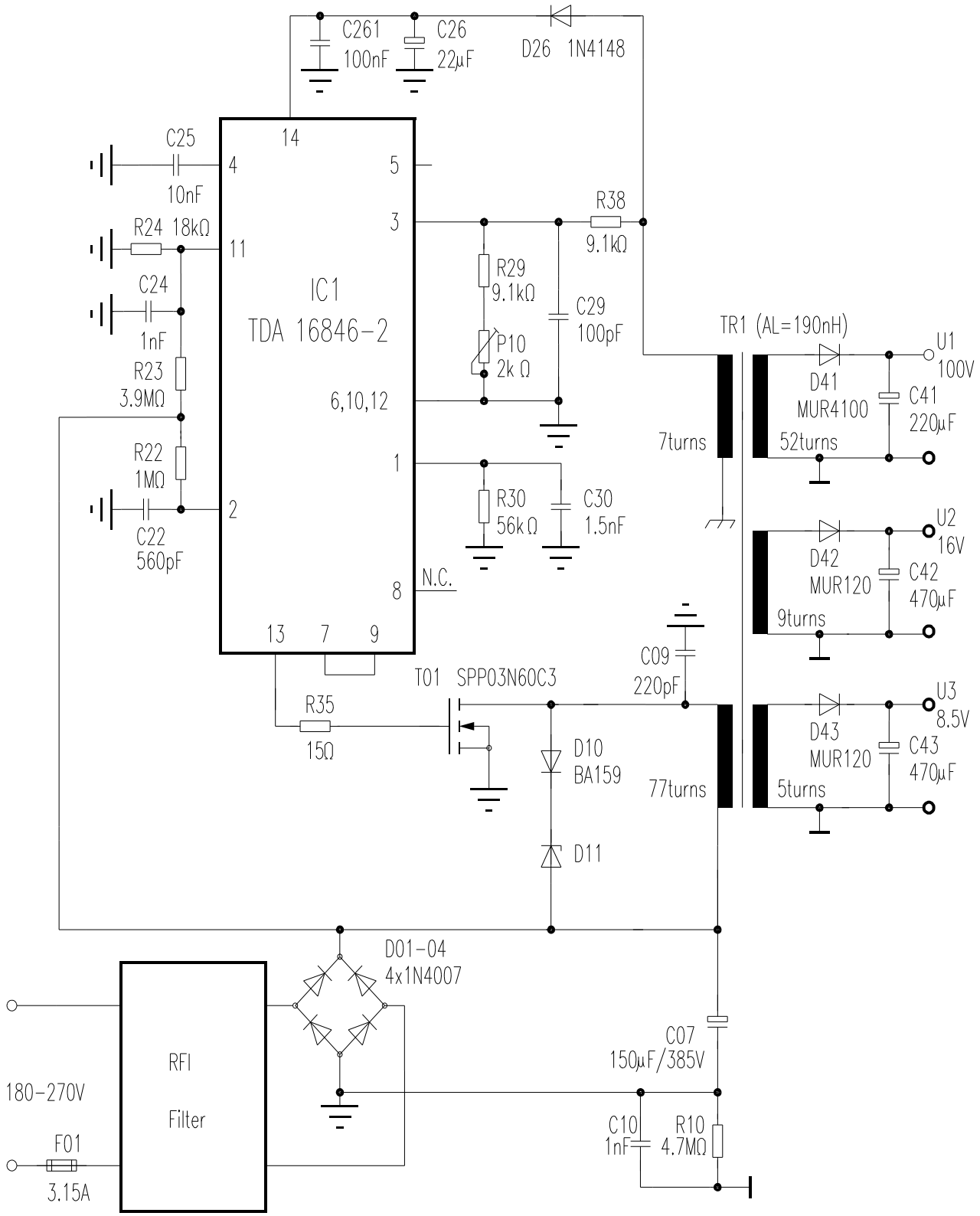



**Figure 16 Circuit Diagram for Standard Application**

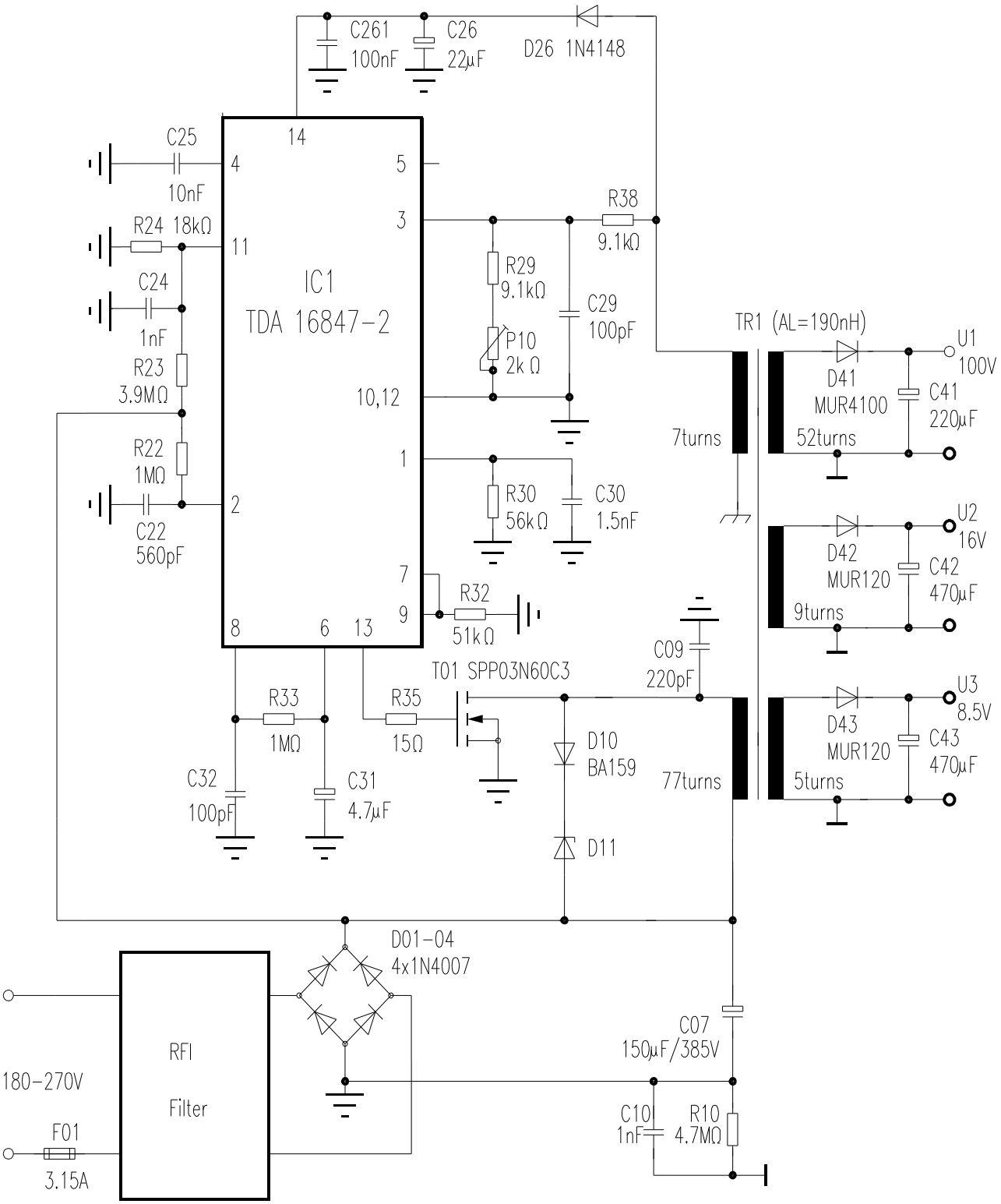
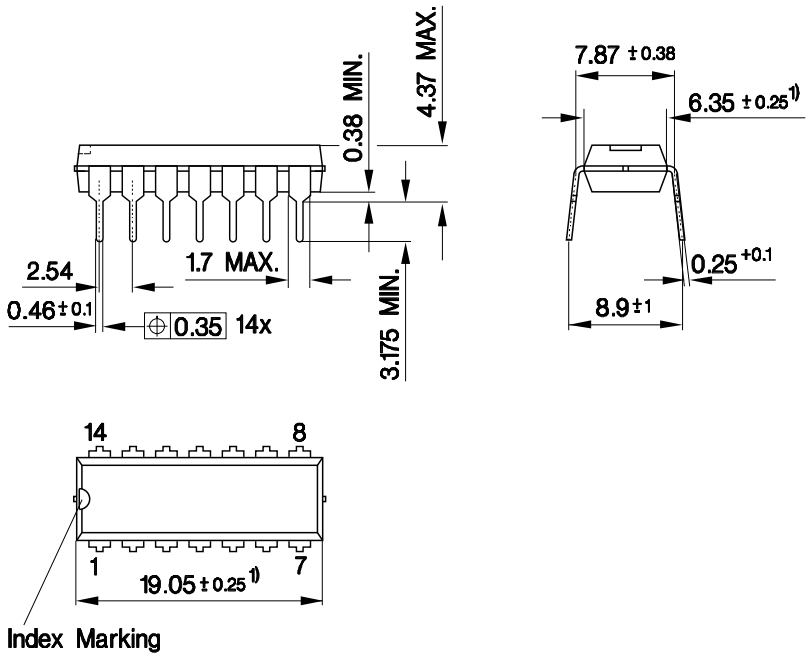



**Figure 17 Circuit Diagram for Application with Temporary High Power Circuit**

## Package Outlines

**P-DIP-14-3**
(Plastic Dual In-line Package)




1) Does not include plastic or metal protrusion of 0.25 max. per side

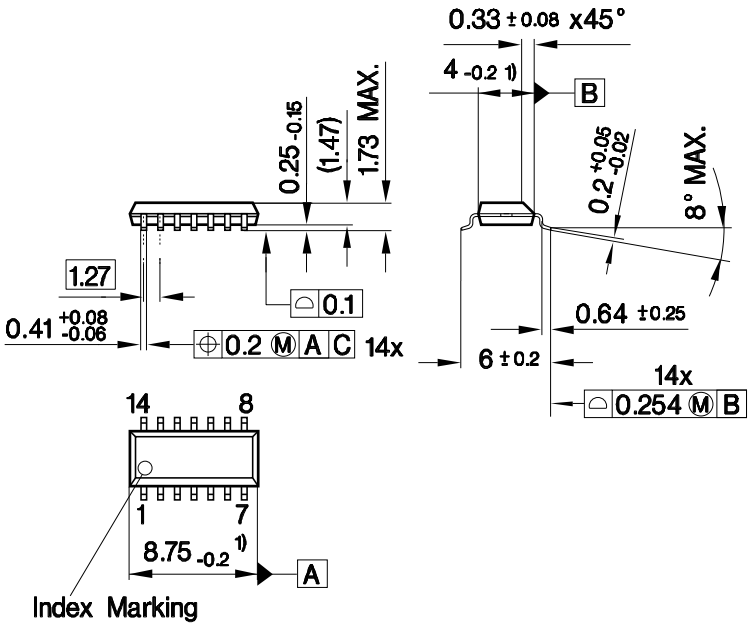
GPD05584

**Sorts of Packing**
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

**P-DSO-14-3**

(Plastic Dual In-line Package)




1) Does not include plastic or metal protrusion of 0.15 max. per side

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm