

Features

- Low on-voltage drop ($V_{CE(sat)}$)
- Low C_{res} / C_{ies} ratio (no cross conduction susceptibility)
- Short circuit withstand time 10 μs
- IGBT co-packaged with ultra fast free-wheeling diode

Applications

- High frequency inverters
- Motor drivers

Description

This IGBT utilizes the advanced PowerMESH™ process resulting in an excellent trade-off between switching performance and low on-state behavior.

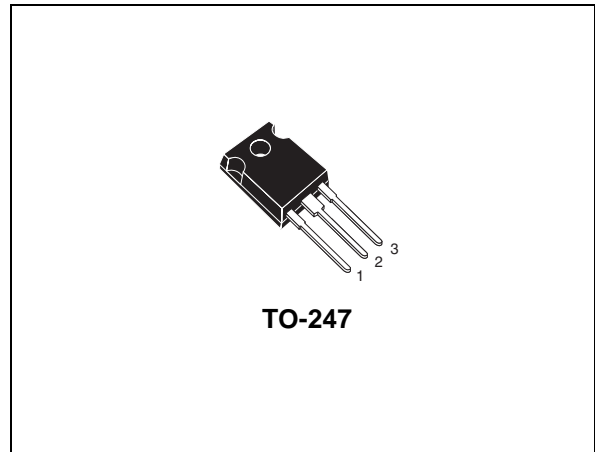


Figure 1. Internal schematic diagram

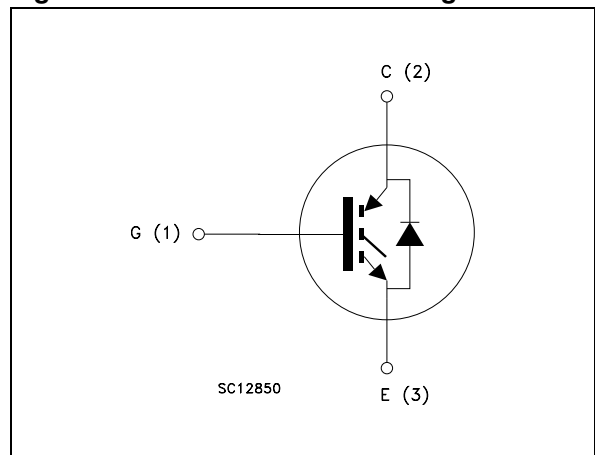


Table 1. Device summary

Order code	Marking	Package	Packaging
STGW40NC60KD	GW40NC60KD	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$)	600	V
$I_C^{(1)}$	Collector current (continuous) at $T_C = 25\text{ °C}$	70	A
$I_C^{(1)}$	Collector current (continuous) at $T_C = 100\text{ °C}$	38	A
$I_{CL}^{(2)}$	Turn-off latching current	220	A
$I_{CP}^{(3)}$	Pulsed collector current	220	A
V_{GE}	Gate-emitter voltage	± 20	V
I_F	Diode RMS forward current at $T_C = 25\text{ °C}$	30	A
I_{FSM}	Surge non repetitive forward current $t_p = 10\text{ ms}$ sinusoidal	120	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	250	W
t_{scw}	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_j = 125\text{ °C}$, $R_G = 10\text{ }\Omega$, $V_{GE} = 12\text{ V}$	10	μs
T_j	Operating junction temperature	- 55 to 150	$^{\circ}\text{C}$

1. Calculated according to the iterative formula:

$$I_c(T_c) = \frac{T_{J(MAX)} - T_c}{R_{thj-c} \times V_{CE(sat)(MAX)} \cdot (T_c, I_c)}$$

2. $V_{clamp} = 80\%, (V_{CES})$, $T_j = 150\text{ °C}$, $R_G = 10\text{ }\Omega$, $V_{GE} = 15\text{ V}$

3. Pulse width limited by max. junction temperature allowed

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case IGBT max.	0.5	$^{\circ}\text{C/W}$
	Thermal resistance junction-case diode max.	1.5	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C/W}$

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage ($V_{GE}=0$)	$I_C=1\text{ mA}$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE}=15\text{ V}$, $I_C=30\text{ A}$		2.1	2.7	V
		$V_{GE}=15\text{ V}$, $I_C=30\text{ A}$, $T_C=125^{\circ}\text{C}$		1.9		V
I_{CES}	Collector cut-off current ($V_{GE}=0$)	$V_{CE}=600\text{ V}$ $V_{CE}=600\text{ V}$, $T_C=125^{\circ}\text{C}$			500 5	μA mA
$V_{GE(th)}$	Gate threshold voltage	$V_{CE}=V_{GE}$, $I_C=250\text{ }\mu\text{A}$	4.5		6.5	V
I_{GES}	Gate-emitter cut-off current ($V_{CE}=0$)	$V_{GE}=\pm 20\text{ V}$			± 100	nA
$g_{fs}^{(1)}$	Forward transconductance	$V_{CE}=15\text{ V}$, $I_C=30\text{ A}$		20		S

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE}=25\text{ V}$, $f=1\text{ MHz}$, $V_{GE}=0$		2870		pF
C_{oes}	Output capacitance			295		pF
C_{res}	Reverse transfer capacitance			69		pF
Q_g	Total gate charge	$V_{CE}=480\text{ V}$, $I_C=30\text{ A}$,		135		nC
Q_{ge}	Gate-emitter charge	$V_{GE}=15\text{ V}$		27		nC
Q_{gc}	Gate-collector charge	(see Figure 18)		69.5		nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 480\text{ V}$, $I_C = 30\text{ A}$		46		ns
t_r	Current rise time	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		18.5		ns
$(di/dt)_{on}$	Turn-on current slope	(see Figure 17)		1530		A/ μ s
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 480\text{ V}$, $I_C = 30\text{ A}$		45		ns
t_r	Current rise time	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		19		ns
$(di/dt)_{on}$	Turn-on current slope	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 17)		1400		A/ μ s
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 480\text{ V}$, $I_C = 30\text{ A}$		38		ns
$t_{d(off)}$	Turn-off delay time	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		164		ns
t_f	Current fall time	(see Figure 17)		87		ns
$t_r(V_{off})$	Off voltage rise time	$V_{CC} = 480\text{ V}$, $I_C = 30\text{ A}$,		70		ns
$t_{d(off)}$	Turn-off delay time	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$		208		ns
t_f	Current fall time	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 17)		130		ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
E_{on}	Turn-on switching losses	$V_{CC} = 480\text{ V}$, $I_C = 30\text{ A}$		595		μ J
$E_{off}^{(1)}$	Turn-off switching losses	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		716		μ J
E_{ts}	Total switching losses	(see Figure 17)		311		μ J
E_{on}	Turn-on switching losses	$V_{CC} = 480\text{ V}$, $I_C = 30\text{ A}$		808		μ J
$E_{off}^{(1)}$	Turn-off switching losses	$R_G = 10\ \Omega$, $V_{GE} = 15\text{ V}$,		1200		μ J
E_{ts}	Total switching losses	$T_C = 125\text{ }^\circ\text{C}$ (see Figure 17)		2008		μ J

1. Turn-off losses include also the tail of the collector current.

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_F	Forward on-voltage	$I_F = 30\text{ A}$ $I_F = 30\text{ A}, T_C = 125\text{ °C}$		2.4 1.8		V V
t_{rr}	Reverse recovery time	$I_F = 30\text{ A}, V_R = 50\text{ V},$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 20)		45		ns
Q_{rr}	Reverse recovery charge			56		nC
I_{rrm}	Reverse recovery current			2.55		A
t_{rr}	Reverse recovery time	$I_F = 30\text{ A}, V_R = 50\text{ V},$ $T_C = 125\text{ °C}, di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 20)		100		ns
Q_{rr}	Reverse recovery charge			290		nC
I_{rrm}	Reverse recovery current			5.8		A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

Figure 3. Transfer characteristics

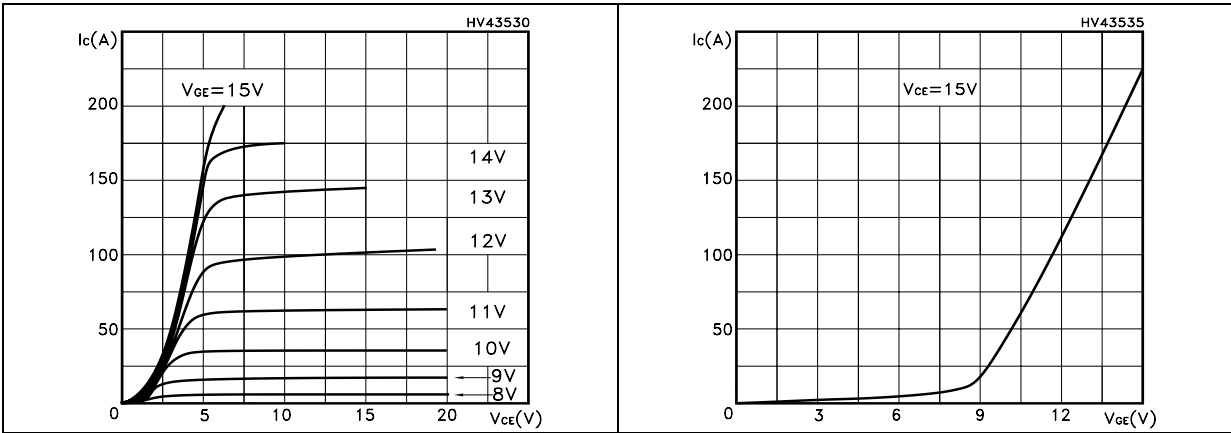


Figure 4. Transconductance

Figure 5. Collector-emitter on voltage vs temperature

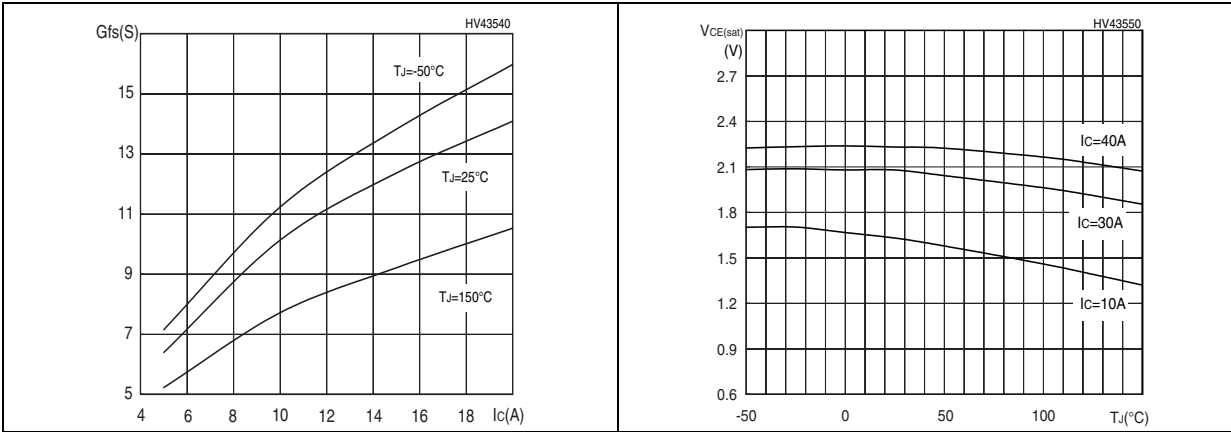


Figure 6. Gate charge vs gate-source voltage

Figure 7. Capacitance variations

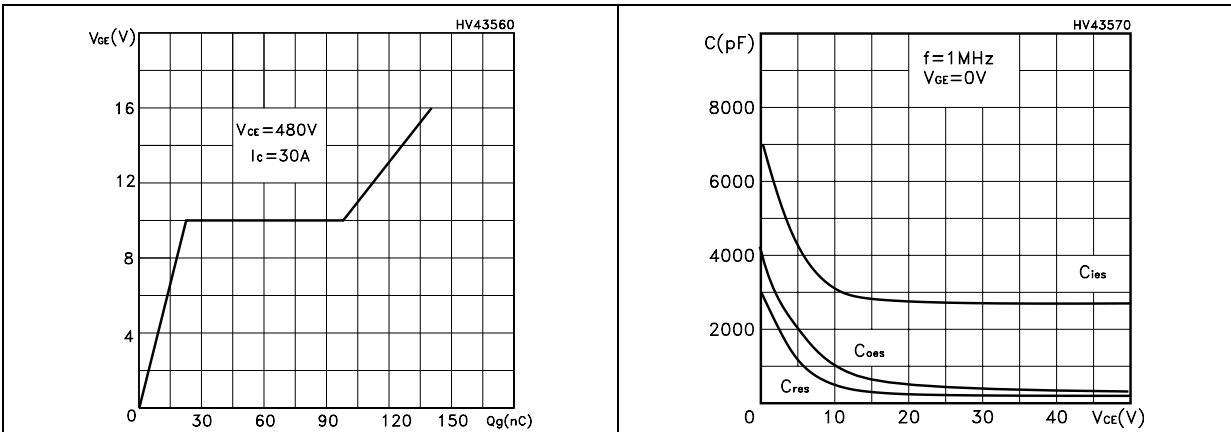


Figure 8. Normalized gate threshold voltage vs temperature

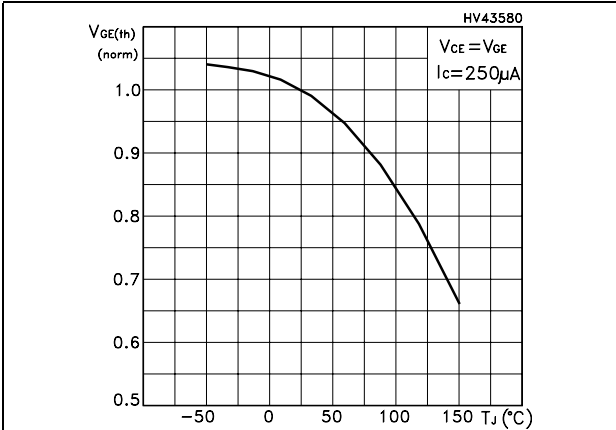


Figure 9. Collector-emitter on voltage vs collector current

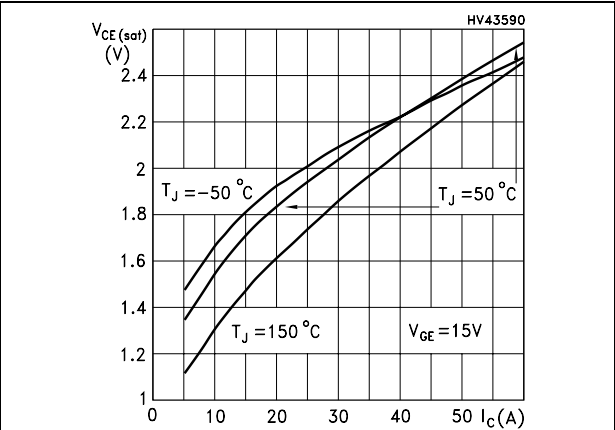


Figure 10. Normalized breakdown voltage vs temperature

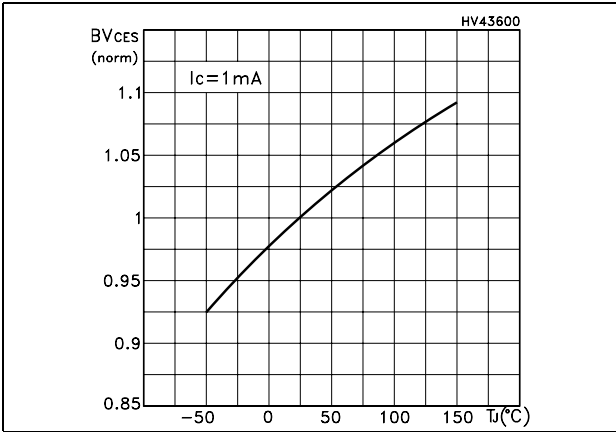


Figure 11. Switching losses vs temperature

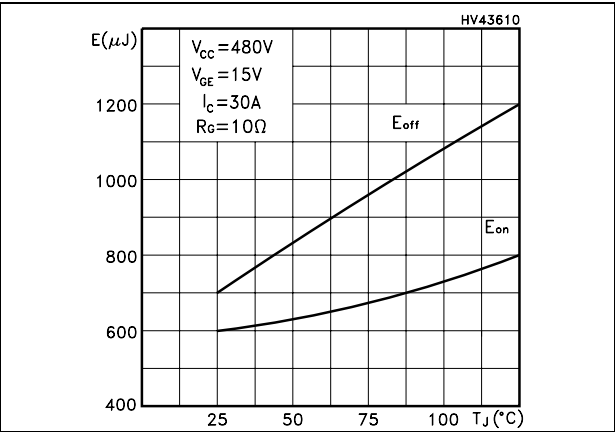


Figure 12. Switching losses vs gate resistance

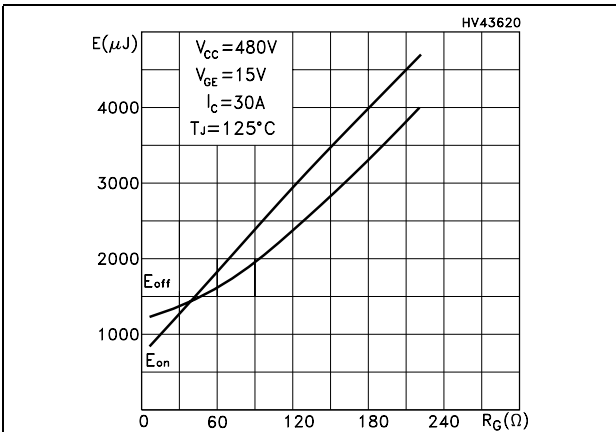


Figure 13. Switching losses vs collector current

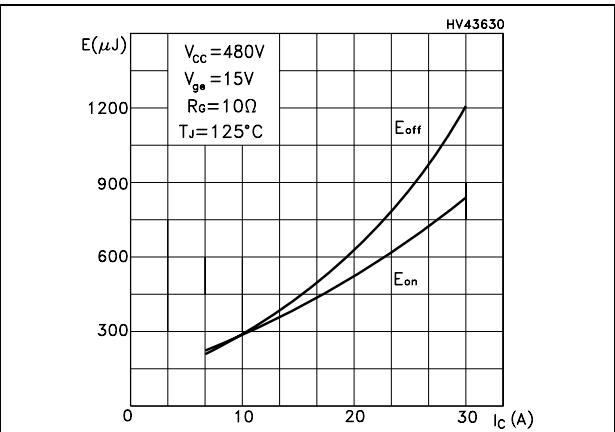


Figure 14. Thermal Impedance

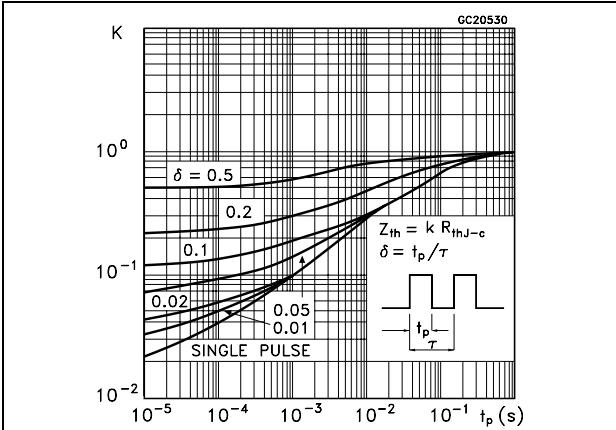


Figure 15. Turn-off SOA

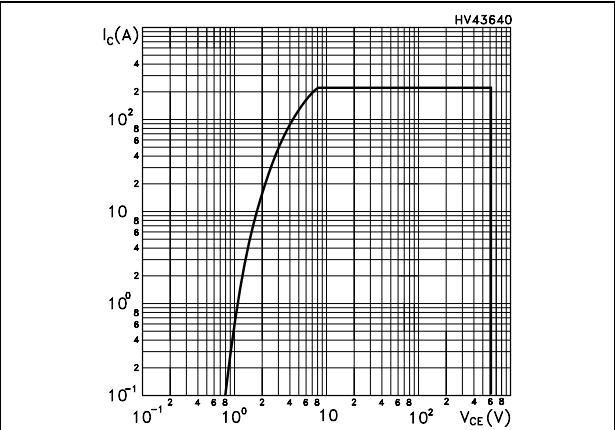
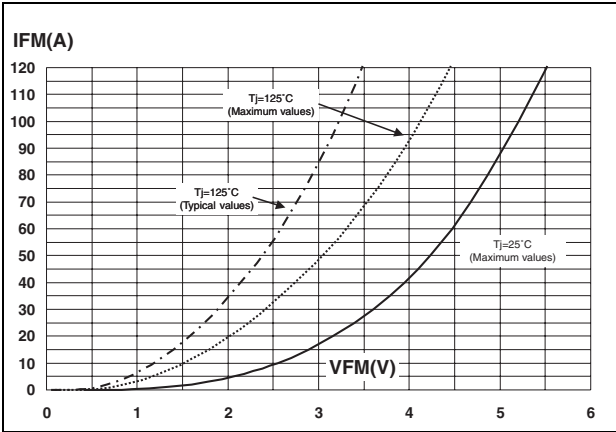


Figure 16. Forward voltage drop versus forward current



3 Test circuit

Figure 17. Test circuit for inductive load switching

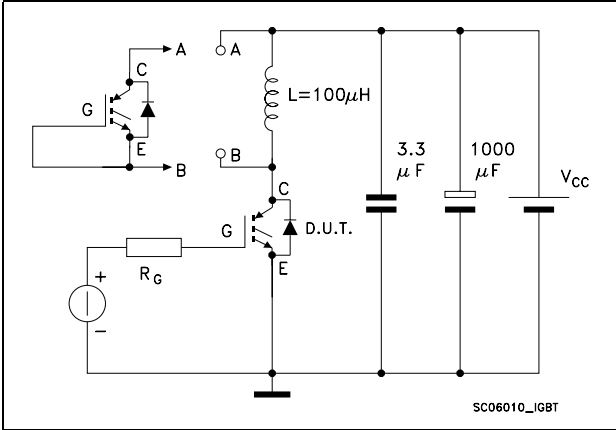


Figure 18. Gate charge test circuit

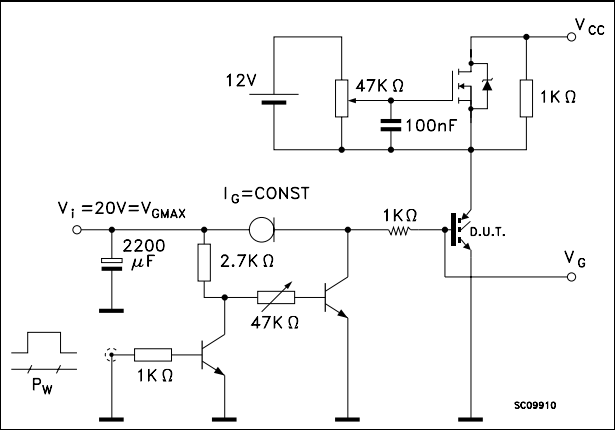


Figure 19. Switching waveforms

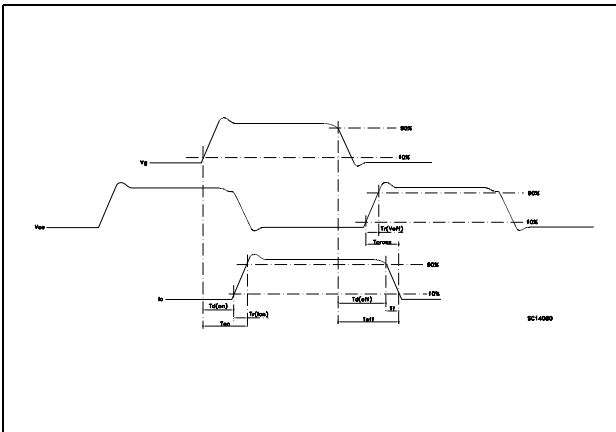
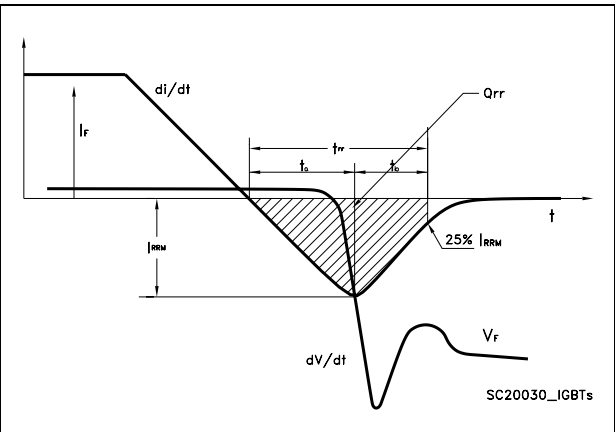


Figure 20. Diode recovery times waveform

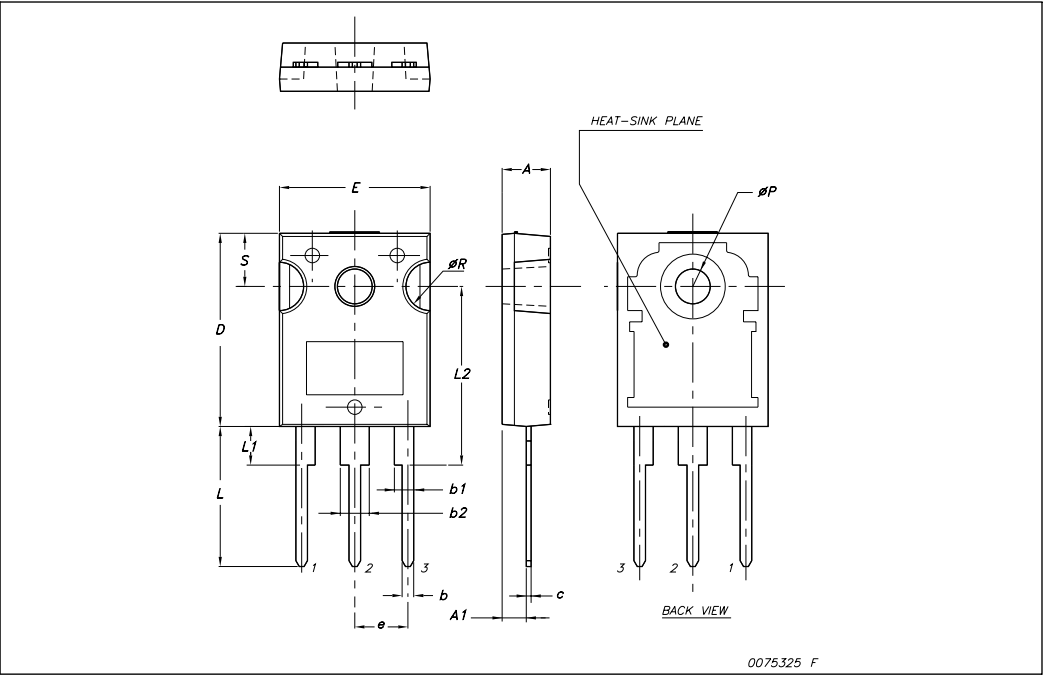


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



0075325 F

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
11-Jun-2008	1	Initial release

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