TXB0104-Q1 4-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing and ±15-kV ESD Protection

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, All Outputs are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A port
    - ±2500-V Human-Body Model (A114-B)
    - ±1000-V Charged-Device Model (C101)
  - B port
    - ±15000-V Human-Body Model (A114-B)
    - ±1000-V Charged-Device Model (C101)

2 Applications

- Automotive infotainment
- Advanced Driver Assistance System (ADAS)
- Telematics

3 Description

Voltage-level translators address the challenges posed by simultaneous use of different supply-voltage levels on the same circuit board. This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. VCCA accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. VCCB accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The TXB0104 is designed so that the OE input circuit is supplied by V_{CCA}.

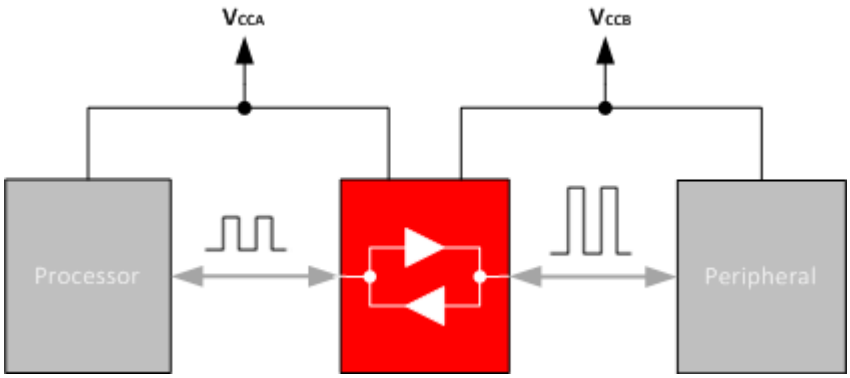
This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0104-Q1	TSSOP (14)	5.00 mm x 4.40 mm
	VQFN (14)	3.50 mm x 3.50 mm
	UQFN (12)	2.00 mm x 1.70 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Block Diagram for TXB010X



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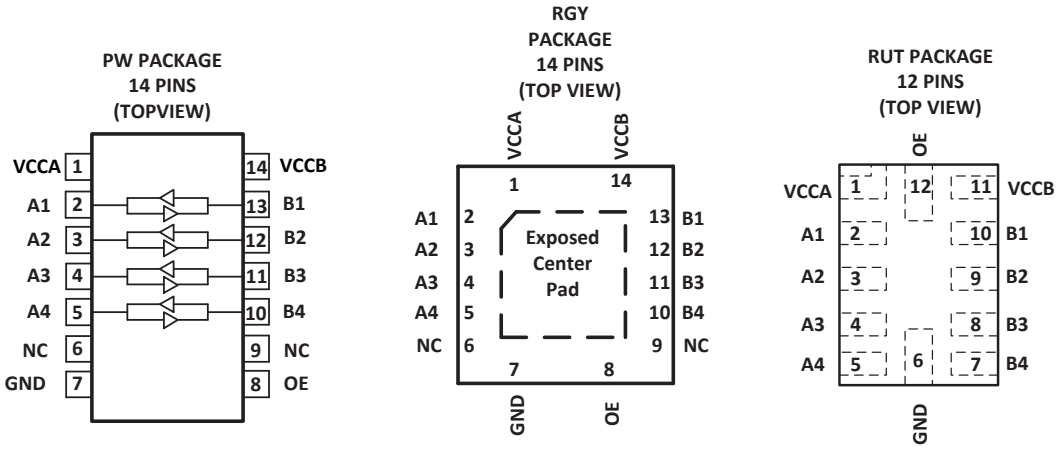
4 Revision History

Changes from Original (June 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions



NC − No internal connection

For RGY, if the exposed center pad is used, it must be connected only to as a secondary ground or left electrically open.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCCA	I	A-port supply voltage 1.2 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}.
2	A1	I/O	Input/output 1. Referenced to V_{CCA}.
3	A2	I/O	Input/output 2. Referenced to V_{CCA}.
4	A3	I/O	Input/output 3. Referenced to V_{CCA}.
5	A4	I/O	Input/output 4. Referenced to V_{CCA}.
6	NC	–	No connection. Not internally connected.
7	GND	–	Ground
8	OE	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
9	NC	–	No connection. Not internally connected.
10	B4	I/O	Input/output 4. Referenced to V_{CCB}.
11	B3	I/O	Input/output 3. Referenced to V_{CCB}.
12	B2	I/O	Input/output 2. Referenced to V_{CCB}.
13	B1	I/O	Input/output 1. Referenced to V_{CCB}.
14	VCCB	I	B-port supply voltage 1.65 V ≤ V_{CCB} ≤ 5.5 V.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.6	V
V_{CCB}			–0.5	6.5	
V_I	Input voltage	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	-0.5	6.5	
V_O	Voltage applied to any output in the high or low state(2)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per JEDEC	A Port	±2500	V
			B Port	±15000	
		Charged-device model (CDM), per JEDEC	A Port	±1000	
			B Port	±1000	

6.3 Recommended Operating Conditions(1)(2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} × 0.65(3)	V_{CCI}	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V_{CCI} × 0.35(3)	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	0	V_{CCA} × 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A-port	1.2 V to 3.6 V	1.65 V to 5.5 V	0	3.6	V
		B-port			0	5.5	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	
T_A	Operating free-air temperature				–40	125	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC[1]		TXB0104-Q1			UNIT
		PW	RGY	RUT	
		14 PINS	14 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121	52.8	119.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	67.7	42.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	28.9	52.5	
ψ_{JT}	Junction-to-top characterization parameter	6.4	2.6	0.7	
ψ_{JB}	Junction-to-board characterization parameter	62.2	29.0	52.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.3	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{OHA}		I_{OH} = –20 µA	1.2 V			1.1					V
			1.4 V to 3.6 V					V_{CCA} – 0.4			
V_{OLA}		I_{OL} = 20 µA	1.2 V			0.9					V
			1.4 V to 3.6 V							0.4	
V_{OHB}		I_{OH} = –20 µA		1.65 V to 5.5 V				V_{CCB} – 0.4			V
V_{OLB}		I_{OL} = 20 µA		1.65 V to 5.5 V						0.4	V
I_I	OE	V_I = V_{CCI} or GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1			±5	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 V to 5.5 V			±1			±10	µA
	B port	V_I or V_O = 0 to 5.5 V	0 V to 3.6 V	0 V			±1			±10	
I_{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1			±10	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		0.06					µA
			1.4 V to 3.6 V	1.65 V to 5.5 V						20	
			3.6 V	0 V						15	
			0 V	5.5 V						–15	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.4					µA
			1.4 V to 3.6 V	1.65 V to 5.5 V						20	
			3.6 V	0 V						–15	
			0 V	5.5 V						15	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.5					µA
			1.4 V to 3.6 V	1.65 V to 5.5 V						40	
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05					µA
			1.4 V to 3.6 V	1.65 V to 5.5 V						15	
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3					µA
			1.4 V to 3.6 V	1.65 V to 5.5 V						15	
C_i	OE	PW, RGY package	1.2 V to 3.6 V	1.65 V to 5.5 V		3					pF
		RUT package	1.2 V to 3.6 V	1.65 V to 5.5 V		4					pF
C_{io}	A port	PW, RGY package	1.2 V to 3.6 V	1.65 V to 5.5 V		5					pF
		RUT package				6					pF
	B port	PW, RGY package				11					pF
		RUT package				13					pF

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

6.6 Timing Requirements: V_{CCA} = 1.2 V

T_A = 25°C, V_{CCA} = 1.2 V

			V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
	Data rate	For PW, RGY, RUT package	20	20	20	20	Mbps
t_w	Pulse duration	Data inputs	50	50	50	50	ns

6.7 Timing Requirements: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	For PW, RGY package		40		40		40		40	Mbps
		For RUT package		37		37		40		40	Mbps
t_w	Pulse duration	Data inputs, For PW, RGY package	25		25		25		25		ns
		Data inputs, For RUT package	27		27		25		25		ns

6.8 Timing Requirements: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	For PW, RGY package		55		55		55		55	Mbps
		For RUT package		37		37		55		55	Mbps
t_w	Pulse duration	Data inputs, For PW, RGY package	18		18		18		18		ns
		Data inputs, For RUT package	27		27		18		18		ns

6.9 Timing Requirements: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

			V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	For PW, RGY package		75		80		100	Mbps
		For RUT package		65		80		85	Mbps
t_w	Pulse duration	Data inputs, For PW, RGY package	13		12		10		ns
		Data inputs, For RUT package	15		12		11		ns

6.10 Timing Requirements: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

			V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
	Data rate	For PW, RGY package		100		100	Mbps
		For RUT package		90		90	Mbps
t_w	Pulse duration	Data inputs, For PW, RGY package	10		10		ns
		Data inputs, For RUT package	11		11		ns

6.11 Switching Characteristics: V_{CCA} = 1.2 V

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
t_{pd}	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
t_{en}	OE	A	1	1	1	1	µs
		B	1	1	1	1	
t_{dis}	OE	A	320	320	320	330	ns
		B	150	110	150	110	
t_{rA}, t_{fA}	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
t_{rB}, t_{fB}	B-port rise and fall times		2.1	1.5	1.2	1.1	ns

6.12 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		15.9		13.1		13		12.9	ns
	B	A		17.2		15		14.7		16.7	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A		340		280		280		300	ns
		B		220		220		220		220	
t_{rA}, t_{fA}	A-port rise and fall times			7.1		7.1		7.1		7.1	ns
t_{rB}, t_{fB}	B-port rise and fall times			6.5		5.2		4.8		4.7	ns

6.13 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		14		10.7		9.8		9.5	ns
	B	A		15		11.4		10.6		10.1	
t_{en}	OE	A		1		1		1		1	µs
		B		1		1		1		1	
t_{dis}	OE	A		280		250		250		250	ns
		B		220		220		220		220	
t_{rA}, t_{fA}	A-port rise and fall times			6.2		6.1		6.1		6.1	ns
t_{rB}, t_{fB}	B-port rise and fall times			5.8		5.2		4.8		4.7	ns

6.14 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B		9.3		8.2		7.7	ns
	B	A		9.6		8.1		7.4	
t_{en}	OE	A		1		1		1	µs
		B		1		1		1	
t_{dis}	OE	A		220		220		220	ns
		B		220		220		220	
t_{rA}, t_{fA}	A-port rise and fall times			5		5		5	ns
t_{rB}, t_{fB}	B-port rise and fall times			4.6		4.8		4.7	ns

6.15 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A	B		7.7		7	ns
	B	A		7.9		6.8	
t_{en}	OE	A		1		1	µs
		B		1		1	
t_{dis}	OE	A		280		280	ns
		B		220		220	
t_{rA}, t_{fA}	A-port rise and fall times			4.5		4.5	ns
t_{rB}, t_{fB}	B-port rise and fall times			4.1		4.7	ns

6.16 Operating Characteristics(1)

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}							UNIT
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			V_{CCB}							
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns, OE = V_{CCA} (outputs enabled)	7.8	10	9	8	8	8	9	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C_{pdB}	A-port input, B-port output		38.1	28	28	28	29	29	29	
	B-port input, A-port output		25.4	19	18	18	19	21	22	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, $t_r = t_f$ = 1 ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C_{pdB}	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.04	

(1) Cpd parameter is the capacitance used to determine the no-load dynamic power dissipation per logic function for CMOS devices as per the formula: $P_D = C_{pd} (V_{CC})^2 + I_{CC}V_{CC}$. For more details about the use of C_{pd} to calculate power dissipation, refer to SCAA035.

6.17 Typical Characteristics

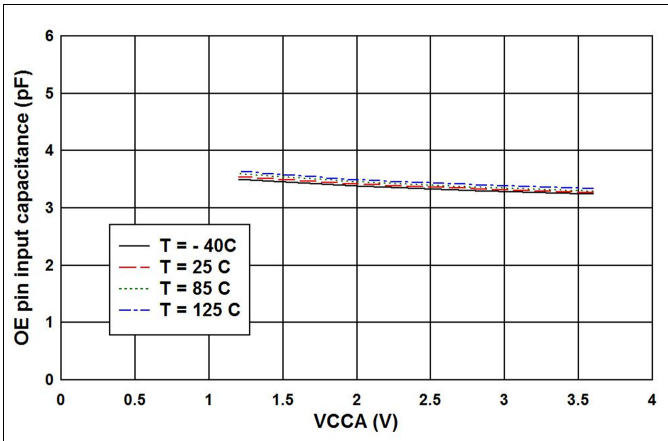


Figure 1. Input capacitance for OE pin (C_I) vs Power Supply (V_{CCA}) for V_{CCB} = 3.3 V (RUT package)

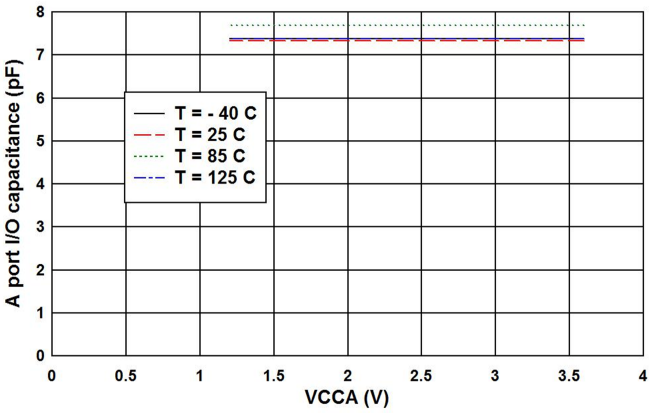


Figure 2. Capacitance for A port I/O pins (C_{IO}) vs Power Supply (V_{CCA}) for V_{CCB} = 3.3 V (RUT package)

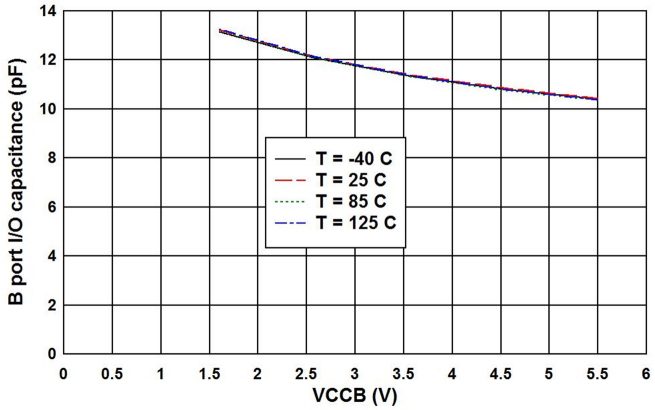
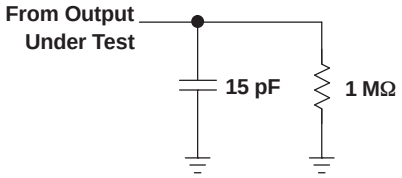
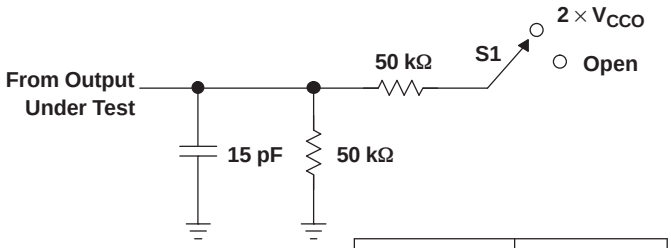


Figure 3. Capacitance for B port I/O pins (C_{IO}) vs Power Supply (V_{CCB}) for V_{CCA} = 3.3 V (RUT package)

7 Parameter Measurement Information

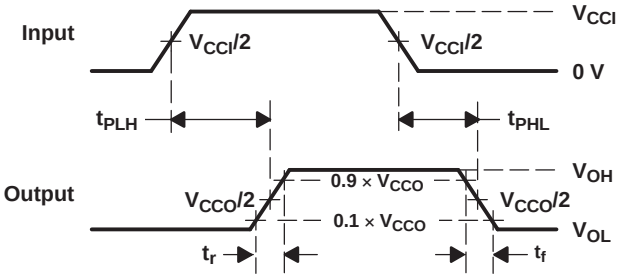


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

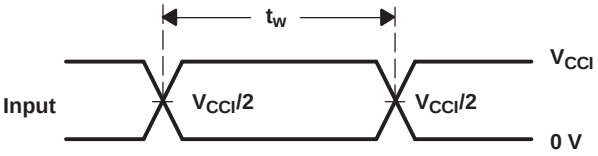


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2 \times V_{CCO}$ Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

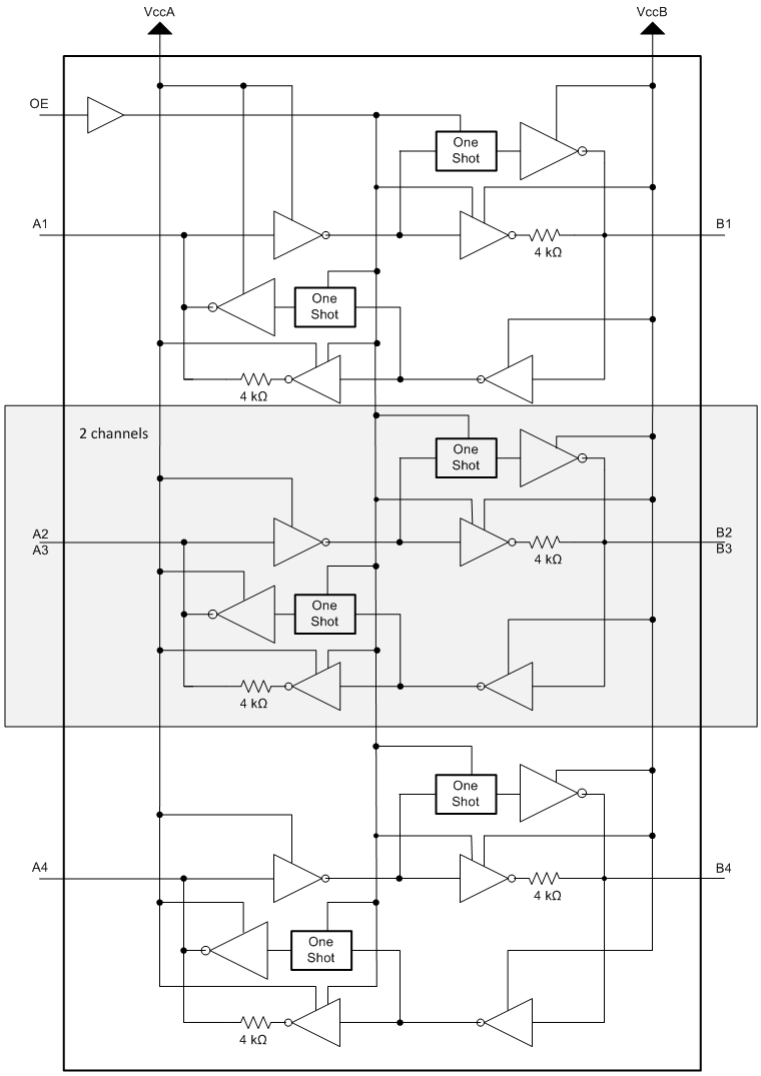
Figure 4. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TXB0104 device is a 4-bit, bi-directional voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI's TXS010X products.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TXB0104 architecture (see *Functional Block Diagram*) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0104 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

Feature Description (continued)

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V, and 40 Ω at V_{CCO} = 3.3 V to 5 V.

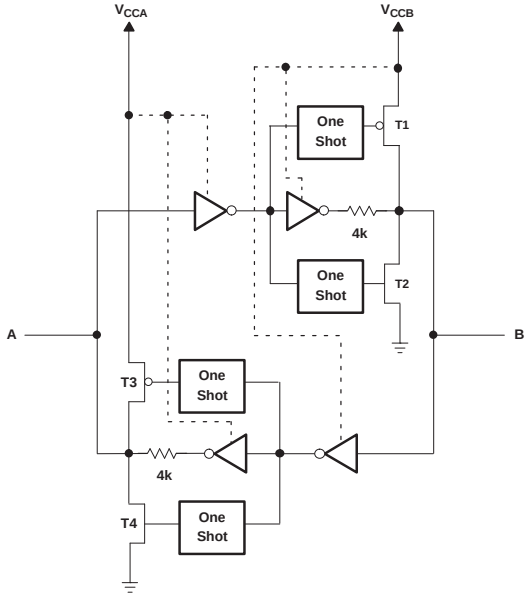
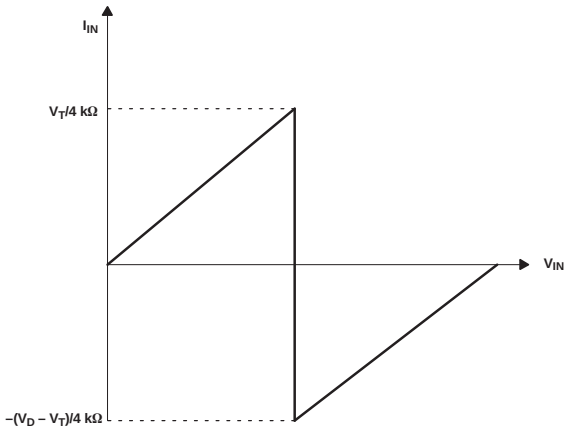


Figure 5. Architecture of TXB0104 I/O Cell

8.3.2 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0104 are shown in Figure 6. For proper operation, the device driving the data I/Os of the TXB0104 must have drive strength of at least ±2 mA.



A. V_T is the input threshold voltage of the TXB0104 (typically $V_{CCI}/2$).
B. V_D is the supply voltage of the external driver.

Figure 6. Typical I_{IN} vs V_{IN} Curve

Feature Description (continued)

8.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one shot (O.S.) triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0104 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.4 Enable and Disable

The TXB0104 has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

8.3.5 Pullup or Pulldown Resistors on I/O Lines

The TXB0104 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0104 have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to ensure that they do not contend with the output drivers of the TXB0104.

For the same reason, the TXB0104 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

8.4 Device Functional Modes

The TXB0104 device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0104 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.

9.2 Typical Application

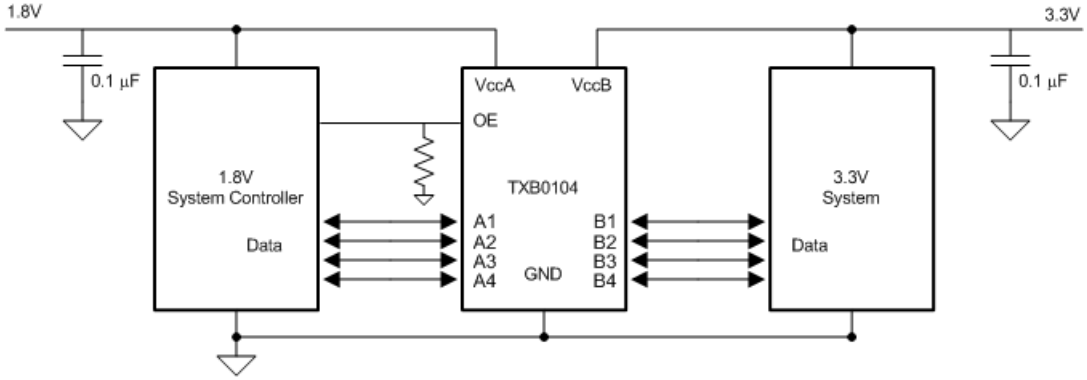


Figure 7. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. And make sure the $V_{CCA} \leq V_{CCB}$.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0104 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0104 device is driving to determine the output voltage range.
  - It is not recommended to have the external pullup or pulldown resistors. If mandatory, it is recommended the value should be larger than 50 kΩ.
- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use the below equations to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\ k\Omega) \quad (1)$$

$$V_{OL} = V_{CCx} \times 4.5\ k\Omega / (R_{PU} + 4.5\ k\Omega)$$

where

- V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 4.5 kΩ is the counting the variation of the serial resistor 4 kΩ in the I/O line (2)

9.2.3 Application Curve

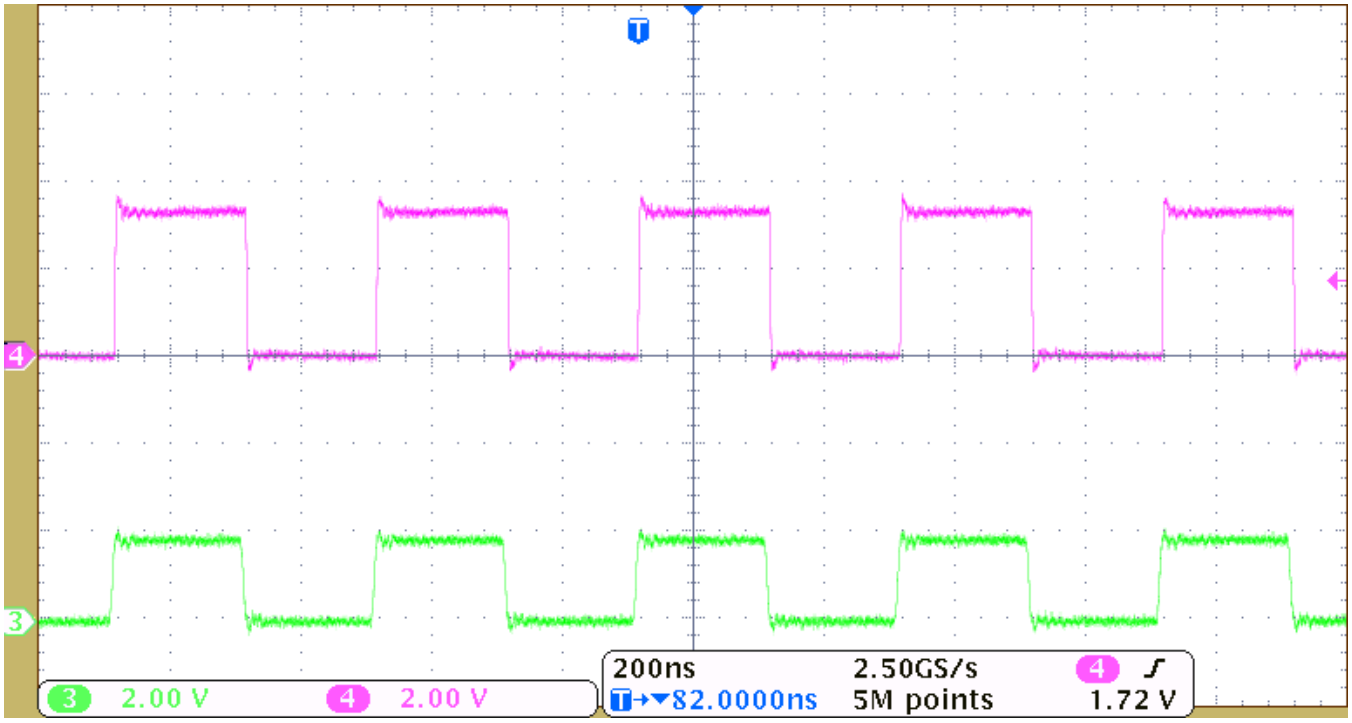


Figure 8. Example of Level Translation of a 2.5-MHz 1.8 V Signal (Green) to a 3.3 V Signal (Pink)

10 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0104 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V). The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the VCCA, VCCB pin, and GND pin
- Short trace-lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example

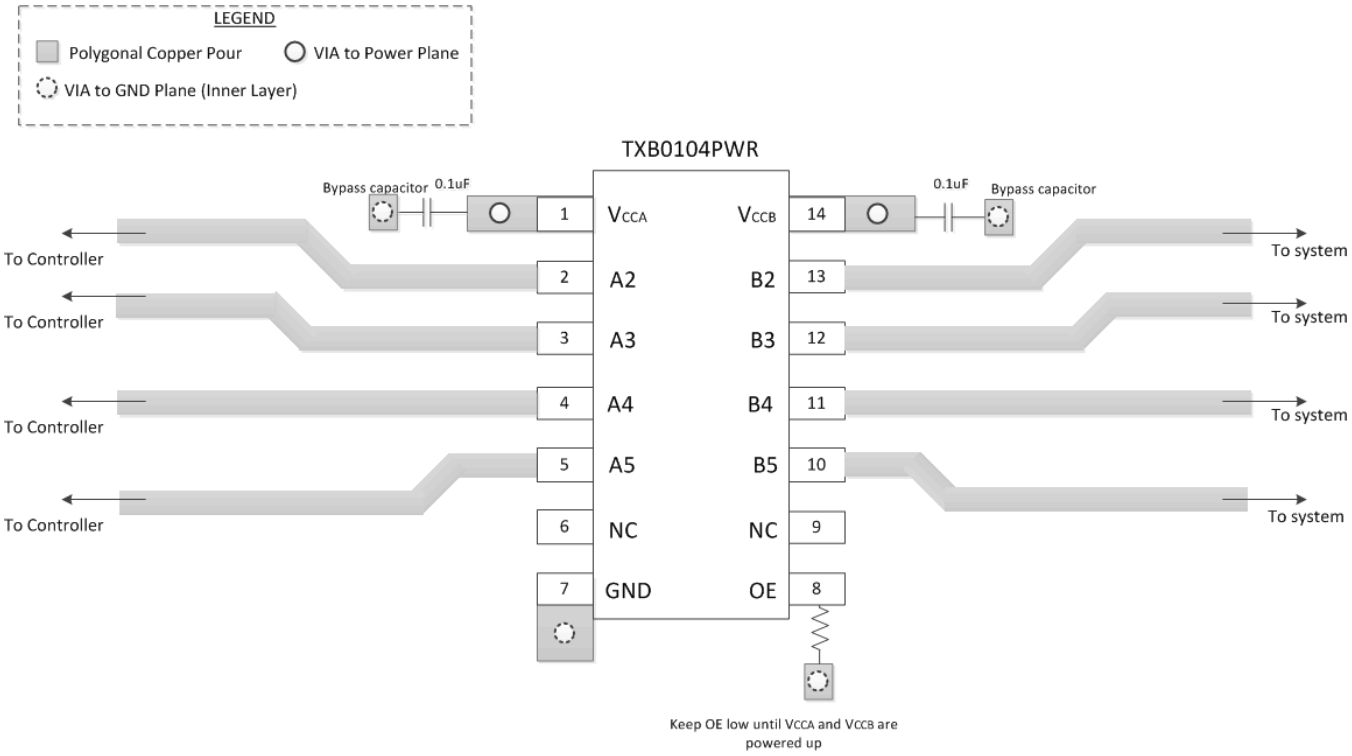


Figure 9. Layout Example Schematic

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0104QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YE04Q1	Samples
TXB0104QRGYRQ1	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	YE04Q1	Samples
TXB0104QRUTRQ1	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SIG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXB0104-Q1 :

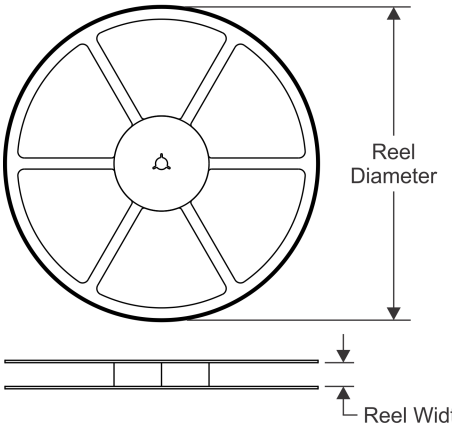
- Catalog: TXB0104

NOTE: Qualified Version Definitions:

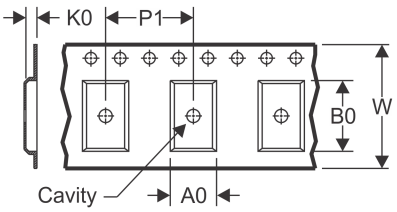
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

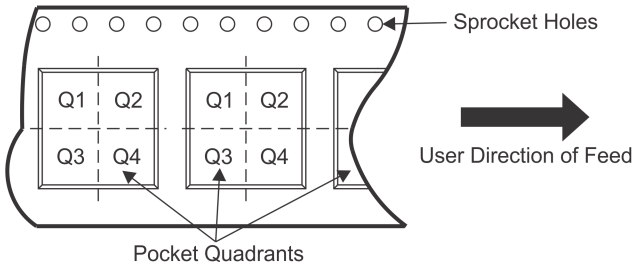


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

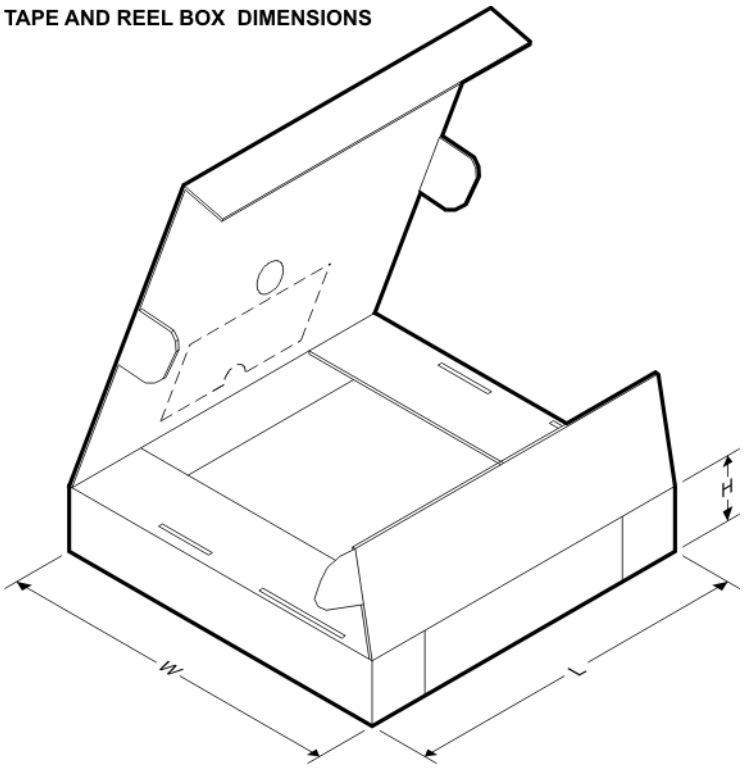
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0104QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXB0104QRGYRQ1	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXB0104QRUTRQ1	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

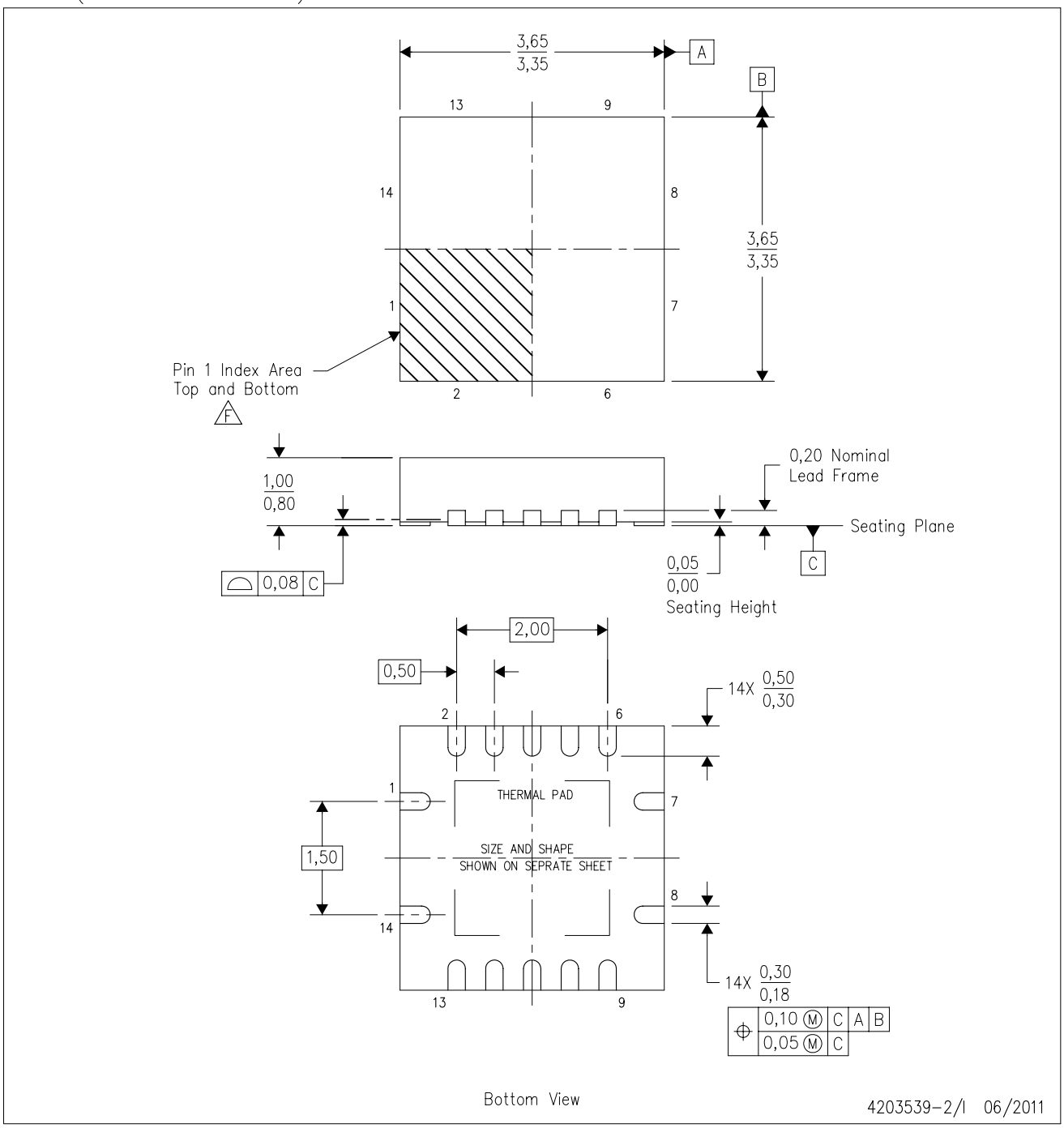
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0104QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
TXB0104QRGYRQ1	VQFN	RGY	14	3000	367.0	367.0	35.0
TXB0104QRUTRQ1	UQFN	RUT	12	3000	202.0	201.0	28.0

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

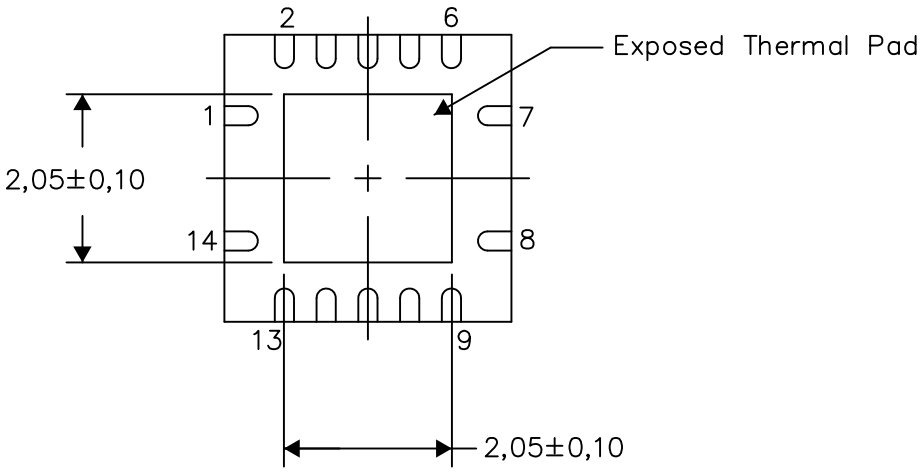
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



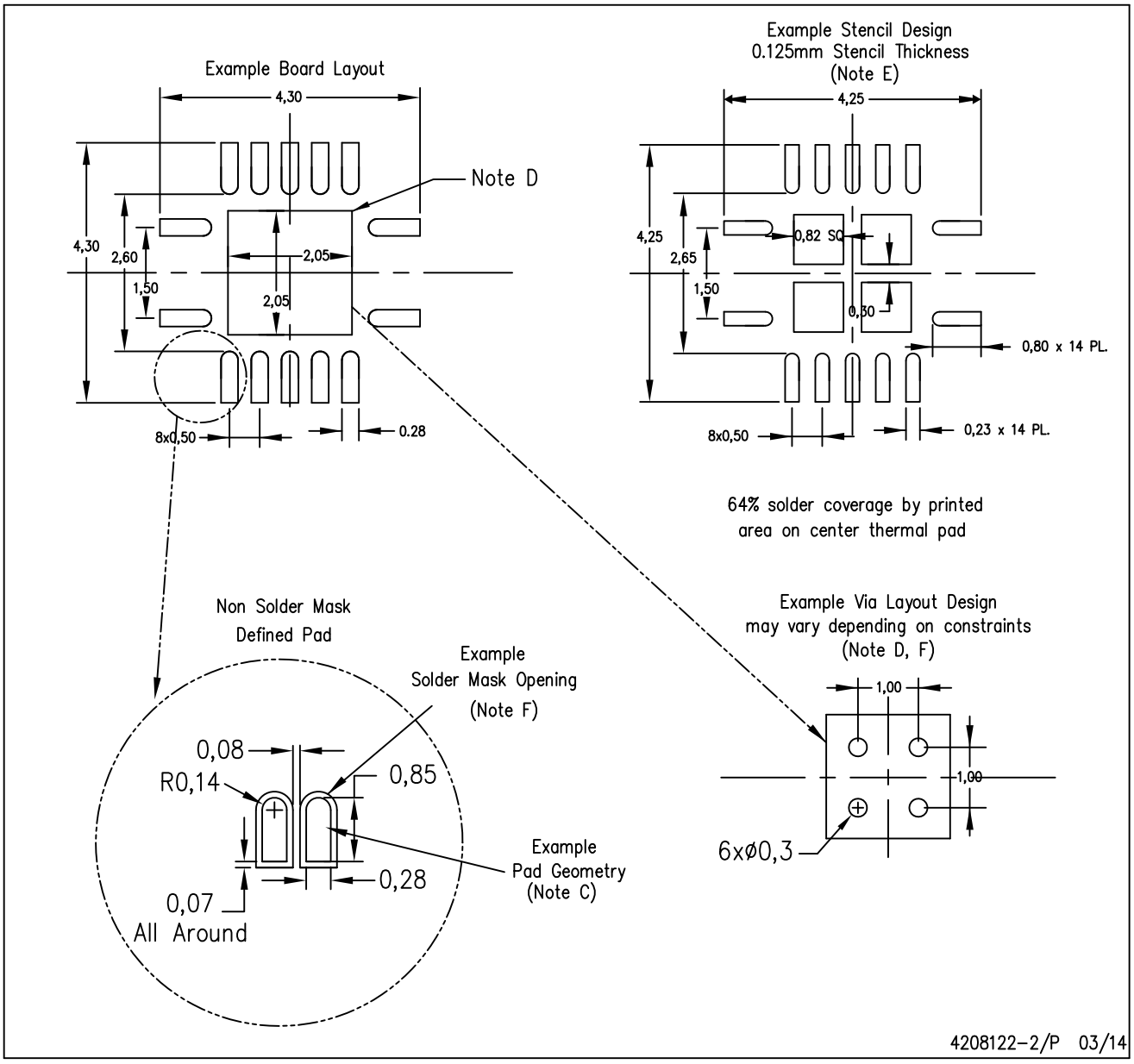
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

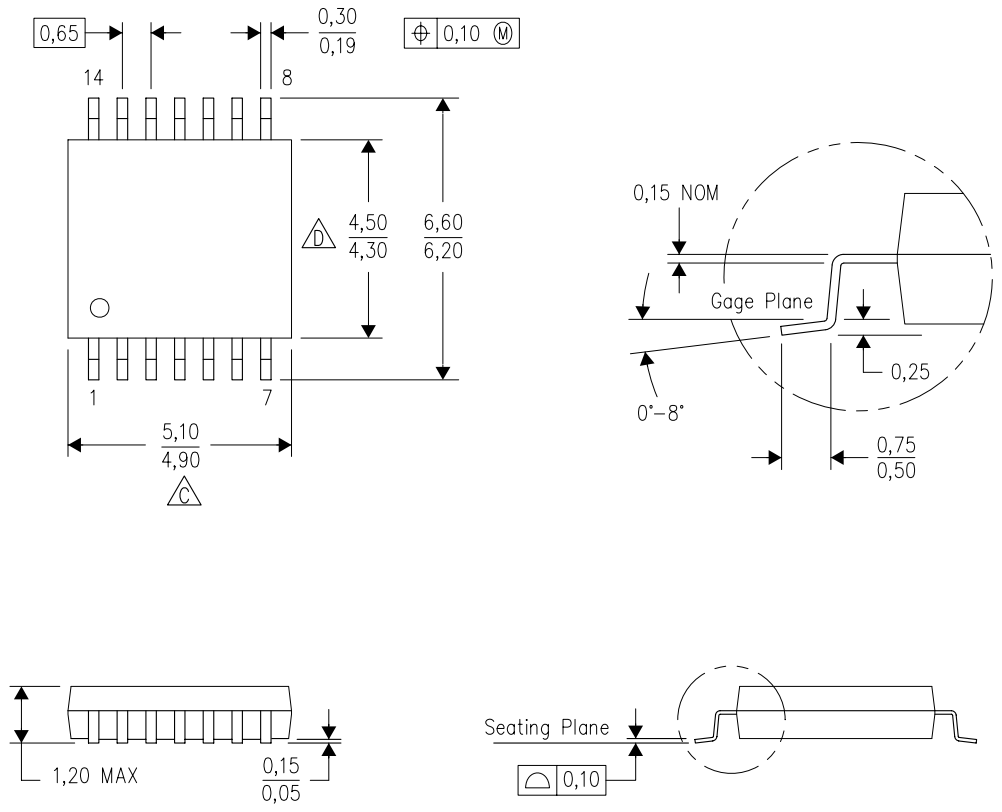
NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

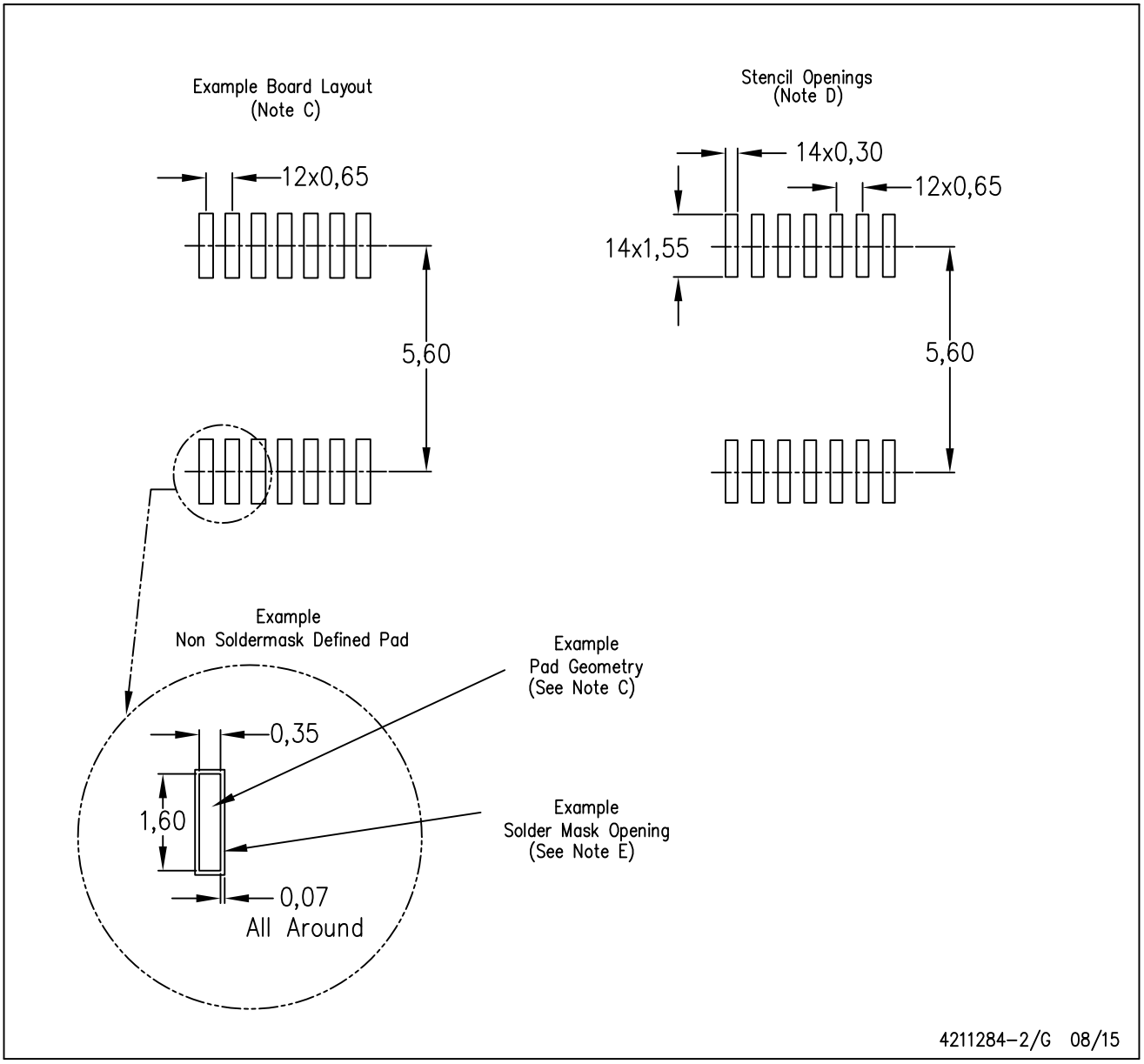
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

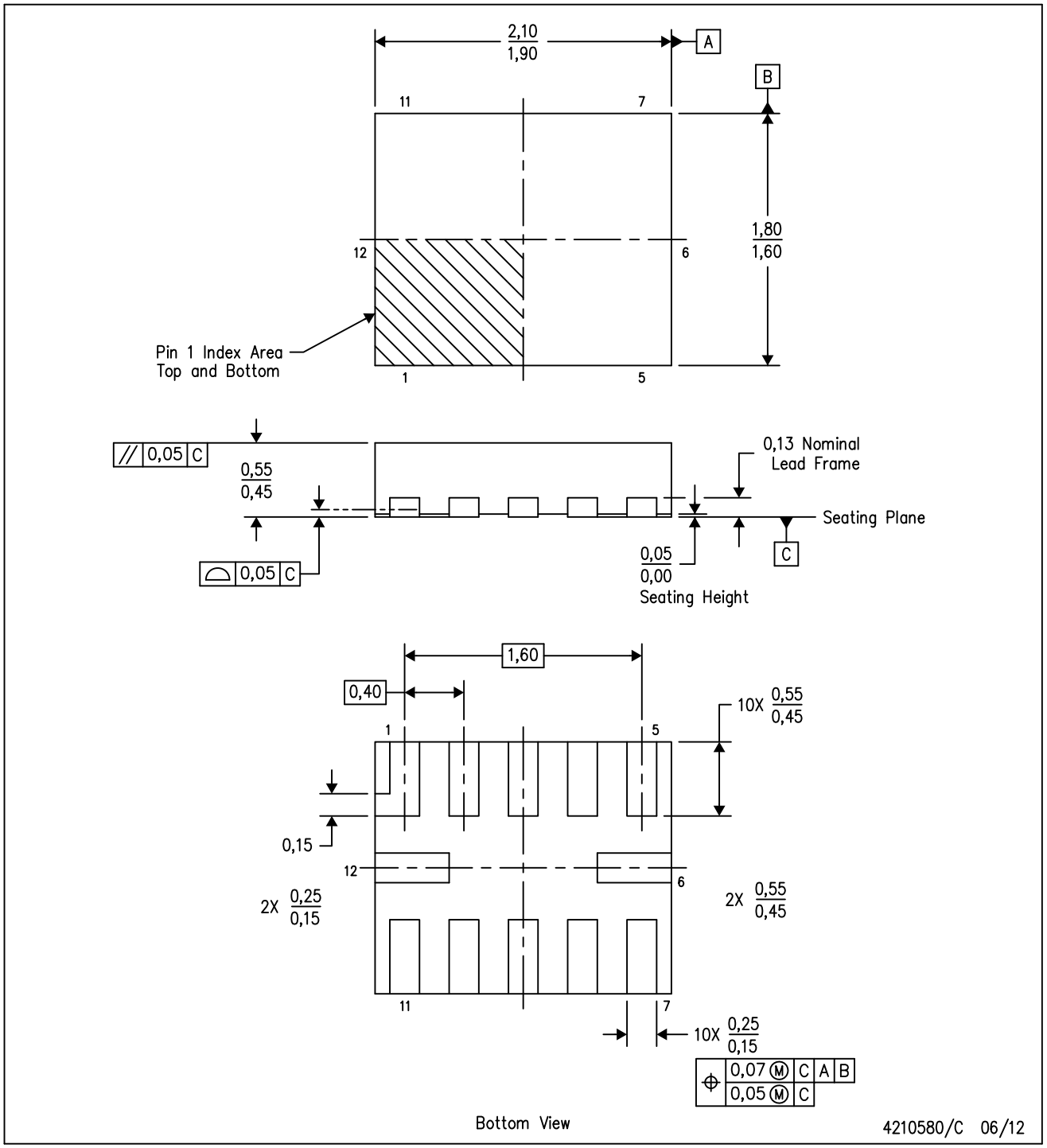
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



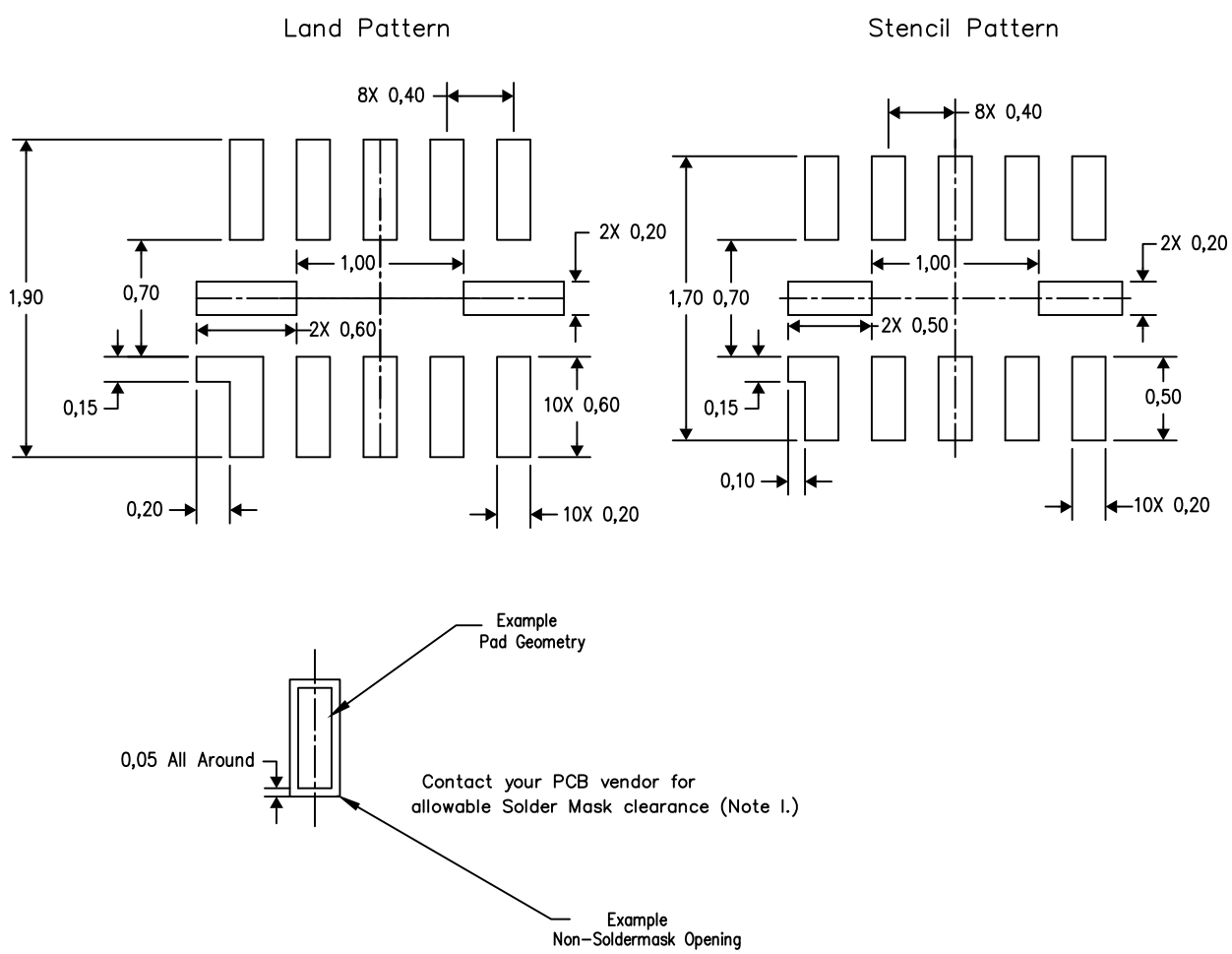
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

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