Si8410/20/21 (5 kV) Si8422/23 (2.5 & 5 kV) Data Sheet

Low-Power, Single and Dual-Channel Digital Isolators

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require V_{DD} bypass capacitors.

Data rates up to 150 Mbps are supported, and all devices achieve worst-case propagation delays of less than 10 ns. Ordering options include a choice of isolation ratings (up to 5 kV) and a selectable fail-safe operating mode to control the default output state during power loss. All products are safety certified by UL, CSA, and VDE, and products in wide-body packages support reinforced insulation withstanding up to 5 kV_{RMS}.

Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communication systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-5 (VDE0884 Part 5)
  - EN60950-1 (reinforced insulation)

KEY FEATURES

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage:
  - 2.6 – 5.5 V
- Up to 5000 V_{RMS} isolation
- High electromagnetic immunity
- Ultra low power (typical)
  - 5 V Operation:
    - < 2.6 mA/channel at 1 Mbps
    - < 6.8 mA/channel at 100 Mbps
  - 2.70 V Operation:
    - < 2.3 mA/channel at 1 Mbps
    - < 4.6 mA/channel at 100 Mbps
- Schmitt trigger inputs
- Selectable fail-safe mode
  - Default high or low output
- Precise timing (typical)
  - 11 ns propagation delay max
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 5 ns minimum pulse width
- Transient immunity 45 kV/µs
- AEC-Q100 qualification
- Wide temperature range
  - –40 to 125 °C at 150 Mbps
- RoHS compliant packages
  - SOIC-16 wide body
  - SOIC-8 narrow body

1. Features List

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2. Ordering Guide

Table 2.1. Ordering Guide[1,2,3]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Default Output State	Isolation Rating	Temp Range	Package Type
Si8422AB-D-IS	1	1	1	High	2.5 kVrms	–40 to 125 °C	NB SOIC-8
Si8422BB-D-IS	1	1	150	High			
Si8423AB-D-IS	2	0	1	High			
Si8423BB-D-IS	2	0	150	High			
Si8410AD-D-IS[4]	1	0	1	Low	5.0 kVrms	–40 to 125 °C	WB SOIC-16
Si8410BD-D-IS[4]	1	0	150	Low			
Si8420AD-D-IS[4]	2	0	1	Low			
Si8420BD-D-IS[4]	2	0	150	Low			
Si8421AD-D-IS[4]	1	1	1	Low			
Si8421BD-D-IS[4]	1	1	150	Low			
Si8422AD-D-IS	1	1	1	High			
Si8422BD-D-IS	1	1	150	High			
Si8423AD-D-IS	2	0	1	High			
Si8423BD-D-IS	2	0	150	High			

1. All devices >1 kV_{RMS} are AEC-Q100 qualified.
2. “Si” and “SI” are used interchangeably.
3. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
4. Refer to Si8410/20/21 data sheet for information regarding 2.5 kV rated versions of these products.
5. An "R" at the end of the part number denotes tape and reel packaging option.

3. Functional Description

3.1 Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si84xx channel is shown in the figure below.

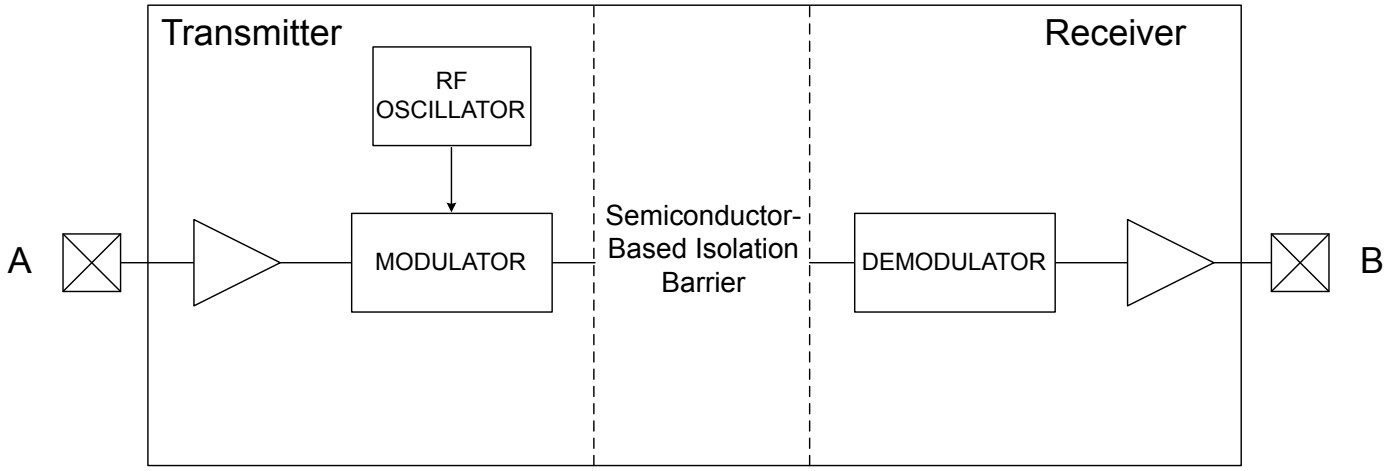


Figure 3.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

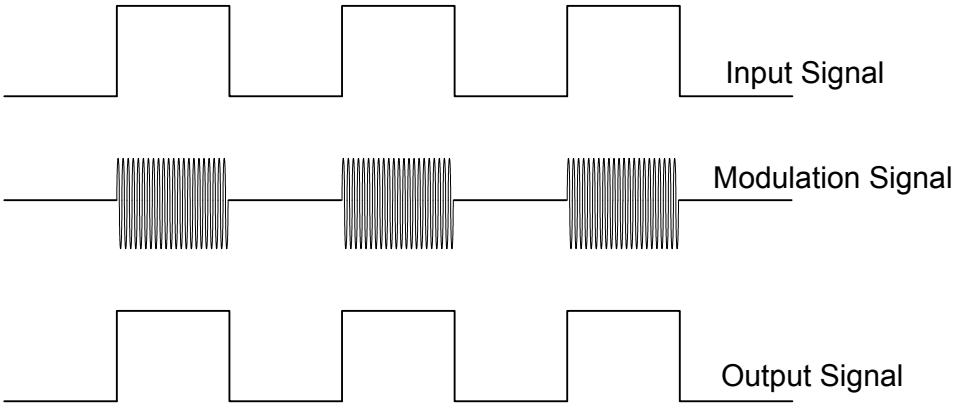


Figure 3.2. Modulation Scheme

3.2 Eye Diagram

The figure below illustrates an eye-diagram taken on an Si8422. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8422 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

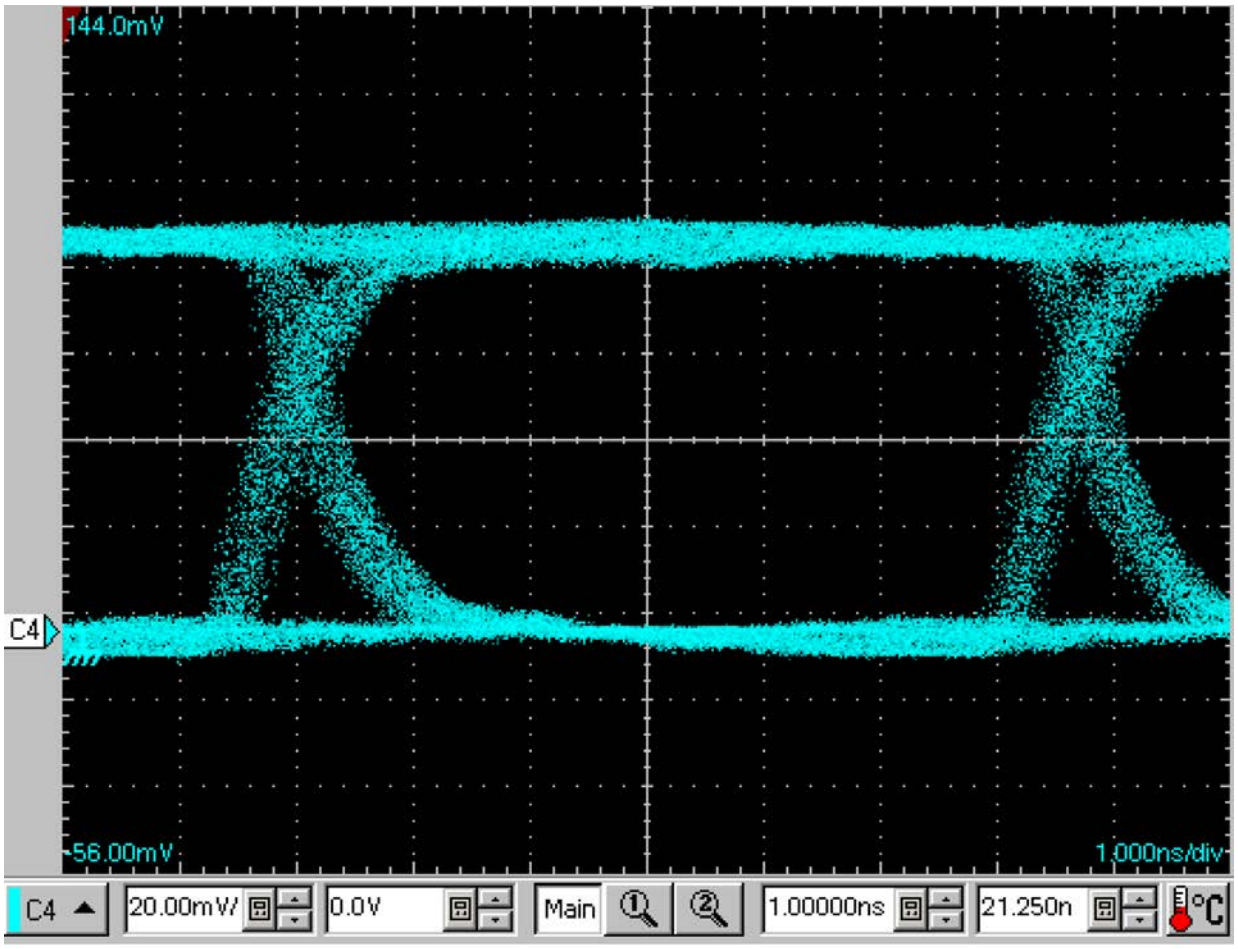


Figure 3.3. Eye Diagram

4. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 4.1 Device Behavior during Normal Operation on page 6, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to the table below to determine outputs when power supply (V_{DD}) is not present.

Table 4.1. Si84xx Logic Operation Table

V_I Input[1,4]	VDDI State[1,2,3]	VDDO State[1,2,3]	V_O Output[1,4]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	H[6] (Si8422/23) L[6] (Si8410/20/21)	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. Powered (P) state is defined as 2.72.60 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. See Section 2. Ordering Guide for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN).

4.1 Device Startup

Outputs are held low during powerup until V_{DD} is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

4.2 Under Voltage Lockout

Under Voltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when V_{DD} is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO-)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

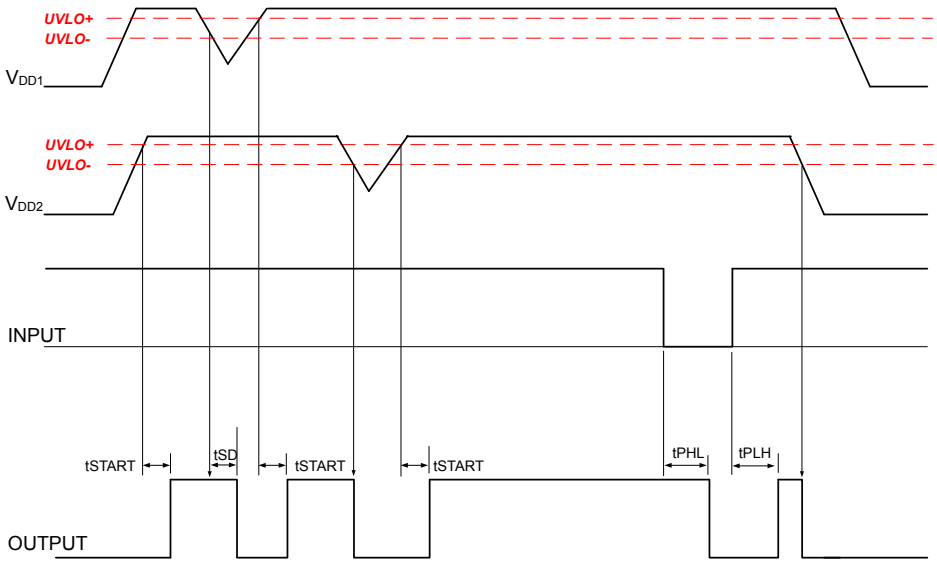


Figure 4.1. Device Behavior during Normal Operation

4.3 Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 5.5 Regulatory Information[1] on page 20 and Table 5.6 Insulation and Safety-Related Specifications on page 21 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

4.3.1 Supply Bypass

The Si841x/2x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, it is further recommended that the user also add 1 µF bypass capacitors and include 100 Ω resistors in series with the inputs and outputs if the system is excessively noisy.

4.3.2 Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

4.3.3 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

4.4 Fail-Safe Operating Mode

Si84xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 4.1 Si84xx Logic Operation Table on page 5 and Section 2. Ordering Guide for more information.

4.5 Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Table 5.2 Electrical Characteristics on page 9 through Table 5.4 Electrical Characteristics[1] on page 17 for actual specification limits.

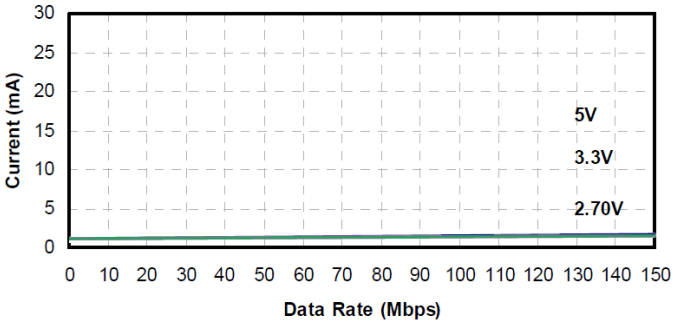


Figure 4.2. Si8410 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

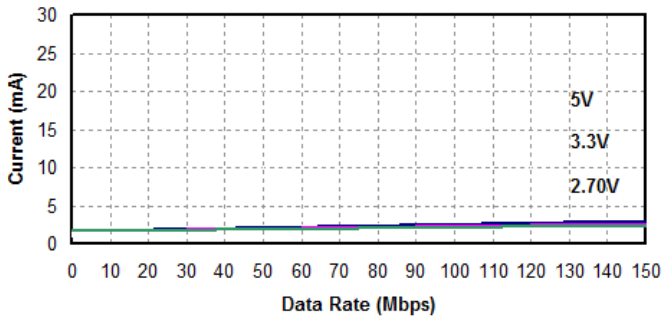


Figure 4.3. Si8420 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

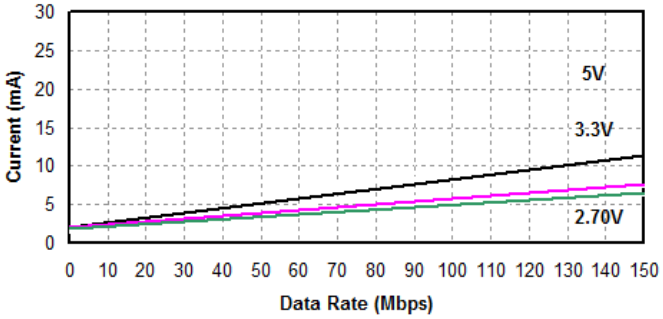


Figure 4.4. Si8421 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

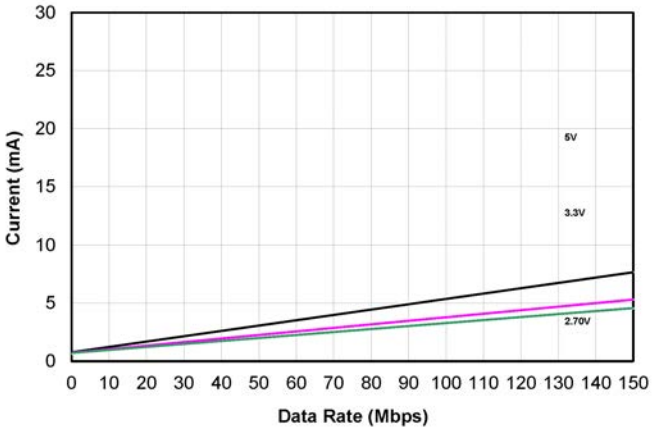


Figure 4.5. Si8410 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

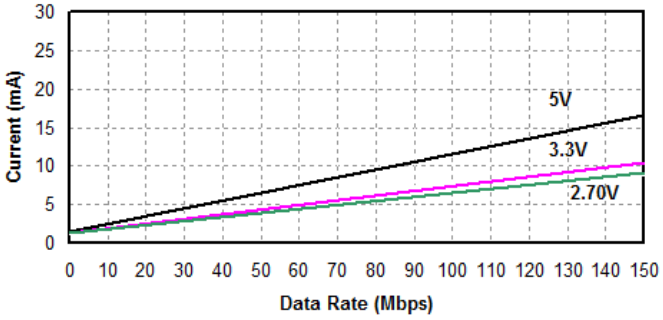


Figure 4.6. Si8420 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

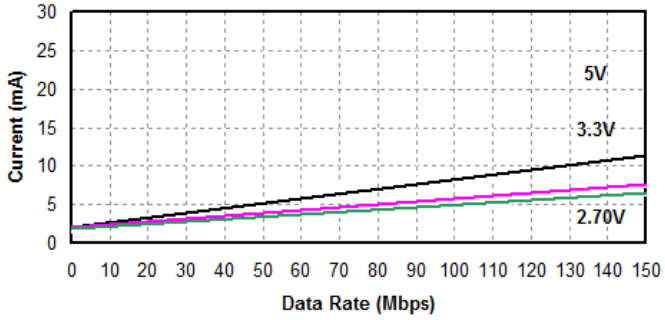


Figure 4.7. Si8422 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

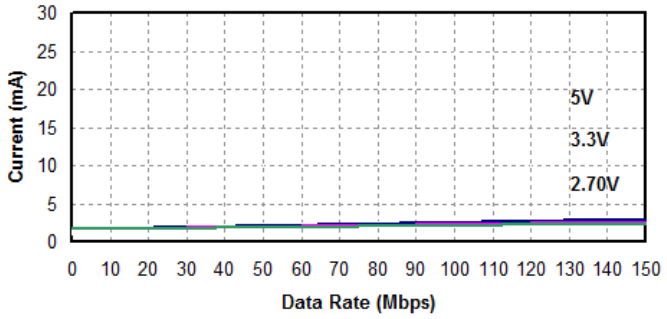


Figure 4.8. Si8423 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

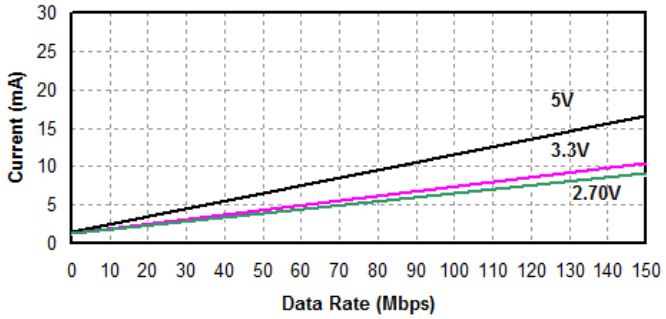


Figure 4.9. Si8423 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

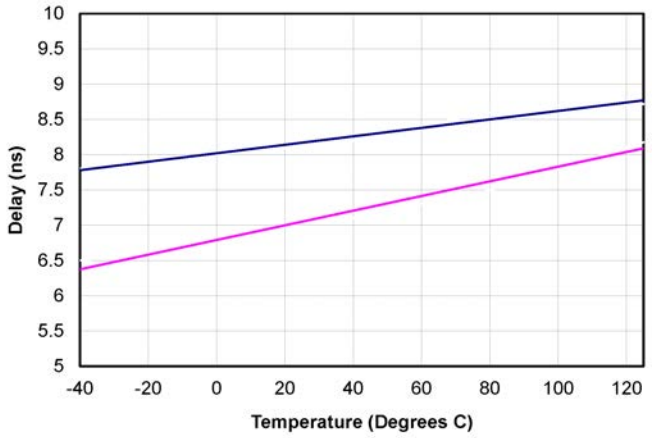


Figure 4.10. Propagation Delay vs. Temperature

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature[1]	T_A	–40	25	125	C°
Supply Voltage	V_{DD1}	2.70	—	5.5	V
	V_{DD2}	2.70	—	5.5	V

Note:
1. The maximum ambient temperature is dependent upon data frequency, output loading, the number of operating channels, and supply voltage.

Table 5.2. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.15	2.3	2.5	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		45	75	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.1	—	1.4	V
Input Hysteresis	V_{HYS}		0.40	0.45	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at Supply)						
Si8410Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.0	1.5	mA
V_{DD2}		All inputs 0 DC	—	3.0	1.5	
V_{DD1}		All inputs 1 DC	—	3.0	4.5	
V_{DD2}		All inputs 1 DC	—	1.0	1.5	
Si8420Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	5.8	8.7	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8421Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	3.7	5.6	
V_{DD2}		All inputs 1 DC	—	3.7	5.6	
Si8422Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3.7	5.6	mA
V_{DD2}		All inputs 0 DC	—	3.7	5.6	
V_{DD1}		All inputs 1 DC	—	1.7	2.6	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
Si8423Ax, Bx						
V_{DD1}		All inputs 0 DC	—	5.4	8.1	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	1.3	2.0	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
1 Mbps Supply Current (All inputs = 500 kHz square wave, C_L = 15 pF on all outputs)						
Si8410Ax, Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.1	1.7	
Si8420Ax, Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	1.9	2.9	
Si8421Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.8	4.2	
Si8422Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.8	4.2	
Si8423Ax, Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	1.9	2.9	
10 Mbps Supply Current (All inputs = 5 MHz square wave, C_L = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	1.5	2.1	
Si8420Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	2.6	3.6	
Si8421Bx						
V_{DD1}			—	3.2	4.5	mA
V_{DD2}			—	3.2	4.5	
Si8422Bx						
V_{DD1}			—	3.2	4.5	mA
V_{DD2}			—	3.2	4.5	
Si8423Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	2.5	3.5	
100 Mbps Supply Current (All inputs = 50 MHz square wave, C_L = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	2.1	3.1	mA
V_{DD2}			—	5.0	6.3	
Si8420Bx						
V_{DD1}			—	3.7	5.4	mA
V_{DD2}			—	9.8	12.3	
Si8421Bx						
V_{DD1}			—	6.8	8.5	mA
V_{DD2}			—	6.8	8.5	
Si8422Bx						
V_{DD1}			—	6.8	8.5	mA
V_{DD2}			—	6.8	8.5	
Si8423Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	9.2	11.5	
Timing Characteristics						
Si841xAx, Si842xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 5.1 Propagation Delay Timing on page 12	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 5.1 Propagation Delay Timing on page 12	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si841xBx, Si842xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 5.1 Propagation Delay Timing on page 12	4.0	8.0	11	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 5.1 Propagation Delay Timing on page 12	—	1.5	3.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2.0	4.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.0	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 3.3 Eye Diagram on page 4	—	350	—	ps
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	20	45	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

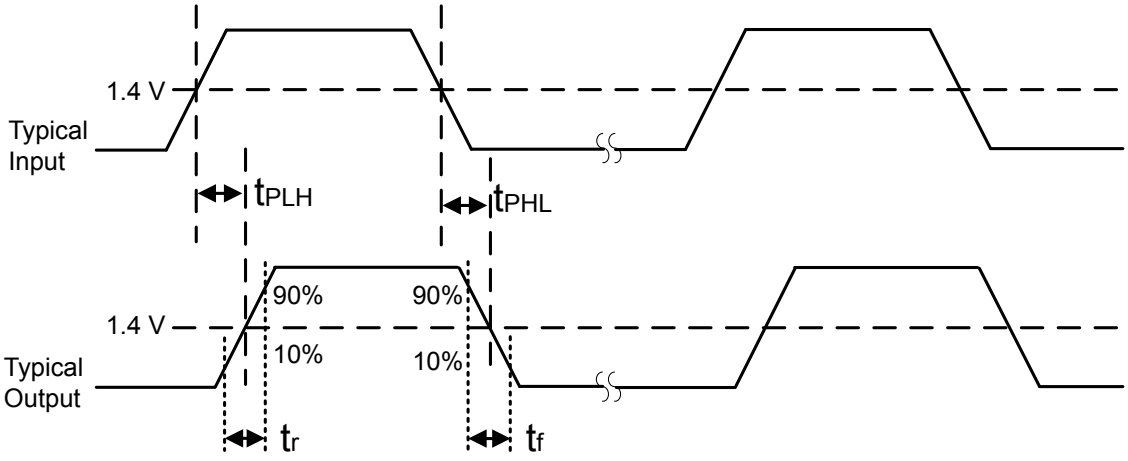


Figure 5.1. Propagation Delay Timing

Table 5.3. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.15	2.3	2.5	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		45	75	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.1	—	1.4	V
Input Hysteresis	V_{HYS}		0.40	0.45	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance (Si8410/20)[1]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8410Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.0	1.5	mA
V_{DD2}		All inputs 0 DC	—	1.0	1.5	
V_{DD1}		All inputs 1 DC	—	3.0	4.5	
V_{DD2}		All inputs 1 DC	—	1.0	1.5	
Si8420Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	5.8	8.7	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
Si8421Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	3.7	5.6	
V_{DD2}		All inputs 1 DC	—	3.7	5.6	
Si8422Ax, Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}		All inputs 0 DC	—	3.7	5.6	mA
V_{DD2}		All inputs 0 DC	—	3.7	5.6	
V_{DD1}		All inputs 1 DC	—	1.7	2.6	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
Si8423Ax, Bx						
V_{DD1}		All inputs 0 DC	—	5.4	8.1	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	1.3	2.0	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
1 Mbps Supply Current (All inputs = 500 kHz square wave, C_L = 15 pF on all outputs)						
Si8410Ax, Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.1	1.7	
Si8420Ax, Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	1.9	2.9	
Si8421Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.8	4.2	
Si8422Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.8	4.2	
Si8423Ax, Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	1.9	2.9	
10 Mbps Supply Current (All inputs = 5 MHz square wave, C_L = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.3	1.8	
Si8420Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	2.3	3.2	
Si8421Bx						
V_{DD1}			—	3.0	4.4	mA
V_{DD2}			—	3.0	4.4	
Si8422Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}			—	3.0	4.4	mA
V_{DD2}			—	3.0	4.4	
Si8423Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	2.2	3.1	
100 Mbps Supply Current (All inputs = 50 MHz square wave, C_L = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	3.6	4.5	
Si8420Bx						
V_{DD1}			—	4.5	5.3	mA
V_{DD2}			—	7.0	8.8	
Si8421Bx						
V_{DD1}			—	5.3	6.6	mA
V_{DD2}			—	5.3	6.6	
Si8422Bx						
V_{DD1}			—	5.3	6.6	mA
V_{DD2}			—	5.3	6.6	
Si8423Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	6.6	8.3	
Timing Characteristics						
Si841xAx, Si842xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 5.1 Propagation Delay Timing on page 12	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 5.1 Propagation Delay Timing on page 12	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si841xBx, Si842xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 5.1 Propagation Delay Timing on page 12	4.0	8.0	11	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 5.1 Propagation Delay Timing on page 12	—	1.5	3.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2.0	4.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.0	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 3.3 Eye Diagram on page 4	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	20	45	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5.4. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.15	2.3	2.5	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		45	75	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.1	—	1.4	V
Input Hysteresis	V_{HYS}		0.40	0.45	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8410Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.0	1.5	mA
V_{DD2}		All inputs 0 DC	—	1.0	1.5	
V_{DD1}		All inputs 1 DC	—	3.0	4.5	
V_{DD2}		All inputs 1 DC	—	1.0	1.5	
Si8420Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.3	2.0	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	5.8	8.7	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
Si8421Ax, Bx						
V_{DD1}		All inputs 0 DC	—	1.7	2.6	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	3.7	5.6	
V_{DD2}		All inputs 1 DC	—	3.7	5.6	
Si8422Ax, Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}		All inputs 0 DC	—	3.7	5.6	mA
V_{DD2}		All inputs 0 DC	—	3.7	5.6	
V_{DD1}		All inputs 1 DC	—	1.7	2.6	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
Si8423Ax, Bx						
V_{DD1}		All inputs 0 DC	—	5.4	8.1	mA
V_{DD2}		All inputs 0 DC	—	1.7	2.6	
V_{DD1}		All inputs 1 DC	—	1.3	2.0	
V_{DD2}		All inputs 1 DC	—	1.7	2.6	
1 Mbps Supply Current (All inputs = 500 kHz square wave, C_L = 15 pF on all outputs)						
Si8410Ax, Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.1	1.7	
Si8420Ax, Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	1.9	2.9	
Si8421Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.8	4.2	
Si8422Ax, Bx						
V_{DD1}			—	2.8	4.2	mA
V_{DD2}			—	2.8	4.2	
Si8423Ax, Bx						
V_{DD1}			—	3.3	5.0	mA
V_{DD2}			—	1.8	2.8	
10 Mbps Supply Current (All inputs = 5 MHz square wave, C_L = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	1.1	1.7	
Si8420Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	2.1	3.0	
Si8421Bx						
V_{DD1}			—	2.9	4.3	mA
V_{DD2}			—	2.9	4.3	
Si8422Bx						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD1}			—	2.9	4.3	mA
V_{DD2}			—	2.9	4.3	
Si8423Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	2.0	2.9	
100 Mbps Supply Current (All inputs = 50 MHz square wave, CL = 15 pF on all outputs)						
Si8410Bx						
V_{DD1}			—	2.0	3.0	mA
V_{DD2}			—	2.0	3.0	
Si8420Bx						
V_{DD1}			—	3.5	5.3	mA
V_{DD2}			—	5.5	6.9	
Si8421Bx						
V_{DD1}			—	4.6	5.8	mA
V_{DD2}			—	4.6	5.8	
Si8422Bx						
V_{DD1}			—	4.6	5.8	mA
V_{DD2}			—	4.6	5.8	
Si8423Bx						
V_{DD1}			—	3.4	5.1	mA
V_{DD2}			—	5.2	6.5	
Timing Characteristics						
Si841xAx, Si842xAx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 5.1 Propagation Delay Timing on page 12	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 5.1 Propagation Delay Timing on page 12	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si841xBx, Si842xBx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 5.1 Propagation Delay Timing on page 12	4.0	8.0	11	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 5.1 Propagation Delay Timing on page 12	—	1.5	3.0	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2.0	4.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.0	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 3.3 Eye Diagram on page 4	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	20	45	—	kV/µs
Start-up Time[4]	t_{SU}		—	15	40	µs

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5.5. Regulatory Information[1]

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si84xx is certified according to IEC 60747-5-5. For more details, see File 5006301-4880-0001.
60747-5-5: Up to 891 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic insulation.

Note:

1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec.
   For more information, see Section 2. Ordering Guide.

Table 5.6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-8	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0 min	4.9 min	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0 min	4.01 min	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.040	mm
Resistance (Input-Output)[2]	R_{IO}		$10^{1,2}$	$10^{1,2}$	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	1.0	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in Section 7.1 Package Outline (16-Pin Wide Body SOIC) and Section 7.2 Package Outline (8-Pin Narrow Body SOIC). VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16 package and 4.7 mm minimum for the NB SOIC-8 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 (1–4, NB SOIC-8) are shorted together to form the first terminal and pins 9–16 (5–8, NB SOIC-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 5.7. IEC 60747-5-5 Insulation Characteristics for Si84xxxx[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-8	
Maximum Working Insulation Voltage	V_{IORM}		891	560	Vpeak
Input to Output Test Voltage		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	1050	
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	4000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 5.8. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max		Unit
			WB SOIC-16	NB SOIC-8	
Case Temperature	T_S		150	150	°C
Safety Input, Output, or Supply Current	I_S	θ_{JA} = 140 °C/W (NB SOIC-8), 100 °C (WB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	220	160	mA
Device Power Dissipation[2]	P_D		150	150	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 5.2 (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5 on page 23 and Figure 5.3 (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5 on page 23.
2. The Si84xx is tested with VDD1 = VDD2 = 5.5 V, T_J = 150 °C, C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 5.9. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	140	°C/W

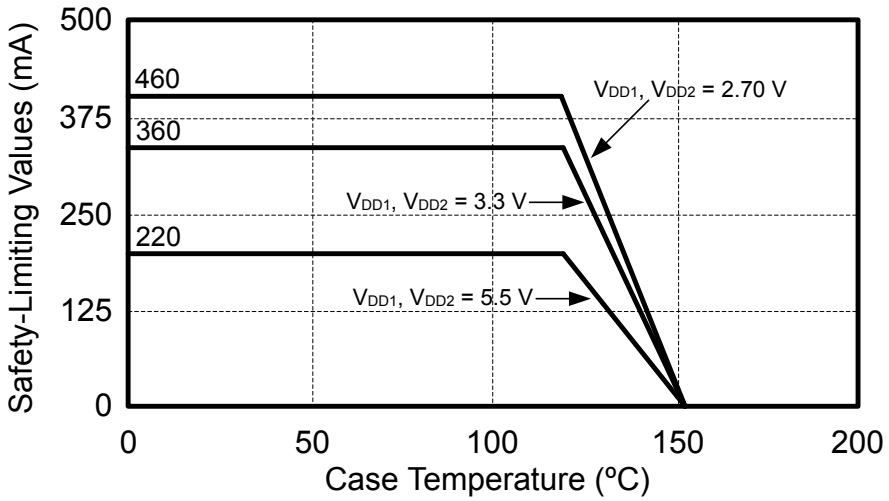


Figure 5.2. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5

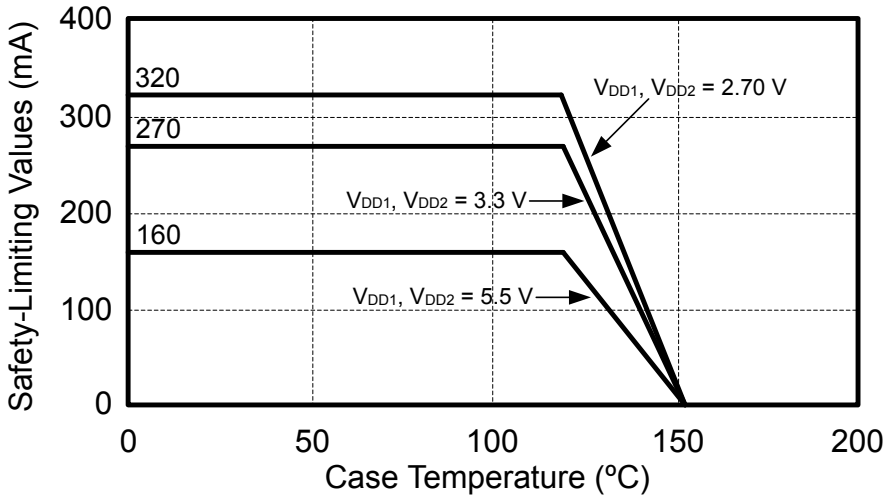


Figure 5.3. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5

Table 5.10. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	C°
Operating Temperature	T_A	–40	—	125	C°
Junction Temperature	T_J	—	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	C°
Maximum Isolation Voltage (1 s) NB SOIC-8		—	—	4500	V_{RMS}
Maximum Isolation Voltage (1 s) WB SOIC-16		—	—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

6. Pin Descriptions

6.1 Pin Descriptions (Wide-Body SOIC)

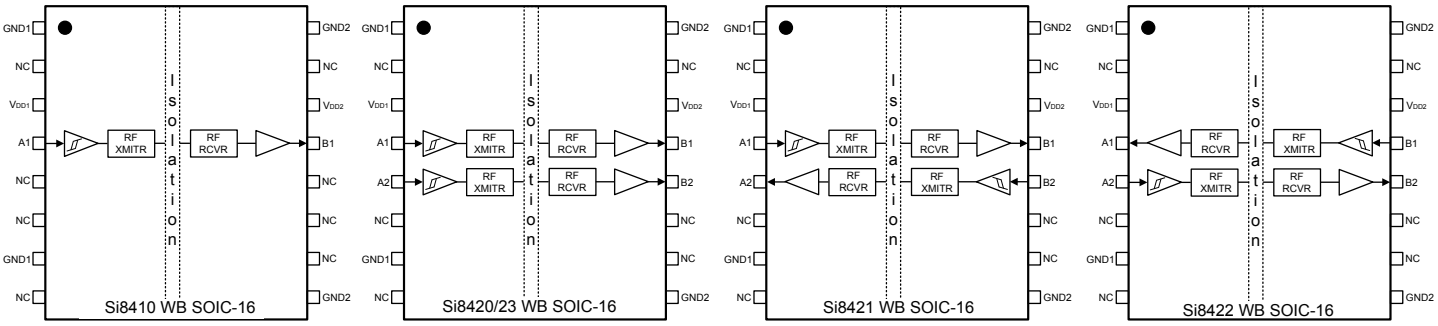


Figure 6.1. Wide-Body SOIC

Table 6.1. Pin Descriptions

Name	SOIC-16 Pin# Si8410	SOIC-16 Pin# Si842x	Type	Description
GND1	1	1	Ground	Side 1 ground.
NC[1]	2, 5, 6, 8,10, 11, 12, 15	2, 6, 8,10, 11, 15	No Connect	NC
V_{DD1}	3	3	Supply	Side 1 power supply.
A1	4	4	Digital I/O	Side 1 digital input or output.
A2	NC	5	Digital I/O	Side 1 digital input or output.
GND1	7	7	Ground	Side 1 ground.
GND2	9	9	Ground	Side 2 ground.
B2	NC	12	Digital I/O	Side 2 digital input or output.
B1	13	13	Digital I/O	Side 2 digital input or output.
V_{DD2}	14	14	Supply	Side 2 power supply.
GND2	16	16	Ground	Side 2 ground.

Note:
1. No Connect. These pins are not internally connected. They can be left floating, tied to V_{DD} or tied to GND.

6.2 Pin Descriptions (Narrow-Body SOIC)

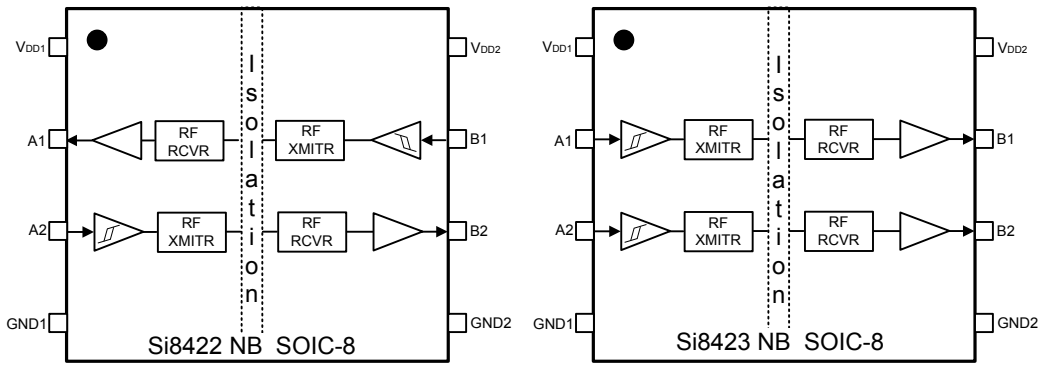


Figure 6.2. Narrow-Body SOIC

Name	SOIC-8 Pin# Si842x	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	4	Ground	Side 1 ground.
A1	2	Digital I/O	Side 1 digital input or output.
A2	3	Digital I/O	Side 1 digital input or output.
B1	7	Digital I/O	Side 2 digital input or output.
B2	6	Digital I/O	Side 2 digital input or output.
V_{DD2}	8	Supply	Side 2 power supply.
GND2	5	Ground	Side 2 ground.

7. Package Outlines

7.1 Package Outline (16-Pin Wide Body SOIC)

The figure below illustrates the package details for the Si84xx Digital Isolator. The table below lists the values for the dimensions shown in the illustration.

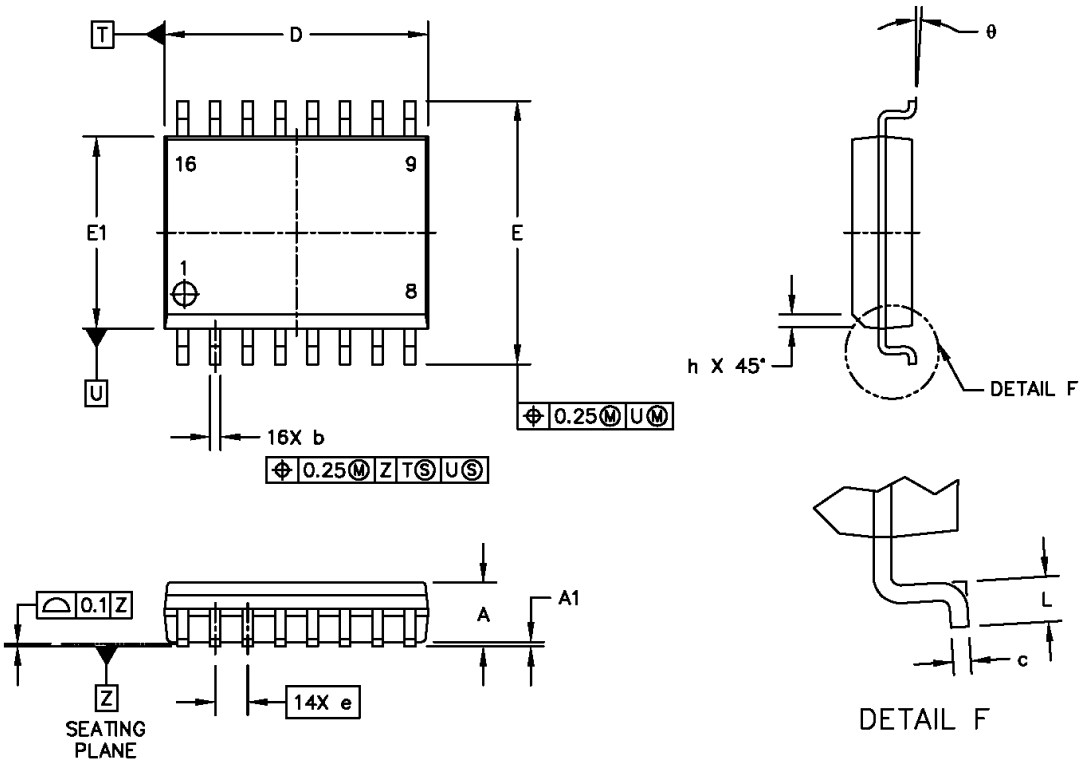


Figure 7.1. 16-Pin Wide Body SOIC

Table 7.1. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

7.2 Package Outline (8-Pin Narrow Body SOIC)

The figure below illustrates the package details for the Si84xx. The table below lists the values for the dimensions shown in the illustration.

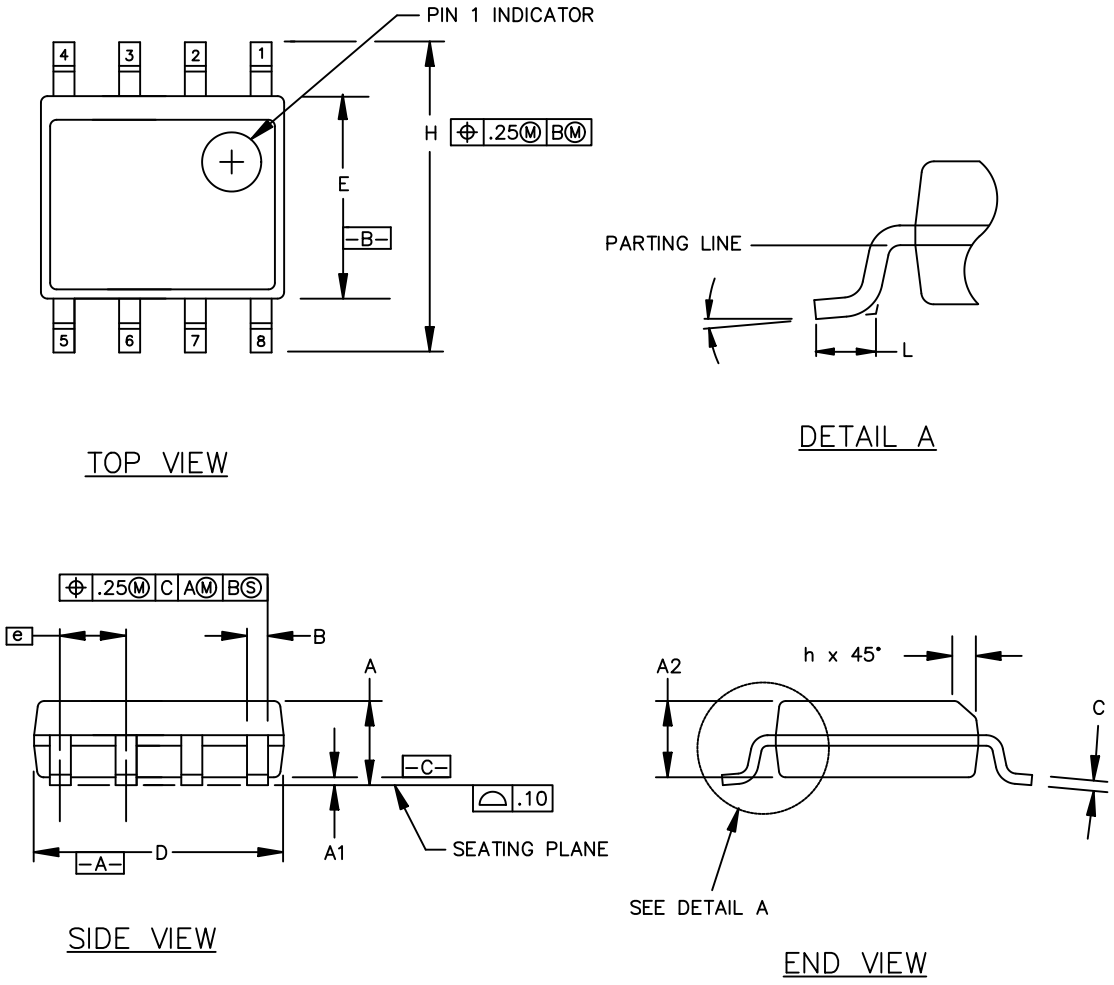


Figure 7.2. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 7.2. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
	0°	8°

8. Land Patterns

8.1 Land Pattern (16-Pin Wide-Body SOIC)

The figure below illustrates the recommended land pattern details for the Si84xx in a 16-pin wide-body SOIC. The table below lists the values for the dimensions shown in the illustration.

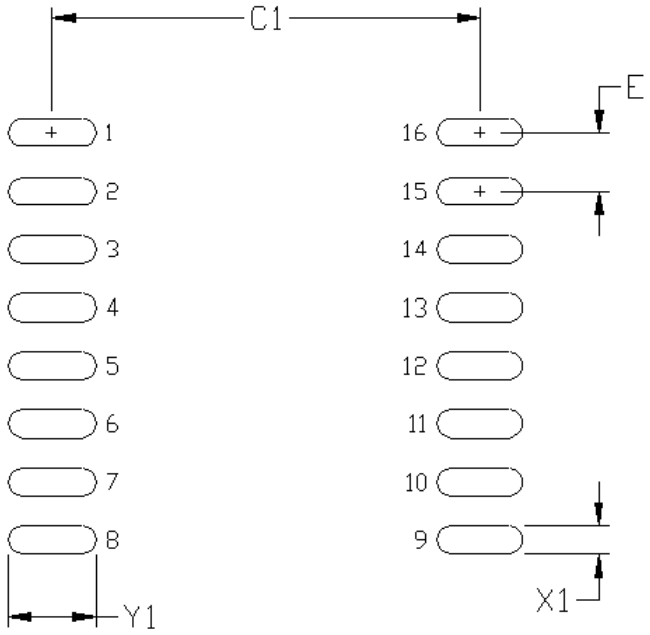


Figure 8.1. 16-Pin SOIC Land Pattern

Table 8.1. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.2 Land Pattern (8-Pin Narrow Body SOIC)

The figure below illustrates the recommended land pattern details for the Si84xx in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

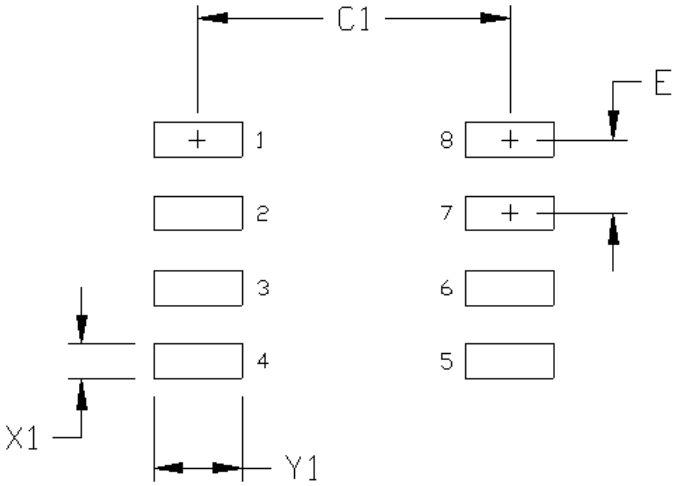


Figure 8.2. PCB Land Pattern: 8-Pin Narrow Body SOIC

Table 8.2. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Markings

9.1 Top Marking (16-Pin Wide Body SOIC)

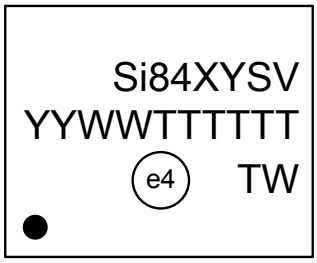


Figure 9.1. Isolator Top Marking

Table 9.1. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 2. Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (2, 1) Y = # of reverse channels (1, 0)[1,2] S = Speed Grade A = 1 Mbps B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing code from assembly house.
Line 3 Marking:	Circle = 1.7 mm Diameter (Center-Justified)	“e4” Pb-Free Symbol.
	Country of Origin ISO Code Abbreviation	TW = Taiwan.
Notes: 1. The Si8422 has one reverse channel. 2. The Si8423 has zero reverse channels.		

9.2 Top Marking (8-Pin Narrow-Body SOIC)

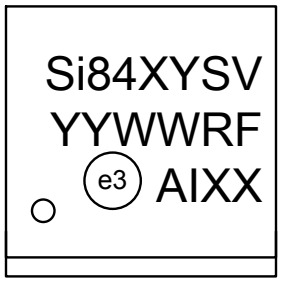


Figure 9.2. Isolator Top Marking

Table 9.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See 2. Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (2, 1) Y = # of reverse channels (1, 0)[1,2] S = Speed Grade A = 1 Mbps B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	R = Product (OPN) Revision F = Wafer Fab	
Line 3 Marking:	Circle = 1.1 mm Diameter Left-Justified	“e3” Pb-Free Symbol. First two characters of the manufacturing code.
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the manufacturing code.

Notes:
1. The Si8422 has one reverse channel.
2. The Si8423 has zero reverse channels.

10. Document Change List

10.1 Revision 0.1

- Initial release.

10.2 Revision 0.1 to Revision 1.0

- Updated features list.
  - Updated transient immunity.
- Removed block diagram from front page.
- Added chip graphics on front page.
- Added Peak Eye Diagram jitter in Table 5.2 Electrical Characteristics on page 9 through Table 5.4 Electrical Characteristics[1] on page 17.
  - Updated transient immunity
- Moved Table 4.1 Si84xx Logic Operation Table on page 5 to Section 4. Device Operation.
- Added Section 4. Device Operation.
- Added Section 4.4 Fail-Safe Operating Mode.
- Moved Section 4.5 Typical Performance Characteristics.
- Deleted RF Radiated Emissions section.
- Deleted RF Magnetic and Common-Mode Transient Immunity section.
- Updated MSL rating to MSL2A.

10.3 Revision 1.0 to Revision 1.1

- Numerous text edits.
- Added table notes to Table 9.1 Top Marking Explanation on page 32 and Table 9.2 Top Marking Explanation on page 33.

10.4 Revision 1.1 to Revision 1.2

- Updated Timing Characteristics in Table 5.2 Electrical Characteristics on page 9 through Table 5.4 Electrical Characteristics[1] on page 17.

10.5 Revision 1.2 to Revision 1.3

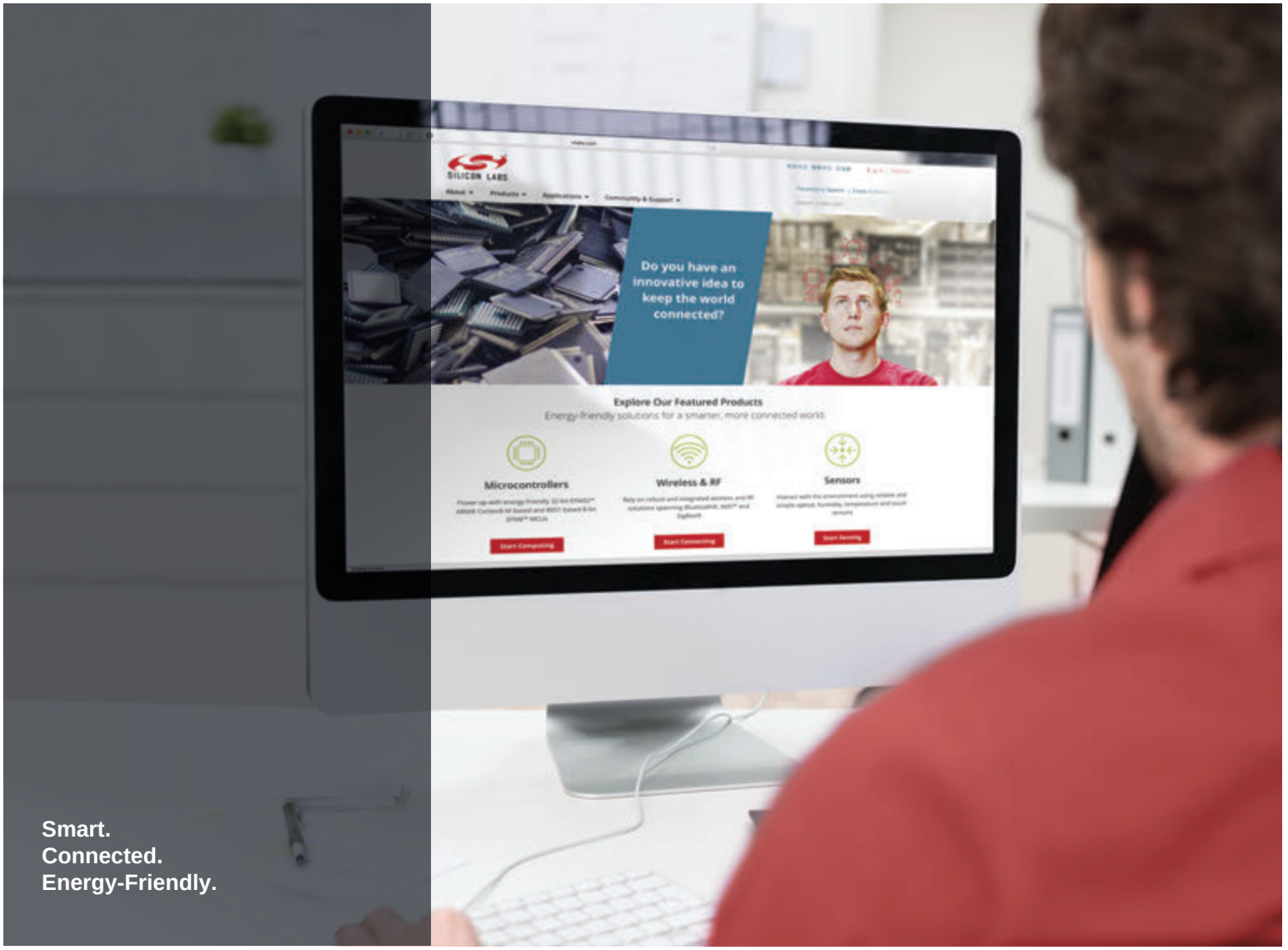
- Added references to AEC-Q100 qualified throughout.
- Changed all 60747-5-2 references to 60747-5-5.
- Updated Table 2.1 Ordering Guide[1,2,3] on page 2.
  - Added table notes 1 and 2.
  - Removed references to moisture sensitivity levels.
  - Added Revision D ordering information.
  - Removed older revisions.
- Updated Section 9.1 Top Marking (16-Pin Wide Body SOIC).

10.6 Revision 1.3 to Revision 1.4

September 16, 2016

- Updated data sheet format.

Table of Contents



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