"Soft" Turn-off Feature

Products with Feature: ACPL-333J, ACPL-330J, ACPL-332J, ACPL-331J, HCPL-316J

Application Note 5315

Introduction

Avago's gate optocoupler "Soft" turn-off feature is used to increase the reliability of an application during short-circuit or over-current periods. This feature works after the DESAT protection is activated, which provides protection for transistor switches (IGBT/MOSFET) against short-circuit and over-current events. The desaturation protection circuit is illustrated in Figure 1. With the "Soft" turn-off feature, the gate voltage will be reduced slowly in order to reduce IGBT current. This is a two stage turn-off system. It will slowly discharge the IGBT gate to prevent a fast change in drain current. The "Soft" IGBT turn-off method will avoid an over-voltage spike across the IGBT caused by lead and wire inductances.

How does desaturation protection and "Soft" shut-down work? This is illustrated in Figure 2.

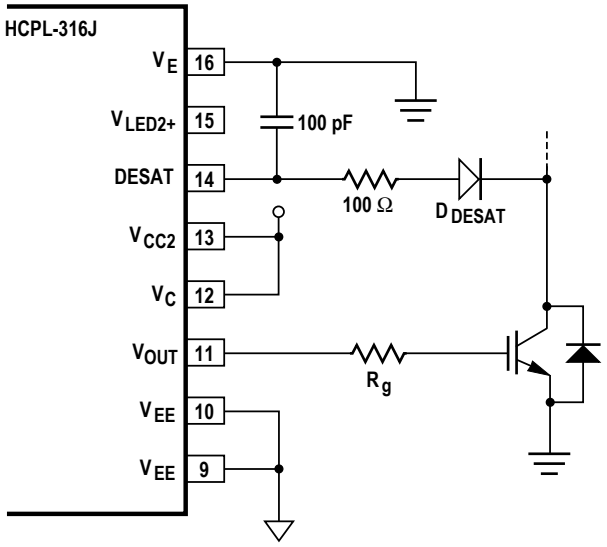

Figure 1. Desaturation Protection using the HCPL-316J

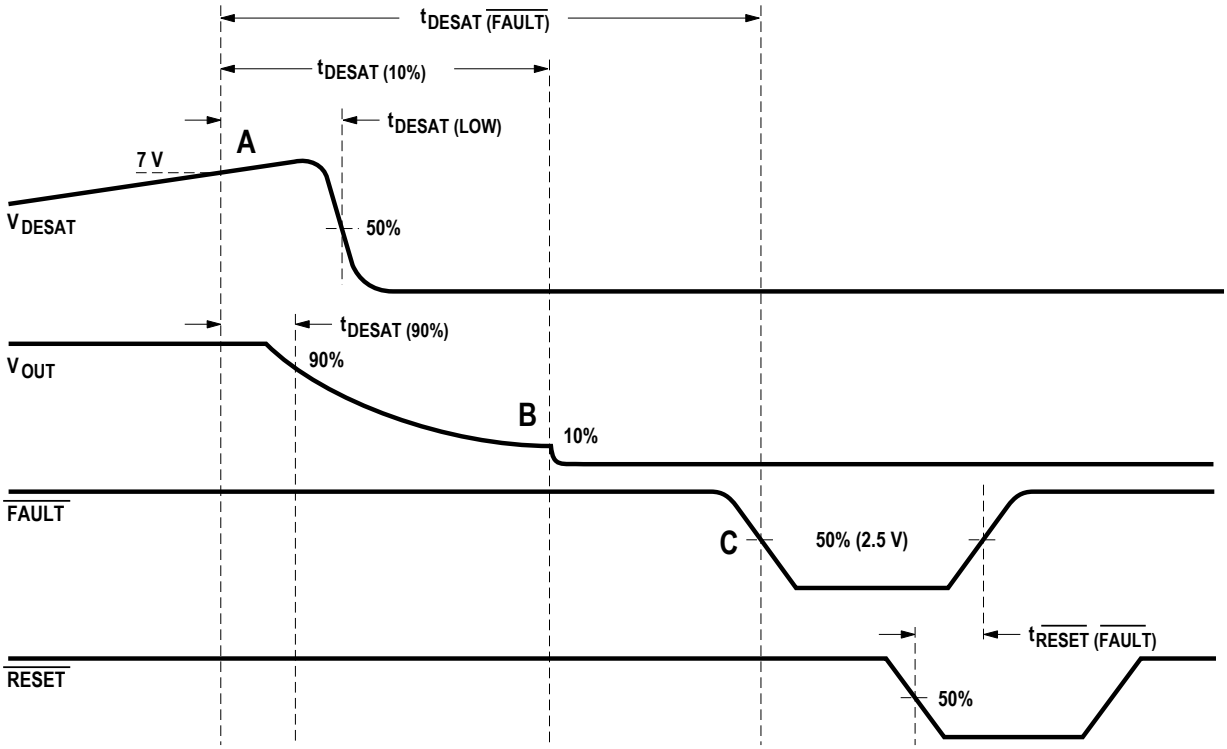

Figure 2. Desaturation, Gate Output Voltage V_{OUT}, FAULT and RESET Waveforms During Short-circuit or Overcurrent

Note:
$t_{DESAT(90\%)}$ is the DESAT Sense to 90% V_{OUT} time delay
$t_{RESET(FAULT)}$ is the RESET to High Level FAULT signal time delay

i. Fault Detection:

IGBT collector-emitter voltage, VCESAT is monitored through the DESAT pin 14. The IGBT is turned off if the voltage threshold (typically 6.5 V to 7 V) is reached (Point A).

ii. Soft Turn-off:

This is a two stage process. In the first stage, a weak pull-down device in the output drive stage will turn on to 'softly' turn off the IGBT. This device slowly discharges the IGBT. This turn off delay time of the gate optocoupler is labeled as DESAT sense to 10% VOUT delay, $t_{DESAT(10\%)}$, in Figure 2. During soft turn-off, the internal 1xDMOS transistor is turned on (Figure 3b).

During the slow turn off, the large output pull-down device, which is the second stage (Point B) remains off until the output gate voltage falls below V_{EE} + 2 V, at which time the large pull-down device, 50x DMOS transistor, clamps the IGBT gate to V_{EE}. The 50x represents a DMOS device 50 times larger than a 1x device (figure 3a).

This $t_{DESAT(10\%)}$ time is dependent on the gate resistor R_g, gate capacitance C_g, output supply voltage V_{CC2}, and DMOS $R_{ds(on)}$ value. In the HCPL-316J datasheet, $t_{DESAT(10\%)}$ is typically 2 μs for R_g = 10 Ω and C_g = 10 nF.

An approximation of the DMOS $R_{ds(on)}$ can be obtained by V_{OUT}/I_{OL} = 2.5/2.3 = 1.09 Ω (Page 9 of the HCPL-316J datasheet, Low Level Output Current). Hence the 1x DMOS $R_{ds(on)}$ is 50 x 1.09 = 54.5 Ω. The time constant can be approximated using $C_g(R_g + 54.5)$.

Using the same calculation method for the ACPL-332J, $R_{ds(on)}$ = 2.5/1.5 = 1.7 Ω. Hence the 1xDMOS $R_{ds(on)}$ is 50x1.7 = 85 Ω.

Two characterization graphs reflecting the influence of Rg and Cg to the DESAT sense to 10% time are shown in Figure 4 and Figure 5. Both graphs can be found on page 13 in the ACPL-332J datasheet

iii. Fault Output and Off State:

After the DESAT sense to Low-level FAULT signal delay time, $t_{DESAT(FAULT)}$, the FAULT signal goes low (Point C). The fault detect circuitry is disabled to prevent false 'fault' signals. The driver outputs will remain low (IGBT off) until the following two conditions are met:

The DESAT detection is low AND there is a RESET signal (HCPL-316J) or a RESET by the next INPUT PWM high signal is sent (ACPL-331J, ACPL-332J), ACPL-332J) or an internal automatic fault RESET after a fixed-mute time of typically 26 μs (ACPL-330J, ACPL-333J).

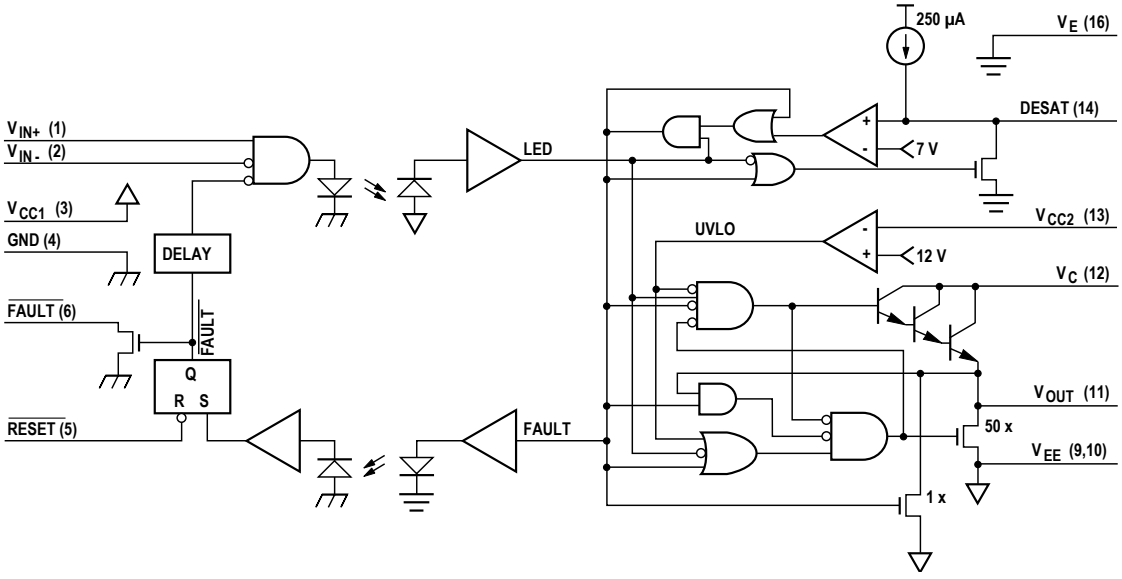

Figure 3a. Behavioral Circuit Schematic

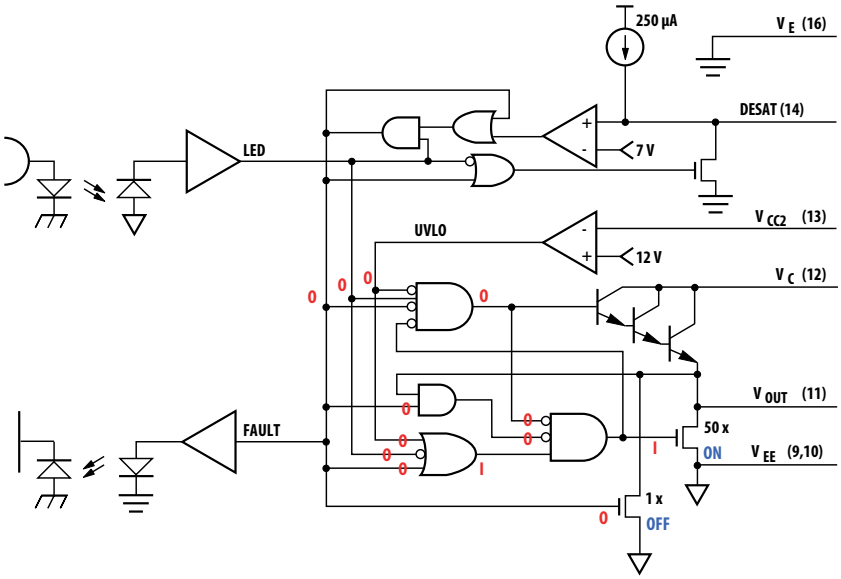

Figure 3b. Normal Operation

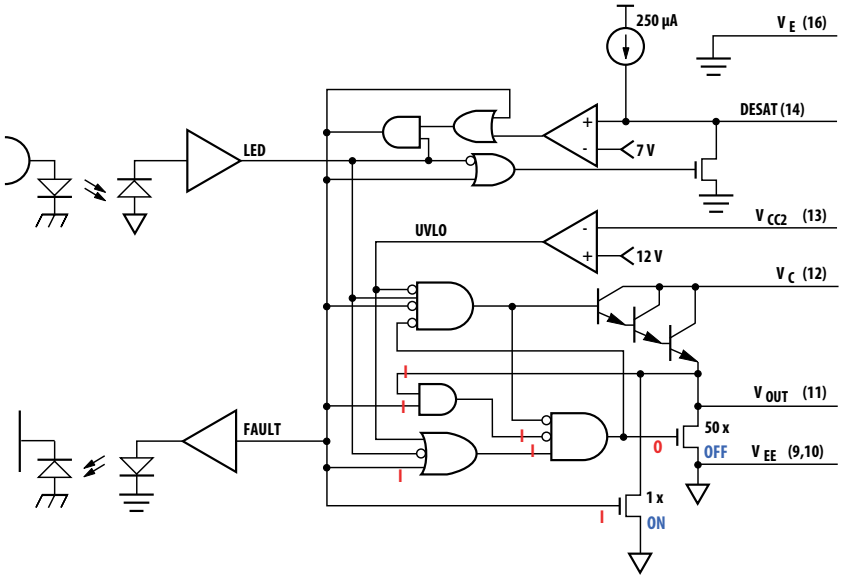

Figure 3c. Soft-shutdown Operation

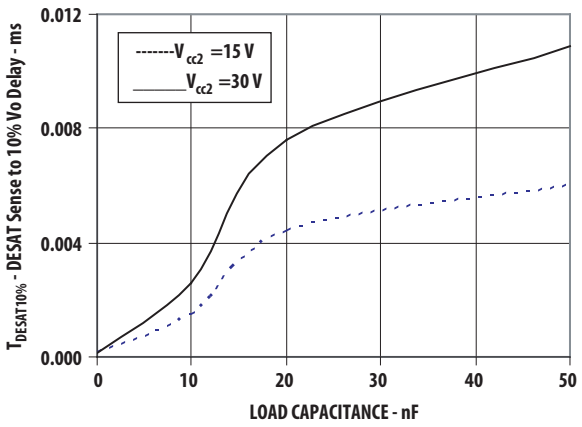

Figure 4. Normal Operation

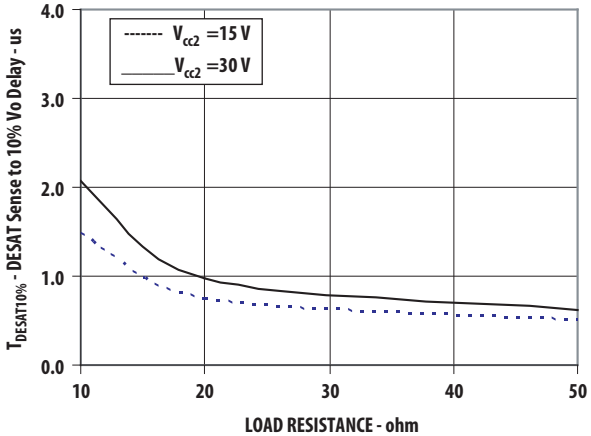

Figure 5. Soft-shutdown Operation

Soft-turn off Function with External Current Buffer Drive:

To increase the IGBT gate drive current, a non-inverting current buffer, Figure 5, can be used. Inverting types are not compatible with the desaturation fault protection circuitry and should be avoided.

To preserve the slow IGBT turn-off feature during a fault condition, a 10 nF capacitor should be connected from the buffer input to VEE and a 10 Ω resistor inserted between the output and the common NPN/PNP base. For this soft-shutdown circuit topology, it is assumed that the load capacitor should be greater than the 10 nF used.

In this circuit, after a desaturation fault is detected, the weak pull-down device 1xDMOS transistor will pull the external RC circuit before the current buffer (R=10 Ω, C=10 nF). Refer back to Section ii, soft turn-off for details.

The circuit topology in Figure 6 is also applicable for other Avago DESAT featured gate optocoupler drivers, like the ACPL-332J, ACPL-331J, ACPL-333J and ACPL-330J.

The MJD44H11/MJD45H11 transistor pair is appropriate for currents up to 8 A maximum. The D44VH10/D45VH10 transistor pair is appropriate for currents up to 15 A maximum.

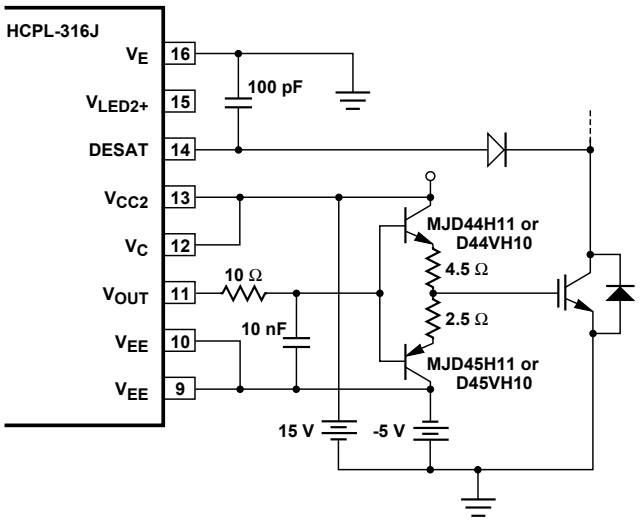

Figure 6. Current Buffer for Increased Drive Current

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