SN74LVC244A Octal Buffer or Driver With 3-State Outputs

1 Features

- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Specified From –40°C to +85°C and –40°C to +125°C
- Maximum t_{pd} of 5.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input or Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Maximum of 5.5 V Down to the V_{CC} Level
- Available in Ultra Small Logic QFN Package (0.5 mm Maximum Height)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

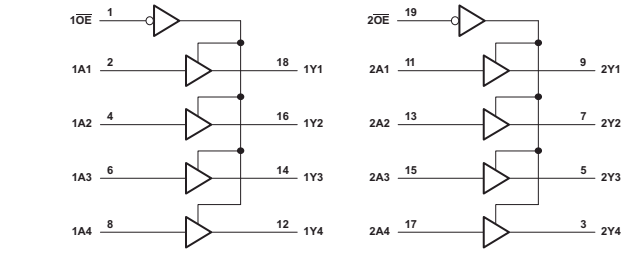
3 Description

These octal bus buffers are designed for 1.65-V to 3.6-V VCC operation. The SN74LVC244A devices are designed for asynchronous communication between data buses.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN74LVC244AN	PDIP (20)	25.40 mm × 6.35 mm
SN74LVC244ANS	SO (20)	12.60 mm × 5.30 mm
SN74LVC244ADB	SSOP (20)	7.50 mm × 5.30 mm
SN74LVC244ADGV	TVSOP (20)	5.00 mm × 4.40 mm
SN74LVC244ADW	SOIC (20)	12.80 mm × 7.50 mm
SN74LVC244ARGY	VQFN (20)	4.50 mm × 3.50 mm
SN74LVC244AZQN	BGA (20)	3.00 mm × 4.00 mm
SN74LVC244APW	TSSOP (20)	6.50 mm × 4.40 mm
SN74LVC244ARWP	X1QFN (20)	2.50 mm × 3.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

Logic Diagram (Positive Logic)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

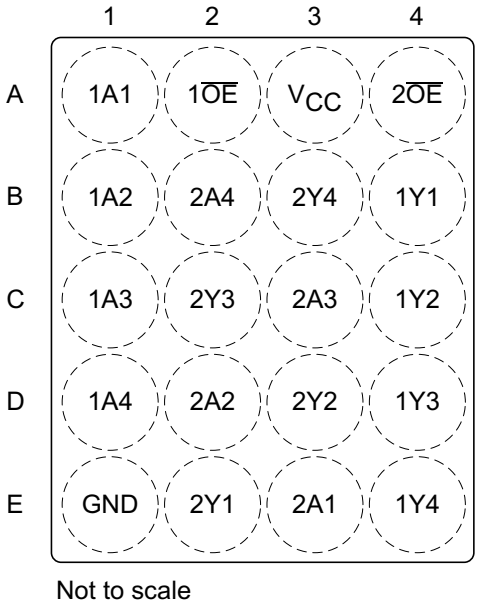
Changes from Revision AB (November 2016) to Revision AC (October 2020)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision AA (June 2016) to Revision AB (November 2016)	Page
• Changed A2 to A4 for 2 $\overline{OE}$ in *Pin Functions* table	3
• Added ambient temperature, T_A for BGA package and all other packages in *Recommended Operating Conditions*	6

Changes from Revision Z (January 2015) to Revision AA (May 2016)	Page
• Updated *Device Information* table to show all available packages	1
• Added RWP Package	3
• Deleted GQN package from *Pin Functions* table	3
• Added RWP thermal information to *Thermal Information* table and updated all thermal information for existing packages	6
• Updated all values for ZQN column in *Thermal Information* table	6
• Added package type in *Thermal Information* table	6

Changes from Revision Y (September 2010) to Revision Z (January 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information* at the end of the datasheet	1
• Updated *Features*	1

5 Pin Configuration and Functions



Not to scale

Figure 5-1. ZQN Package 20-Pin BGA Top View

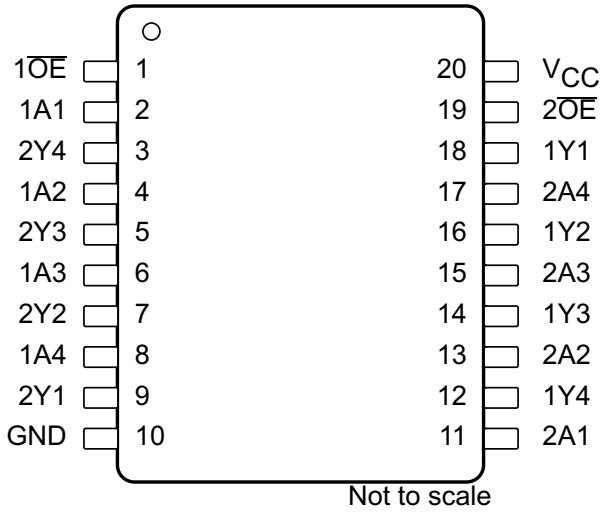


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Figure 5-2. DB, DGV, DW, N, NS, and PW Packages 20-Pin SSOP, TVSOP, SOIC, PDIP, SO, and TSSOP Front View

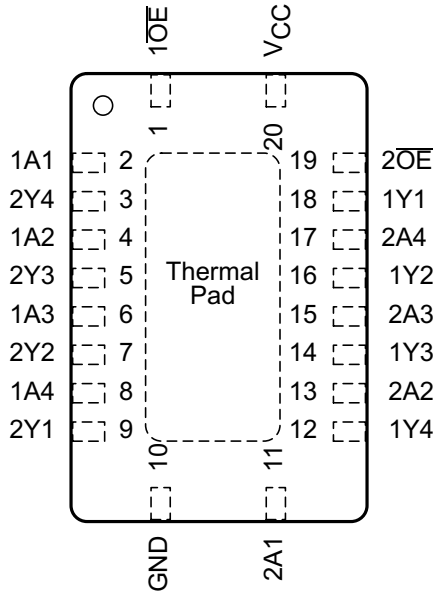

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Figure 5-3. RGY Package 20-Pin VQFN Top View

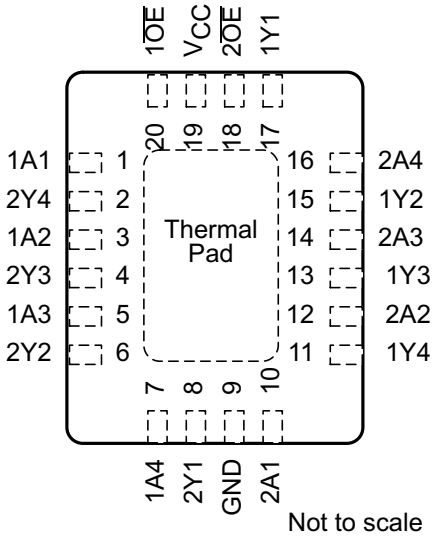

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Figure 5-4. RWP Package 20-Pin X1QFN Top View

Table 5-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	DB, DGV, DW, N, NS, PW, and RGY	ZQN	RWP		
1A1	2	A1	1	I	Port 1 A1 input
1A2	4	B1	3	I	Port 1 A2 input
1A3	6	C1	5	I	Port 1 A3 input
1A4	8	D1	7	I	Port 1 A4 input
1 $\overline{OE}$	1	A2	20	I	Output enable
1Y1	18	B4	17	O	Port 1 Y1 output
1Y2	16	C4	15	O	Port 1 Y2 output
1Y3	14	D4	13	O	Port 1 Y3 output
1Y4	12	E4	11	O	Port 1 Y4 output
2A1	11	E3	10	I	Port 2 A1 input
2A2	13	D2	12	I	Port 2 A2 input
2A3	15	C3	14	I	Port 2 A3 input
2A4	17	B2	16	I	Port 2 A4 input
2 $\overline{OE}$	19	A4	18	I	Output enable
2Y1	9	E2	8	O	Port 2 Y1 output
2Y2	7	D3	6	O	Port 2 Y2 output
2Y3	5	C2	4	O	Port 2 Y3 output
2Y4	3	B3	2	O	Port 2 Y4 output
GND	10	E1	9	—	Ground
V_{CC}	20	A3	19	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
P_{tot}	Power dissipation	T_A = –40°C to +125°C(4) (5)		500	mW
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Section 6.3* table.
(4) For the DW package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
(5) For the DB, DGV, N, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			T_A = 25°C		–40 TO +85°C		–40 TO +125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		0.65 × V_{CC}		0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}		0.35 × V_{CC}		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7		0.7		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4		–4		–4	mA
		V_{CC} = 2.3 V		–8		–8		–8	
		V_{CC} = 2.7 V		–12		–12		–12	
		V_{CC} = 3 V		–24		–24		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4		4		4	mA
		V_{CC} = 2.3 V		8		8		8	
		V_{CC} = 2.7 V		12		12		12	
		V_{CC} = 3 V		24		24		24	
T_A	Ambient temperature	BGA package			–40	85			°C
		All other packages					–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs* , SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC244A									UNIT
		DB(2) (SSOP)	DGV(2) (TVSOP)	DW (2) (SOIC)	ZQN(2) (BGA)	N(2) (PDIP)	NS(2) (SO)	PW(2) (TSSOP)	RGY(3) (VQFN)	RWP(3) (X1QFN)	
		20 PINS									
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.1	128.7	90.9	198.7	61.6	90.1	114.7	50.3	79.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.2	43.7	55.3	106.8	46.5	56.4	48.4	58.4	63.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.3	70.2	58.8	143.1	42.5	57.7	65.6	28.3	46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.6	3.1	29.1	24.1	34.6	28.4	6.8	4.9	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.9	69.5	58.3	119.6	42.4	57.2	65.1	28.4	46.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	n/a	—	—	—	22.7	27.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) The package thermal impedance is calculated in accordance with JESD 51-5.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			–40 TO +85°C		–40 TO +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = –100 µA		1.65 V to 3.6 V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.3		V
	I_{OH} = –4 mA		1.65 V	1.29			1.2		1.05		
	I_{OH} = –8 mA		2.3 V	1.9			1.7		1.55		
	I_{OH} = –12 mA		2.7 V	2.2			2.2		2.05		
			3 V	2.4			2.4		2.25		
	I_{OH} = –24 mA		3 V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 µA		1.65 V to 3.6 V			0.1		0.2		0.3	V
	I_{OL} = 4 mA		1.65 V			0.24		0.45		0.6	
	I_{OL} = 8 mA		2.3 V			0.3		0.7		0.75	
	I_{OL} = 12 mA		2.7 V			0.4		0.4		0.6	
	I_{OL} = 24 mA		3 V			0.55		0.55		0.8	
I_I	V_I = 5.5 V or GND		3.6 V			±1		±5		±20	µA
I_{off}	V_I or V_O = 5.5 V		0			±1		±10		±20	µA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±1		±10		±20	µA
I_{CC}	V_I = V_{CC} or GND	I_O = 0	3.6 V			1		10		40	µA
	3.6 V ≤ V_I ≤ 5.5 V(1)	I_O = 0				1		10		40	
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500		500		5000	µA
C_i	V_I = V_{CC} or GND		3.3 V		4						pF
C_o	V_O = V_{CC} or GND		3.3 V		5.5						pF

(1) This applies in the disabled state only.

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			–40 TO +85°C		–40 TO +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.5 V	1	7	14.4	1	14.9	1	16.4	ns
			1.8 V ± 0.15 V	1	5.9	10.4	1	10.9	1	12.4	
			2.5 V ± 0.2 V	1	4.2	7.4	1	7.9	1	10	
			2.7 V	1	4.2	6.7	1	6.9	1	8.2	
			3.3 V ± 0.3 V	1.5	3.9	5.7	1.5	5.9	1.5	7.2	
t_{en}	$\overline{OE}$	Y	1.5 V	1	8.3	17.8	1	18.3	1	19.8	ns
			1.8 V ± 0.15 V	1	6.4	12.1	1	12.6	1	14.1	
			2.5 V ± 0.2 V	1	4.6	9.1	1	9.6	1	11.7	
			2.7 V	1	5	8.4	1	8.6	1	10.3	
			3.3 V ± 0.3 V	1.5	4.5	7.4	1.5	7.6	1.5	9.4	
t_{dis}	$\overline{OE}$	Y	1.5 V	1	7.2	15.6	1	16.1	1	17.6	ns
			1.8 V ± 0.15 V	1	5.8	11.6	1	12.1	1	13.6	
			2.5 V ± 0.2 V	1	3.7	7.3	1	7.8	1	9.9	
			2.7 V	1	3.8	6.6	1	6.8	1	8.6	
			3.3 V ± 0.3 V	1.5	3.8	6.3	1.5	6.5	1.5	8	
$t_{sk(o)}$			3.3 V ± 0.3 V					1		1.5	ns

6.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	1.8 V	43	pF
			2.5 V	43	
			3.3 V	44	
	Outputs disabled	f = 10 MHz	1.8 V	1	
			2.5 V	1	
			3.3 V	2	

6.8 Typical Characteristics

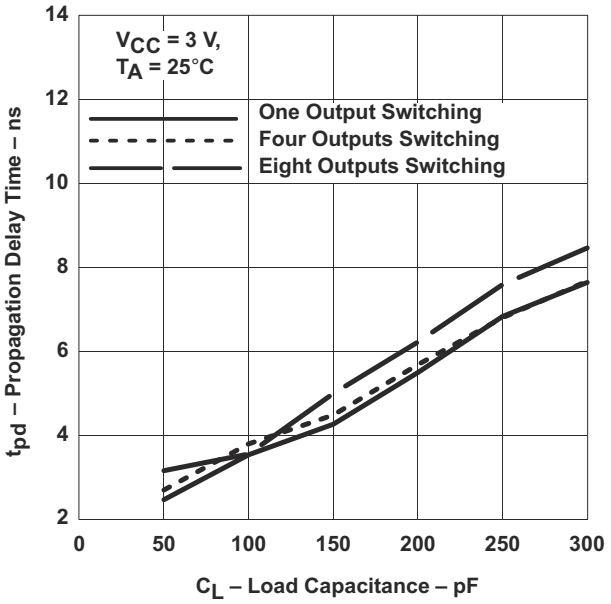


Figure 6-1. Propagation Delay (Low to High Transition) vs Load Capacitance

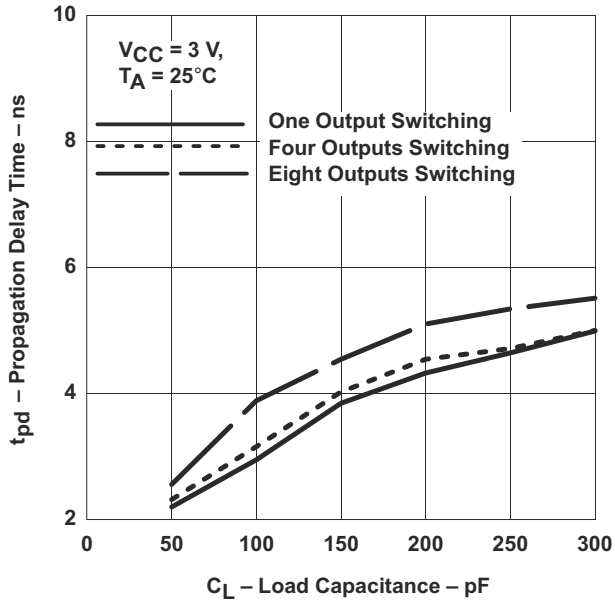
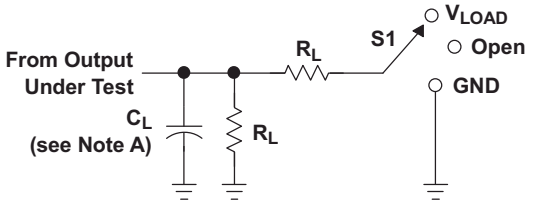


Figure 6-2. Propagation Delay (High to Low Transition) vs Load Capacitance

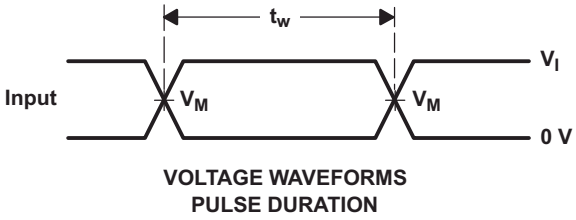
7 Parameter Measurement Information



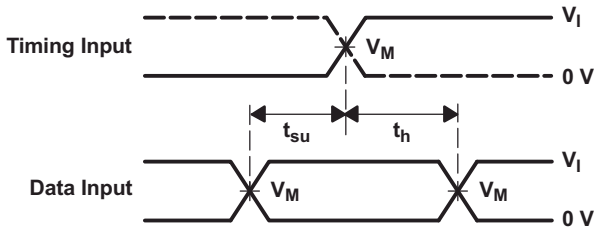
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

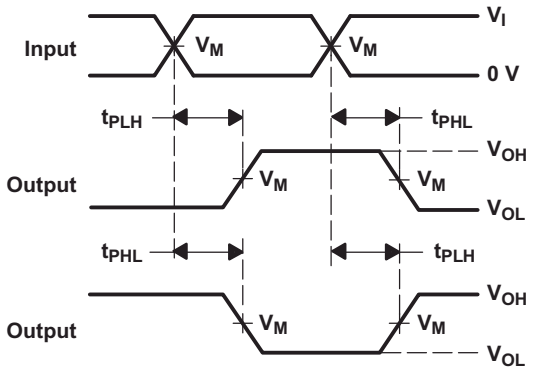
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.5 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



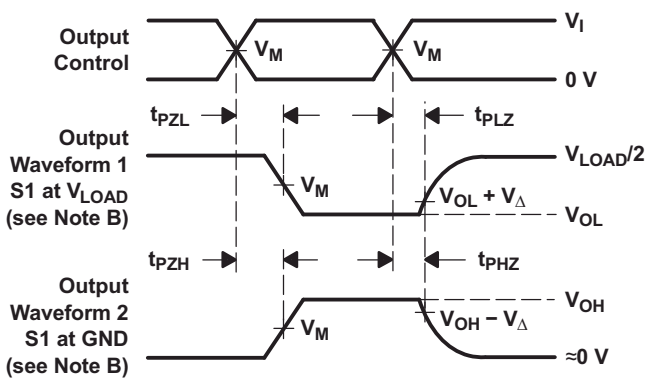
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

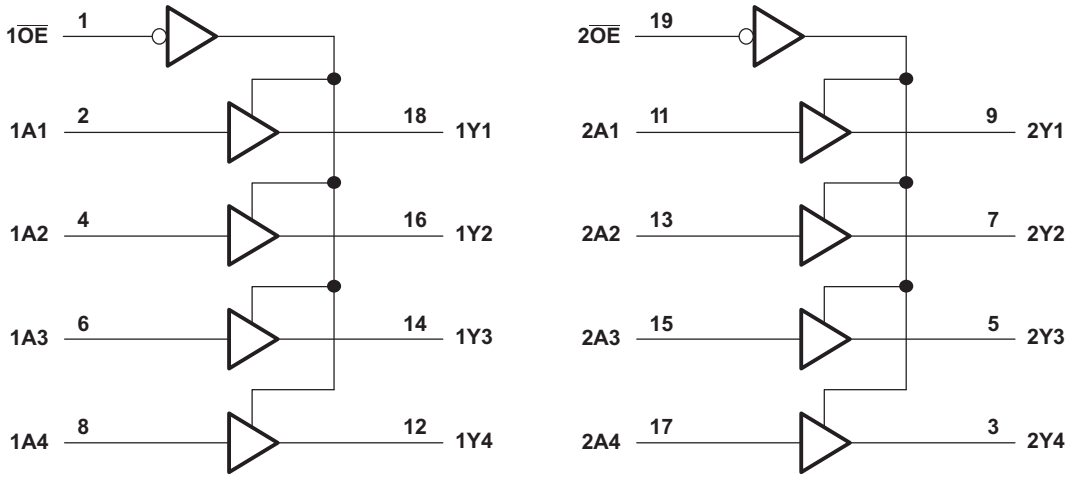
Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC244A device is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. The device passes data from the A inputs to the Y outputs when $\overline{OE}$ is low. The outputs are in the high-impedance state when $\overline{OE}$ is high. $\overline{OE}$ should be tied to V_{CC} through a pullup resistor to ensure the high-impedance state during power up or power down; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



Pin numbers shown are for the DB, DGV, DW, N, NS, PW, and RGY packages.

Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

- Allows down voltage translation
  - 5 V to 3.3 V
  - 5 V or 3.3 V to 1.8 V
- Inputs accept voltage levels up to 5.5 V
- It is available in ultra small logic 20 pin QFN package at 0.5 mm max height with 0.4 mm pitch.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LVC244A.

Table 8-1. Function Table

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Hi-Z

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SN74LVC244A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it ideal for down translation.

9.2 Typical Application

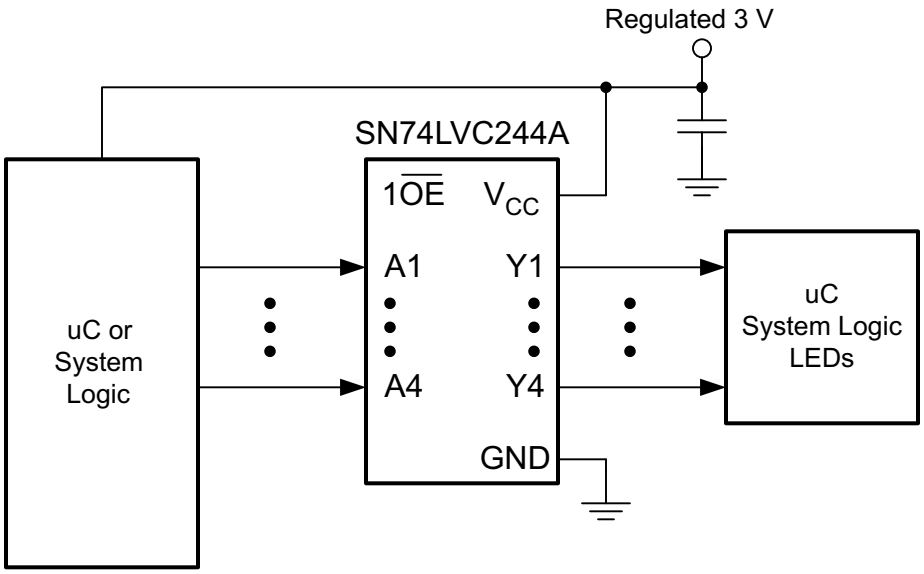


Figure 9-1. Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents in excess of maximum limits. The high drive will also create fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specification, see (Δt/ΔV) in the *Section 6.3* table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in the *Section 6.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Section 6.3* table at any valid V_{CC}.
2. Recommended maximum Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the *Section 6.1* table.
   - Outputs should not be pulled above V_{CC}.

9.2.3 Application Curves

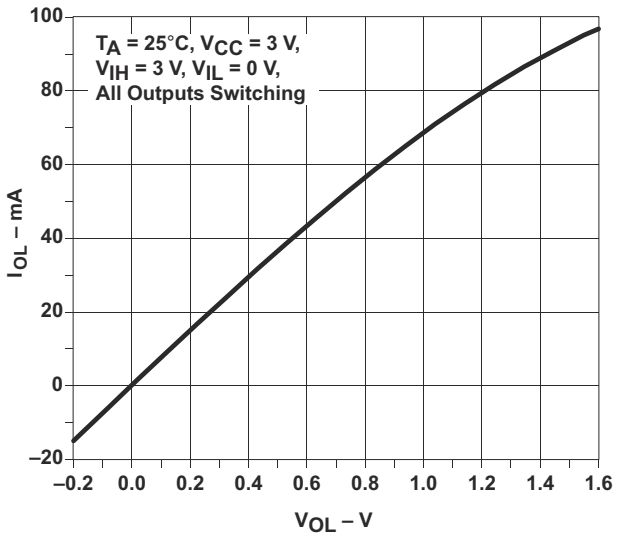


Figure 9-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

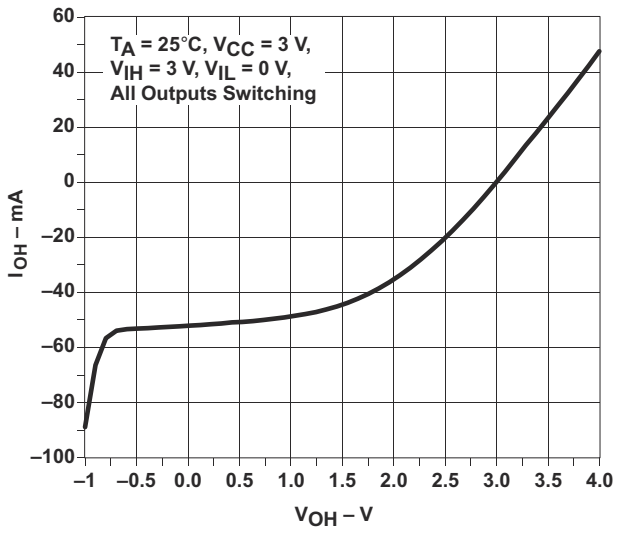


Figure 9-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

10 Power Supply Recommendations

The power supply may be any voltage between the MIN and MAX supply voltage rating located in the *Section 6.3* table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1 µF capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01 µF or 0.022 µF capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

Inputs should not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

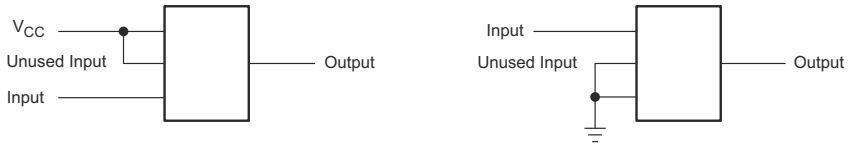


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC244ADBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADBRE4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244ADWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244AN	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74LVC244AN	Samples
SN74LVC244ANSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC244A	Samples
SN74LVC244APW	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWE4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWG4	ACTIVE	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWRG3	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWT	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244APWTE4	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC244APWTG4	ACTIVE	TSSOP	PW	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples
SN74LVC244ARGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC244A	Samples
SN74LVC244ARGYRG4	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC244A	Samples
SN74LVC244ARWPR	ACTIVE	X1QFN	RWP	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC244A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC244A :

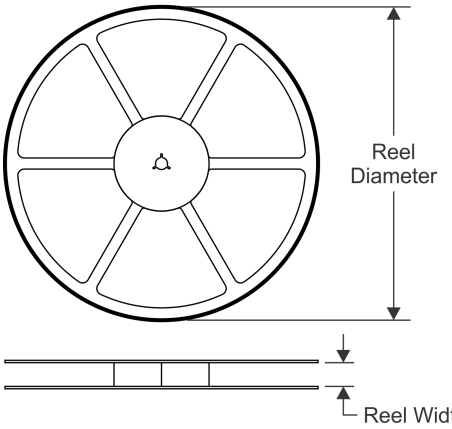
- Automotive: SN74LVC244A-Q1

NOTE: Qualified Version Definitions:

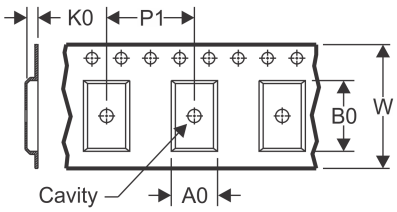
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

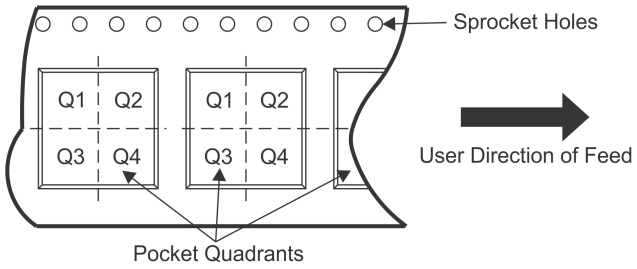


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

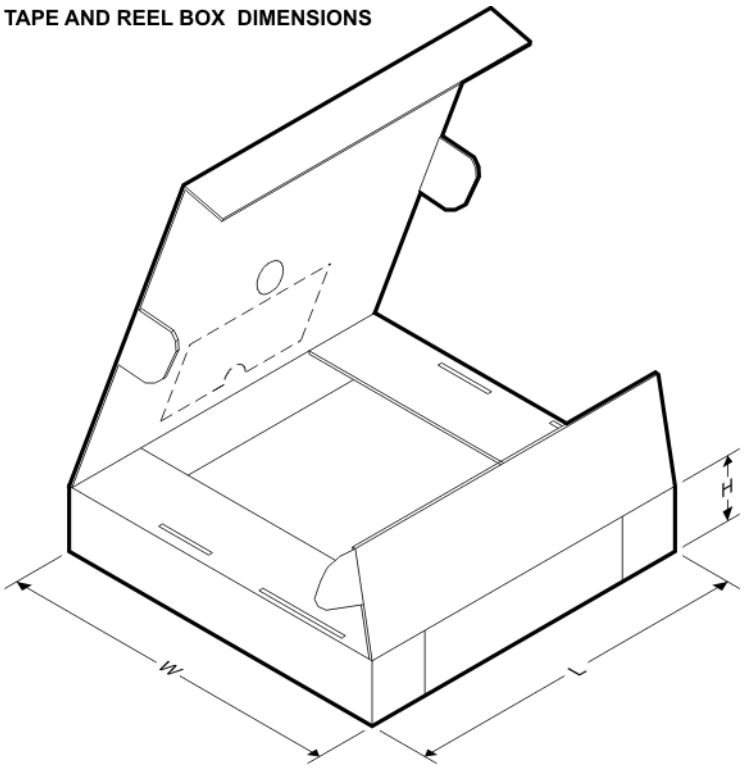
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC244ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC244ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC244ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC244ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LVC244ADWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC244ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC244APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC244APWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC244APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC244APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC244ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LVC244ARWPR	X1QFN	RWP	20	2000	178.0	13.5	2.85	3.65	0.75	8.0	12.0	Q1

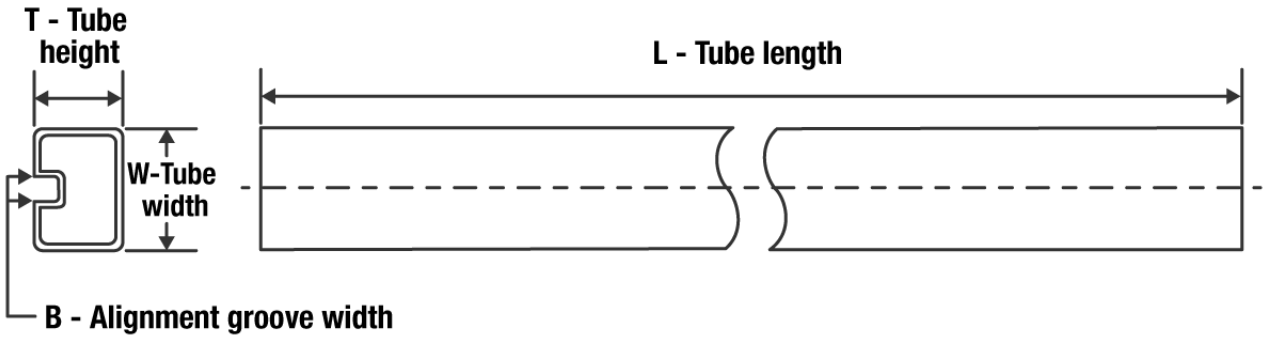
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC244ADBR	SSOP	DB	20	2000	853.0	449.0	35.0
SN74LVC244ADGVR	TVSOP	DGV	20	2000	853.0	449.0	35.0
SN74LVC244ADWR	SOIC	DW	20	2000	364.0	361.0	36.0
SN74LVC244ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC244ADWRG4	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC244ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC244APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC244APWR	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74LVC244APWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVC244APWRG4	TSSOP	PW	20	2000	853.0	449.0	35.0
SN74LVC244APWT	TSSOP	PW	20	250	853.0	449.0	35.0
SN74LVC244ARGYR	VQFN	RGY	20	3000	853.0	449.0	35.0
SN74LVC244ARWPR	X1QFN	RWP	20	2000	189.0	185.0	36.0

TUBE



*All dimensions are nominal

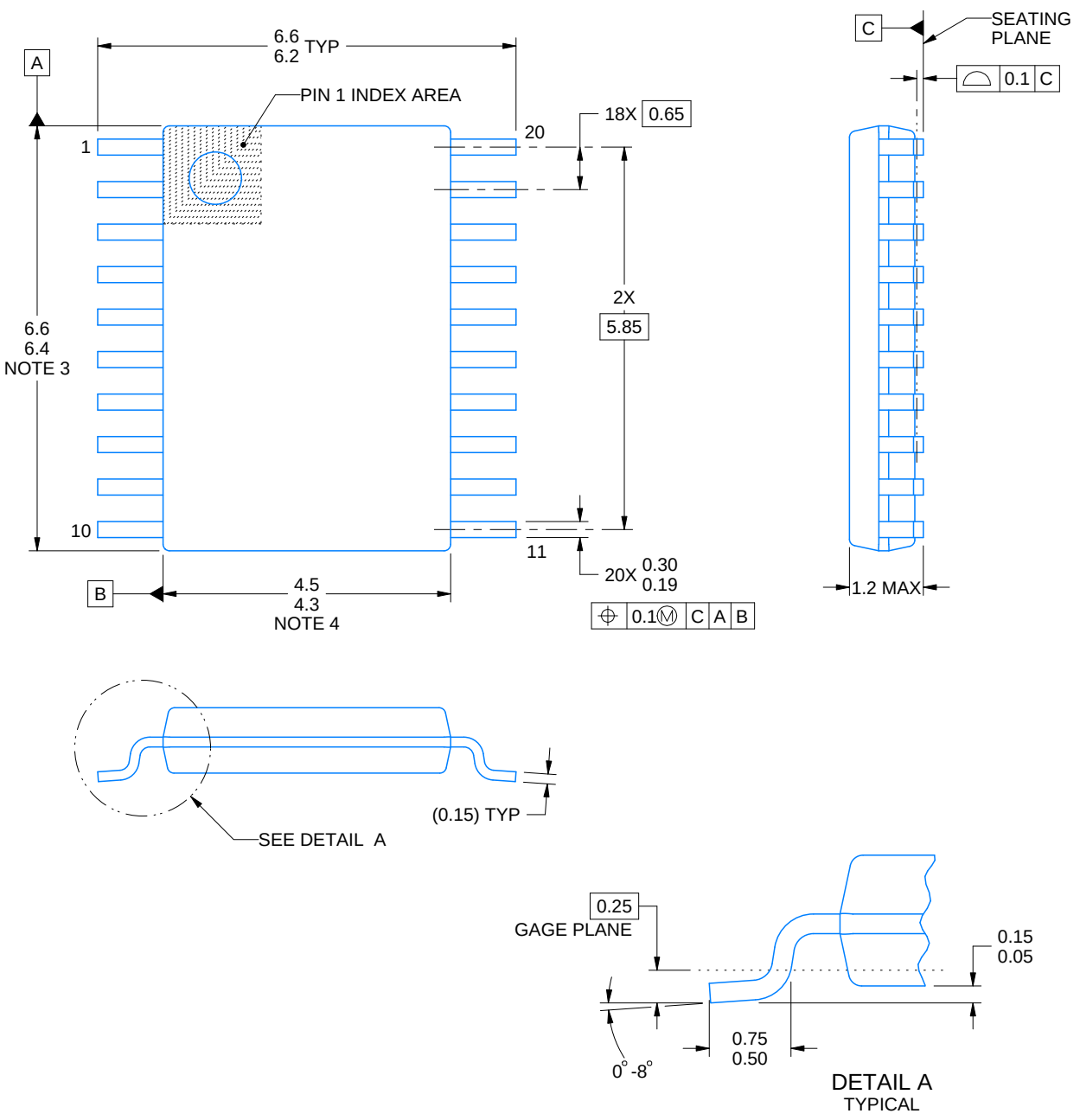
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC244ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC244ADWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC244ADWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC244AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74LVC244APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC244APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC244APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

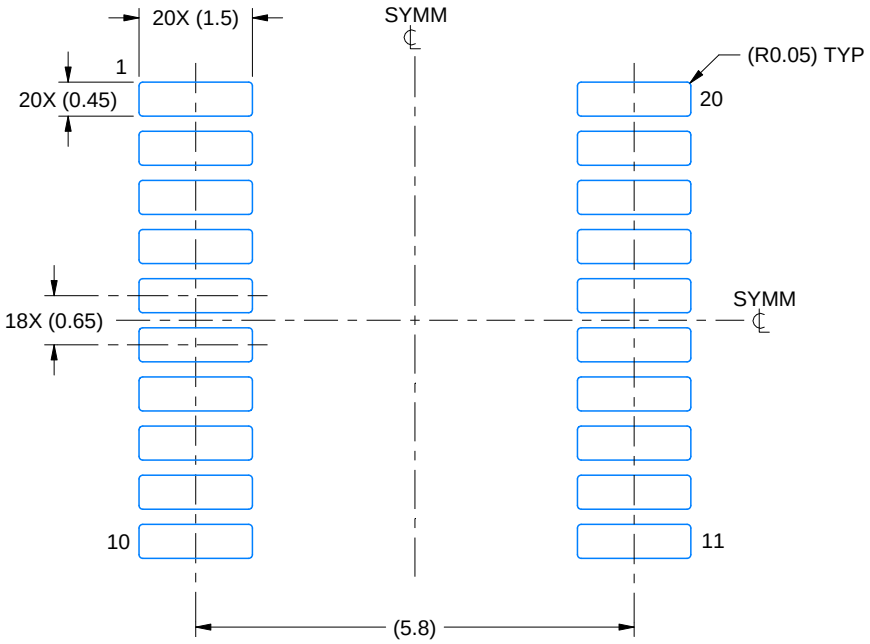
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



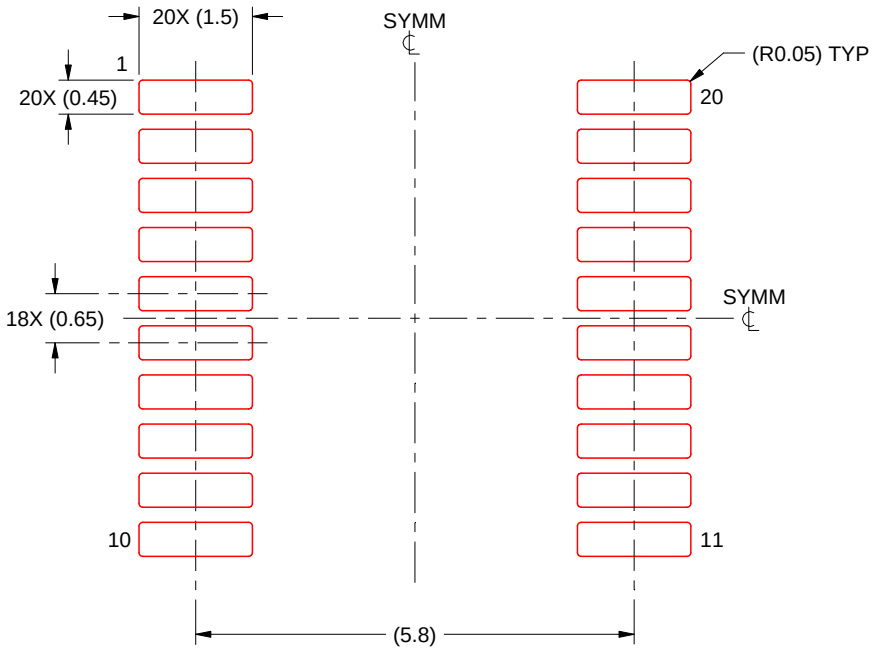
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



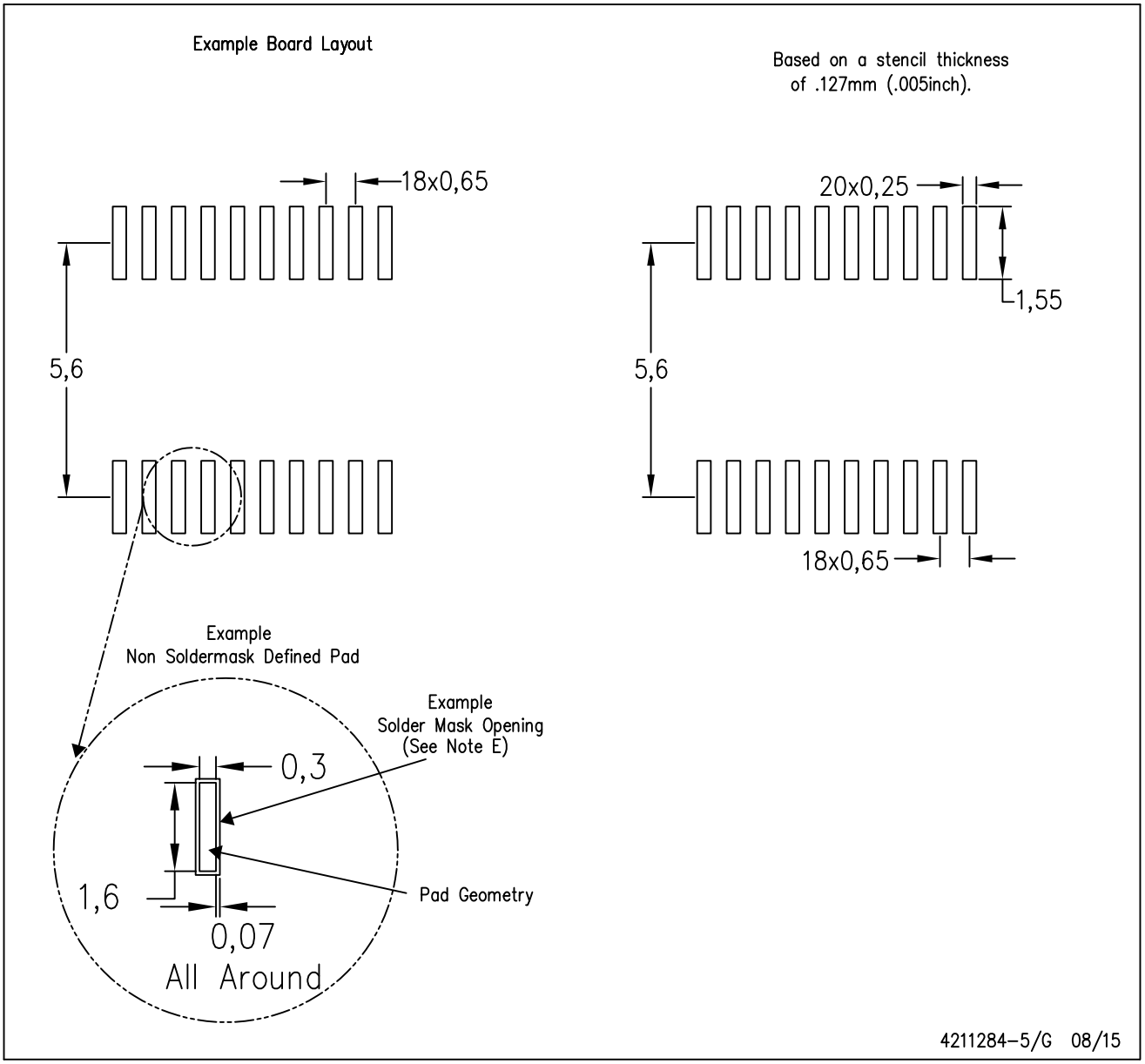
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



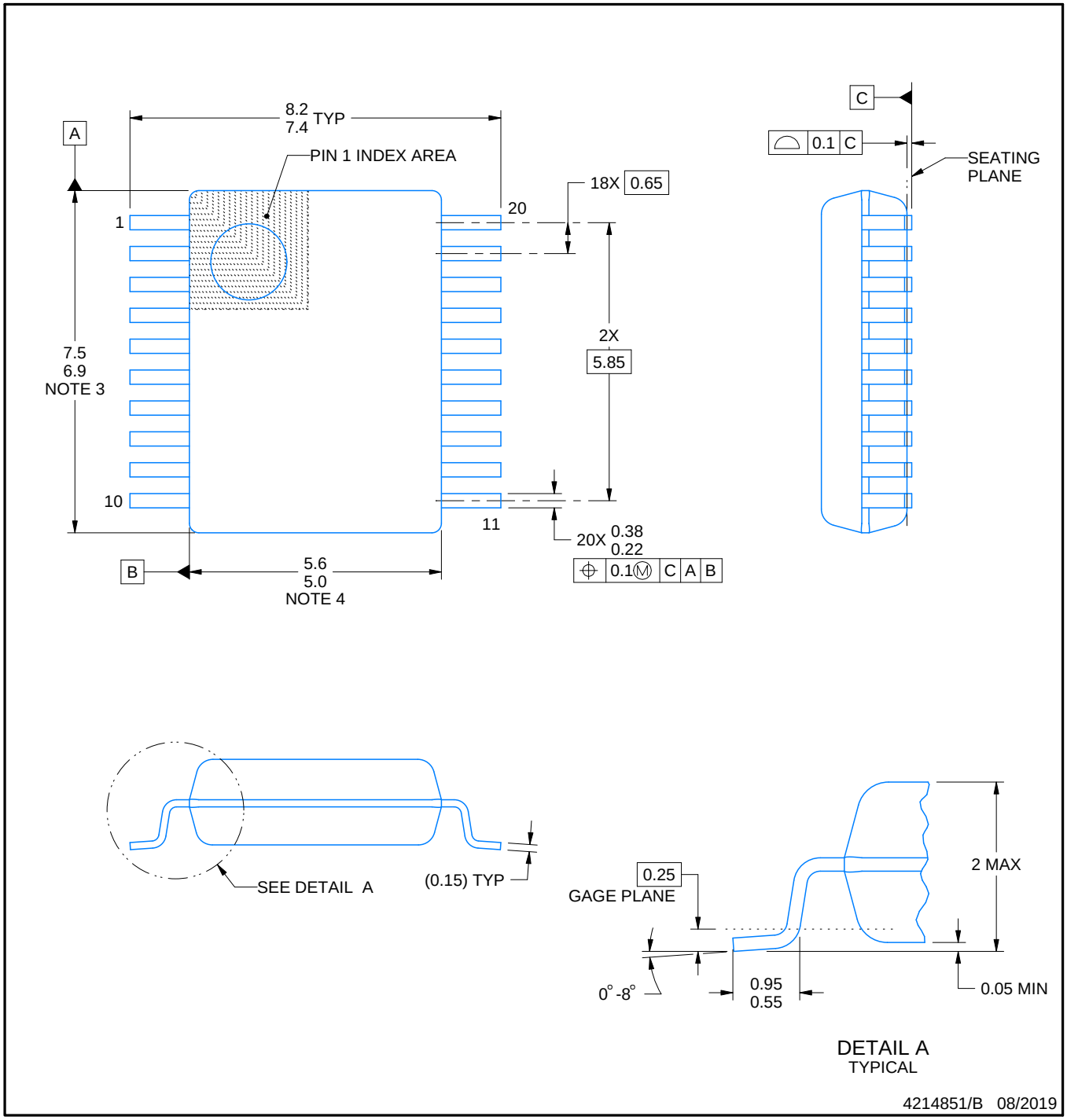
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0020A

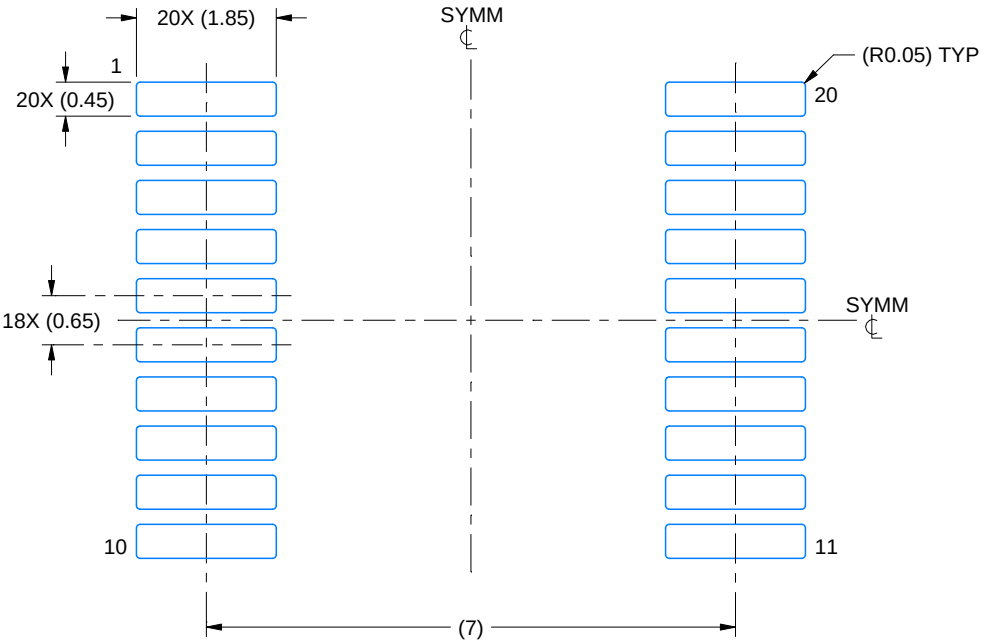
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

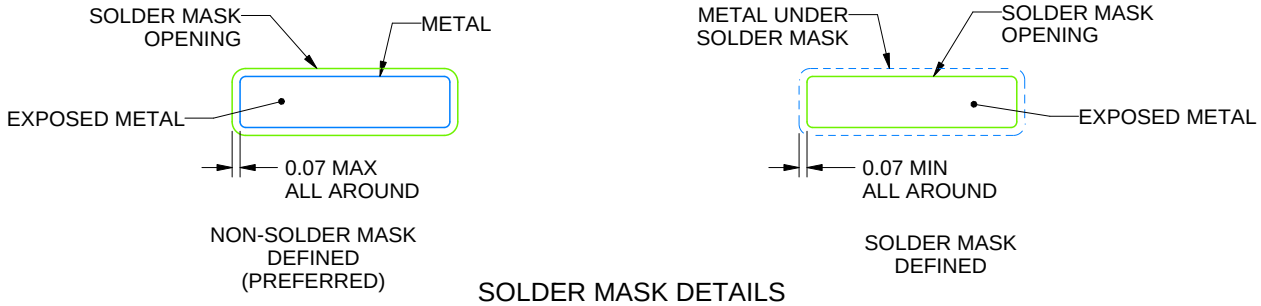


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

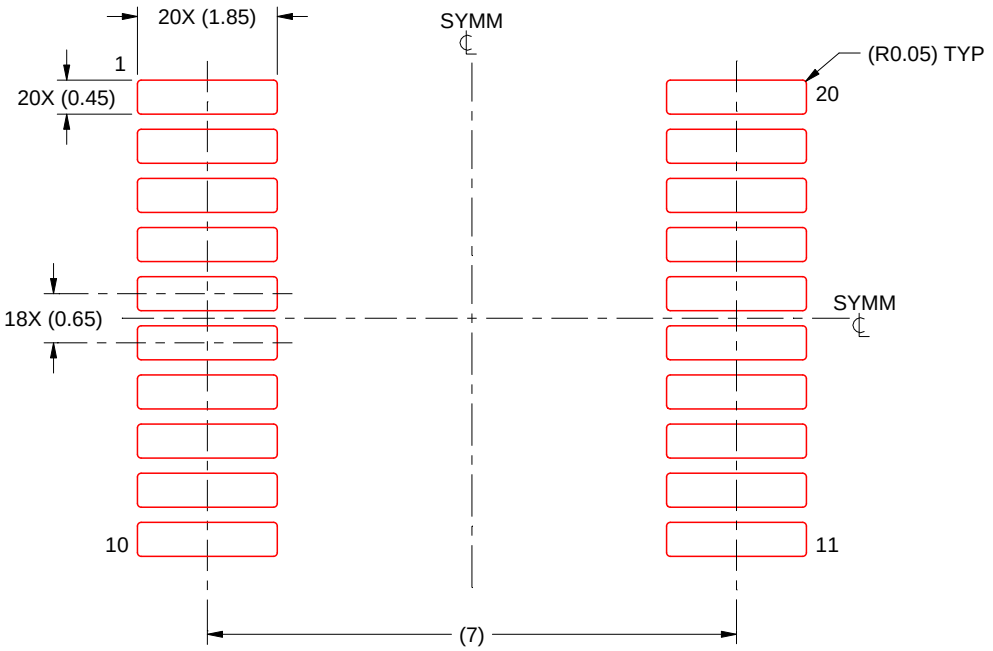
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

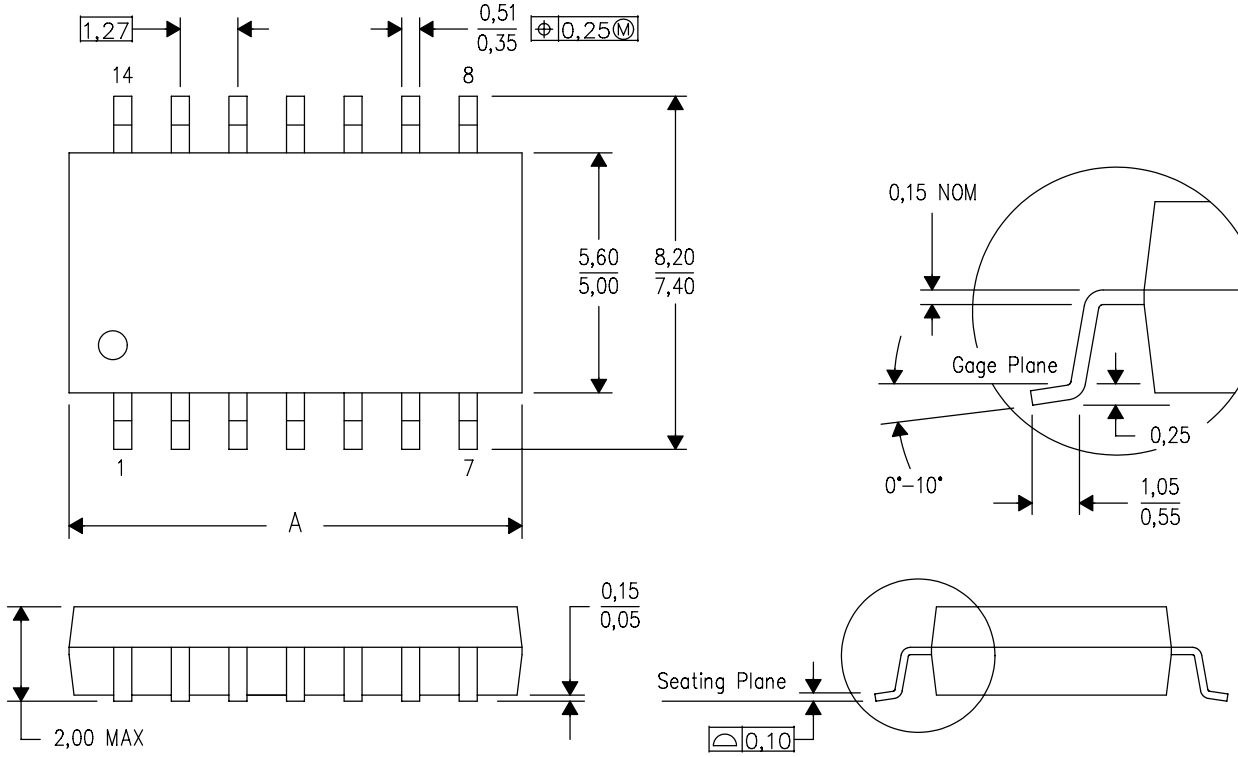
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

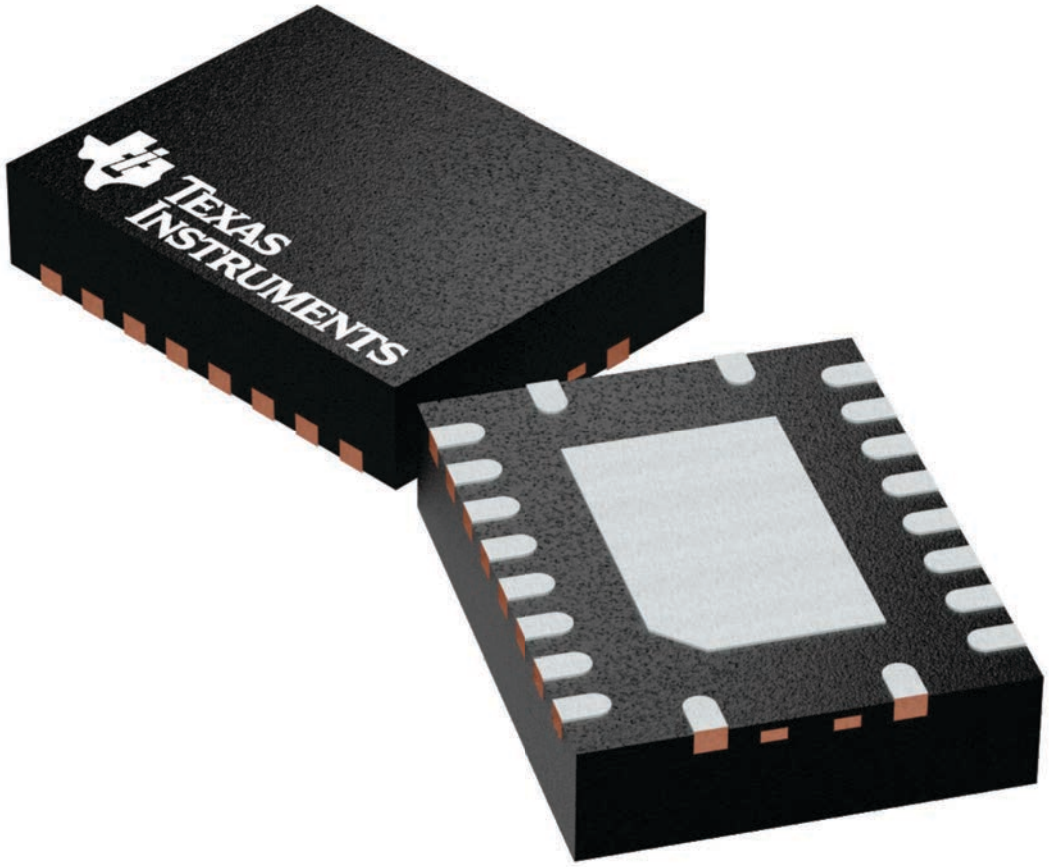
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



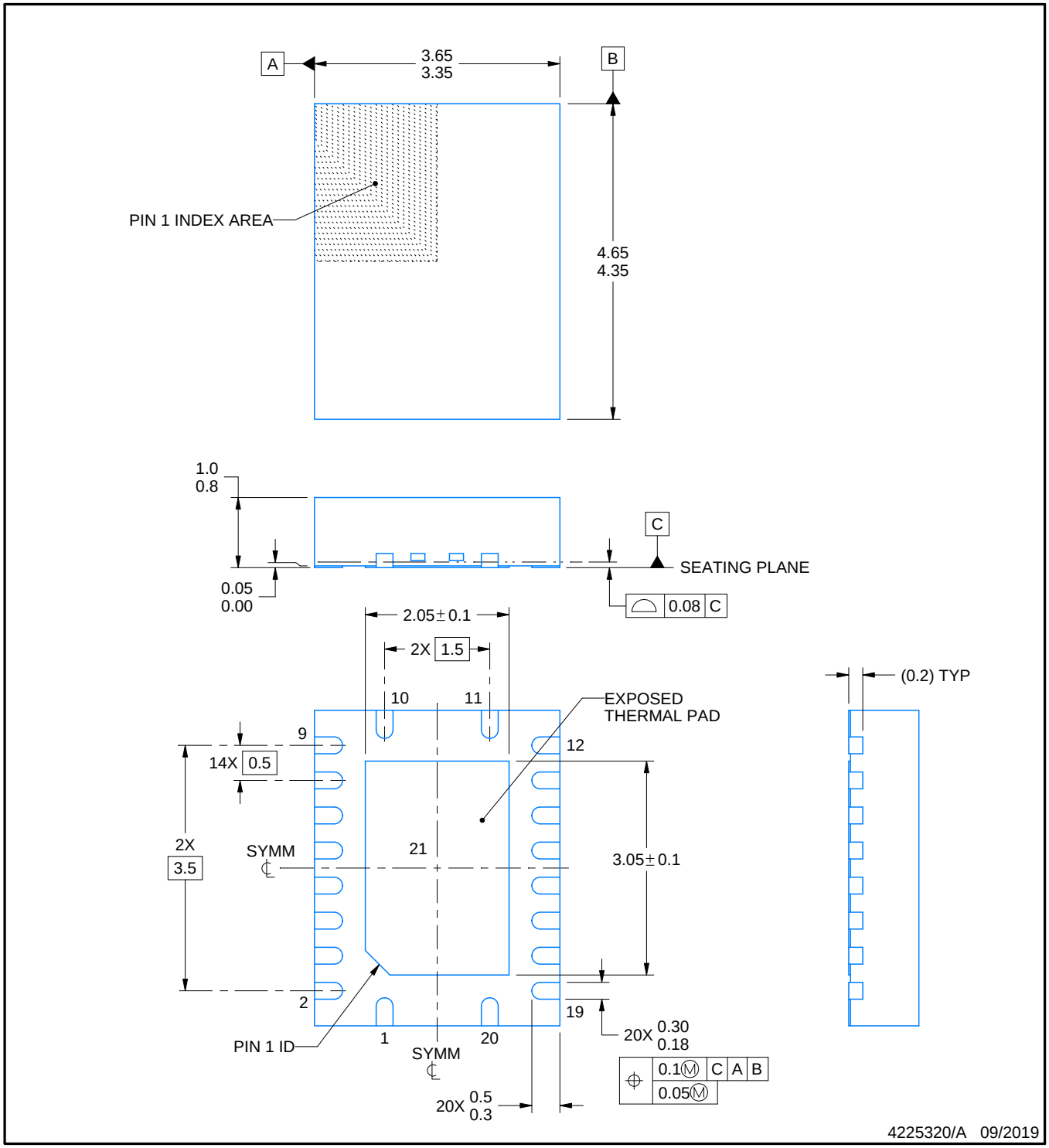
4225264/A

PACKAGE OUTLINE

RGY0020A

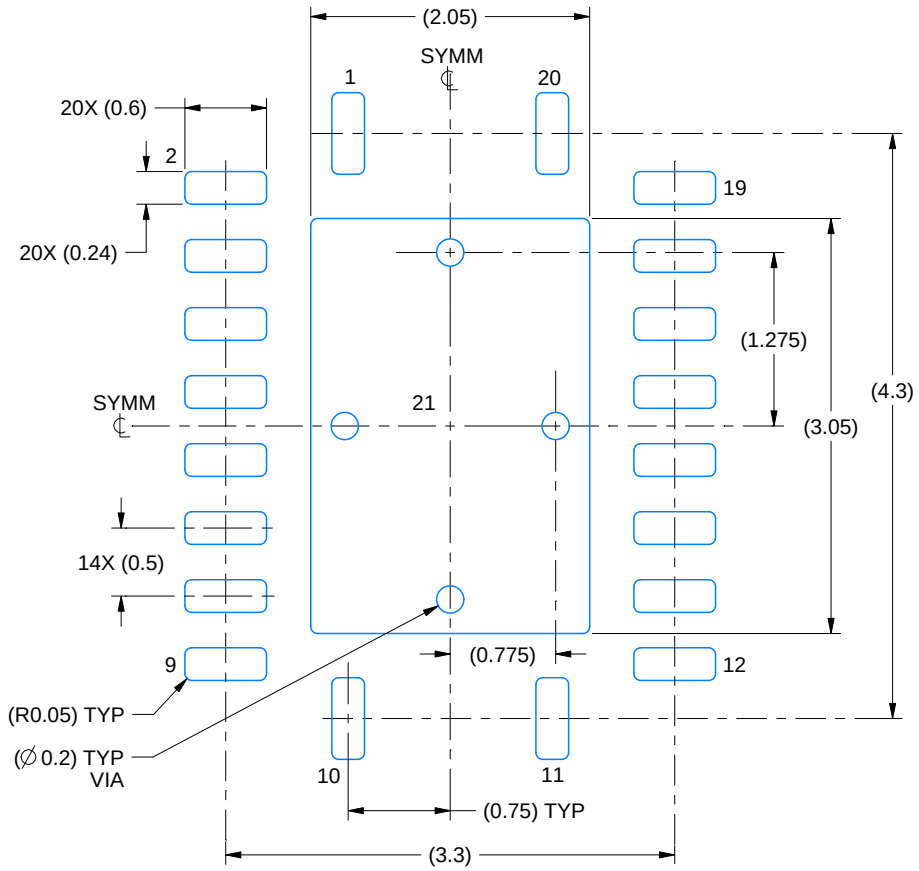
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

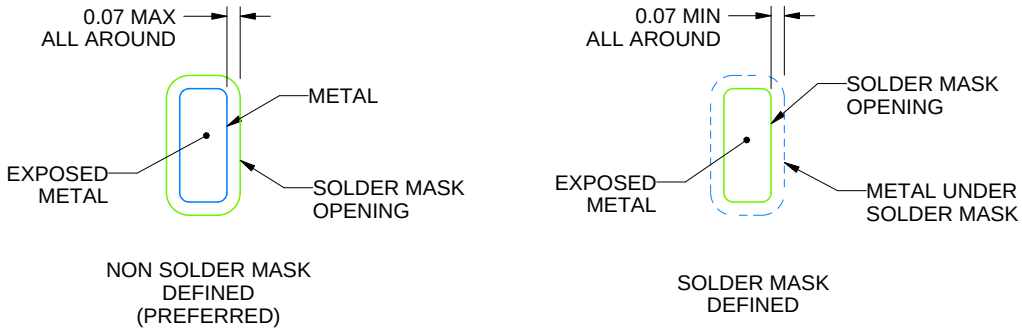


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

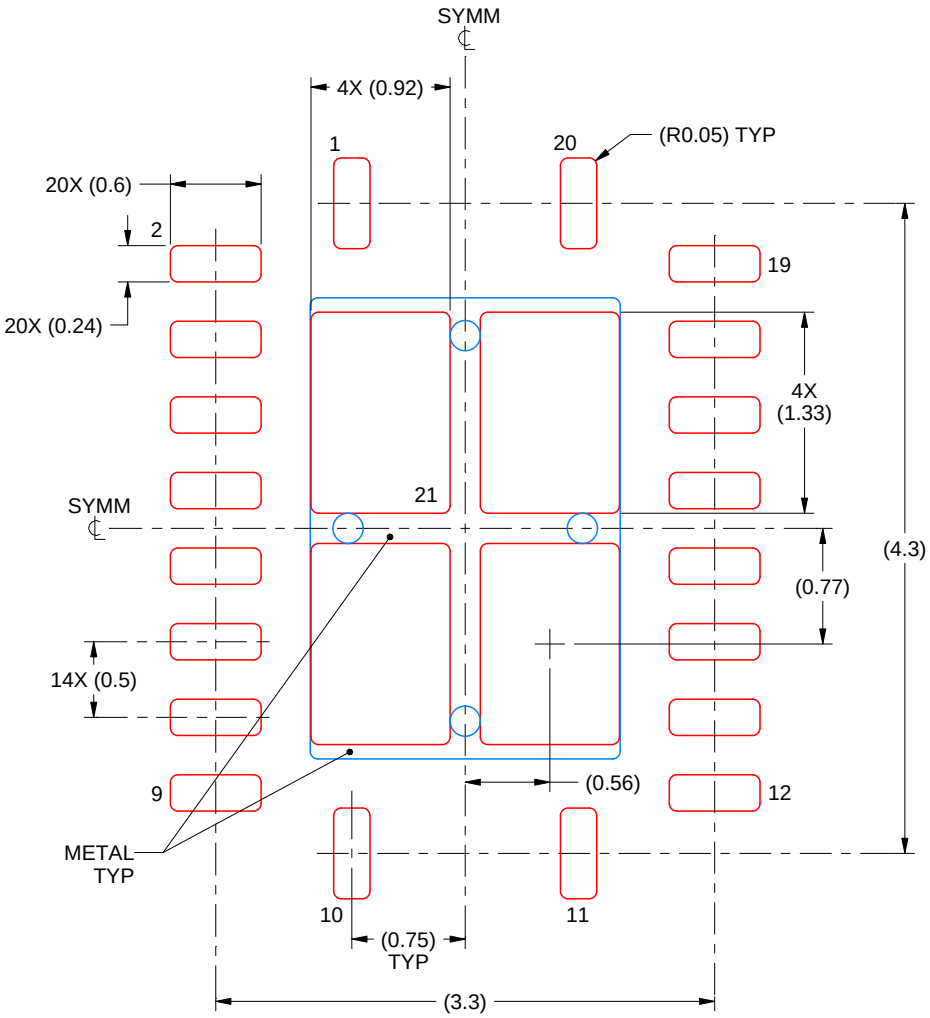


SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

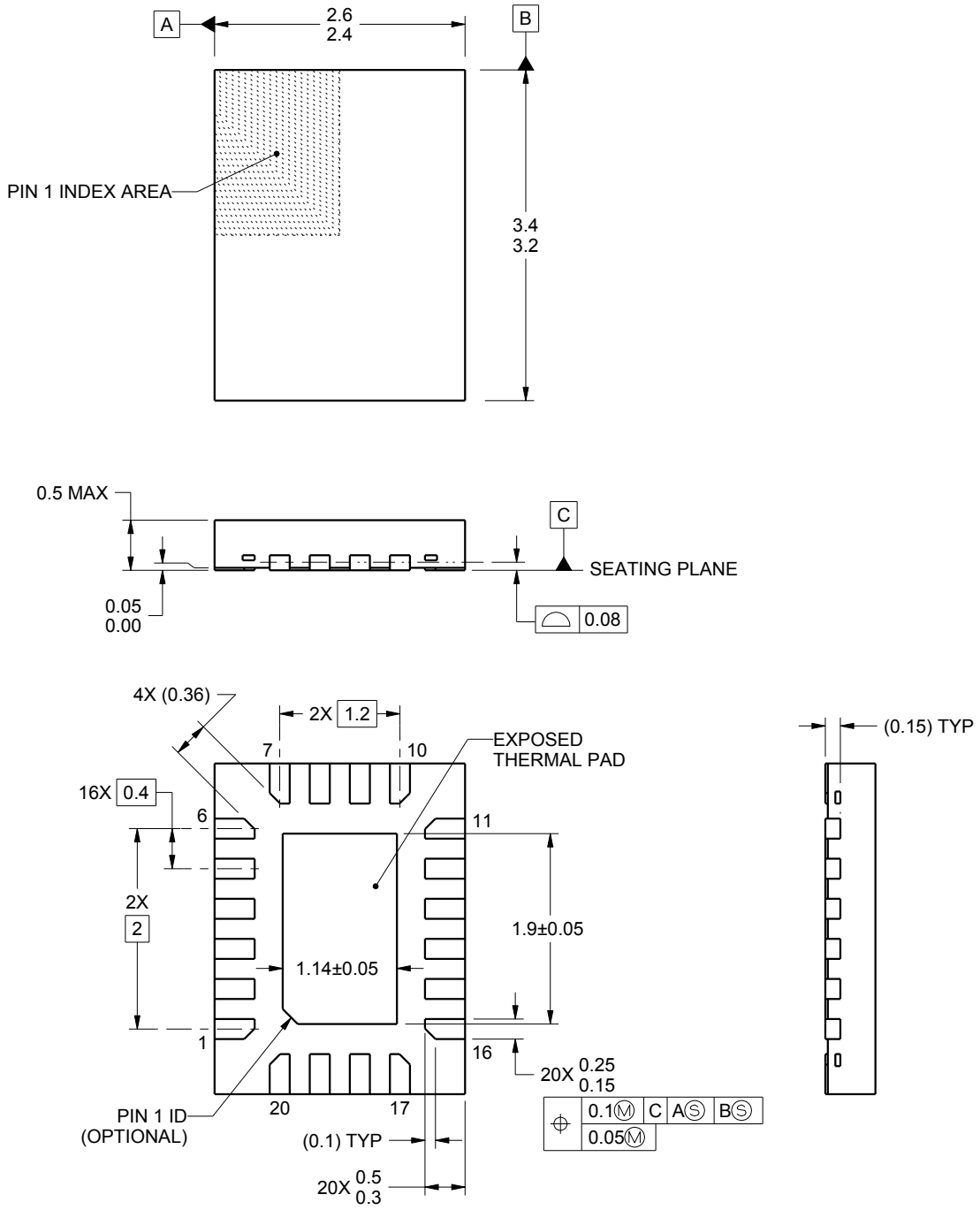
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RWP0020A

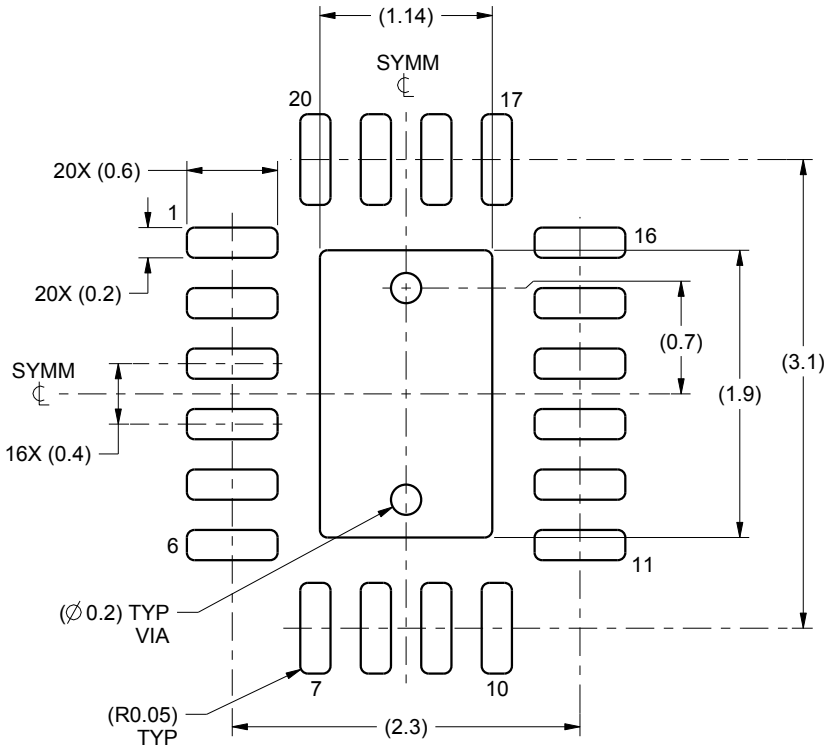
X1QFN - 0.5 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

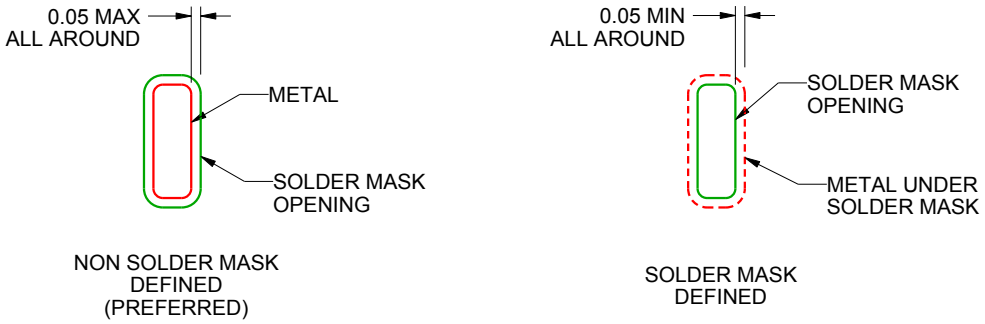


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

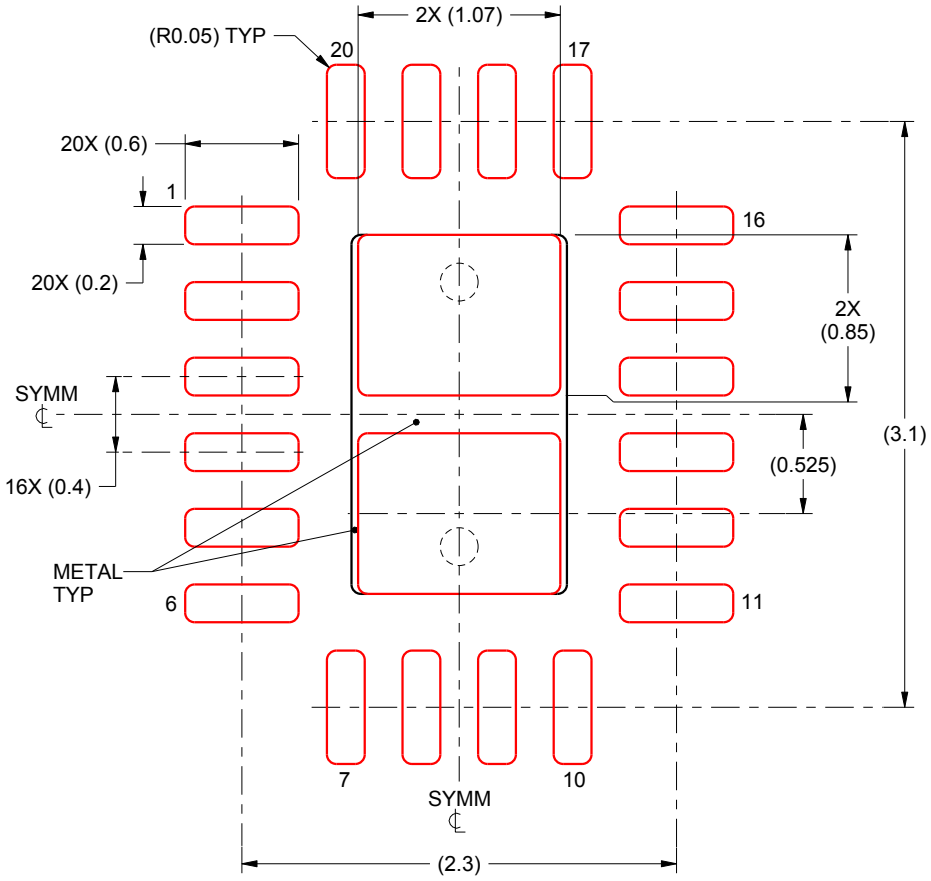


SOLDER MASK DETAILS

4221912/A 03/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221912/A 03/2015

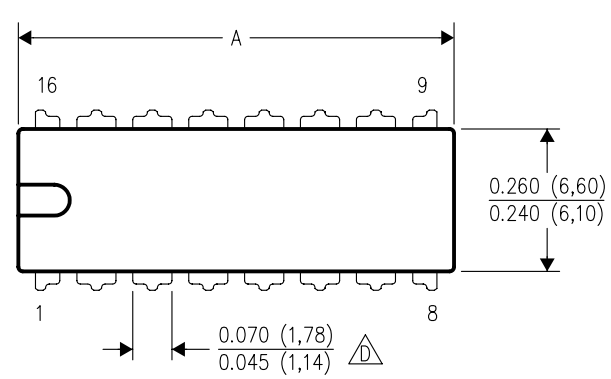
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

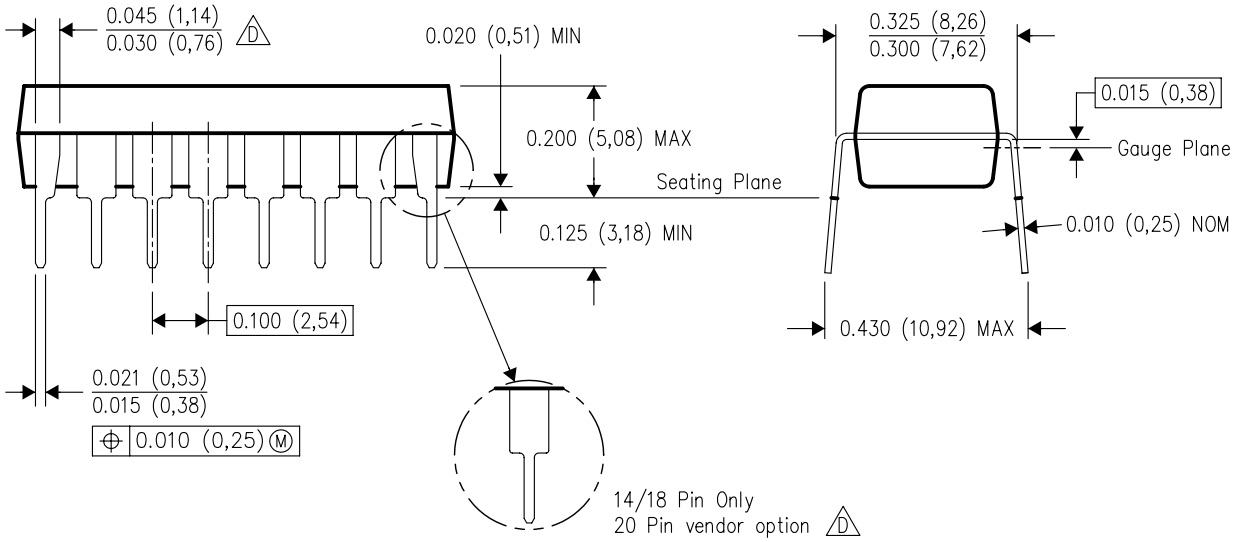
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

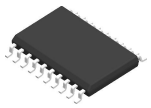


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

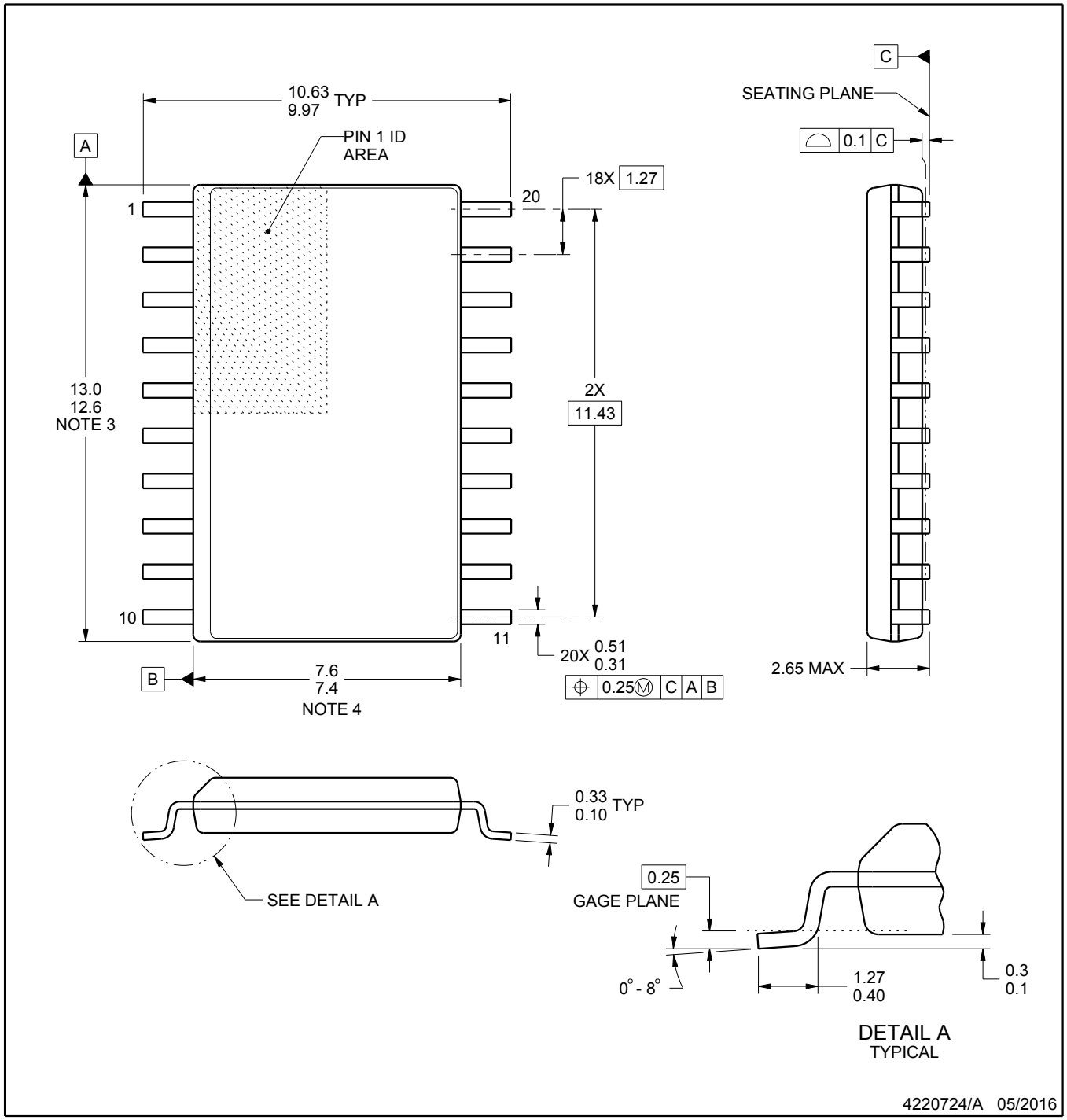


PACKAGE OUTLINE

DW0020A

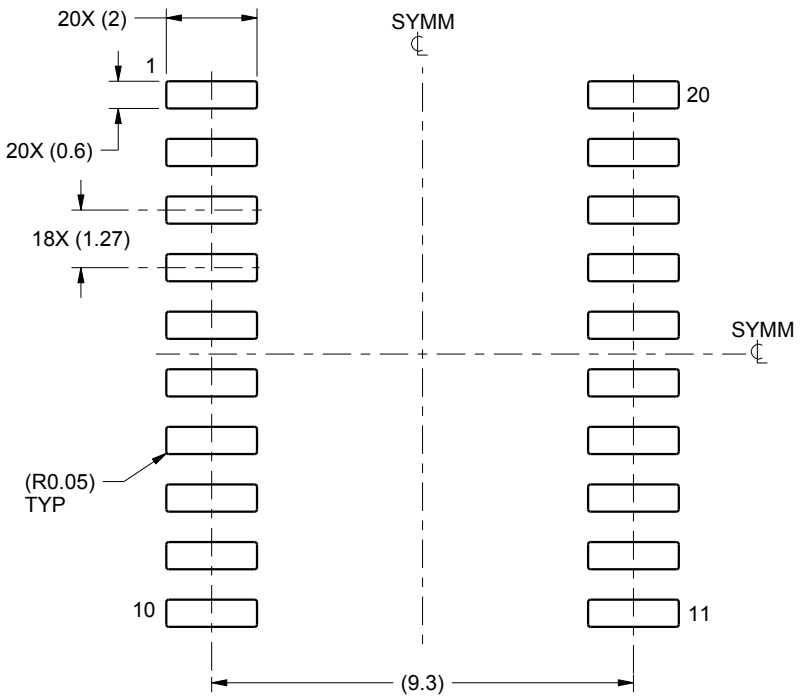
SOIC - 2.65 mm max height

SOIC

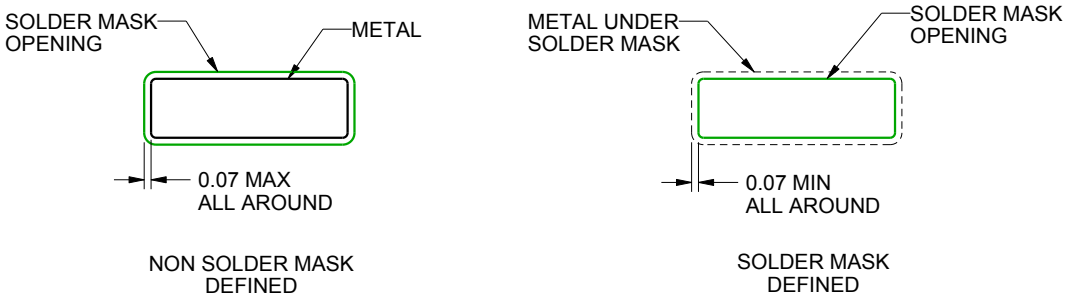


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

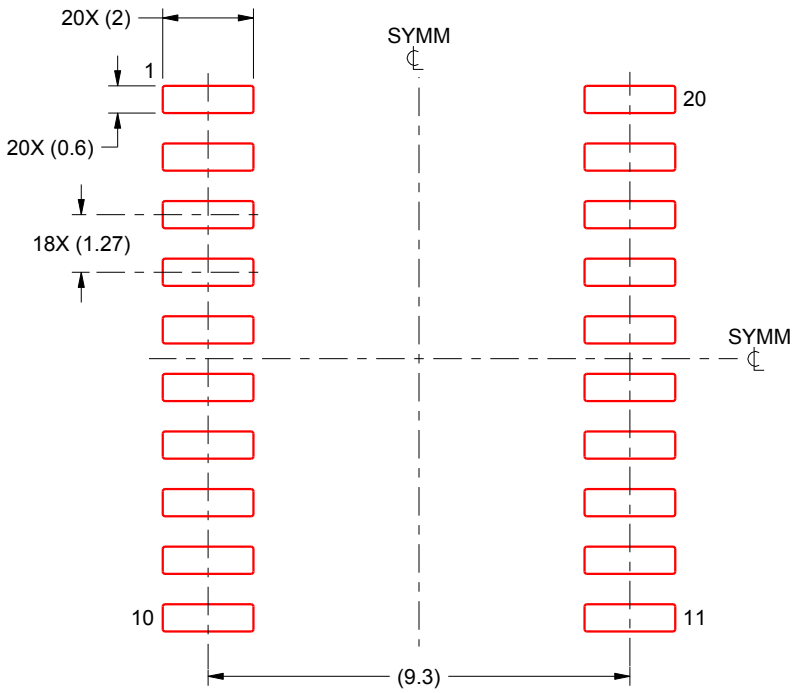


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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