LM7341 Rail-to-Rail Input/Output ±15V, 4.6 MHz GBW, Operational Amplifier in SOT-23 Package

Check for Samples: LM7341

FEATURES

- **(V_S = ±15V, T_A = 25°C, Typical Values.)**
- **Tiny 5-pin SOT-23 Package Saves Space**
- **Greater than Rail-to-Rail Input CMVR −15.3V to 15.3V**
- **Rail-to-Rail Output Swing −14.84V to 14.86V**
- **Supply Current 0.7 mA**
- **Gain Bandwidth 4.6 MHz**
- **Slew Rate 1.9 V/μs**
- **Wide Supply Range 2.7V to 32V**
- **High Power Supply Rejection Ratio 106 dB**
- **High Common Mode Rejection Ratio 115 dB**
- **Excellent Gain 106 dB**
- **Temperature Range −40°C to 125°C**
- **Tested at −40°C, 125°C and 25°C at 2.7V, ±5V and ±15V**

APPLICATIONS

- **Automotive**
- **Industrial Robotics**
- **Sensor Output Buffers**
- **Multiple Voltage Power Supplies**
- **Reverse Biasing of Photodiodes**
- **Low Current Optocouplers**
- **High Side Sensing**
- **Comparator**
- **Battery Chargers**
- **Test Point Output Buffers**
- **Below Ground Current Sensing**

DESCRIPTION

The LM7341 is a rail-to-rail input and output amplifier in a small SOT-23 package with a wide supply voltage and temperature range. The LM7341 has a 4.6 MHz gain bandwidth and a 1.9 volt per microsecond slew rate, and draws 0.75 mA of supply current at no load.

The LM7341 is tested at −40°C, 125°C and 25°C with modern automatic test equipment. Detailed performance specifications at 2.7V, ±5V, and ±15V and over a wide temperature range make the LM7341 a good choice for automotive, industrial, and other demanding applications.

Greater than rail-to-rail input common mode range with a minimum 76 dB of common mode rejection at ±15V makes the LM7341 a good choice for both high and low side sensing applications.

LM7341 performance is consistent over a wide voltage range, making the part useful for applications where the supply voltage can change, such as automotive electrical systems and battery powered electronics.

The LM7341 uses a small SOT23-5 package, which takes up little board space, and can be placed near signal sources to reduce noise pickup.

Typical Performance Characteristics

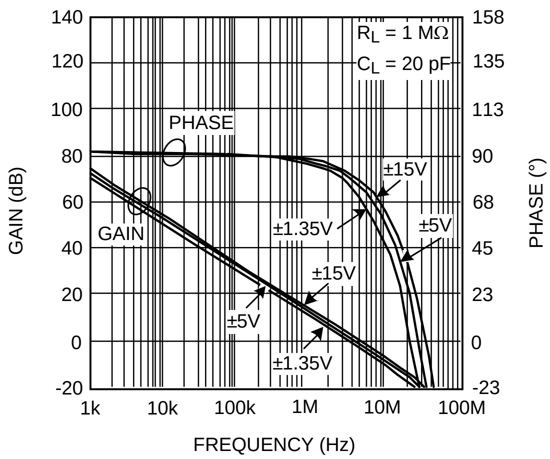


Figure 1. Open Loop Frequency Response

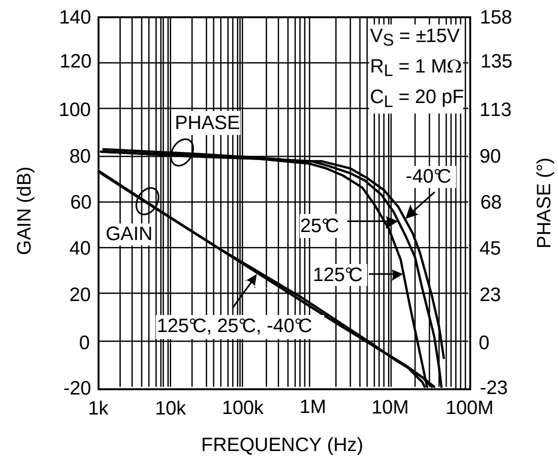


Figure 2. Open Loop Frequency Response

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±15V
Voltage at Input/Output Pin		(V^+) + 0.3V, (V^-) −0.3V
Supply Voltage ($V_S = V^+ - V^-$)		35V
Input Current		±10 mA
Output Current(4)		±20 mA
Power Supply Current		25 mA
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp. (10 sec.)	260°C
Storage Temperature Range		−65°C to 150°C
Junction Temperature(5)		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly unto a PC board.

Operating Ratings(1)

Supply Voltage ($V_S = V^+ - V^-$)		2.5V to 32V
Temperature Range(2)		−40°C to 125°C
Package Thermal Resistance ($θ_{JA}$)	5-Pin SOT-23	325°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/θ_{JA}$. All numbers apply for packages soldered directly unto a PC board.

2.7V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_{OUT} = 1.35V and R_L > 1 MΩ to 1.35V. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V and V_{CM} = 2.2V	−4 **−5**	±0.2	+4 **+5**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift			±2		μV/°C
I_B	Input Bias Current	V_{CM} = 0.5V	−180 **−200**	−90		nA
		V_{CM} = 2.2V		30	60 **70**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V and V_{CM} = 2.2V		1	40 **50**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.0V	82 **80**	106		dB
		0V ≤ V_{CM} ≤ 2.7V	62 **60**	80		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V V_{CM} = 0.5V	86 **84**	106		dB
CMVR	Common Mode Voltage Range	CMRR > 60 dB		−0.3	**0.0**	V
			2.7	3.0		
A_{VOL}	Open Loop Voltage Gain	0.5V ≤ V_O ≤ 2.2V R_L = 10 kΩ to 1.35V	12 **8**	65		V/mV
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 1.35V V_{ID} = 100 mV		50	120 **150**	mV from either rail
		R_L = 2 kΩ to 1.35V V_{ID} = 100 mV		95	150 **200**	
	Output Voltage Swing Low	R_L = 10 kΩ to 1.35V V_{ID} = −100 mV		55	120 **150**	
		R_L = 2 kΩ to 1.35V V_{ID} = −100 mV		100	150 **200**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = 0V V_{ID} = 200 mV	6 **4**	12		mA
		Sinking, V_{OUT} = 0V V_{ID} = −200 mV	5 **3**	10		
I_S	Supply Current	V_{CM} = 0.5V and V_{CM} = 2.2V		0.6	0.9 **1.0**	mA
SR	Slew Rate	±1V Step		1.5		V/μs
GBW	Gain Bandwidth	f = 100 kHz, R_L = 100 kΩ		3.6		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		35		nV/√Hz
i_n	Input Referred Voltage Noise Density	f = 1 kHz		0.28		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 10 kHz		−66		dB
t_{PD}	Propagation Delay	Overdrive = 50 mV (3)		4		μs
		Overdrive = 1V (3)		3		
t_r	Rise Time	20% to 80% (3)		1		μs
t_f	Fall Time	80% to 20% (3)		1		μs

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The maximum differential voltage between the input pins is V_{IN} Differential = ±15V.

±5V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = +5V, V^- = −5V, V_{CM} = V_{OUT} = 0V and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [1]	Typ [2]	Max [1]	Units
V_{OS}	Input Offset Voltage	V_{CM} = −4.5V and V_{CM} = 4.5V	−4 **−5**	±0.2	+4 **+5**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift			±2		μV/°C
I_B	Input Bias Current	V_{CM} = −4.5V	−200 **−250**	−95		nA
		V_{CM} = 4.5V		35	70 **80**	
I_{OS}	Input Offset Current	V_{CM} = −4.5V and V_{CM} = 4.5V		1	40 **50**	nA
CMRR	Common Mode Rejection Ratio	−5V ≤ V_{CM} ≤ 3V	84 **82**	112		dB
		−5V ≤ V_{CM} ≤ 5V	72 **70**	92		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V, V_{CM} = −4.5V	86 **84**	106		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 65 dB		−5.3	**−5.0**	V
			5.0	5.3		
A_{VOL}	Open Loop Voltage Gain	−4V ≤ V_O ≤ 4V R_L = 10 kΩ to 0V	20 **12**	110		V/mV
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0V, V_{ID} = 100 mV		80	150 **200**	mV from either rail
		R_L = 2 kΩ to 0V, V_{ID} = 100 mV		170	300 **400**	
	Output Voltage Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV		90	150 **200**	
		R_L = 2 kΩ to 0V V_{ID} = −100 mV		210	300 **400**	
I_{OUT}	Output Current	Sourcing, V_{OUT} = −5V V_{ID} = 200 mV	6 **4**	11		mA
		Sinking, V_{OUT} = 5V V_{ID} = −200 mV	6 **4**	12		
I_S	Supply Current	V_{CM} = −4.5V and V_{CM} = 4.5V		0.65	1.0 **1.1**	mA
SR	Slew Rate	±4V Step		1.7		V/μs
GBW	Gain Bandwidth	f = 100 kHz, R_L = 100 kΩ		4.0		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		33		$nV/\sqrt{Hz}$
i_n	Input Referred Voltage Noise Density	f = 1 kHz		0.26		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 10 kHz		−66		dB
t_{PD}	Propagation Delay	Overdrive = 50 mV [3]		8		μs
		Overdrive = 1V [3]		6		
t_r	Rise Time	20% to 80% [3]		5		μs
t_f	Fall Time	80% to 20% [3]		5		μs

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The maximum differential voltage between the input pins is V_{IN} Differential = ±15V.

±15V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_A = 25°C, V^+ = 15V, V^- = −15V, V_{CM} = V_{OUT} = 0V and R_L > 1 MΩ to 0V. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −14.5V and V_{CM} = 14.5V	−4 **−5**	±0.2	+4 **+5**	mV
TCV_{OS}	Input Offset Voltage Temperature Drift			±2		µV/°C
I_B	Input Bias Current	V_{CM} = −14.5V	−250 **−300**	−110		nA
		V_{CM} = 14.5V		40	80 **90**	
I_{OS}	Input Offset Current	V_{CM} = −14.5V and V_{CM} = 14.5V		1	40 **50**	nA
CMRR	Common Mode Rejection Ratio	−15V ≤ V_{CM} ≤12V	84 **82**	115		dB
		−15V ≤ V_{CM} ≤ 15V	78 **76**	100		
PSRR	Power Supply Rejection Ratio	2.7V ≤ V_S ≤ 30V, V_{CM} = −14.5V	86 **84**	106		dB
CMVR	Common Mode Voltage Range	CMRR > 80 dB		−15.3	**−15.0**	V
			15.0	15.3		
A_{VOL}	Open Loop Voltage Gain	−13V ≤ V_O ≤ 13V R_L = 10 kΩ to 0V	25 **15**	200		V/mV
V_{OUT}	Output Voltage Swing High	R_L = 10 kΩ to 0V V_{ID} = 100 mV		135	300 **400**	mV from either rail
	Output Voltage Swing Low	R_L = 10 kΩ to 0V V_{ID} = −100 mV		160	300 **400**	
I_{OUT}	Output Current (3)	Sourcing, V_{OUT} = −15V V_{ID} = 200 mV	5 **3**	10		mA
		Sinking, V_{OUT} = 15V V_{ID} = −200 mV	8 **5**	13		
I_S	Supply Current	V_{CM} = −14.5V and V_{CM} = 14.5V		0.7	1.2 **1.3**	mA
SR	Slew Rate	±12V Step		1.9		V/µs
GBW	Gain Bandwidth	f = 100 kHz, R_L = 100 kΩ		4.6		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		31		nV/√Hz
i_n	Input Referred Voltage Noise Density	f = 1 kHz		0.27		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 10 kHz		−65		dB
t_{PD}	Propagation Delay	Overdrive = 50 mV (4)		17		µs
		Overdrive = 1V (4)		12		
t_r	Rise Time	20% to 80% (4)		13		µs
t_f	Fall Time	80% to 20% (4)		13		µs

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly unto a PC board.
(4) The maximum differential voltage between the input pins is V_{IN} Differential = ±15V.

Connection Diagram

5-Pin SOT-23

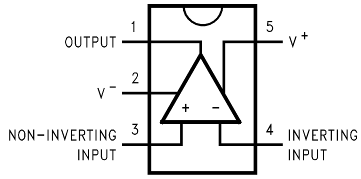


Figure 3. Top View

Typical Performance Characteristics

Output Swing vs. Sourcing Current

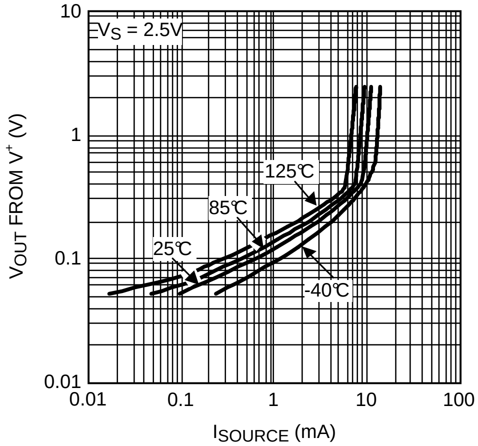


Figure 4.

Output Swing vs. Sinking Current

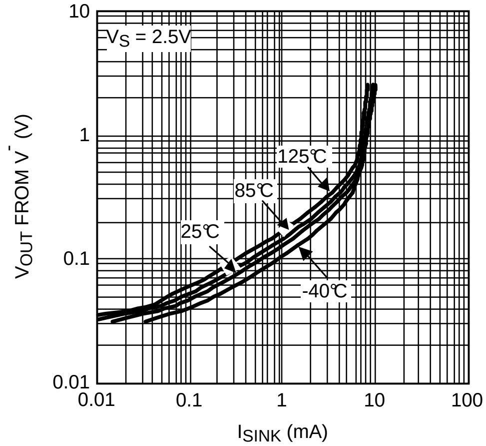


Figure 5.

Output Swing vs. Sourcing Current

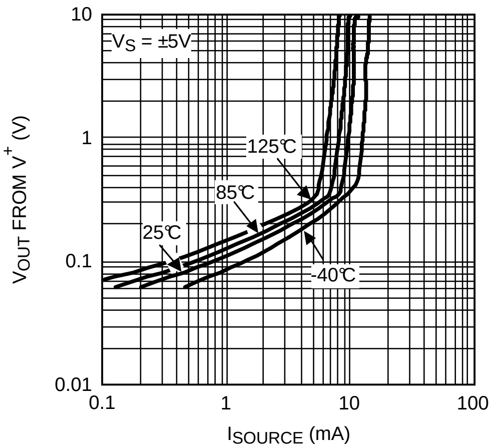


Figure 6.

Output Swing vs. Sinking Current

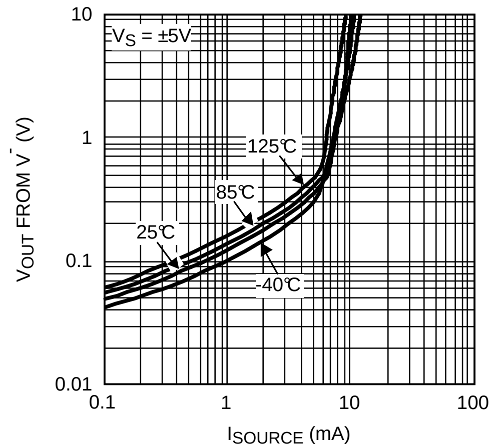


Figure 7.

Output Swing vs. Sourcing Current

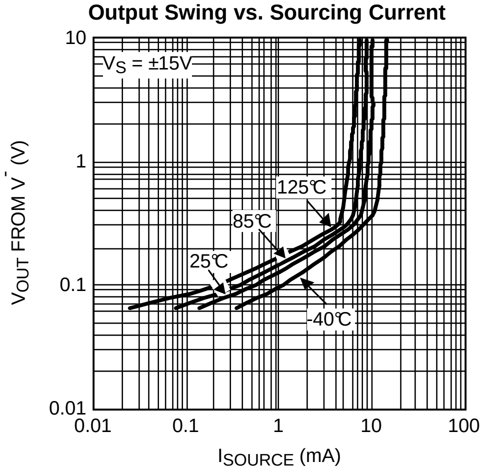


Figure 8.

Output Swing vs. Sinking Current

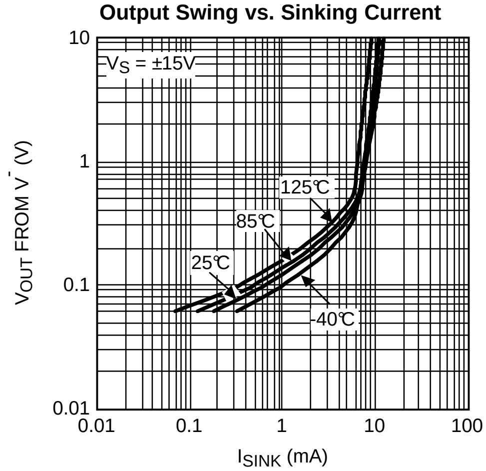


Figure 9.

Typical Performance Characteristics (continued)

V_{OS} Distribution

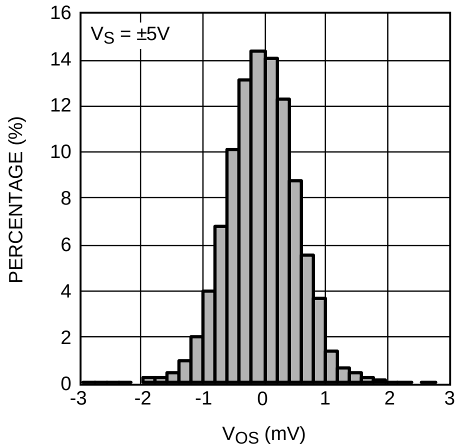


Figure 10.

V_{OS} vs. V_{CM} (Unit 1)

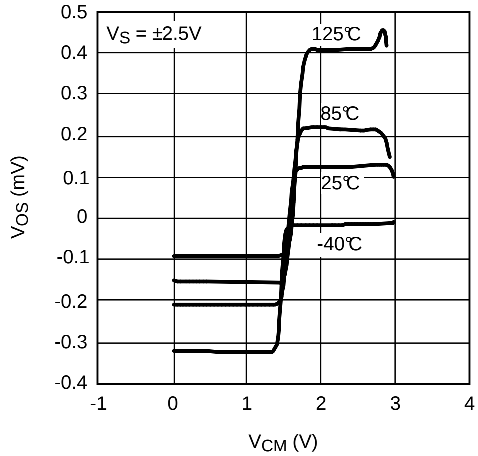


Figure 11.

V_{OS} vs. V_{CM} (Unit 2)

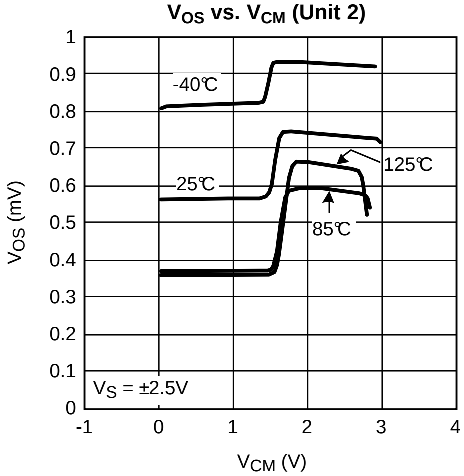


Figure 12.

V_{OS} vs. V_{CM} (Unit 3)

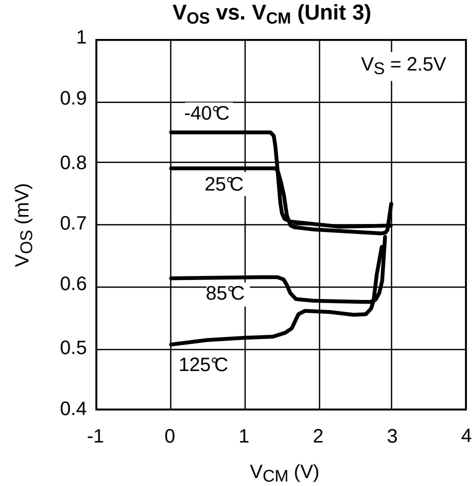


Figure 13.

V_{OS} vs. V_{CM} (Unit 1)

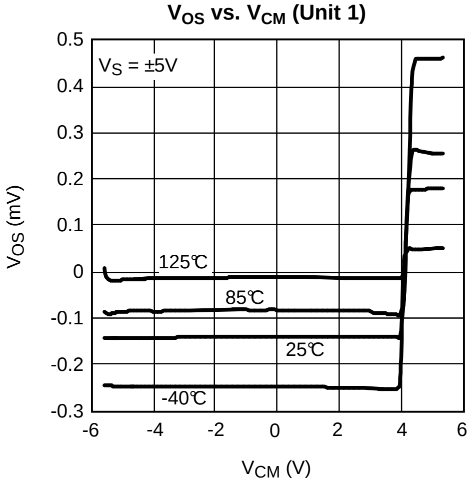


Figure 14.

V_{OS} vs. V_{CM} (Unit 2)

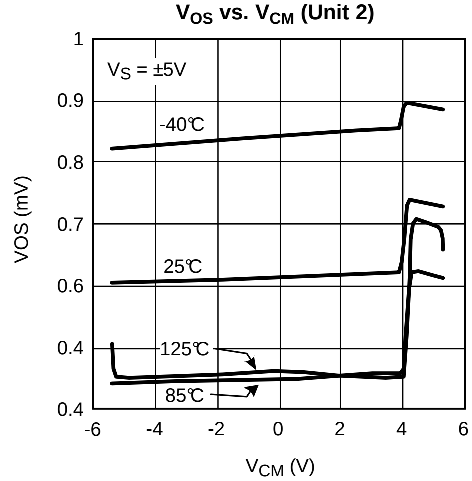


Figure 15.

Typical Performance Characteristics (continued)

V_{OS} vs. V_{CM} (Unit 3)

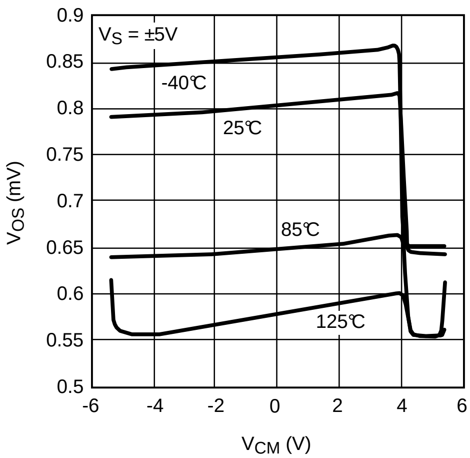


Figure 16.

V_{OS} vs. V_{CM} (Unit 1)

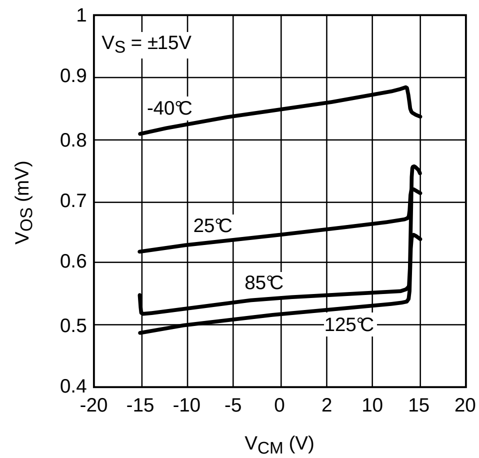


Figure 17.

V_{OS} vs. V_{CM} (Unit 2)

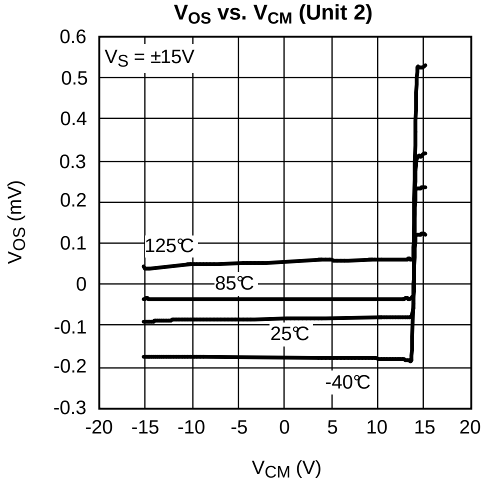


Figure 18.

V_{OS} vs. V_{CM} (Unit 3)

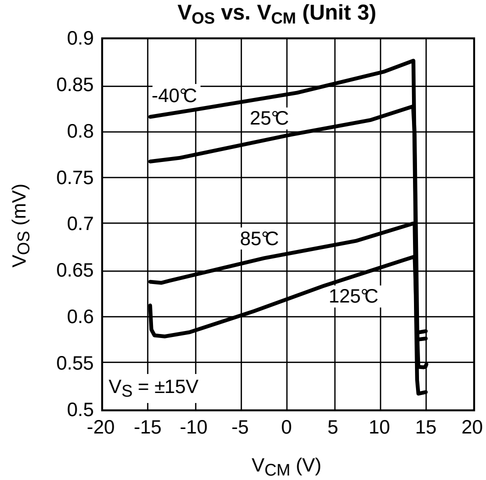


Figure 19.

V_{OS} vs. V_S (Unit 1)

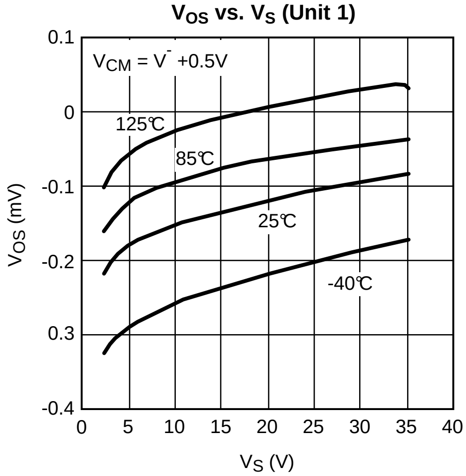


Figure 20.

V_{OS} vs. V_S (Unit 2)

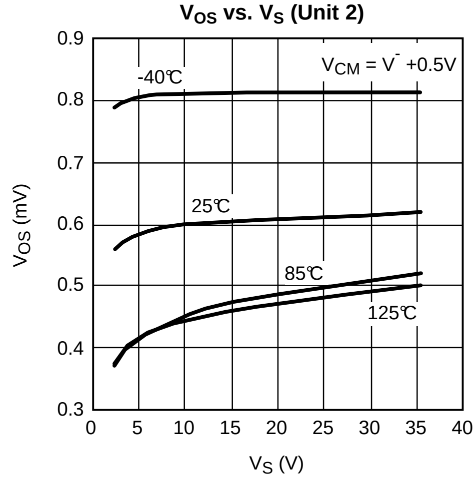


Figure 21.

Typical Performance Characteristics (continued)

V_{OS} vs. V_S (Unit 3)

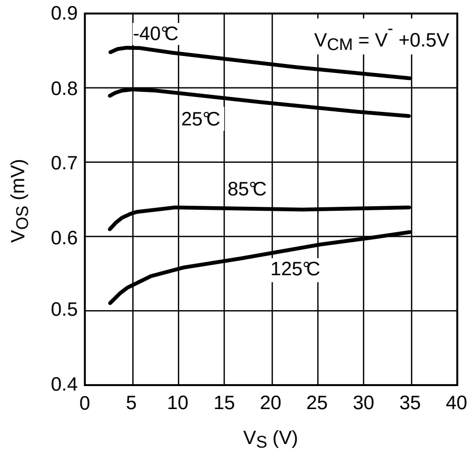


Figure 22.

V_{OS} vs. V_S (Unit 1)

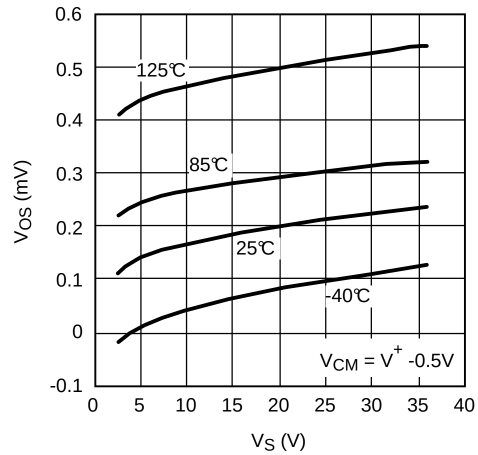


Figure 23.

V_{OS} vs. V_S (Unit 2)

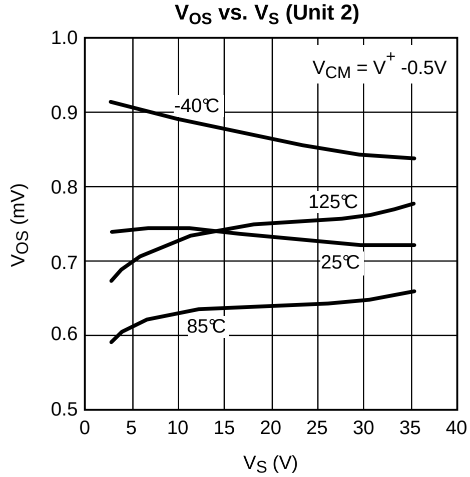


Figure 24.

V_{OS} vs. V_S (Unit 3)

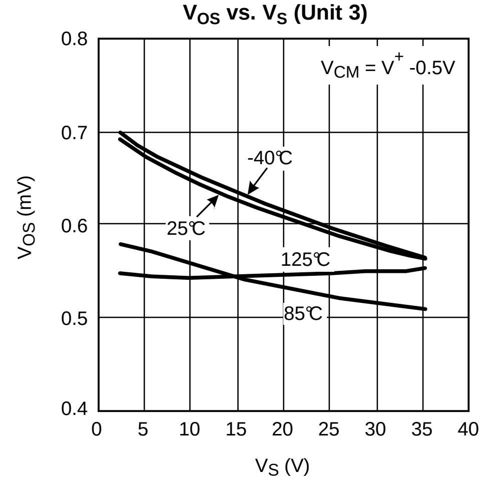


Figure 25.

I_{BIAS} vs. V_{CM}

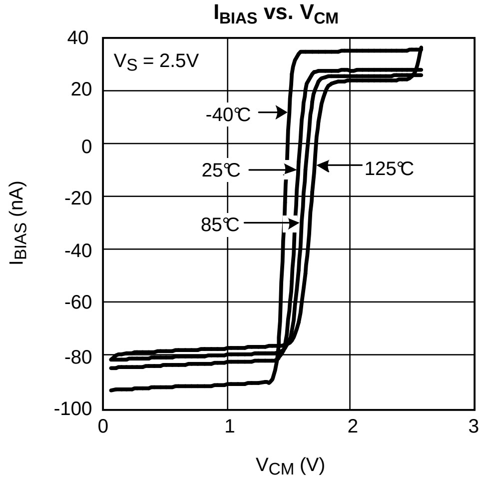


Figure 26.

I_{BIAS} vs. V_{CM}

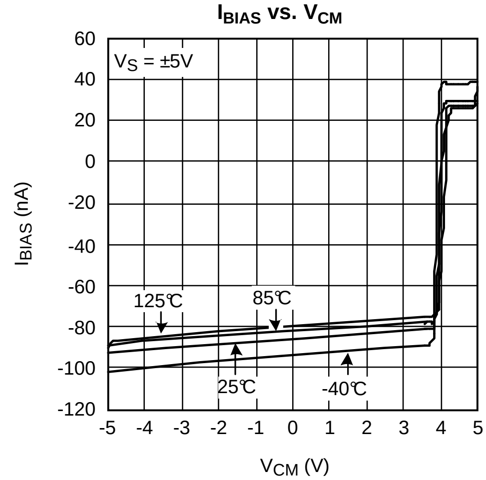


Figure 27.

Typical Performance Characteristics (continued)

I_{BIAS} vs. V_{CM}

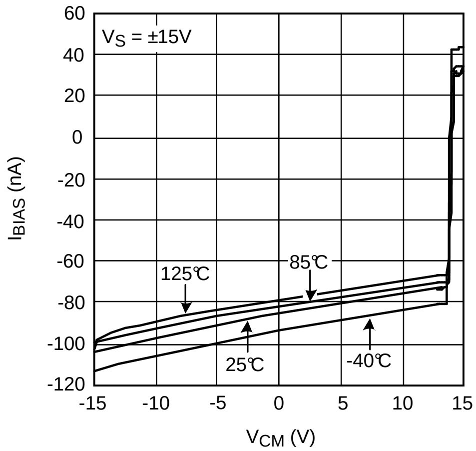


Figure 28.

I_{BIAS} vs. V_S

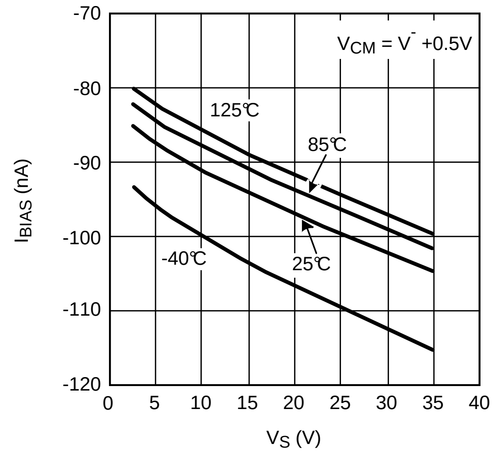


Figure 29.

I_{BIAS} vs. V_S

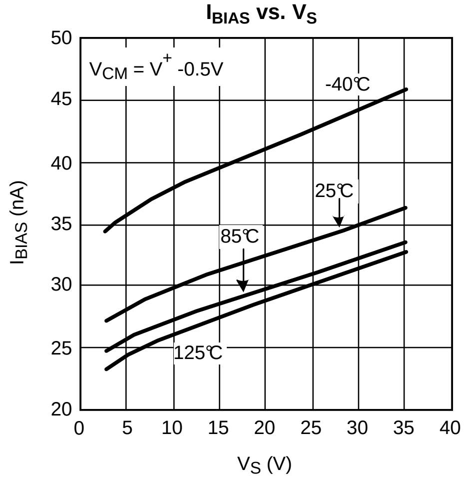


Figure 30.

I_S vs. V_{CM}

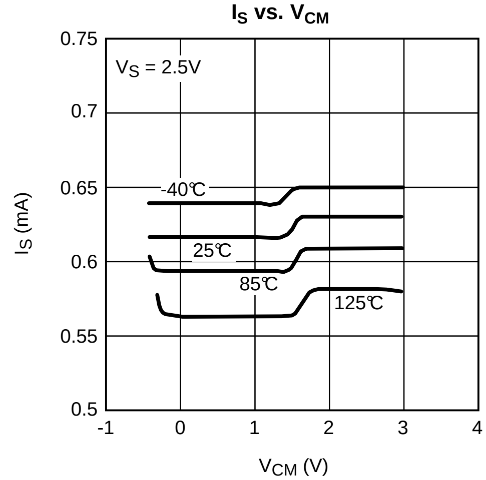


Figure 31.

I_S vs. V_{CM}

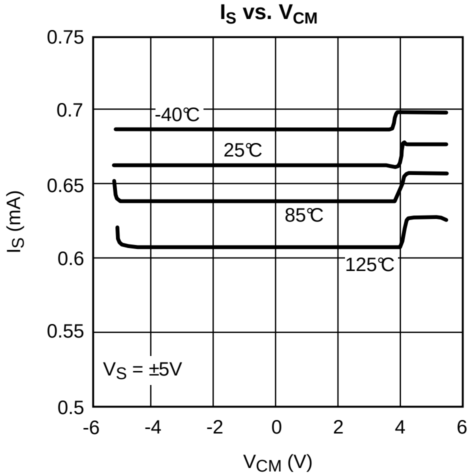


Figure 32.

I_S vs. V_{CM}

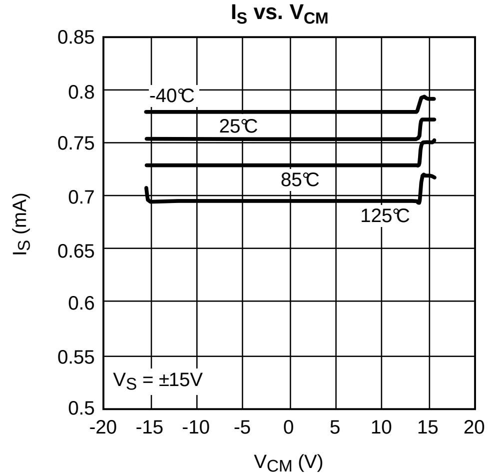


Figure 33.

Typical Performance Characteristics (continued)

I_S vs. V_{CM}

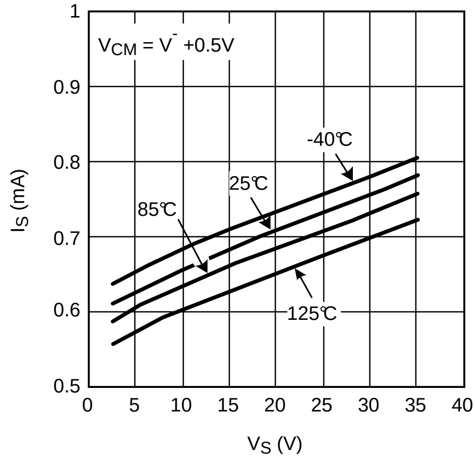


Figure 34.

I_S vs. V_{CM}

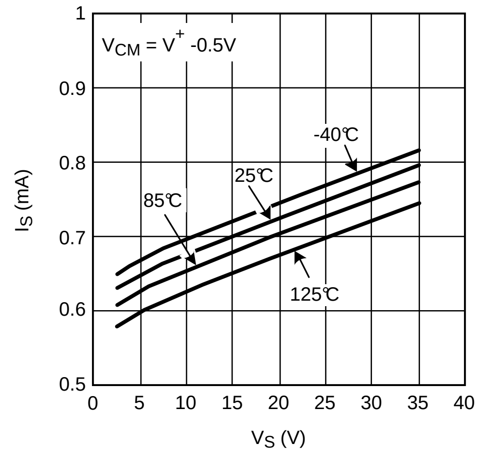


Figure 35.

Positive Output Swing vs. Supply Voltage

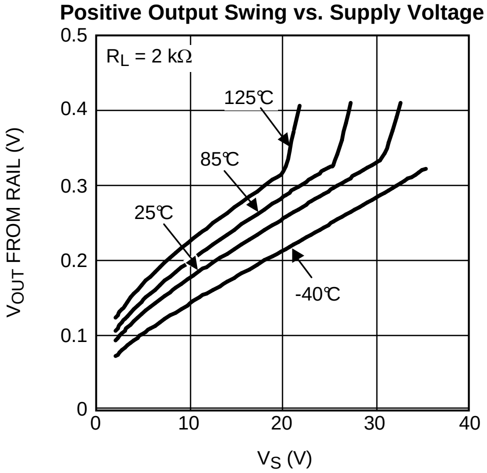


Figure 36.

Positive Output Swing vs. Supply Voltage

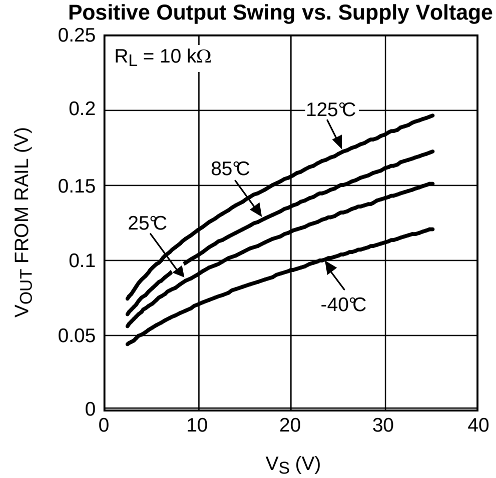


Figure 37.

Negative Output Swing vs. Supply Voltage

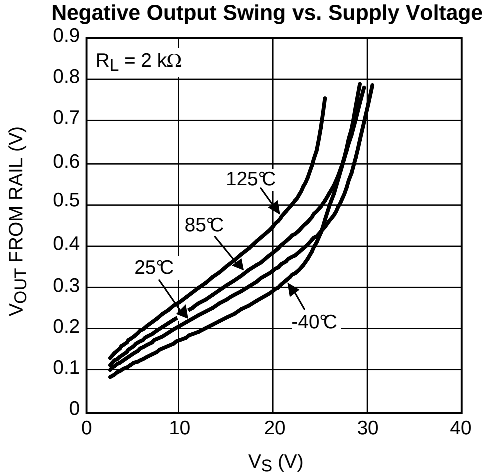


Figure 38.

Negative Output Swing vs. Supply Voltage

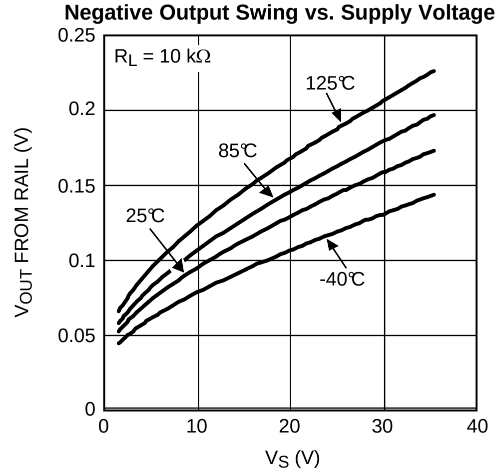


Figure 39.

Typical Performance Characteristics (continued)

Open Loop Frequency with Various Capacitive Load

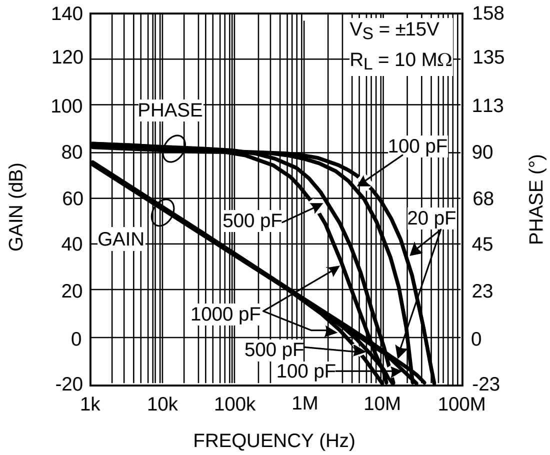


Figure 40.

Open Loop Frequency with Various Resistive Load

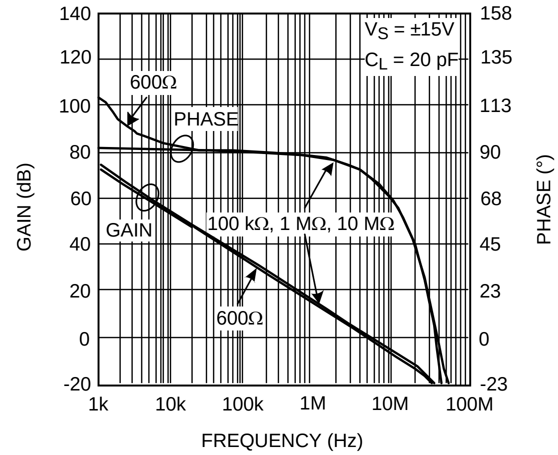


Figure 41.

Open Loop Frequency with Various Supply Voltage

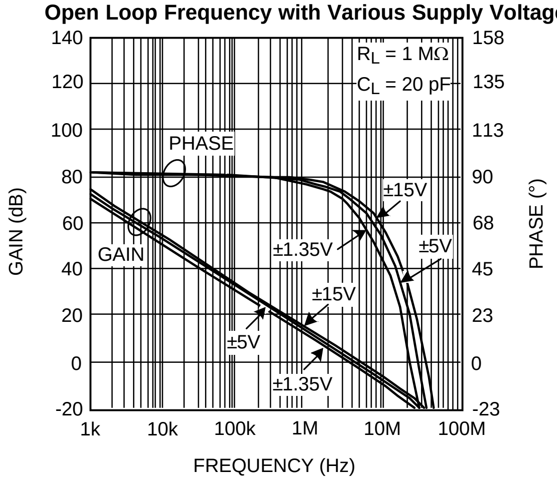


Figure 42.

Open Loop Frequency Response with Various Temperatures

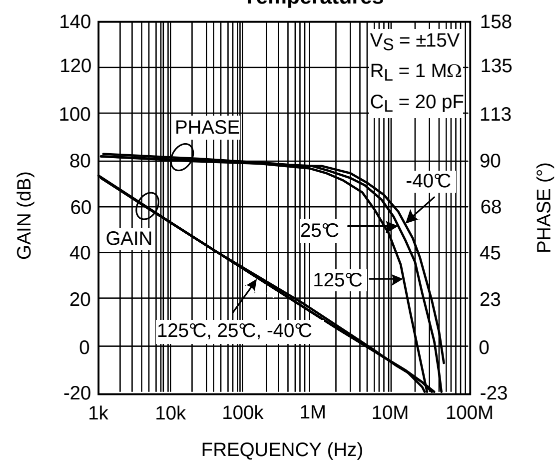


Figure 43.

CMRR vs. Frequency

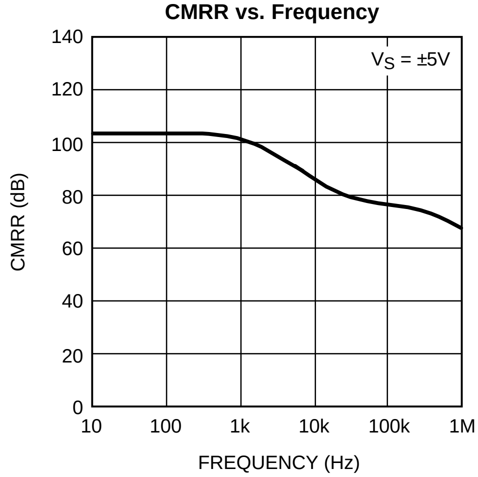


Figure 44.

+PSRR vs. Frequency

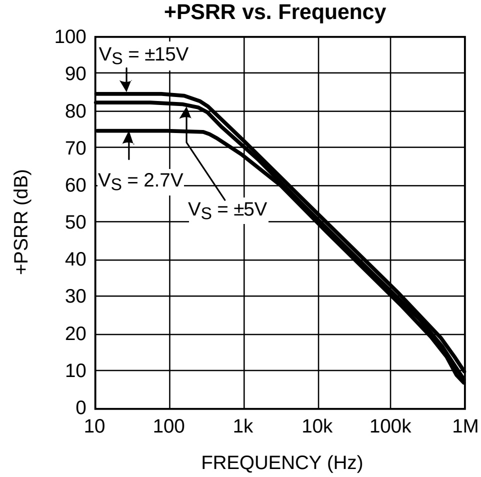


Figure 45.

Typical Performance Characteristics (continued)

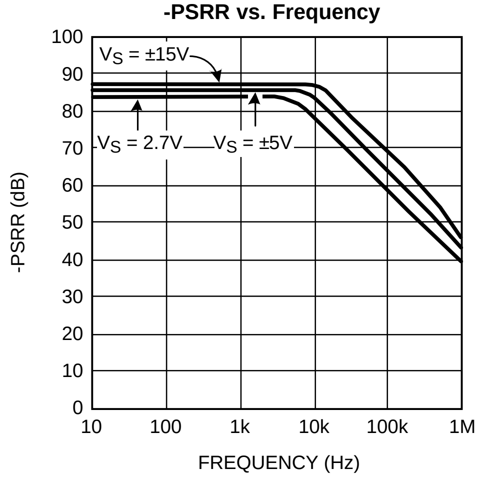


Figure 46.

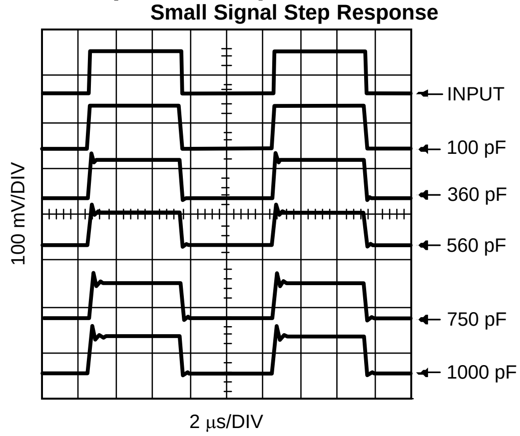


Figure 47.

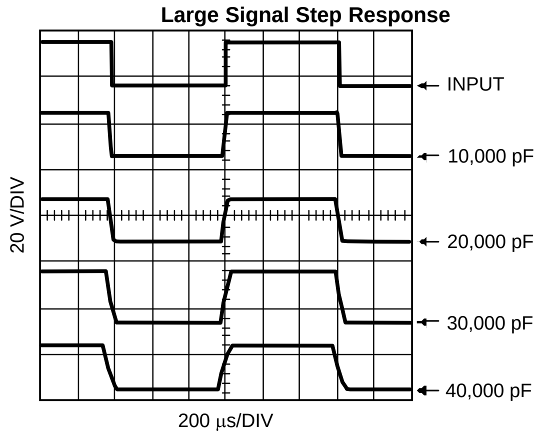


Figure 48.

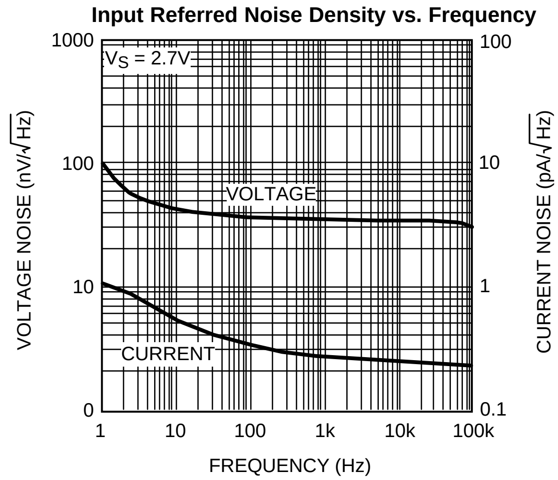


Figure 49.

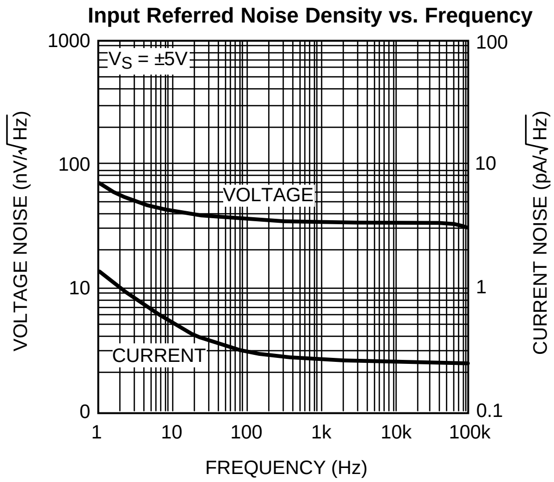


Figure 50.

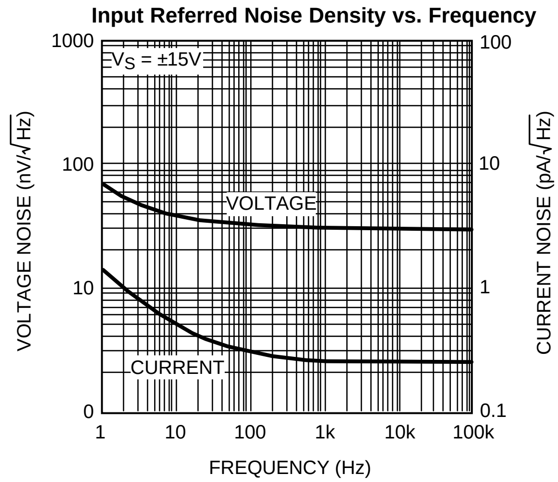


Figure 51.

Typical Performance Characteristics (continued)

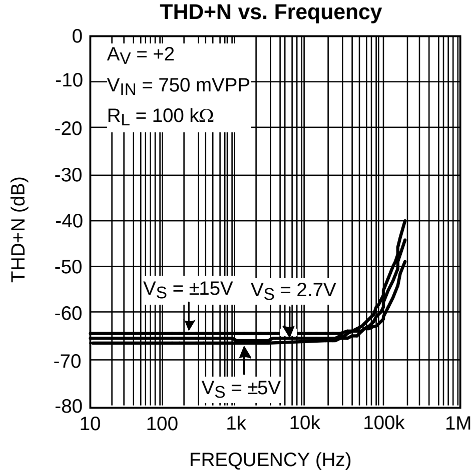


Figure 52.

APPLICATION INFORMATION

GENERAL INFORMATION

Low supply current and wide bandwidth, greater than rail-to-rail input range, full rail-to-rail output, good capacitive load driving ability, wide supply voltage and low distortion all make the LM7341 ideal for many diverse applications.

The high common-mode rejection ratio and full rail-to-rail input range provides precision performance when operated in non-inverting applications where the common-mode error is added directly to the other system errors.

CAPACITIVE LOAD DRIVING

The LM7341 has the ability to drive large capacitive loads. For example, 1000 pF only reduces the phase margin to about 30 degrees.

POWER DISSIPATION

Although the LM7341 has internal output current limiting, shorting the output to ground when operating on a +30V power supply will cause the op amp to dissipate about 350 mW. This is a worst-case example. In the 5-pin SOT-23 package, the higher thermal resistance will cause a calculated rise of 113°C. This can raise the junction temperature to above the absolute maximum temperature of 150°C.

Operating from split supplies greatly reduces the power dissipated when the output is shorted. Operating on ±15V supplies can only cause a temperature rise of 57°C in the 5-pin SOT-23 package, assuming the short is to ground.

WIDE SUPPLY RANGE

The high power-supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) provide precision performance when operated on battery or other unregulated supplies. This advantage is further enhanced by the very wide supply range (2.5V–32V) offered by the LM7341. In situations where highly variable or unregulated supplies are present, the excellent PSRR and wide supply range of the LM7341 benefit the system designer with continued precision performance, even in such adverse supply conditions.

SPECIFIC ADVANTAGES OF 5-Pin SOT-23 (TinyPak)

The obvious advantage of the 5-pin SOT-23, TinyPak, is that it can save board space, a critical aspect of any portable or miniaturized system design. The need to decrease overall system size is inherent in any handheld, portable, or lightweight system application.

Furthermore, the low profile can help in height limited designs, such as consumer hand-held remote controls, sub-notebook computers, and PCMCIA cards.

An additional advantage of the tiny package is that it allows better system performance due to ease of package placement. Because the tiny package is so small, it can fit on the board right where the op amp needs to be placed for optimal performance, unconstrained by the usual space limitations. This optimal placement of the tiny package allows for many system enhancements, not easily achieved with the constraints of a larger package. For example, problems such as system noise due to undesired pickup of digital signals can be easily reduced or mitigated. This pick-up problem is often caused by long wires in the board layout going to or from an op amp. By placing the tiny package closer to the signal source and allowing the LM7341 output to drive the long wire, the signal becomes less sensitive to such pick-up. An overall reduction of system noise results.

Often times system designers try to save space by using dual or quad op amps in their board layouts. This causes a complicated board layout due to the requirement of routing several signals to and from the same place on the board. Using the tiny op amp eliminates this problem.

Additional space savings parts are available in tiny packages from Texas Instruments, including low power amplifiers, precision voltage references, and voltage regulators.

LOW DISTORTION, HIGH OUTPUT DRIVE CAPABILITY

The LM7341 offers superior low-distortion performance, with a total-harmonic-distortion-plus-noise of −66 dB at f = 10 kHz. The advantage offered by the LM7341 is its low distortion levels, even at high output current and low load resistance.

Typical Applications

HANDHELD REMOTE CONTROLS

The LM7341 offers outstanding specifications for applications requiring good speed/power trade-off. In applications such as remote control operation, where high bandwidth and low power consumption are needed. The LM7341 performance can easily meet these requirements.

OPTICAL LINE ISOLATION FOR MODEMS

The combination of the low distortion and good load driving capabilities of the LM7341 make it an excellent choice for driving opto-coupler circuits to achieve line isolation for modems. This technique prevents telephone line noise from coupling onto the modem signal. Superior isolation is achieved by coupling the signal optically from the computer modem to the telephone lines; however, this also requires a low distortion at relatively high currents. Due to its low distortion at high output drive currents, the LM7341 fulfills this need, in this and in other telecom applications.

REMOTE MICROPHONE IN PERSONAL COMPUTERS

Remote microphones in Personal Computers often utilize a microphone at the top of the monitor which must drive a long cable in a high noise environment. One method often used to reduce the nose is to lower the signal impedance, which reduces the noise pickup. In this configuration, the amplifier usually requires 30 dB–40 dB of gain, at bandwidths higher than most low-power CMOS parts can achieve. The LM7341 offers the tiny package, higher bandwidths, and greater output drive capability than other rail-to-rail input/output parts can provide for this application.

LM7341 AS A COMPARATOR

The LM7341 can also be used as a comparator and provides quite reasonable performance. Note however that unlike a typical comparator an op amp has a maximum allowed differential voltage between the input pins. For the LM7341, as stated in the Absolute Maximum Ratings section, this maximum voltage is V_{IN} Differential = ±15V. Beyond this limit, even for a short time, damage to the device may occur.

As an inverting comparator at V_S = 30V and 1V of overdrive there is typically 12 µs of propagation delay. At V_S = 30V and 50 mV of overdrive there is typically 17 µs of propagation delay.

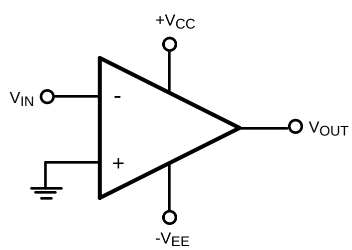


Figure 53. Inverting Comparator

Similarly a non-inverting comparator at V_S = 30V and 1V of overdrive there is typically 12 µs of propagation delay. At V_S = 30V and 50 mV of overdrive there is typically 17 µs of propagation delay.

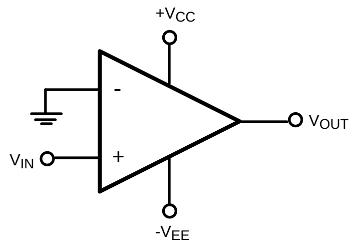


Figure 54. Non-Inverting Comparator

COMPARATOR WITH HYSTERESIS

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis or positive feedback.

INVERTING COMPARATOR WITH HYSTERESIS

The inverting comparator with hysteresis requires a three resistor network that is referenced to the supply voltage V_{CC} of the comparator, as shown in Figure 55. When V_{IN} at the inverting input is less than V_A, the voltage at the non-inverting node of the comparator ($V_{IN} < V_A$), the output voltage is high (for simplicity assume V_{OUT} switches as high as V_{CC}). The three network resistors can be represented as $R_1||R_3$ in series with R_2. The lower input trip voltage V_{A1} is defined as

$$V_{A1} = V_{CC}R_2 / ((R_1||R_3) + R_2) \quad (1)$$

When V_{IN} is greater than V_A ($V_{IN} > V_A$), the output voltage is low, very close to ground. In this case the three network resistors can be presented as $R_2||R_3$ in series with R_1. The upper trip voltage V_{A2} is defined as

$$V_{A2} = V_{CC}\ (R_2||R_3) / ((R_1 + (R_2||R_3)) \quad (2)$$

The total hysteresis provided by the network is defined as

$$\text{Delta } V_A = V_{A1} - V_{A2} \quad (3)$$

For example to achieve 50 mV of hysteresis when V_{CC} = 30V set R_1 = 4.02 kΩ, R_2 = 4.02 kΩ, and R_3 = 1.21 MΩ. With these resistors selected the error due to input bias current is approximately 1 mV. To minimize this error it is best to use low resistor values on the inputs.

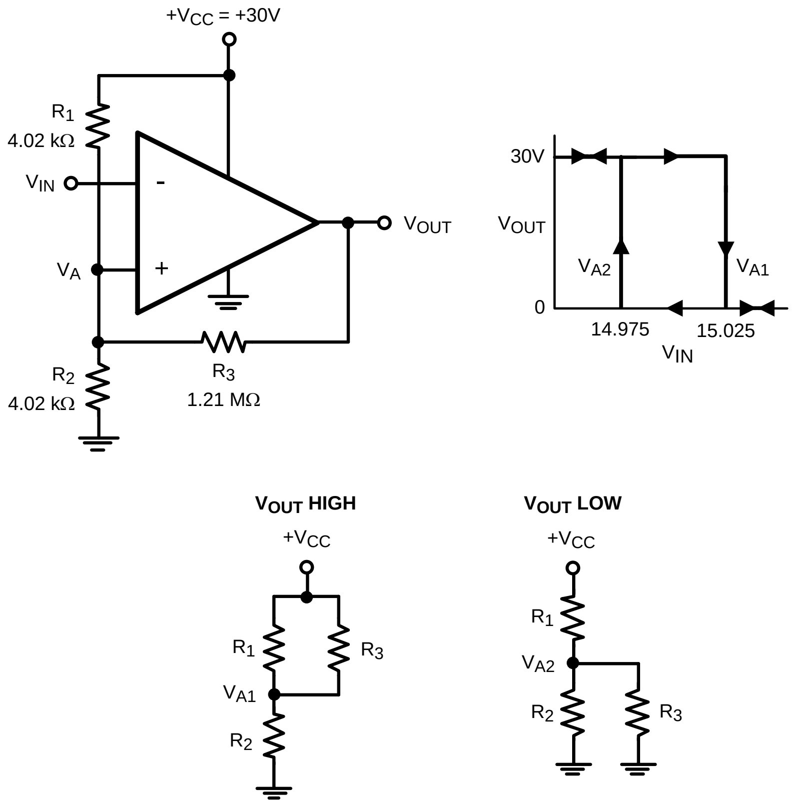


Figure 55. Inverting Comparator with Hysteresis

NON-INVERTING COMPARATOR WITH HYSTERESIS

A non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1} where V_{IN1} is calculated by

$$V_{IN1} = R_1*(V_{REF}/R_2) + V_{REF} \quad (4)$$

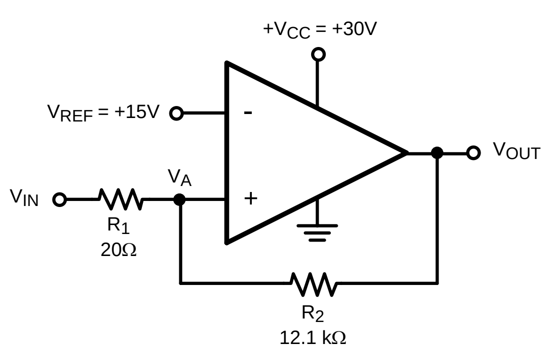
When V_{IN} is high, the output is also high, to make the comparator switch back to it's low state, V_{IN} must equal V_{REF} before V_A will again equal V_{REF} . V_{IN} can be calculated by

$$V_{IN2} = (V_{REF}\,(R_1+ R_2) - V_{CC}R_1)/R_2 \quad (5)$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}.

$$\text{Delta } V_{IN} = V_{CC}R_1/R_2 \quad (6)$$

For example to achieve 50 mV of hysteresis when V_{CC} = 30V set R_1 = 20Ω and R_2 = 12.1 kΩ.



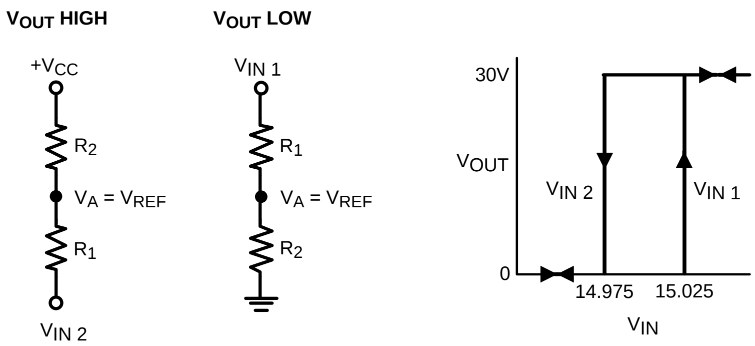


Figure 56. Non-Inverting Comparator with Hysteresis

OTHER SOT-23 AMPLIFIERS

The **LM7321** is a rail-to-rail input and output amplifier that can tolerate unlimited capacitive load. It works from 2.7V to ±15V and across the −40°C to 125°C temperature range. It has 20 MHz gain-bandwidth, and is available in both 5-Pin SOT-23 and 8-Pin SOIC packages.

The **LM6211** is a 20 MHz part with CMOS input, which runs on 5V to 24V single supplies. It has rail-to-rail output and low noise.

The **LMP7701** is a rail-to-rail input and output precision part with an input voltage offset under 220 microvolts and low noise. It has 2.5 MHz bandwidth and works on 2.7V to 12V supplies.

SMALLER SC70 AMPLIFIERS

The **LMV641** is a 10 MHz amplifier which uses only 140 micro amps of supply current. The input voltage offset is less than 0.5 mV.

The **LMV851** is an 8 MHz amplifier which uses only 0.4 mA supply current, and is available in the smaller SC70 package. The LMV851 also resists Electro Magnetic Interference (EMI) from mobile phones and similar high frequency sources. It works on 2.7V to 5.5 V supplies.

Detailed information on these and a wide range of other parts can be found at www.ti.com.

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM7341MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV4A	Samples
LM7341MFE/NOPB	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV4A	Samples
LM7341MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AV4A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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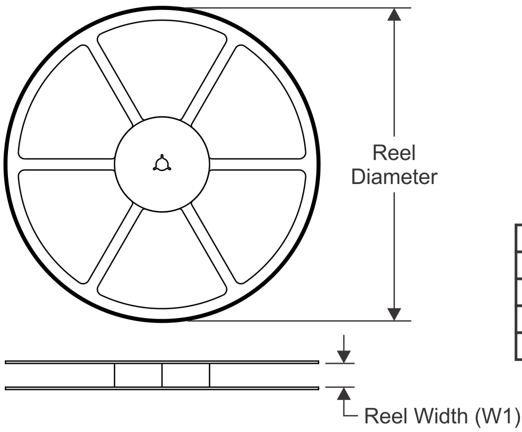
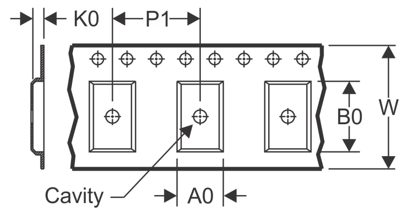
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

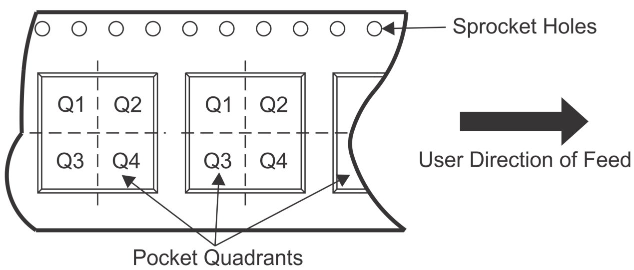


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

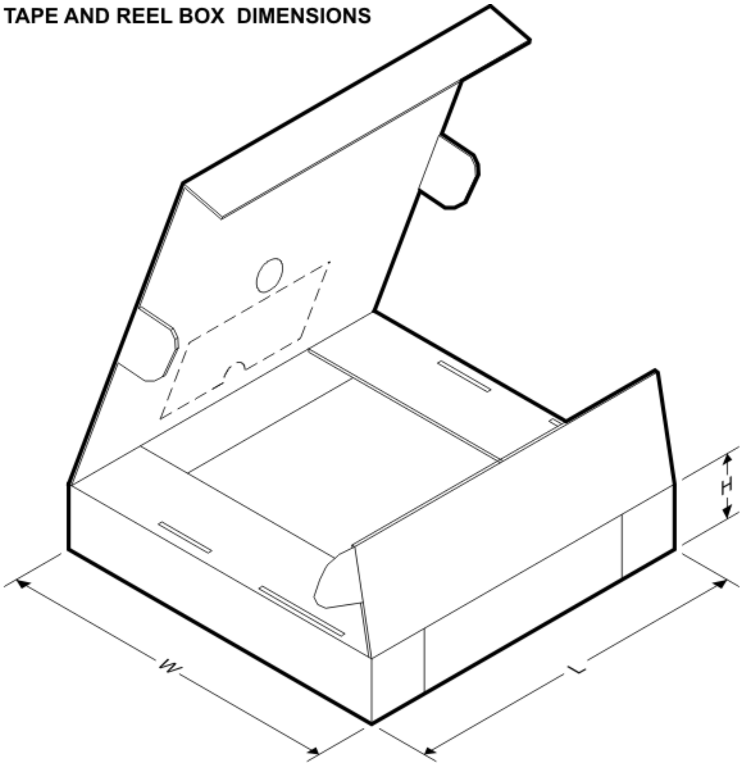
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM7341MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7341MFE/NOPB	SOT-23	DBV	5	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM7341MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



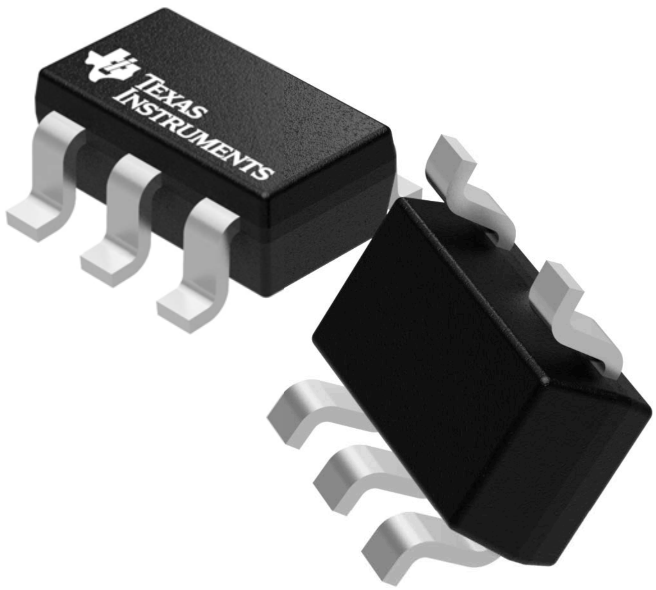
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM7341MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM7341MFE/NOPB	SOT-23	DBV	5	250	210.0	185.0	35.0
LM7341MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DBV 5 — SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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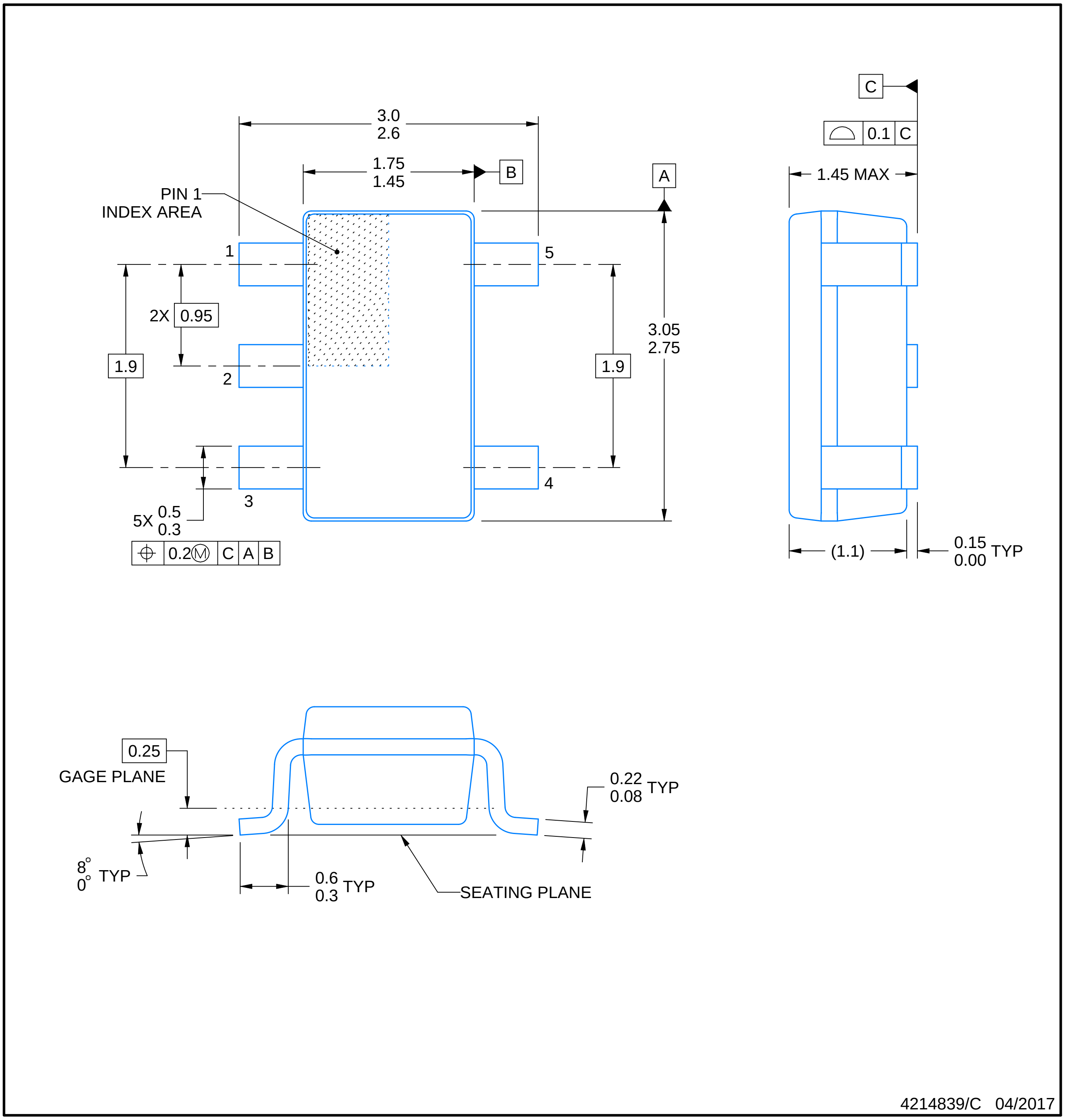

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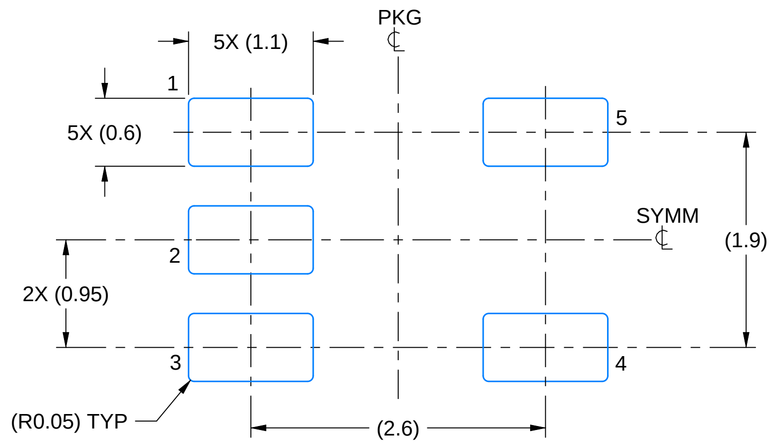
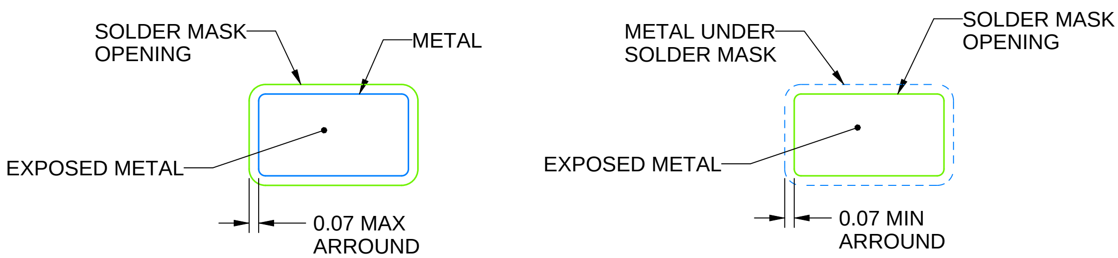
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

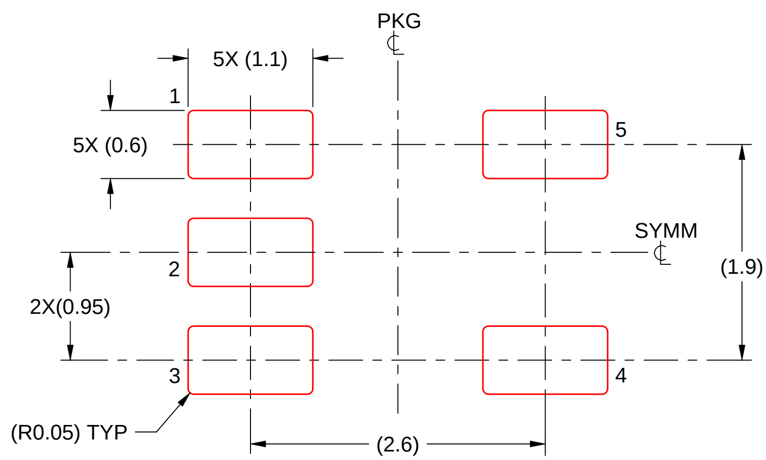
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

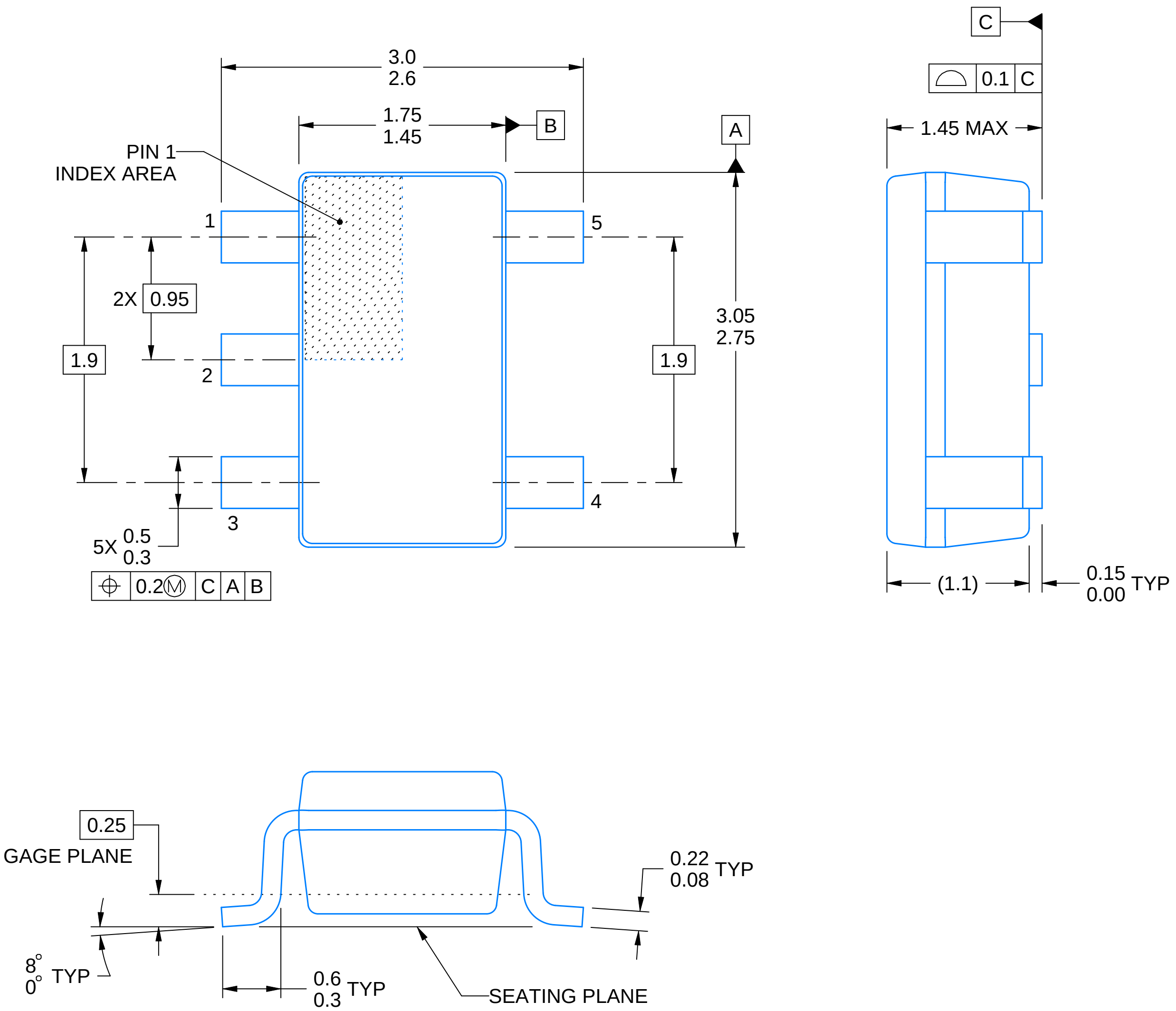


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



4214839/C 04/2017

NOTES:

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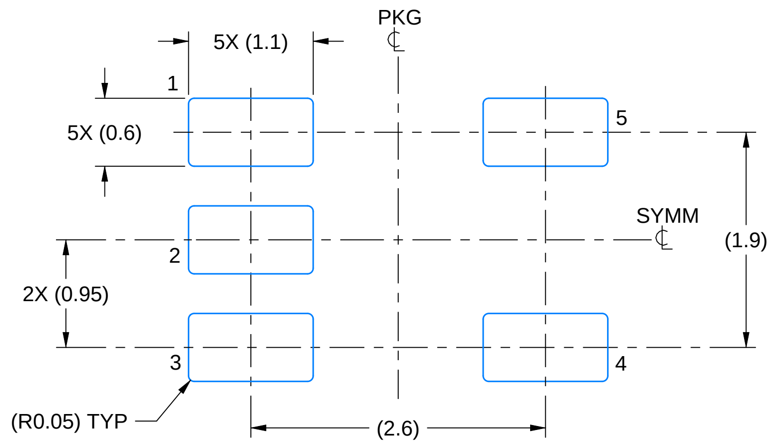
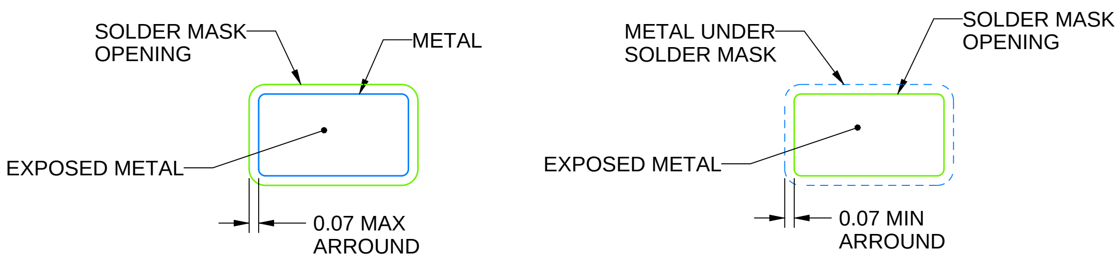


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

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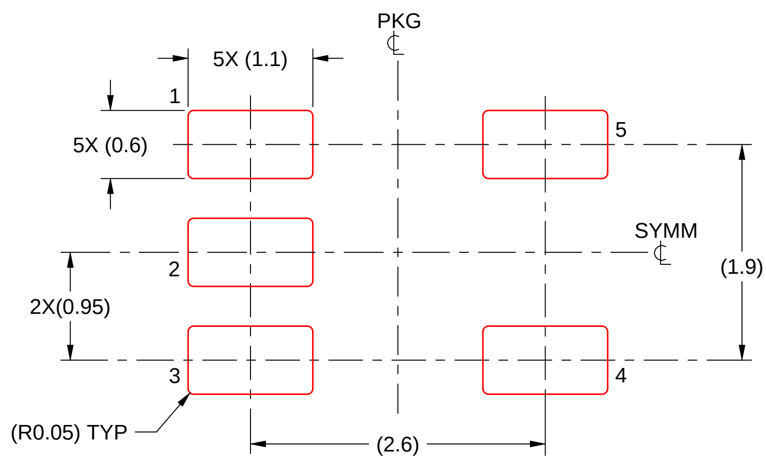
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

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