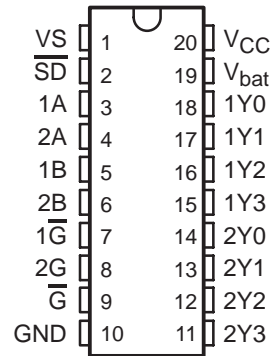# SN74BCT2414
MEMORY DECODER
WITH ON-CHIP SUPPLY VOLTAGE MONITOR

SCBS059B – MARCH 1989 – REVISED NOVEMBER 1993

- **BiCMOS Design Substantially Reduces Standby Current**
- **Two Independent 2-Line to 4-Line Decoders or One 3-Line to 8-Line Decoder**
- **Separate Enable Inputs for Easy Cascading**
- **Two Supply Voltage Terminals (V_{CC} and V_{bat})**
- **Built-In Supply-Voltage Monitor for V_{CC}**
- **Automatic Cut Off of Outputs During V_{CC} Fail**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)

VS	1		20	V_{CC}
$\overline{SD}$	2		19	V_{bat}
1A	3		18	1Y0
2A	4		17	1Y1
1B	5		16	1Y2
2B	6		15	1Y3
$1\overline{G}$	7		14	2Y0
2G	8		13	2Y1
$\overline{G}$	9		12	2Y2
GND	10		11	2Y3

description

The SN74BCT2414 is a decoder specially designed to be used in memory systems with battery backup during power failure. The two independent 2-line to 4-line decoders with separate and common control inputs may be externally cascaded to implement a 3-line to 8-line decoder.
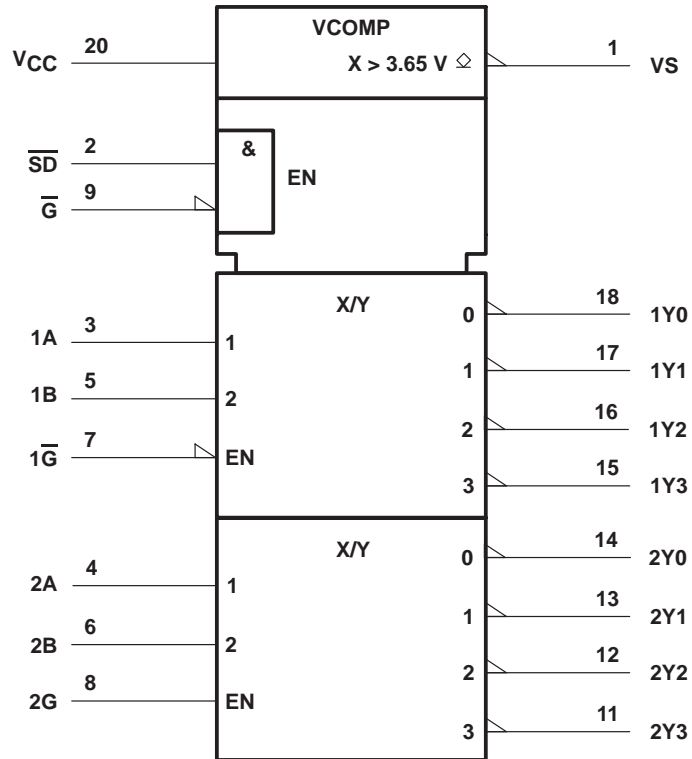
The circuit has two supply voltage inputs: the voltage monitor (bandgap) is powered via the V_{CC} terminal; the internal logic of the circuit is powered via the V_{bat} terminal. In case V_{CC} drops below 3.65 V (nominal), the voltage monitor forces the voltage-control (VS) and decoder outputs (Y) to the high level. VS may be used to disconnect the supply voltage of the memories (V_{bat}) from the system supply. This output is switched off when the on-chip supply voltage monitor detects a power failure.

The SN74BCT2414 is characterized for operation from 0°C to 70°C.

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POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

SN74BCT2414
MEMORY DECODER
WITH ON-CHIP SUPPLY VOLTAGE MONITOR

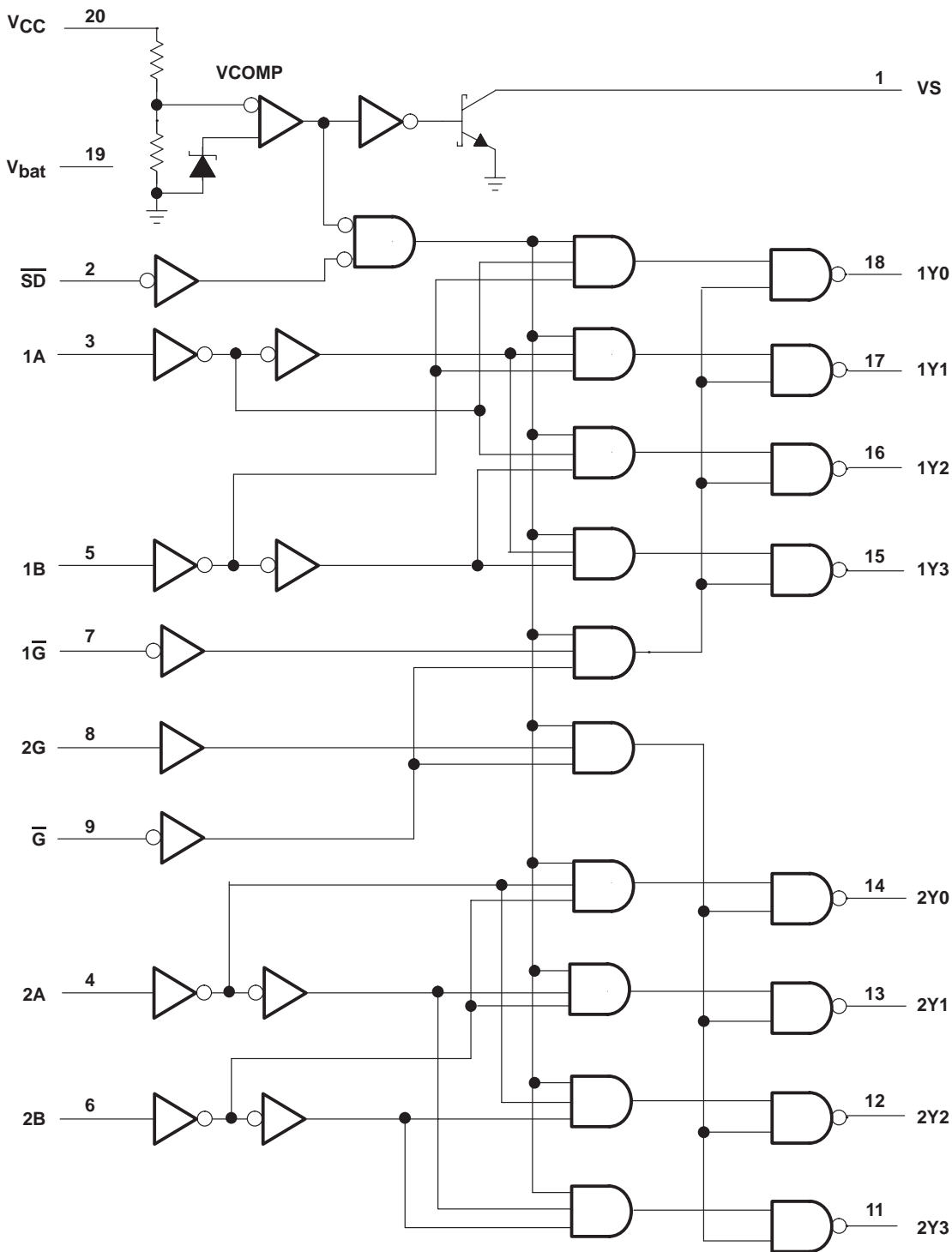SCBS059B – MARCH 1989 – REVISED NOVEMBER 1993

logic symbol†

	VCOMP	
V_{CC} 20	X > 3.65 V ◇	1 VS
$\overline{SD}$ 2	& EN	
$\overline{G}$ 9		
	X/Y	
1A 3	1	0 18 1Y0
1B 5	2	1 17 1Y1
$1\overline{G}$ 7	EN	2 16 1Y2
		3 15 1Y3
	X/Y	
2A 4	1	0 14 2Y0
2B 6	2	1 13 2Y1
2G 8	EN	2 12 2Y2
		3 11 2Y3

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS
INSTRUMENTS

logic diagram (positive logic)

FUNCTION TABLES

INPUTS					OUTPUTS			
CONTROL			SELECT					
$\overline{G}$	1$\overline{G}$	$\overline{SD}$	1B	1A	1Y0	1Y1	1Y2	1Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	L	H	L	L	L	H	H	H
L	L	H	L	H	H	L	H	H
L	L	H	H	L	H	H	L	H
L	L	H	H	H	H	H	H	L

INPUTS					OUTPUTS			
CONTROL			SELECT					
$\overline{G}$	2G	$\overline{SD}$	2B	2A	2Y0	2Y1	2Y2	2Y3
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	H	H	L	L	L	H	H	H
L	H	H	L	H	H	L	H	H
L	H	H	H	L	H	H	L	H
L	H	H	H	H	H	H	H	L

NOTE: For a 3-line to 8-line decoder, the following pins must be shorted: 1$\overline{G}$ to 2G, 1A to 2A and 1B to 2B.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{bat} .... −0.5 V to 7 V
Supply voltage range, V_{CC} .... −0.5 V to 7 V
Supply voltage V_{CC} with respect to V_{bat} .... −1.5 V
Input voltage range, V_I .... −0.5 V to V_{CC} + 0.5 V
Off-state output voltage range at VS .... −0.5 V to 7 V
Voltage range applied to any Y output in the power-off state .... −0.5 V to 7 V
Voltage applied to any Y output in the power-off state with respect to V_{bat} .... 0.5 V
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

TEXAS INSTRUMENTS

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	V
V_{bat}	Supply voltage			4.5	5	5.5	V
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_{IK}	Input clamp current					−18	mA
I_{OH}	High-level output current					−400	µA
I_{OL}	Low-level output current	Y outputs				8	mA
		VS outputs				20	
t_t	Input transition time			0		10	ns/V
T_A	Operating free-air temperature			0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{bat} = V_{CC} = 4.5 V	I_{OH} = − 20 µA	4.4			V
			I_{OH} = − 400 µA	3.5			
		V_{bat} = 2 V, V_{CC} = 0,	I_{OH} = − 50 µA	1.8			
V_{OL}	All except VS	V_{bat} = V_{CC} = 4.5 V	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.5	
	VS	V_{bat} = V_{CC} = 4.5 V,	I_{OL} = 20 mA			1	
V_T[‡]					3.65		V
I_I		V_{bat} = V_{CC} = 5.5 V,	V_I = 5.5 V			100	µA
I_{IH}		V_{bat} = V_{CC} = 5.5 V,	V_I = 2.7 V			±20	µA
I_{IL}		V_{bat} = V_{CC} = 5.5 V,	V_I = 0.5 V			±20	µA
I_{OH}	VS	V_{bat} = 4.5 V,	V_{CC} = 0			1	µA
I_O[§]		V_{bat} = V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−200	mA
I_{CC}		V_{bat} = V_{CC} = 5.5 V	Outputs high			3	mA
			Outputs low			3	
I_{bat}		V_{bat} = 2.5 V,	V_{CC} = 0		1	10	µA
		V_{bat} = V_{CC} = 5.5 V	Outputs high			20	
			Outputs low			3	mA
C_i		V_{bat} = V_{CC} = 5 V,	V_I = 0 or 3 V		4		pF
C_o	Any Y	V_{bat} = V_{CC} = 0			6.5		pF
	VS				5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This value represents the V_{CC} monitor threshold voltage. Typical range is from 3.5 V to 3.8 V.
§ This output condition has been chosen to produce a current that closely approximates one half of the short-circuit output current, I_{OS}. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A or B	Any Y	1	5	10	1	12	ns
t_{PHL}			2	5.8	10	2	12	
t_{PLH}	Any $\overline{G}$	Any Y	1	4.5	9	1	10	ns
t_{PHL}			2	5.5	9	2	11	
t_{PLH}	$\overline{SD}$	Any Y	2	6.5	11	2	12	ns
t_{PHL}			2	6.5	11	2	12	

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	V_{CC}	Any Y	10	25	50	10	250	ns
t_{PHL}			15	45	100	15	250	
t_{PLH}	V_{CC}	VS	10	28	50	10	250	ns
t_{PHL}			20	50	100	20	250	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 1:   Load circuits and voltage waveforms are shown in Section 1.

APPLICATION INFORMATION

A typical application circuit for a battery-buffered memory in a microcomputer system is shown in Figure 1 which uses the SN74BCT2414. When power fails, the supply-voltage supervisor (TL7705) resets the microcomputer and disables the memory by switching the shutdown input $\overline{\text{SD}}$ of the memory decoder to a logic zero. All memory decoder outputs are forced to a logic one. Abnormal write commands from the microprocessor, which may be issued during further voltage breakdown, no longer affect the contents of the memory. When the system supply voltage becomes lower than approximately 3.65 V, the voltage monitor inside the SN74BCT2414 memory decoder disconnects the input buffers of this circuit from the decoding logic internally and keeps all outputs at a logic one. The VS output is also switched off, disconnecting the system supply voltage from the memory circuits. During this low-voltage condition, the memory decoder and the memory circuits are supplied by the battery.
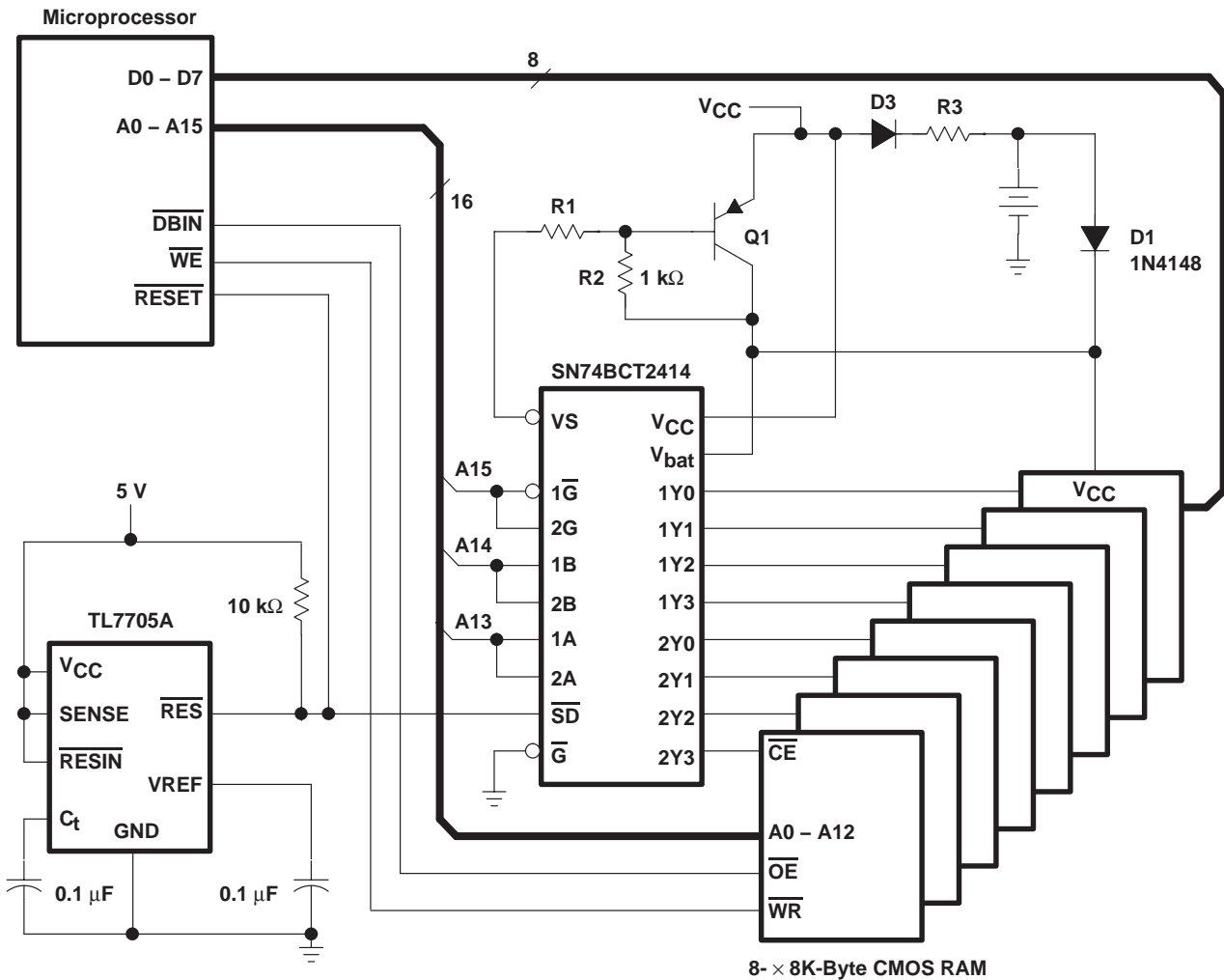
For further information on this device, please contact factory.

Figure 1. Memory System With Battery Backup

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74BCT2414DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2414	Samples
SN74BCT2414DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT2414	Samples
SN74BCT2414N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74BCT2414N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R−PDIP−T)**   **PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
  B. This drawing is subject to change without notice.
  C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
  D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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C

SEATING PLANE

◯ 0.1 C

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

18X 1.27

20

1

13.0
12.6
NOTE 3

2X
11.43

10

11

20X 0.51 / 0.31

B

7.6
7.4
NOTE 4

⊕ 0.25Ⓜ C A B

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25
GAGE PLANE

0.3 / 0.1

0° - 8°

1.27 / 0.40

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM ₵

1

20X (0.6)

18X (1.27)

SYMM ₵

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.