Ordering number : ENA0600

SANYO Semiconductors
DATA SHEET

LA6579H — Monolithic Linear IC For CD-R Four-Channel Bridge (BTL) Driver

Overview

The LA6579H is a 4-channel bridge (BTL) driver for CD-R.

Functions

- Bridge-connected (BTL) power amplifier incorporating four channels
- I_O max 1A
- Level shift circuit incorporated
- MUTE circuit (all circuits ON/OFF)
- High output voltage (dynamic range) (6.5V : TYP, CH1 only)
- Input OP-AMP incorporated (CH1 only)
- Input OP-AMP (CH1) selector function incorporated

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	*1	14	V
	V_{CC}_P*	V_{CC}P1, V_{CC}P2 *1	14	V
Allowable power dissipation	Pd max	Independent IC	0.8	W
		Specified board	1.8	W
Maximum input voltage	V_{IN}B		13	V
Maximum output current	I_O max	Each output	1	A
MUTE pin voltage	VMUTE		13	V
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board size : 114.3×76.1×1.6mm³, glass epoxy.

*1 Note : Connect power pins of V_{CC}_S, V_{CC}_P1 and V_{CC}_P2 externally.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5 to 13	V

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Electrical Characteristics at Ta = 25°C, V_{CC}_S = V_{CC}_P1 = V_{CC}_P2 = 8V, VREF = 1.65V, MUTE = 3.3V unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
ALL Blocks						
No-load current drain ON 1	I_{CC}-ON	All outputs ON, MUTE:HI		30	45	mA
No-load current drain ON 2	I_{CC}-OFF	All channels ON, MUTE:LOW		5	10	mA
MUTE ON voltage	VMUTE-ON	MUTE *1	2			V
MUTE OFF voltage	VMUTE-OFF	MUTE *1			0.5	V
Output AMP Block (BTL-AMP) (CH1)						
Input AMP offset voltage	V_{OFF}_OP-AMP	CH1, input OP-AMP_A and B	-50		50	mV
Output voltage	V_O1	R_L=8Ω *2	6.2	6.5		V
Input and output gain	VG1	*3	5.4	6	6.6	Times
Slew rate	SR1	AMP Independent Multiply 2 between outputs. *3		0.5		V/µs
Input OP_AMP						
Output offset voltage	V_{OFF}1	Input OP-AMP_A and B	-10		10	mV
OP-AMP_SINK	OP_SINK	Input OP-AMP, SINK current	2			mA
OP-AMP_SOURCE	OP_SOURCE	Input OP-AMP, SOUECE current	300	500		µA
[Input OP_AMP changeover]						
Input AMP changeover voltage 1	V_{IN}1-SW	Select CH1, input OP-AMP_B *5	1		0.5	V
Input AMP changeover voltage 2	V_{IN}1-SW	Select CH1, input OP-AMP_B *5	2			V
Output AMP (CH2 to 4)						
Output offset voltage	V_{OFF}2	Between + and – outputs of each CH	-50		50	mV
Output voltage	V_O2	Between each plus and minus outputs *2	5	5.4		V
Input and output gain	VG2	*3	5.4	6	6.6	Times
Slew rate	SR2	AMP Independent Multiply 2 between outputs. *3		0.5		V/µs
3.3V power supply						
3.3 VREG output voltage	3.3VREG	I_O = 200mA	3.18	3.3	3.42	V
REG-IN SINK current	REG-IN-SINK	Base current of external PNP transistor	5	10		mA
Line regulation	ΔV_OLN	6V ≤ V_{CC} ≤ 12V, I_O = 200mA		20	150	mV
Load regulation	ΔV_OLD	5mA ≤ I_O ≤ 200mA		50	200	mV

Note *1 : MUTE output ON with HI and OFF with LOW (AMP output OFF with HI impedance). Operative for all channels.

*2 : Voltage at both ends of an 8Ω load inserted between outputs. H or L for input. Output in the saturation condition.

*3 : CH1 input OP_AMP at 0dB (BUFFER)

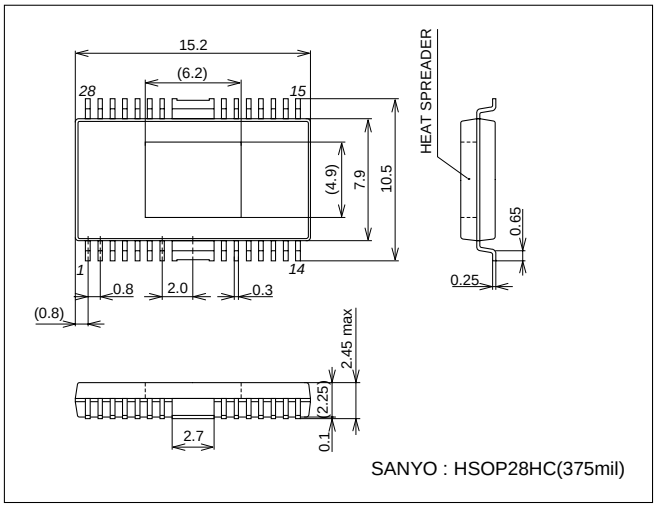
*4 : Design guarantee value

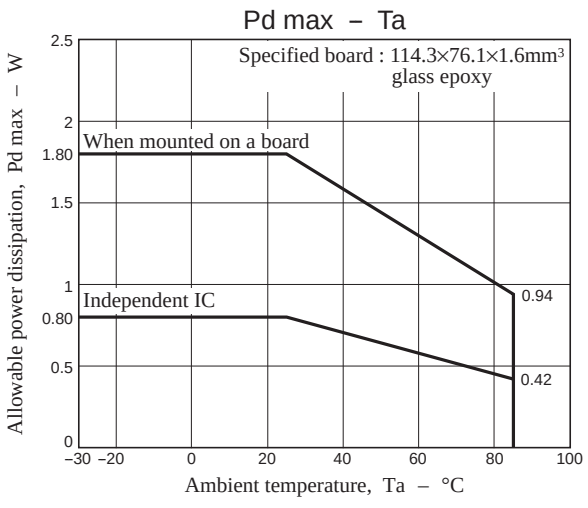
*5 : OP-AMP_A is operated when V_{IN}_SW is H. OP-AMP_B is operated when it is L.

Package Dimensions

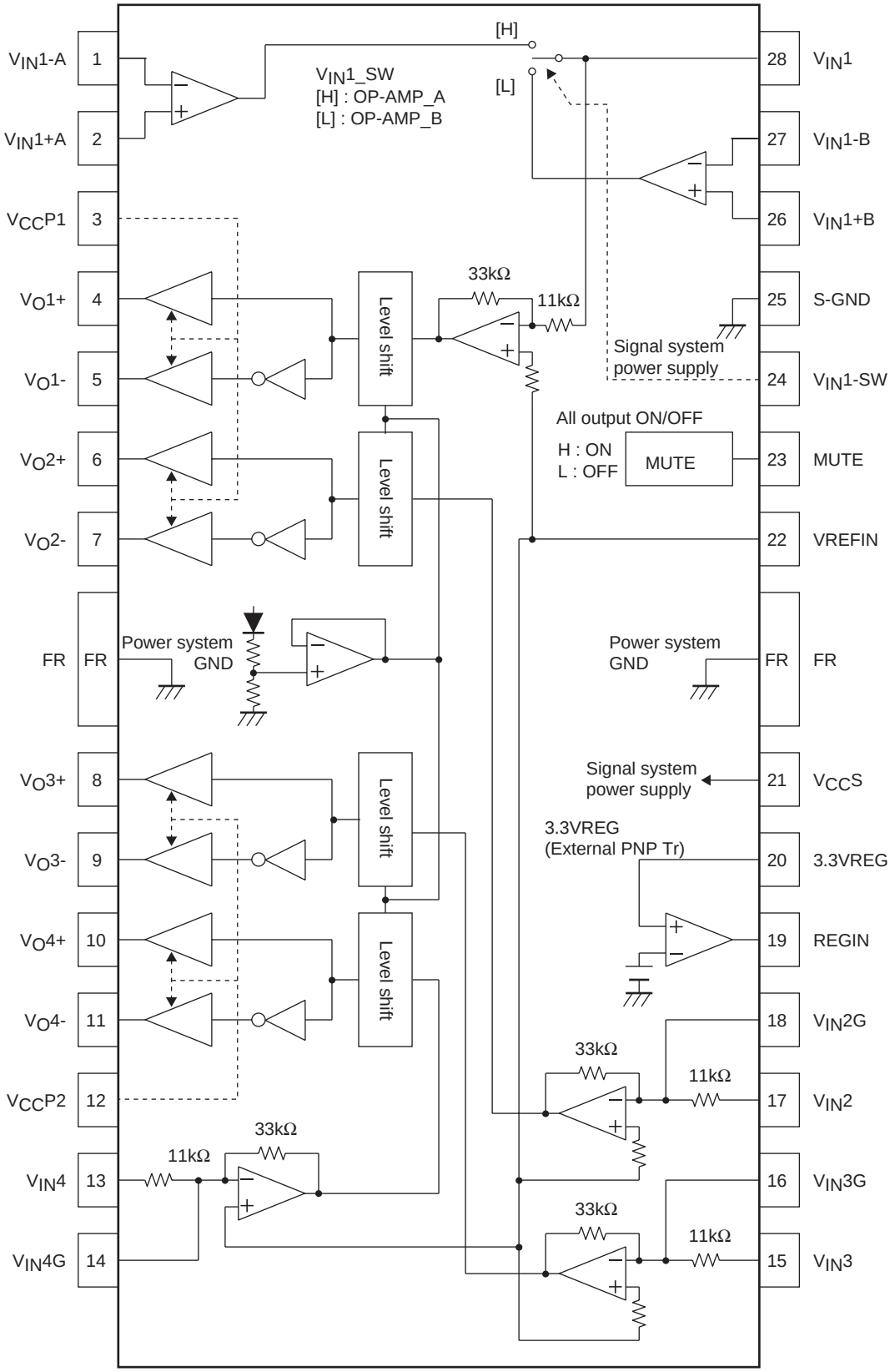
unit : mm (typ)

3234B





Block Diagram



Pin Functions

Pin No.	Symbol	Pin descriptions
1	$V_{IN}1$-A	CH1 input AMP_A inverted input
2	$V_{IN}1$+A	CH1 input AMP_A non-inverted input
3	$V_{CC}P1$	CH1 and CH2 power stage power supply
4	V_O1+	Output pin (+) for channel 1
5	V_O1-	CH1 Output pin (-) for channel 1
6	V_O2+	Output pin (+) for channel 2
7	V_O2-	Output pin (-) for channel 2
8	V_O3+	Output pin (+) for channel 3
9	V_O3-	Output pin (-) for channel 3
10	V_O4+	Output pin (+) for channel 4
11	V_O4-	Output pin (-) for channel 4
12	$V_{CC}P2$	CH3 and CH4 power stage power supply
13	$V_{IN}4$	Input pin for channel 4
14	$V_{IN}4G$	Input pin for channel 4 (for gain adjustment)
15	$V_{IN}3$	Input pin for channel 3
16	$V_{IN}3G$	Input pin for channel 3 (for gain adjustment)
17	$V_{IN}2$	Input pin for channel 2
18	$V_{IN}2G$	Input pin for channel 2 (for gain adjustment)
19	REGIN	External PNP transistor, base connection
20	3.3VREG	3.3VREG output pin, external PNP transistor, collector connection
21	$V_{CC}S$	Signal system GND
22	VREFIN	Reference voltage application pin
23	MUTE	Output ON/OFF pin
24	$V_{IN}1$_SW	CH1 input OP_AMP changeover pin
25	S_GND	Signal system GND
26	$V_{IN}1$+B	CH1 AMP_B non-inverted input pin
27	$V_{IN}1$-B	CH1 AMP_B inverted input pin
28	$V_{IN}1$	CH1 input pin, input OP_AMP output pin

Note : The center frame (FR) becomes GND (P-GND) for the power system. Keep this at the minimum potential together with the signal GND (S-GND).
Short-circuit V_{CC}_S (signal system power supply), $V_{CC}P1$, and $V_{CC}P2$ (output stage power supply) externally.

MUTE, VREF-SW

Relation of MUTE and VREF-SW

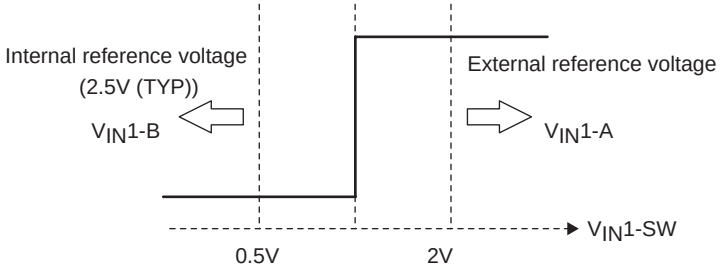
MUTE	Output			
	CH1	CH2	CH3	CH4
H	ON			
L	OFF			

*1 Output to be HI impedance with output OFF.

*2 MUTE operative for all channels.

$V_{IN}1$_SW and CH1 input OP_AMP

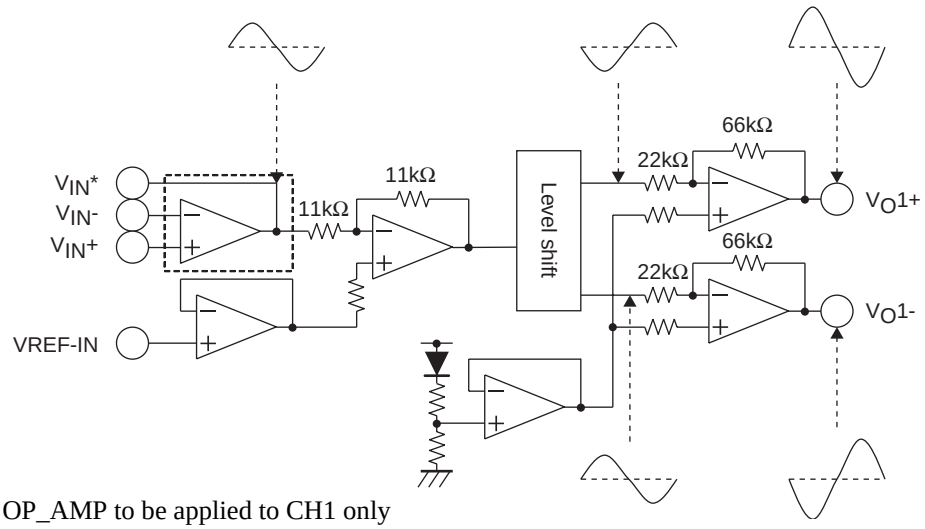
$V_{IN}1$_SW	CH1 input OP_AMP
H	AMP_A
L	AMP_B



On MUTE

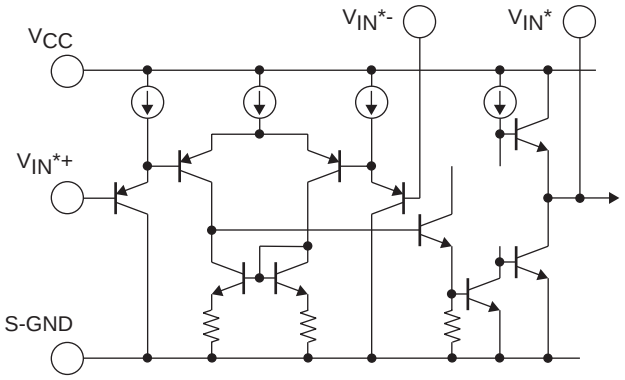
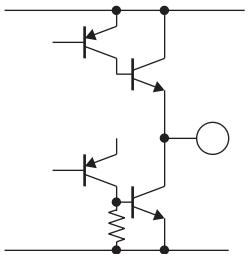
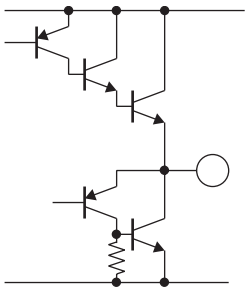
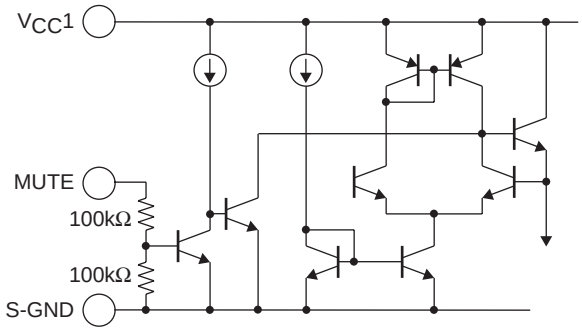
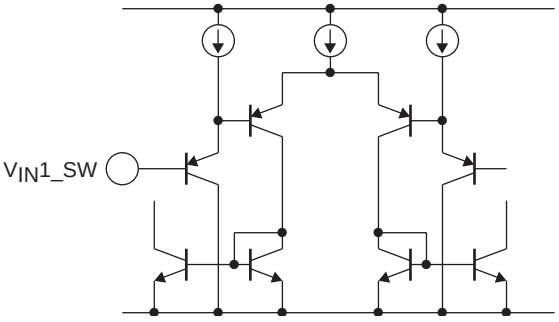
MUTE	Output AMP
L	OFF
H	ON

Outline of inputs and outputs



Input OP_AMP to be applied to CH1 only

Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
28 27 26 18 17 16 15 14 13	$V_{IN}1$ $V_{IN}1$-B $V_{IN}1$+B $V_{IN}2$G $V_{IN}2$ $V_{IN}3$G $V_{IN}3$ $V_{IN}4$G $V_{IN}4$	Input	Input pin Set the total gain with the gain of this input AMP.	
4 5	V_O1+ V_O1-	Output (CH1)	Output pin for channel 1	
6 7 8 9 10 11	V_O2+ V_O2- V_O3+ V_O3- V_O4+ V_O4-	Output (CH2 to 4)	CH2 to 4 output pins	
23	MUTE	MUTE	ON/OFF of corresponding CH output MUTE : H output ON MUTE : L output OFF * Output OFF when the MUTE pin is open (similarly to MUTE : L)	
24	$V_{IN}1$_SW	CH1 Input AMP changeover	CH1 input OP-AMP changeover function. AMP_A or AMP_B is selected according to the voltage applied to $V_{IN}1$_SW. H : V_{IN}_A L : V_{IN}_B	

Sample Application Circuit