TPS2291xx Ultra-small, Low On Resistance Load Switch With Controlled Turn-on

1 Features

- Integrated Single Load Switch
- Four Pin Wafer-Chip-Scale Package (Nom)
  - 0.9 mm × 0.9 mm, 0.5-mm Pitch, 0.5-mm Height (YZV)
- Input Voltage Range: 1.4 V to 5.5 V
- Low ON-Resistance
  - r_{ON} = 60 mΩ at VIN = 5 V
  - r_{ON} = 61 mΩ at VIN = 3.3 V
  - r_{ON} = 74 mΩ at VIN = 1.8 V
  - r_{ON} = 84 mΩ at VIN = 1.5 V
- 2-A Maximum Continuous Switch Current
- Low Threshold Control Input
- Controlled Slew-rate
- Under-Voltage Lock Out
- Full-Time Reverse Current Protection
- Quick Output Discharge Transistor (TPS22913B/C Devices)

2 Applications

- Notebook Computer and Ultrabook™
- Tablets and Set-Top-Boxes
- Portable Industrial / Medical Equipment
- Portable Media Players
- Point Of Sale Pins
- GPS Navigation Devices
- Digital Cameras
- Portable Instrumentation
- Smartphones / Wireless Handsets

3 Description

The TPS22910A, TPS22912C, and TPS22913B/C are small, low r_{ON} load switches with controlled turn on. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.4 V to 5.5 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage GPIO control signals.

The TPS22910A, TPS22912C, and TPS22913B/C devices provide reverse current protection in ON and OFF states. An internal reverse voltage comparator disables the power-switch when the output voltage (V_{OUT}) is driven higher than the input voltage (V_{IN}), by V_{RCP}, to quickly (10 µs typ) stop the flow of current towards the input side of the switch. Reverse current protection is always active, even when the power-switch is disabled. Additionally, under-voltage lockout (UVLO) protection turns the switch off if the input voltage is too low.

The TPS22913B/C contains a 150-Ω on-chip load resistor for quick output discharge when the switch is turned off.

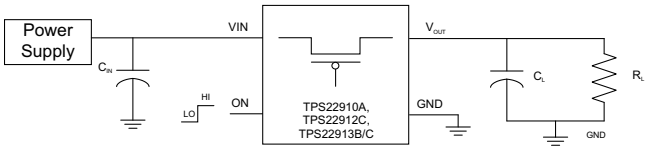
This family of devices have various slew rate options to avoid inrush current (see *Device Comparison Table* for details), are available in an ultra-small, space-saving 4-pin WCSP packages, and are characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22910A	DSBGA (4)	0.90 mm × 0.90 mm
TPS22912C		
TPS22913B		
TPS22913C		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



On-State Resistance vs Input Voltage

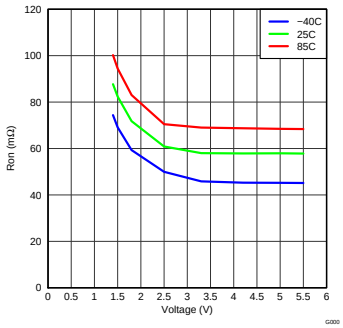


Table of Contents

5 Revision History

Changes from Revision E (June 2014) to Revision F — **Page**

- Updated 'ON' pin description in the Pin Functions table. ... 3

Changes from Revision D (May 2014) to Revision E — **Page**

- Updated Switching Characteristics table ... 6
- Updated Typical DC Characteristics section. ... 7
- Updated Timing Waveforms graphic. ... 17
- Updated Application Curves section. ... 22

Changes from Revision C (May 2013) to Revision D — **Page**

- Combined TPS22910A, TPS22912C, and TPS22913B/C datasheets. ... 1

6 Device Comparison Table

DEVICE	r_{ON} (typ) at 3.3 V	RISE TIME at 3.3V (typ)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22910A	61 mΩ	1 µs	No	2 A	Active Low
TPS22912C	61 mΩ	1000 µs	No	2 A	Active High
TPS22913B	61 mΩ	66 µs	Yes	2 A	Active High
TPS22913C	61 mΩ	660 µs	Yes	2 A	Active High

7 Pin Configuration and Functions

YZV PACKAGE

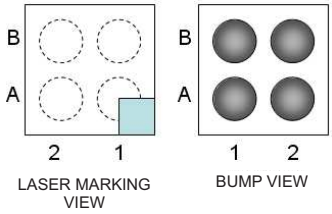


Table 1. Pin Assignments

B	ON	GND
A	VIN	VOUT
	2	**1**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1	O	Switch output
VIN	A2	I	Switch input, use a bypass capacitor (ceramic) to ground.
GND	B1	–	Ground
ON	B2	I	Switch control input. Do not leave floating

8 Specifications

8.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	6	V
V_{ON}	Input voltage range	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		2.5	A
T_A	Operating free-air temperature range	–40	85	°C
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

8.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.4	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	
V_{IH}	High-level input voltage, ON	VIN = 1.4 V to 5.5 V	1.1	5.5	V
V_{IL}	Low-level input voltage, ON	VIN = 3.61 V to 5.5 V		0.6	V
		VIN = 1.4 V to 3.6 V		0.4	V
C_{IN}	Input capacitor		1 (1)		µF

(1) Refer to the application section.

8.4 Thermal Information

THERMAL METRIC (1)		TPS22910 CSP 4 PINS	TPS22912 CSP 4 PINS	TPS22913 CSP 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.1	189.1	189.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	1.9	1.9	1.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	36.8	36.8	
ψ_{JT}	Junction-to-top characterization parameter	11.3	11.3	11.3	
ψ_{JB}	Junction-to-board characterization parameter	36.8	36.8	36.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

The electrical characteristics in this section apply to all devices unless otherwise noted. For TPS22910A V_{ON} = 0 V where enabled and V_{ON} = V_{IN} where disabled. For TPS22912C and TPS22913B/C V_{ON} = V_{IN} where enabled and V_{ON} = 0 V where disabled. V_{IN} = 1.4 V to 5.5 V, T_A = –40ºC to 85ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0 mA, V_{IN} = 5.25 V, V_{ON} = Enabled	Full		2	10	µA
		I_{OUT} = 0 mA, V_{IN} = 4.2 V, V_{ON} = Enabled			2	7.0	
		I_{OUT} = 0 mA, V_{IN} = 3.6 V, V_{ON} = Enabled			2	7.0	
		I_{OUT} = 0 mA, V_{IN} = 2.5 V, V_{ON} = Enabled			0.9	5	
		I_{OUT} = 0 mA, V_{IN} = 1.5 V, V_{ON} = Enabled			0.7	5	
$I_{IN(off)}$	Off supply current	R_L = 1 MΩ, V_{IN} = 5.25 V, V_{ON} = Disabled	Full		1.2	10	µA
		R_L = 1 MΩ, V_{IN} = 4.2 V, V_{ON} = Disabled			0.2	7.0	
		R_L = 1 MΩ, V_{IN}= 3.6 V, V_{ON} = Disabled			0.1	7.0	
		R_L = 1 MΩ, V_{IN} = 2.5 V, V_{ON} = Disabled			0.1	5	
		R_L = 1 MΩ, V_{IN} = 1.5 V, V_{ON} = Disabled			0.1	5	
$I_{IN(Leakage)}$	Leakage current	V_{OUT} = 0 V, V_{IN}= 5.25 V, V_{ON} = Disabled	Full		1.2	10	µA
		V_{OUT} = 0 V, V_{IN} = 4.2 V, V_{ON} = Disabled			0.2	7.0	
		V_{OUT} = 0 V, V_{IN} = 3.6 V, V_{ON} = Disabled			0.1	7.0	
		V_{OUT} = 0 V, V_{IN} = 2.5 V, V_{ON} = Disabled			0.1	5	
		V_{OUT} = 0 V, V_{IN} = 1.5 V, V_{ON} = Disabled			0.1	5	
r_{ON}	On-resistance	V_{IN} = 5.25 V, I_{OUT} = –200 mA	25°C		60	80	mΩ
			Full			110	
		V_{IN} = 5.0 V, I_{OUT} = –200 mA	25°C		60	80	
			Full			110	
		V_{IN} = 4.2 V, I_{OUT} = –200 mA	25°C		60	80	
			Full			110	
		V_{IN} = 3.3 V, I_{OUT} = –200 mA	25°C		60.7	80	
			Full			110	
		V_{IN} = 2.5 V, I_{OUT} = –200 mA	25°C		63.4	90	
			Full			120	
		V_{IN} = 1.8 V, I_{OUT} = –200 mA	25°C		74.2	100	
			Full			130	
		V_{IN} = 1.5 V, I_{OUT} = –200 mA	25°C		83.9	120	
			Full			150	
RPD(1)	Output pull down resistance	V_{IN} = 3.3 V, I_{OUT} = 30 mA, V_{ON} = 0	25°C		153	200	Ω
UVLO	Under voltage lockout	V_{IN} increasing, V_{ON} = 0 V, I_{OUT} = –100 mA	Full			1.2	V
		V_{IN} decreasing, V_{ON} = 0 V, R_L = 10 Ω		0.50			
I_{ON}	ON input leakage current	V_{ON} = 1.4 V to 5.25 V or GND	Full			1	µA
V_{RCP}	Reverse current voltage threshold	TPS22910A, TPS22913B/C			44		mV
		TPS22912C			54		
t_{DELAY}	Reverse current response delay	V_{IN} = 5 V			10		µs
I_{RCP}(leak)	Reverse current protection leakage after reverse current event.	V_{OUT} – V_{IN} > V_{RCP}	25°C		0.3		µA

(1) Only applies to the TPS22913B/C devices

8.6 Switching Characteristics, Typical

PARAMETER		TEST CONDITION	TPS22910A	TPS22912C	TPS22913B	TPS22913C	UNIT
VIN = 5 V, T_A = 25ºC (unless otherwise noted)							
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	2	840	76	770	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	5.5	6.6	6.6	6.6	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	1	912	82	838	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	3	3	3	3	
VIN = 3.3 V, T_A = 25ºC (unless otherwise noted)							
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	2.5	1147	102	1048	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	7	8.6	8.5	8.6	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	1	1030	97	980	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	3.5	3	3	3	
VIN = 1.5 V, T_A = 25ºC (unless otherwise noted)							
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF	4.5	2513	234	2344	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF	16.5	17.4	17	18	
t_R	VOUT rise time	R_L = 10 Ω, C_L = 0.1 µF	2	1970	244	1823	
t_F	VOUT fall time	R_L = 10 Ω, C_L = 0.1 µF	7	6.5	6.5	6.5	

8.7 Typical DC Characteristics

The typical characteristics curves in this section apply to all devices unless otherwise noted.

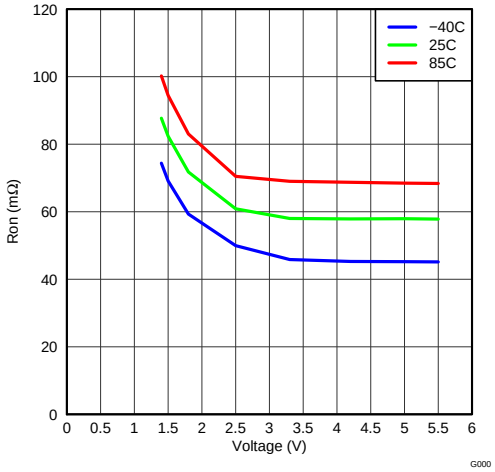


Figure 1. On-State Resistance vs Input Voltage

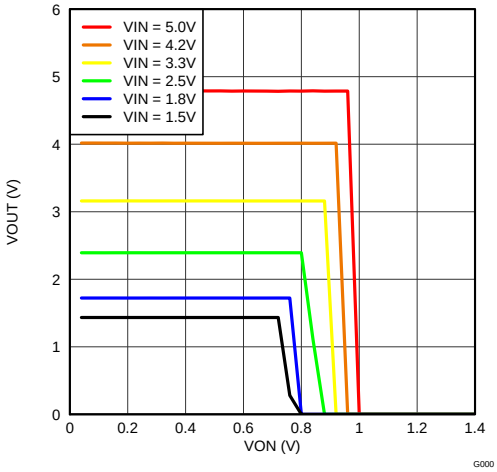


Figure 2. TPS22910A On Input Threshold (Active Low)

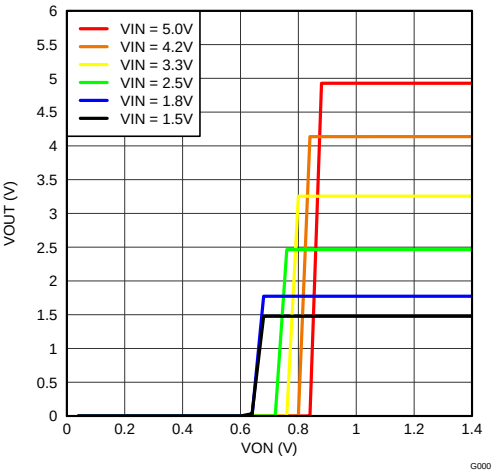


Figure 3. TPS22912C and TPS22913B/C On Input Threshold (Active High)

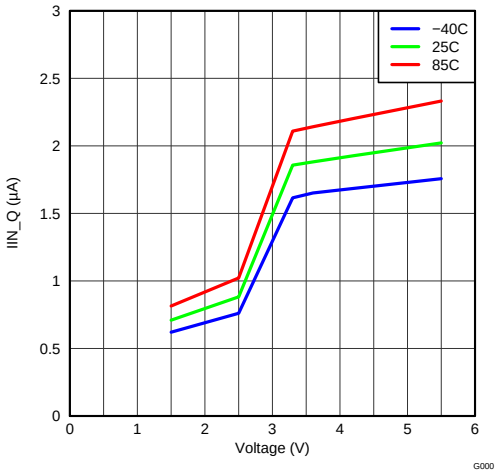


Figure 4. Input Current, Quiescent vs Input Voltage

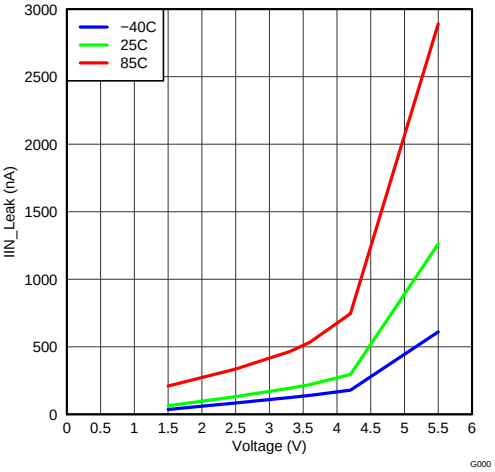


Figure 5. Input Current, Leak vs Input Voltage

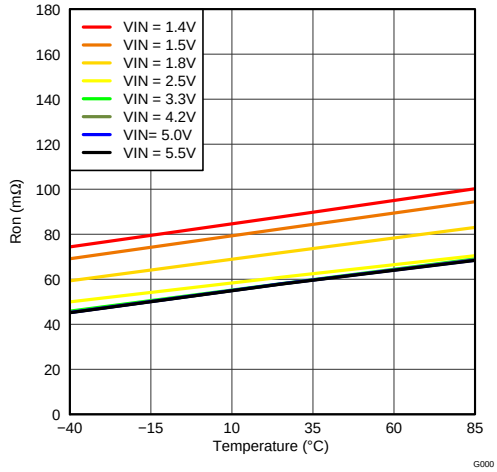


Figure 6. On-state Resistance vs Temperature

Typical DC Characteristics (continued)

The typical characteristics curves in this section apply to all devices unless otherwise noted.

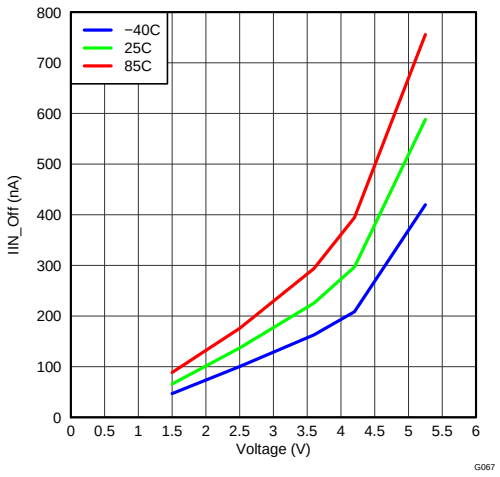


Figure 7. Input Current, Off vs Input Voltage

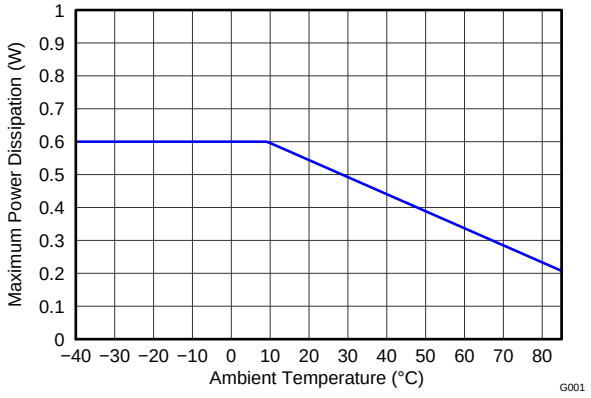


Figure 8. Allowable Power Dissipation

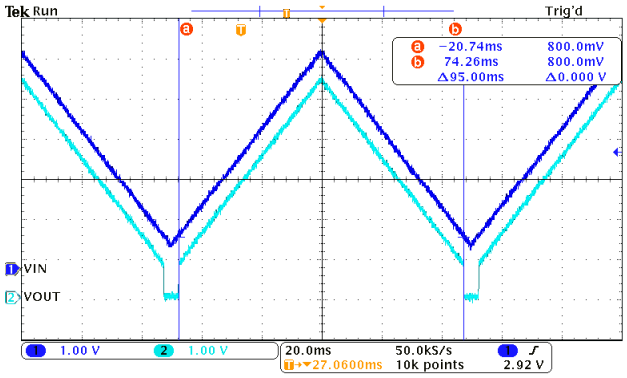


Figure 9. Under Voltage Lockout Response (IOUT = –100mA)

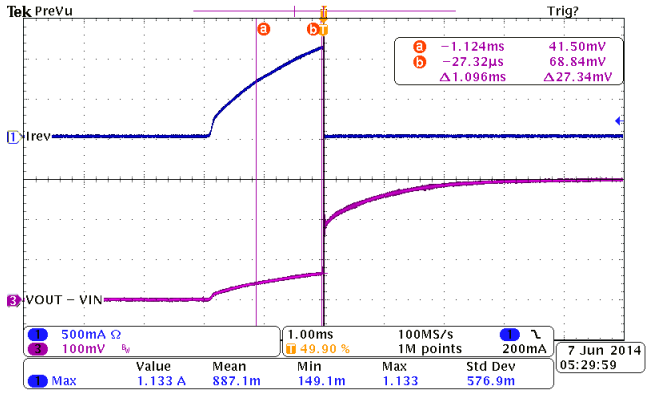


Figure 10. Full-Time Reverse Current Protection (VIN = 3.0 V, VOUT Ramp up From 3.0 V to 3.3 V)

8.8 Typical AC Characteristics, TPS22910A

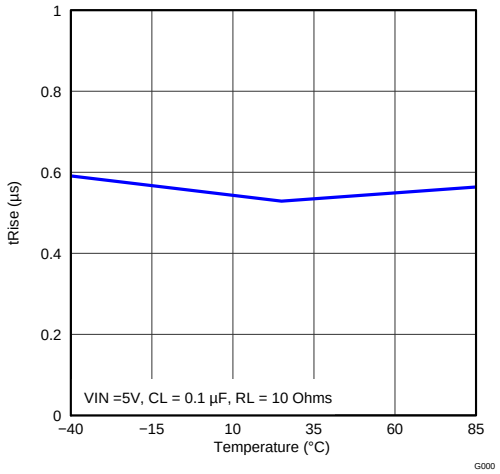


Figure 11. Rise Time vs Temperature

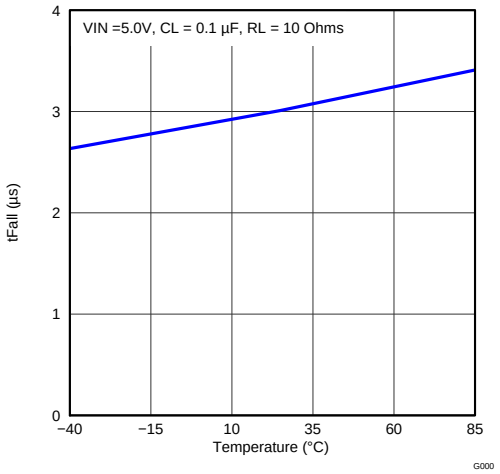


Figure 12. Fall Time vs Temperature

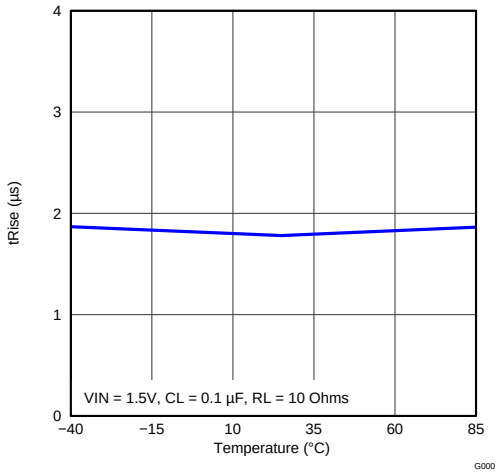


Figure 13. Rise Time vs Temperature

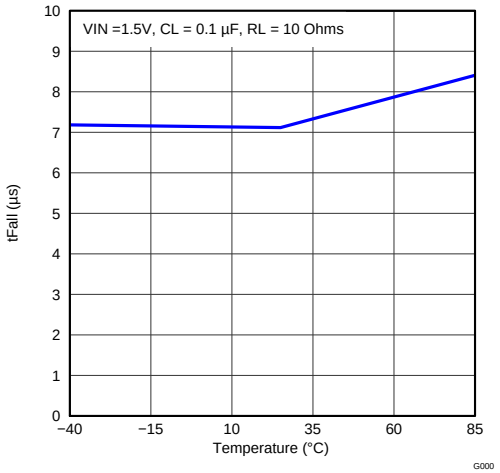


Figure 14. Fall Time vs Temperature

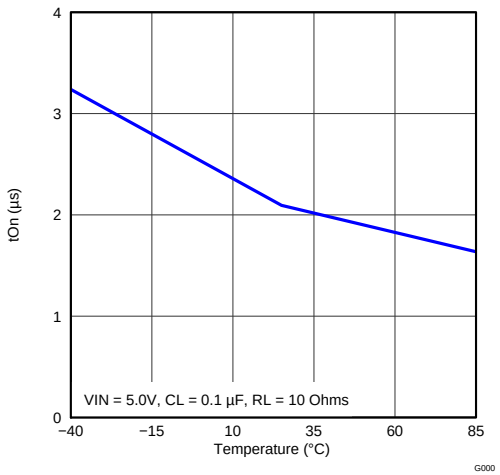


Figure 15. Turn-on Time vs Temperature

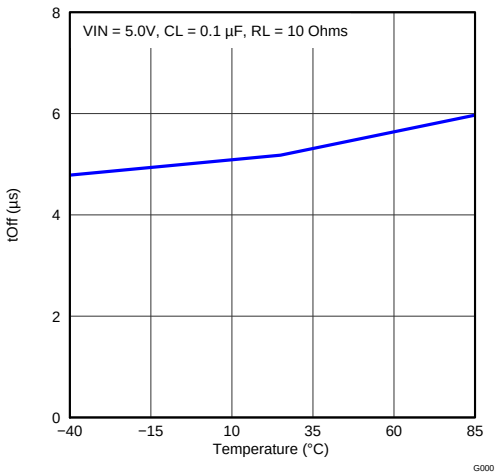


Figure 16. Turn-off Time vs Temperature

Typical AC Characteristics, TPS22910A (continued)

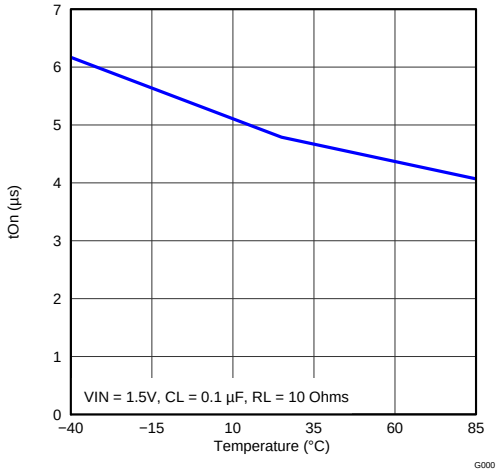


Figure 17. Turn-on Time vs Temperature

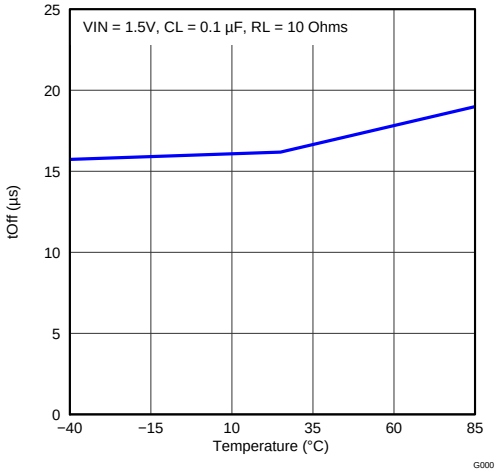


Figure 18. Turn-off Time vs Temperature

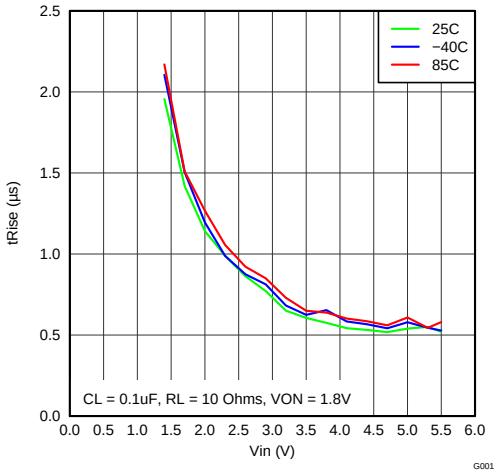


Figure 19. Rise Time vs Input Voltage

8.9 Typical AC Characteristics, TPS22912C

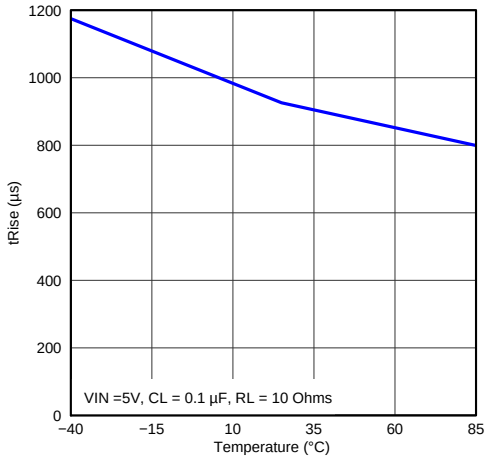


Figure 20. Rise Time vs Temperature

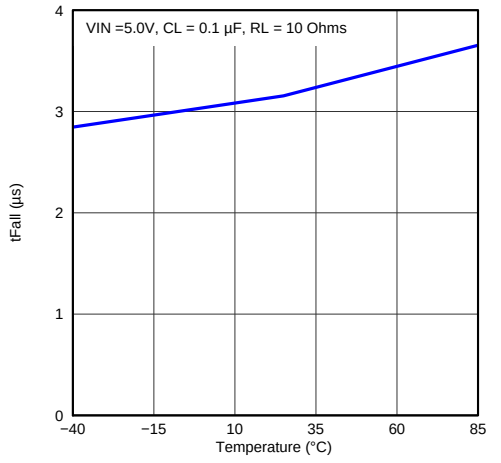


Figure 21. Fall Time vs Temperature

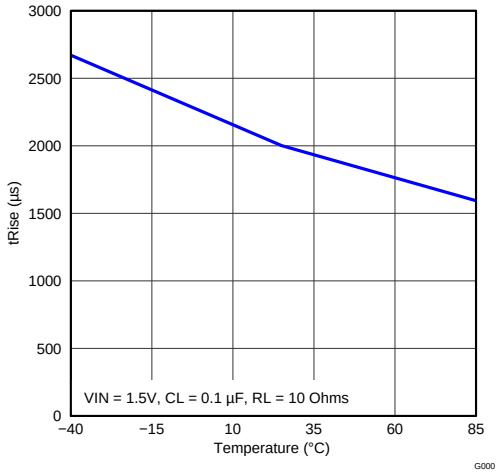


Figure 22. Rise Time vs Temperature

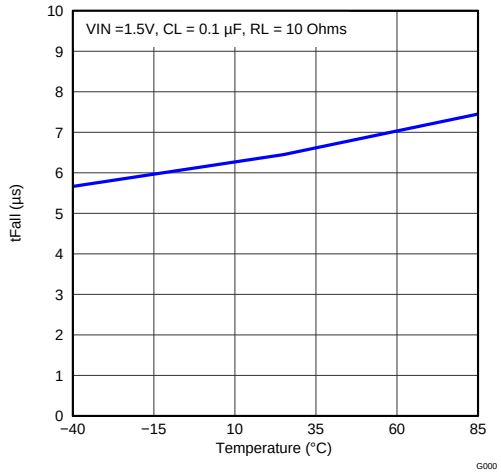


Figure 23. Fall Time vs Temperature

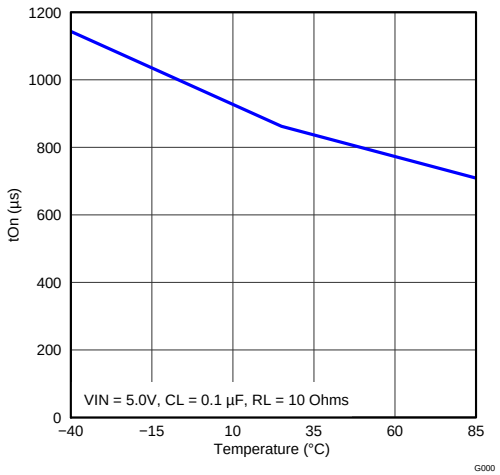


Figure 24. Turn-on Time vs Temperature

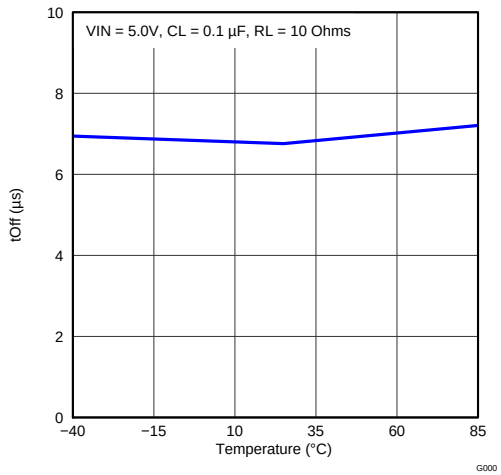


Figure 25. Turn-off Time vs Temperature

Typical AC Characteristics, TPS22912C (continued)

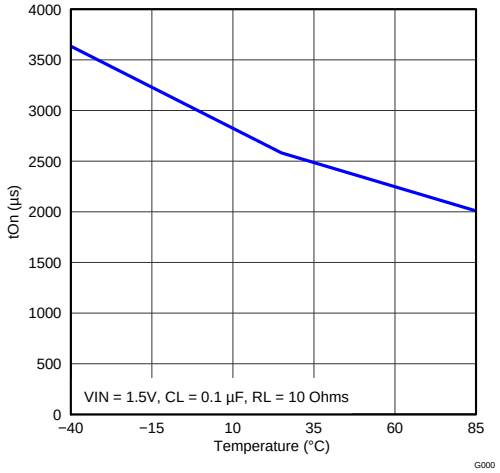


Figure 26. Turn-on Time vs Temperature

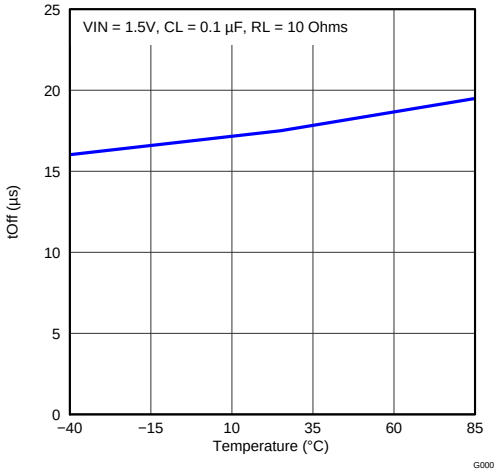


Figure 27. Turn-off Time vs Temperature

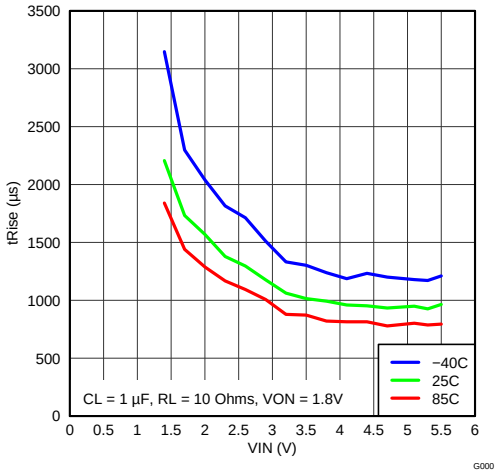


Figure 28. Rise Time vs Input Voltage

8.10 Typical AC Characteristics, TPS22913B

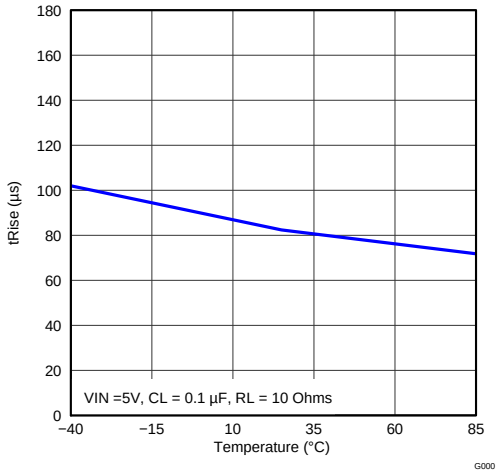


Figure 29. Rise Time vs Temperature

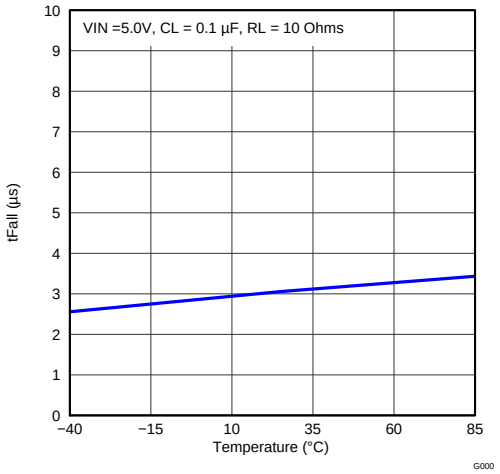


Figure 30. Fall Time vs Temperature

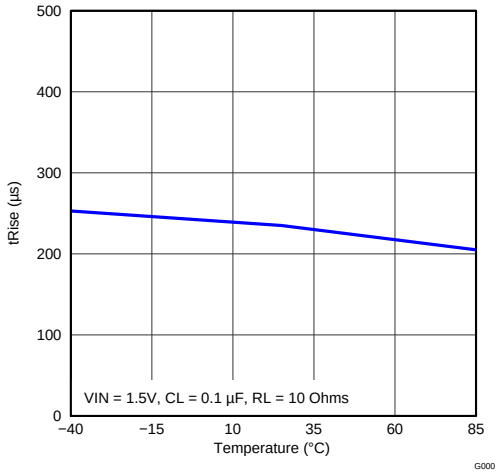


Figure 31. Rise Time vs Temperature

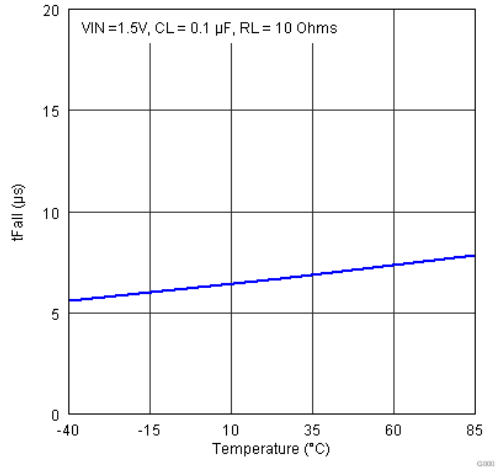


Figure 32. Fall Time vs Temperature

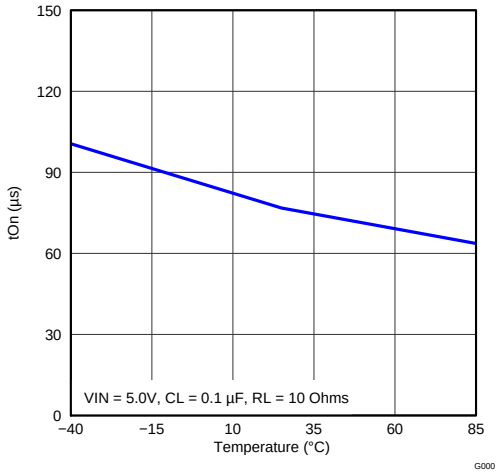


Figure 33. Turn-on Time vs Temperature

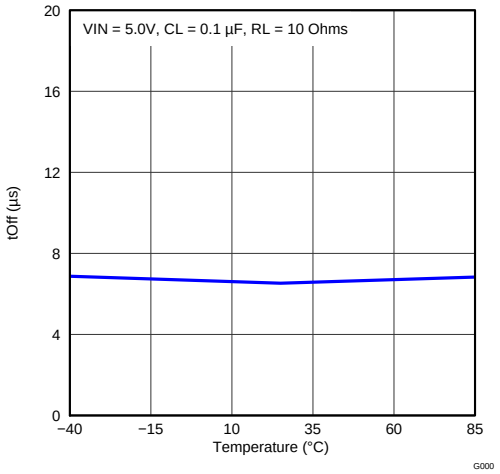


Figure 34. Turn-off Time vs Temperature

Typical AC Characteristics, TPS22913B (continued)

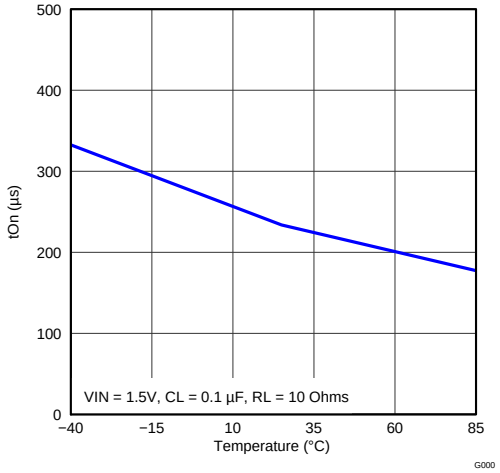


Figure 35. Turn-on Time vs Temperature

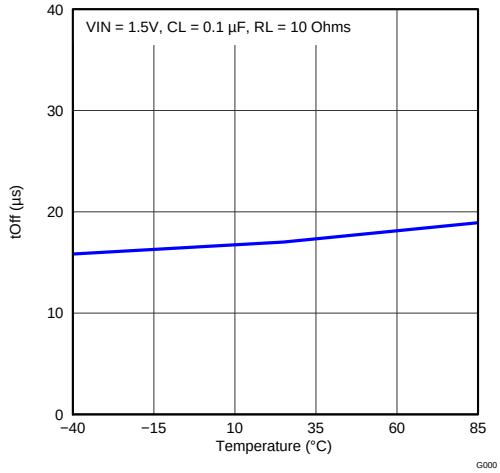


Figure 36. Turn-off Time vs Temperature

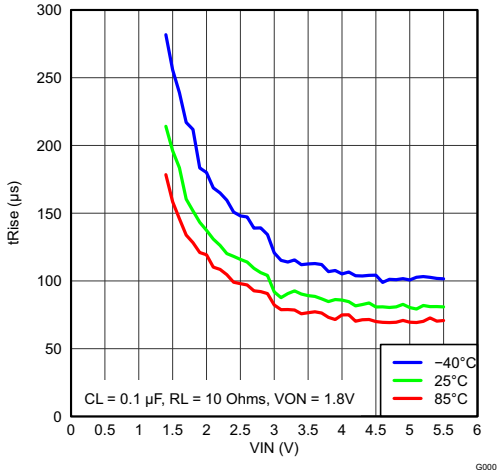


Figure 37. Rise Time vs Input Voltage

8.11 Typical AC Characteristics, TPS22913C

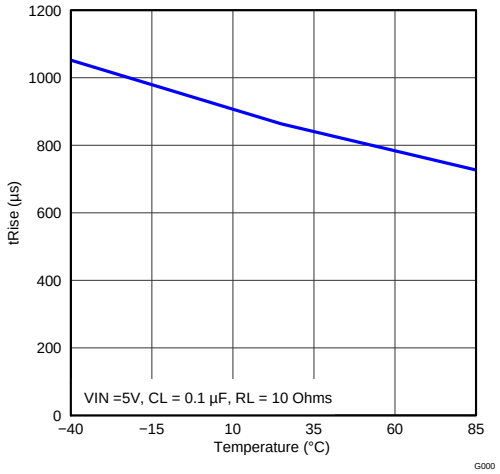


Figure 38. Rise Time vs Temperature

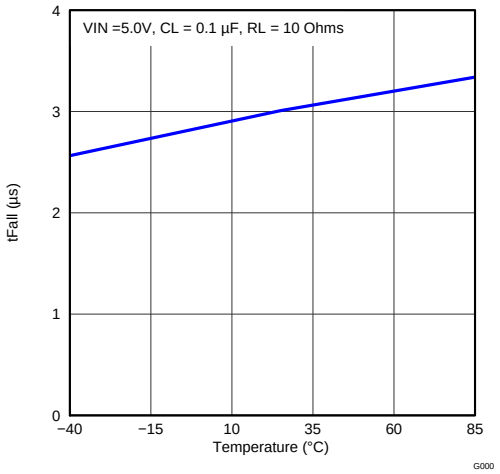


Figure 39. Fall Time vs Temperature

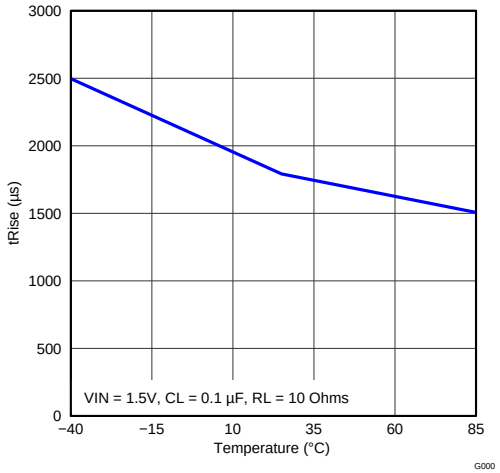


Figure 40. Rise Time vs Temperature

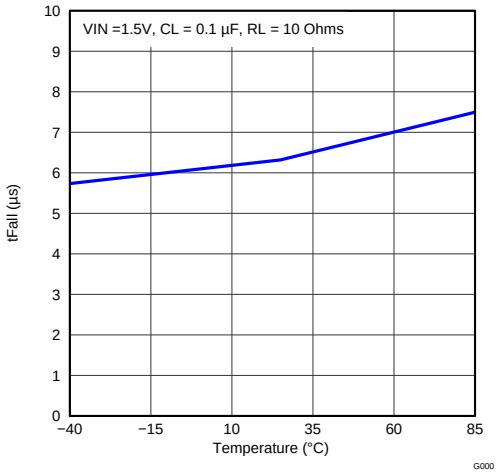


Figure 41. Fall Time vs Temperature

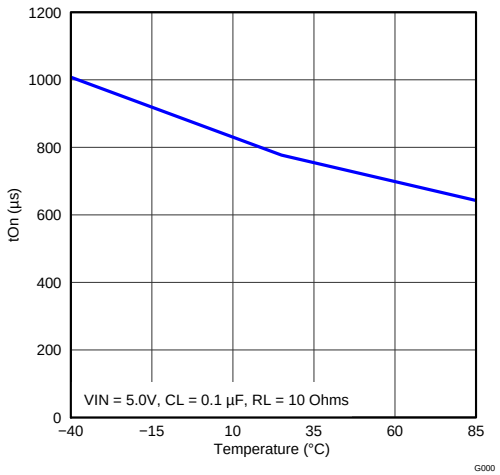


Figure 42. Turn-on Time vs Temperature

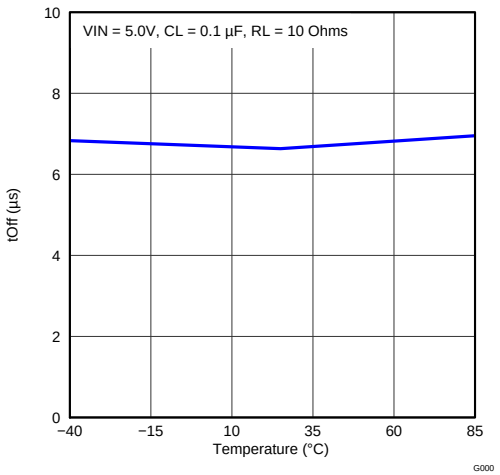


Figure 43. Turn-Off Time vs Temperature

Typical AC Characteristics, TPS22913C (continued)

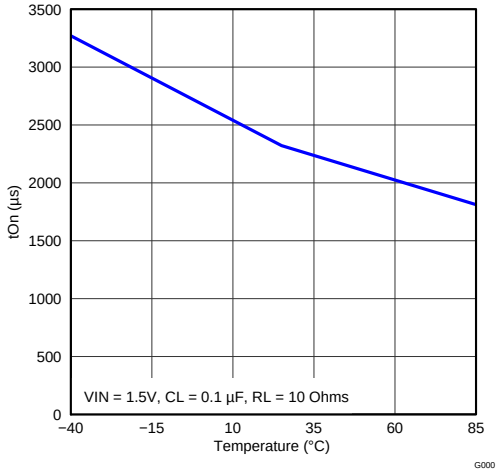


Figure 44. Turn-On Time vs Temperature

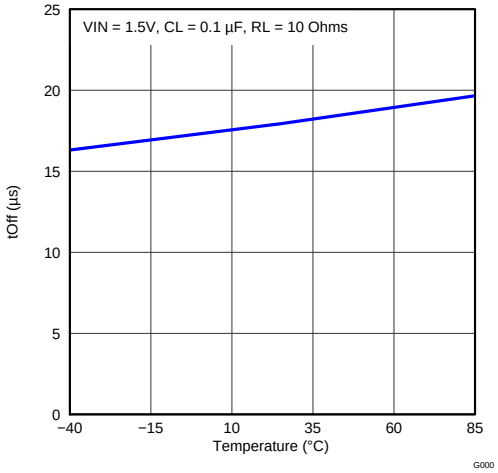


Figure 45. Turn-Off Time vs Temperature

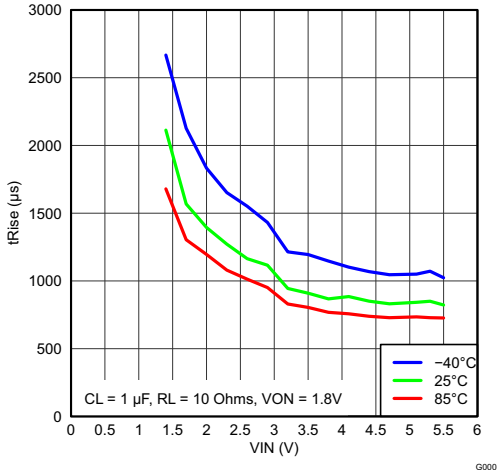


Figure 46. Rise Time vs Input Voltage

9 Parameter Measurement Information

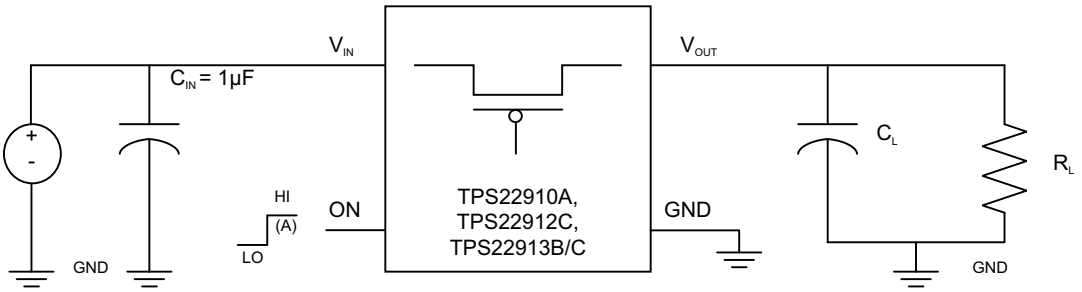
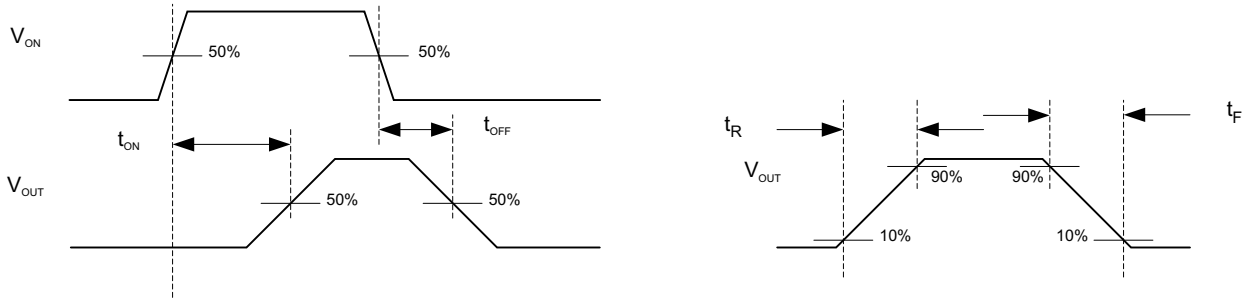


Figure 47. Timing Test Circuit



A. Rise and fall times of the control signal is 100 ns.

Figure 48. Timing Waveforms

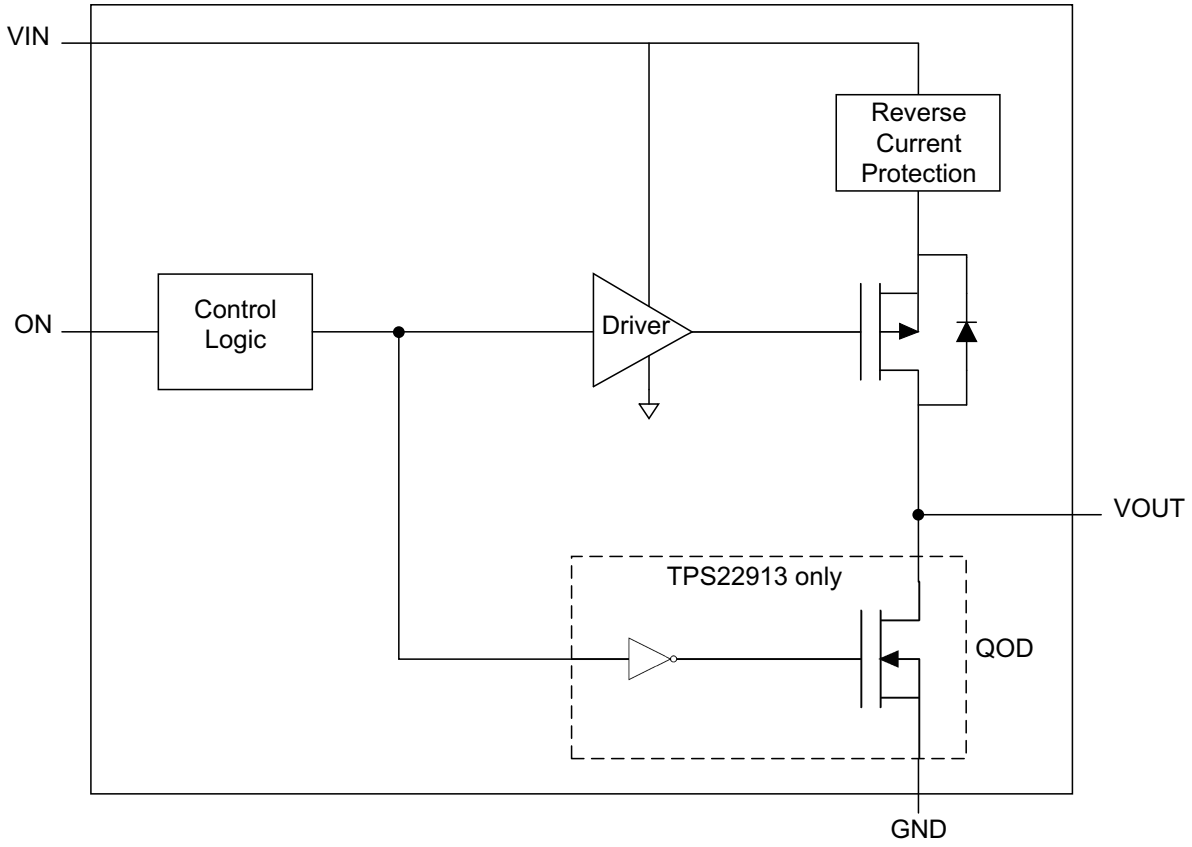
10 Detailed Description

10.1 Overview

This family of devices are single channel, 2-A load switches in ultra-small, space saving 4-pin WCSP package. These devices implement a low resistance P-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

These devices are designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and BOM count.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 On/Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, 3.3-V, or 5.5-V GPIO.

10.3.2 Under-Voltage Lockout

Under-voltage lockout protection turns off the switch if the input voltage drops below the under-voltage lockout threshold (UVLO). With the ON pin active, the input voltage rising above the under-voltage lockout threshold will cause a controlled turn-on of the switch to limit current over-shoot.

Feature Description (continued)

10.3.3 Full-Time Reverse Current Protection

In a scenario where V_{OUT} is greater than V_{IN}, there is potential for reverse current to flow through the pass FET or the body diode. The devices monitor V_{IN} and V_{OUT} voltage levels. When the reverse current voltage threshold (V_{RCP}) is exceeded, the switch is disabled (within 10µs typ). Additionally, the body diode is disengaged so as to prevent any reverse current flow to VIN. The peak instantaneous reverse current is the current it takes to activate the reverse current protection. After the reverse current protection has activated due to the peak instantaneous reverse current, the DC (off-state) leakage current from V_{OUT} and V_{IN} is referred to as I_{RCP}(leak) (see Figure 49). The pass FET, and the output voltage (V_{OUT}), will resume normal operation when the reverse voltage scenario is no longer present.

The following formula can be used to calculate the amount of peak instantaneous reverse current for a particular application:

$$I_{RC} = \frac{V_{RCP}}{r_{ON(VIN)}}$$

Where,

I_{RC} is the amount of reverse current,
$r_{ON(VIN)}$ is the on-resistance at the VIN of the reverse current condition.
V_{RCP} is the reverse voltage threshold.

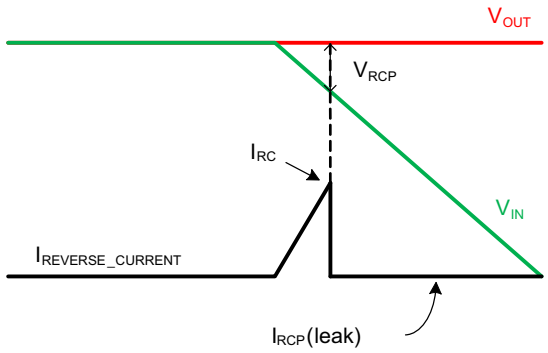


Figure 49. Reverse Current

10.4 Device Functional Modes

Table 2 describes what the VOUT pin will be connected to for a particular device as determined by the ON pin

Table 2. VOUT Function Table

ON	TPS22910A	TPS22912C	TPS22913B/C
L	VIN	Open	GND
H	Open	VIN	VIN

11 Application and Implementation

11.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

11.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN condition of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

Where,

ΔV = Voltage drop from VIN to VOUT

I_{LOAD} = Load current

R_{ON} = On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

11.1.2 On/Off Control

The ON pin controls the state of the switch. The ON pin has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

11.1.3 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

11.1.4 Output Capacitor (Optional)

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by using a device with a longer rise time.

11.2 Typical Application

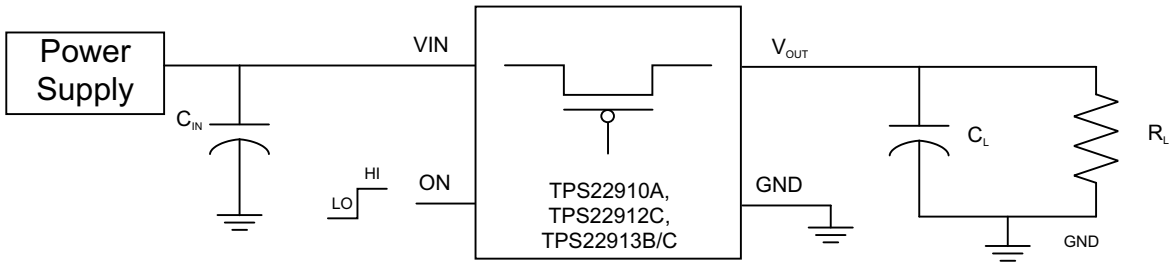


Figure 50. Typical Application

Typical Application (continued)

11.2.1 Design Requirements

Design Parameter	Example Value
VIN	1.5 V to 5 V
CL	0.1 µF to 1 µF
Maximum Acceptable Inrush Current	1 A

11.2.2 Detailed Design Procedure

11.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to VIN voltage. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times \frac{dv}{dt} \tag{2}$$

Where,

C = Output capacitance

$\frac{dv}{dt}$ = Output slew rate

The TPS22910A, TPS22912C, and TPS22913B/C offer several different rise time options to control the inrush current during turn-on. The appropriate device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. An output capacitance of 1.0 µF will be used since the inrush follows the following equations:

$$1.0\ \text{A} = 1.0\ \mu\text{F} \times \frac{dv}{dt} \tag{3}$$

$$\frac{dv}{dt} = 1\ \text{V/µs} \tag{4}$$

To ensure an inrush current of less than 1 A, a device with a slew rate less than 1 V/µs must be used

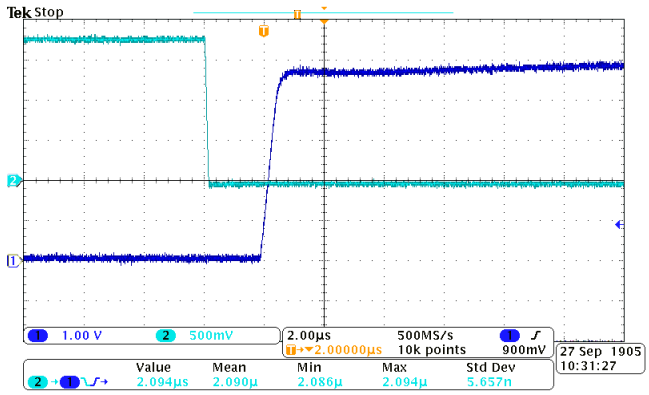
The TPS22910A has a typical rise time of 1 µs at 3.3 V . This results in a slew rate of 3.3 V/µs which is above the 1 V/µs requirement meaning the TPS22910 could not be used to meet the design requirements.

The TPS22913B has a typical rise time of 66 µs at 3.3 V. This results in a slew rate of 50 mV/µs which is below the 1 V/µs requirement; therefor, the TPS22913B could be used to meet the design requirements. The TPS22912C or TPS22913C have lower slew rates than the TPS22913B, so they could also be used, but the output would rise more slowly.

11.2.3 Application Curves

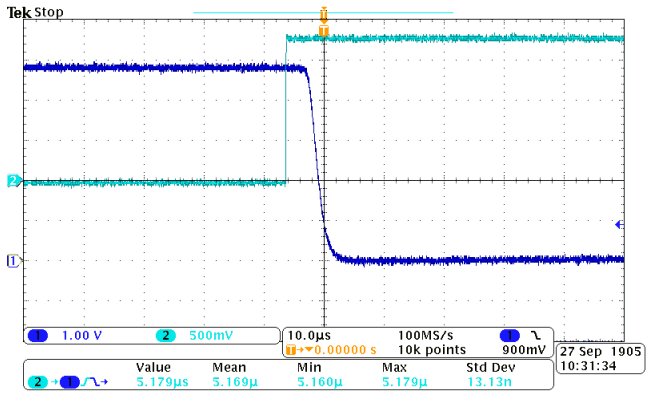
11.2.3.1 Typical Application Characteristics for TPS22910A

The dark blue curve (Channel 1) represents the VOUT pin of the device. The light blue curve (Channel 2) represents the ON pin of the device.



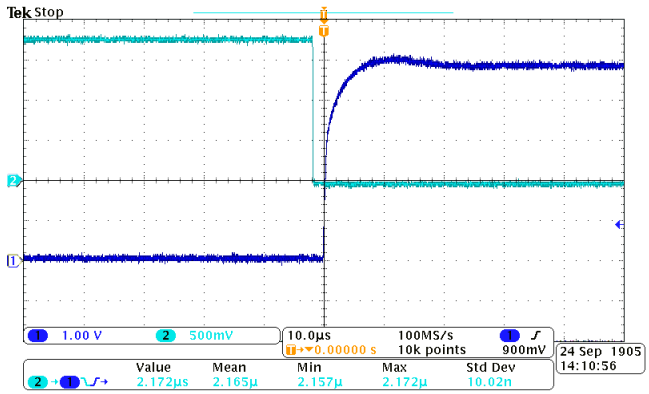
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 0.1 µF R_L = 10Ω

Figure 51. Turn-on Response



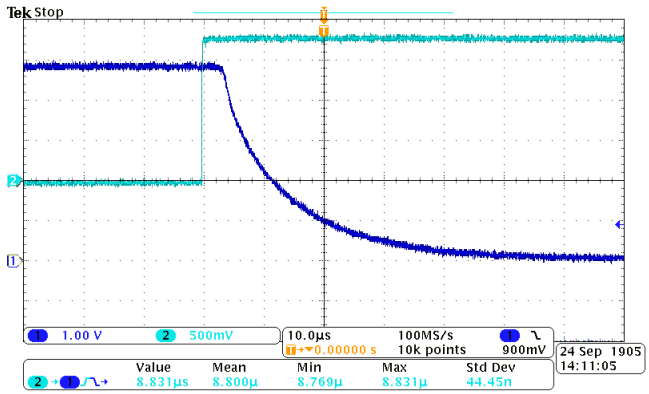
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 0.1 µF R_L = 10Ω

Figure 52. Turn-off Response



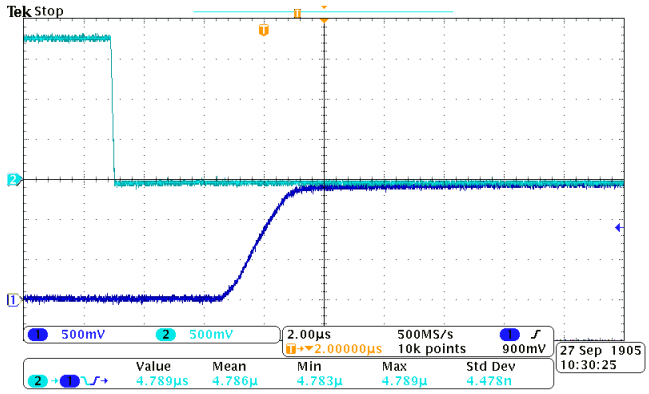
V_{IN} = 5 V T_A = 25°C C_{IN} =10 µF
C_L = 1 µF R_L = 10 Ω

Figure 53. Turn-on Response Time



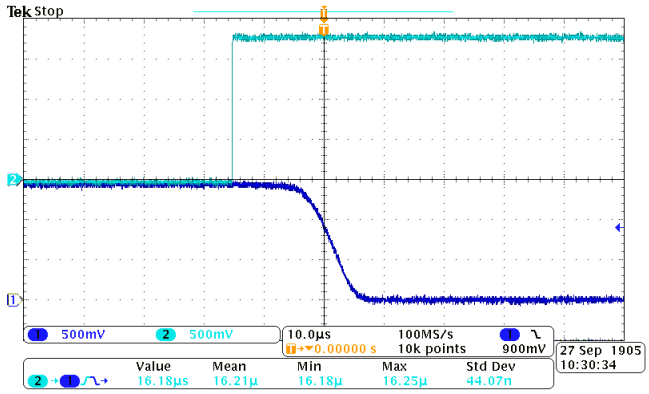
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10Ω

Figure 54. Turn-off Response Time



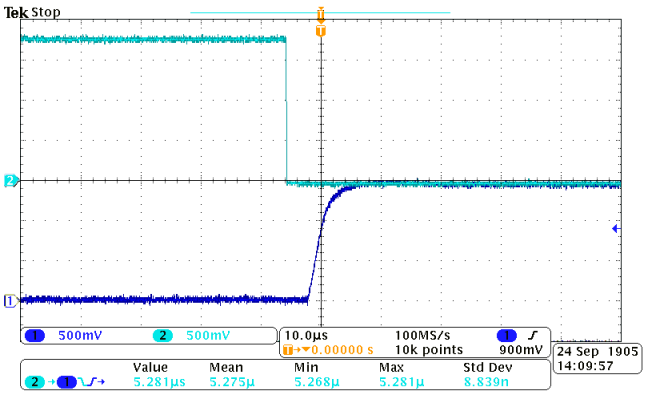
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 0.1 µF R_L = 10Ω

Figure 55. Turn-on Response Time



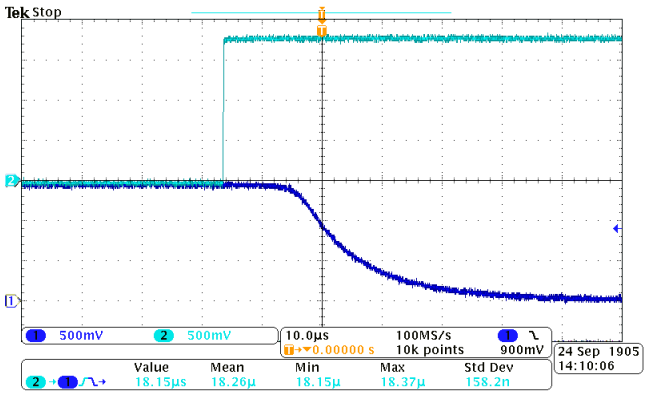
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 0.1 µF R_L = 10Ω

Figure 56. Turn-off Response Time



V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10Ω

Figure 57. Turn-on Response Time

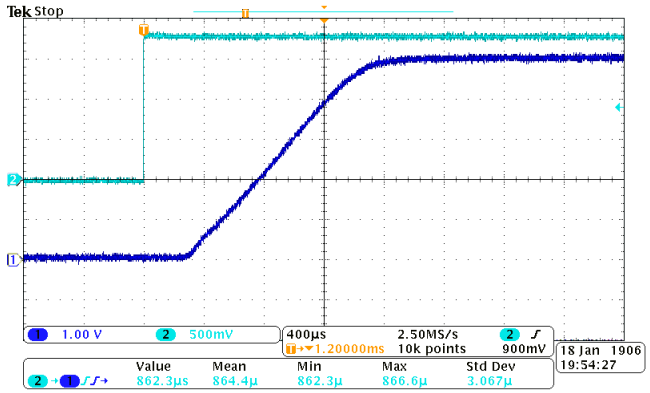


V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10Ω

Figure 58. Turn-off Response Time

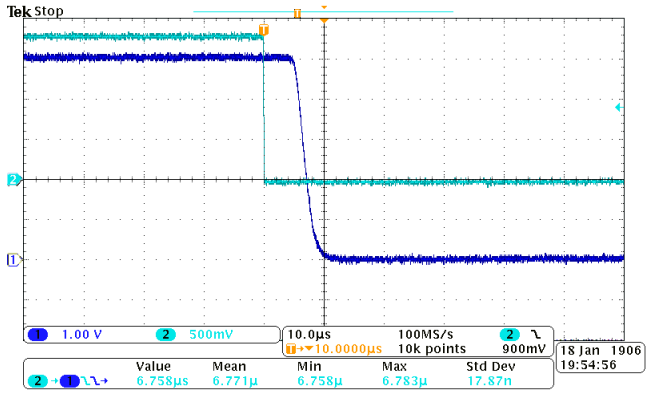
11.2.3.2 Typical Application Characteristics for TPS22912C

The dark blue curve (Channel 1) represents the VOUT pin of the device. The light blue curve (Channel 2) represents the ON pin of the device.



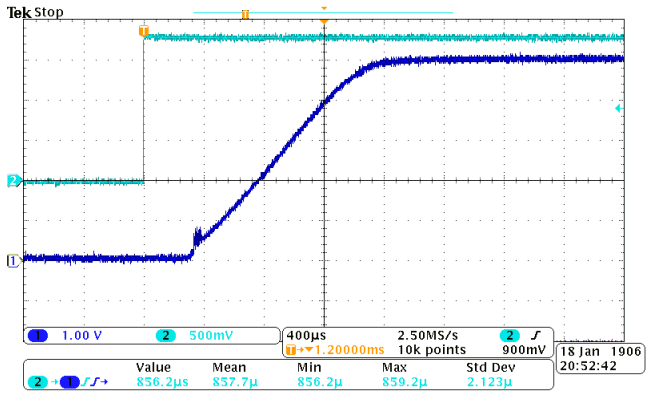
V_{IN} = 5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10Ω

Figure 59. Turn-on Response



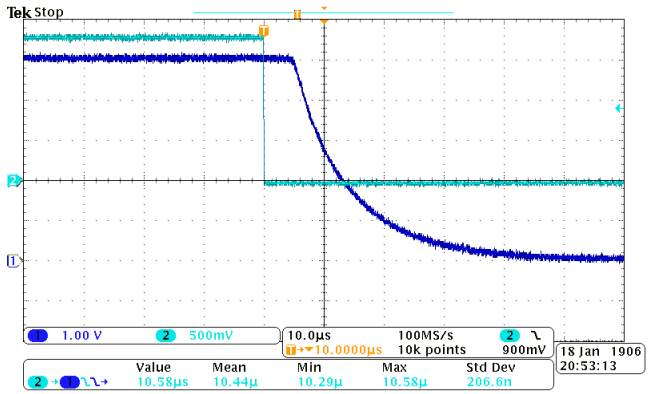
V_{IN} = 5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 60. Turn-off Response



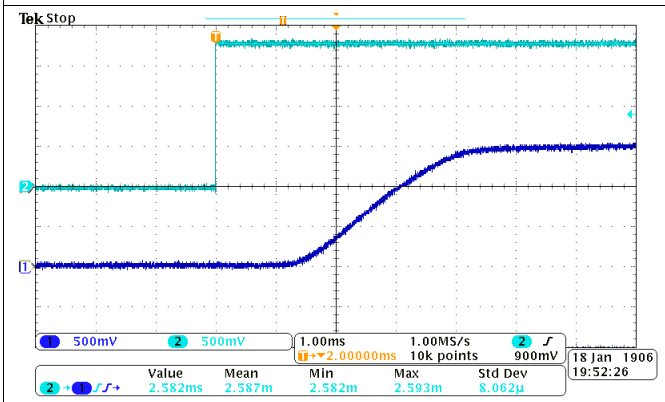
V_{IN} = 5 V T_A = 25°C C_{IN} =10 µF
C_L = 1 µF R_L = 10 Ω

Figure 61. Turn-on Response Time



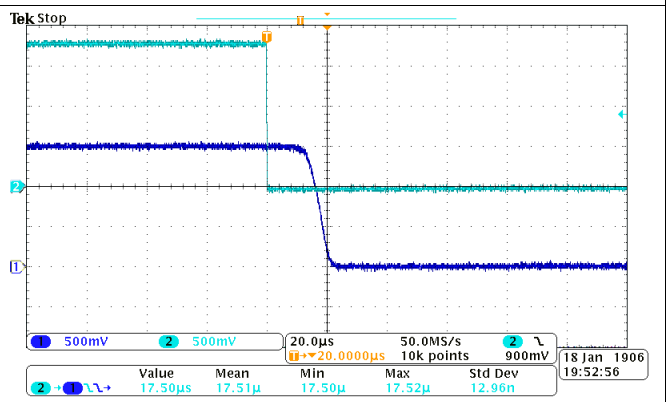
V_{IN} = 5 T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 62. Turn-off Response Time



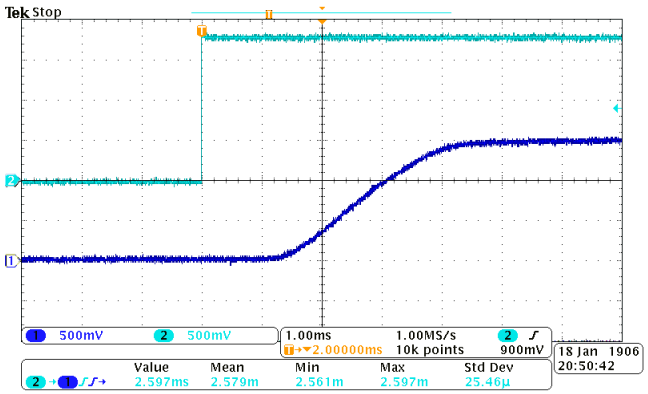
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 63. Turn-on Response Time



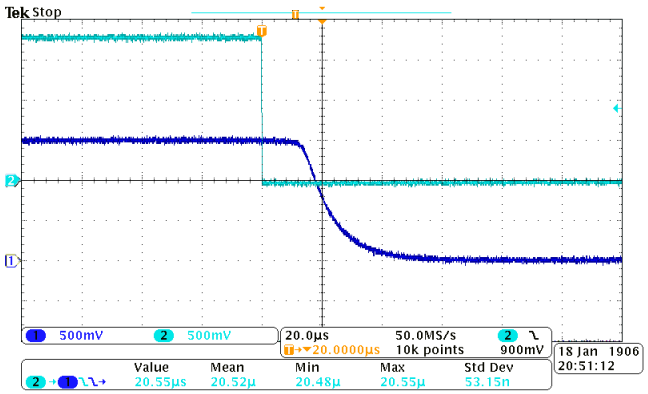
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 64. Turn-off Response Time



V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 65. Turn-on Response Time

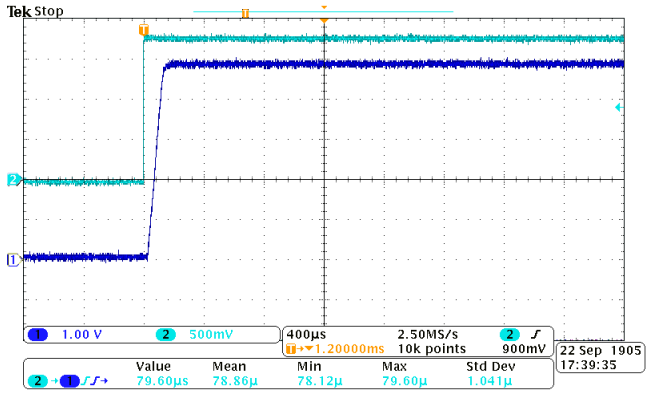


V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 66. Turn-off Response Time

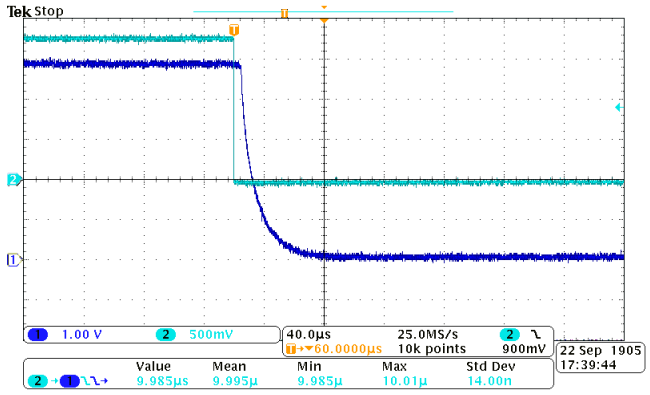
11.2.3.3 Typical Application Characteristics For TPS22913B

The dark blue curve (Channel 1) represents the VOUT pin of the device. The light blue curve (Channel 2) represents the ON pin of the device.



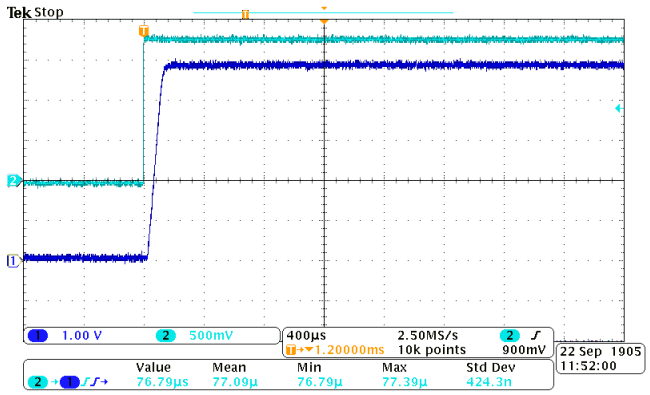
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 67. Turn-on Response



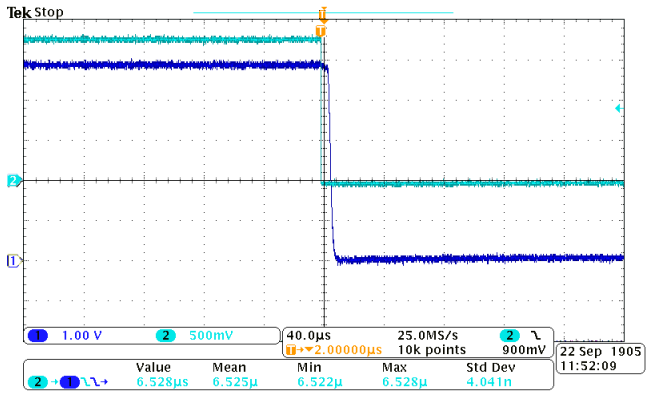
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 68. Turn-off Response



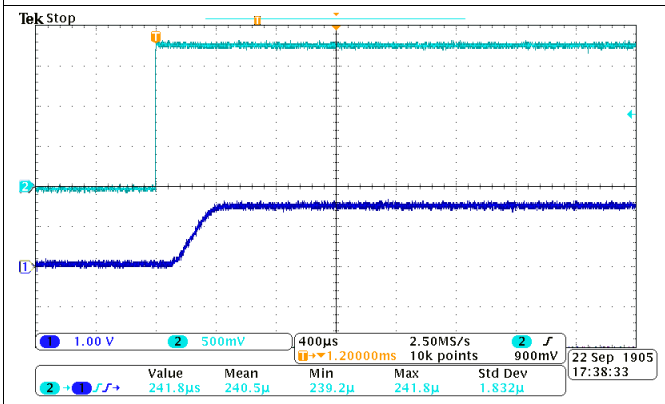
V_{IN} = 5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 69. Turn-on Response Time



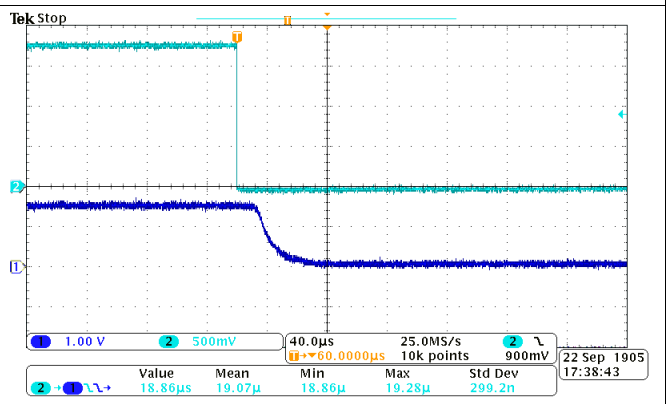
V_{IN} = 5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 70. Turn-off Response Time



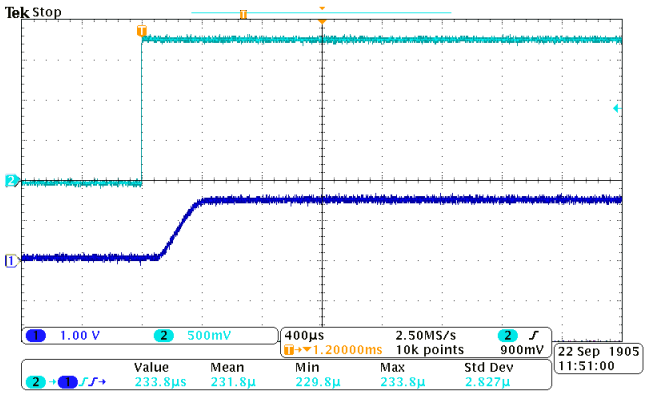
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 71. Turn-on Response Time



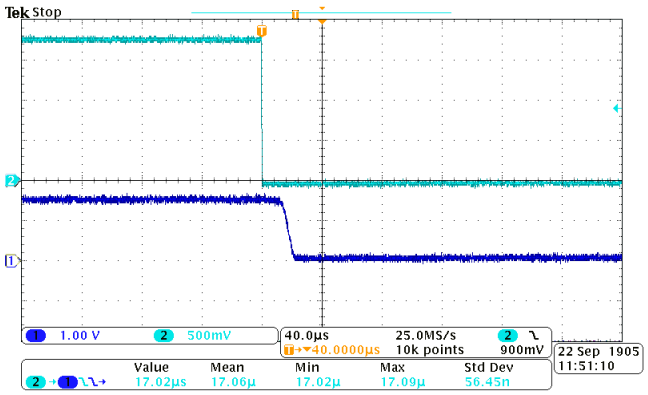
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 72. Turn-off Response Time



V_{IN} = 1.5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 73. Turn-on Response Time

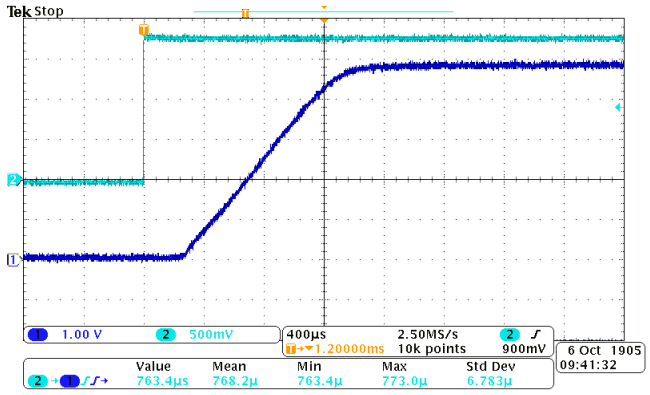


V_{IN} = 1.5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 74. Turn-off Response Time

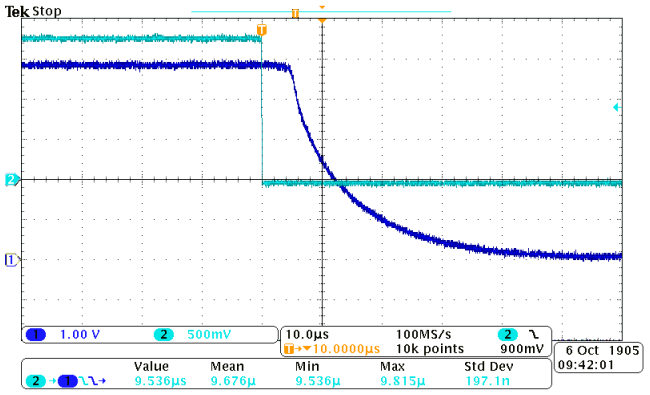
11.2.3.4 Typical Application Characteristics for TPS22913C

The dark blue curve (Channel 1) represents the VOUT pin of the device. The light blue curve (Channel 2) represents the ON pin of the device.



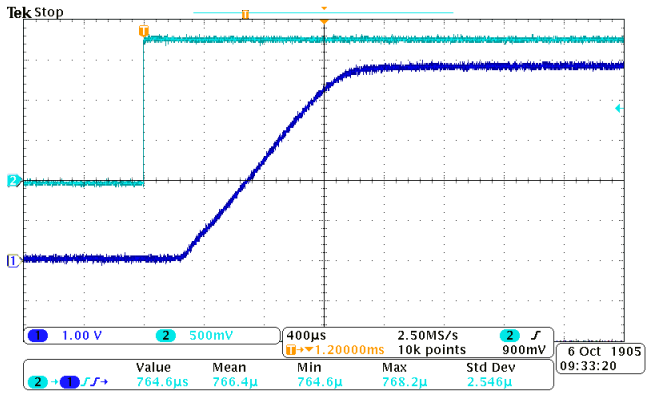
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 75. Turn-On Response Time



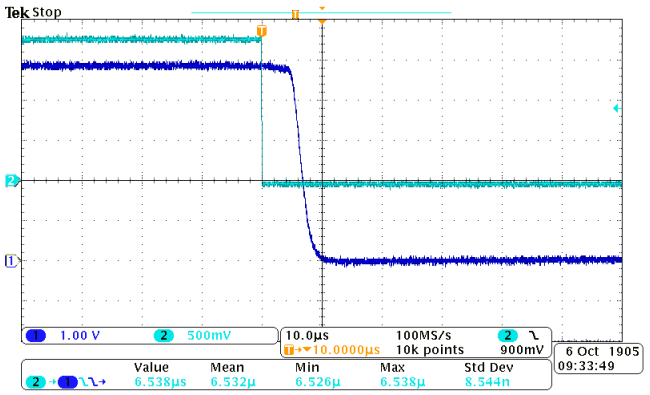
V_{IN} = 5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 76. Turn-Off Response Time



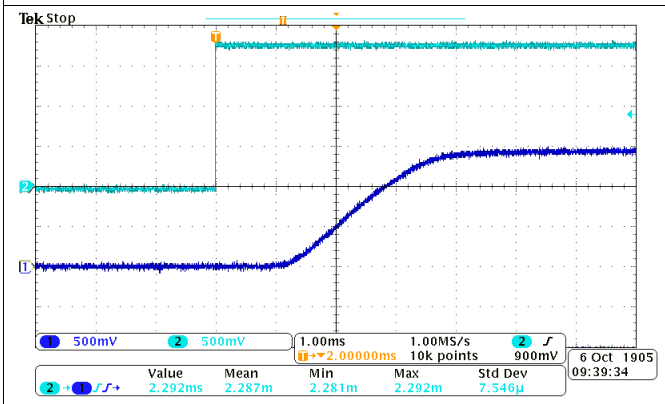
V_{IN} = 5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 77. Turn-On Response Time



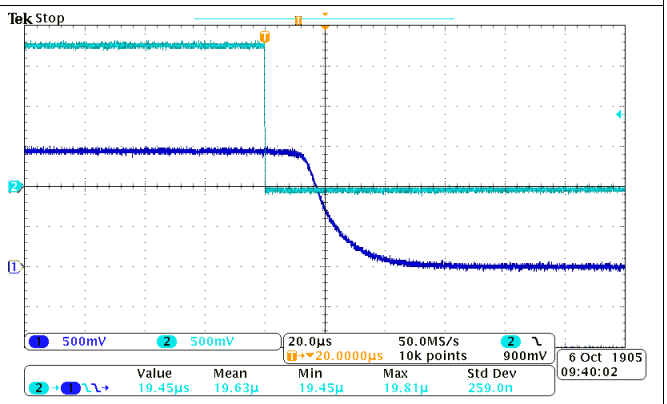
V_{IN} = 5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 78. Turn-Off Response Time



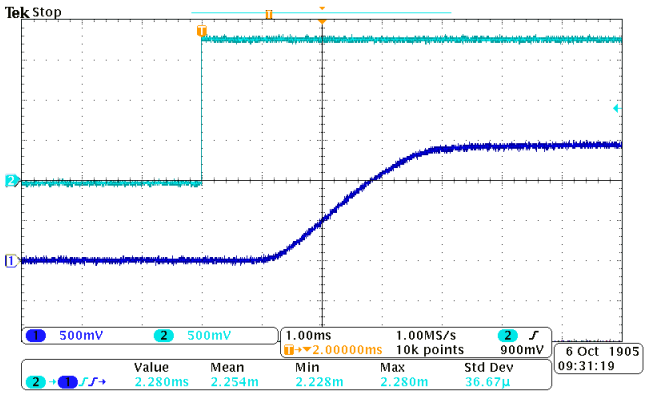
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 79. Turn-Off Response Time



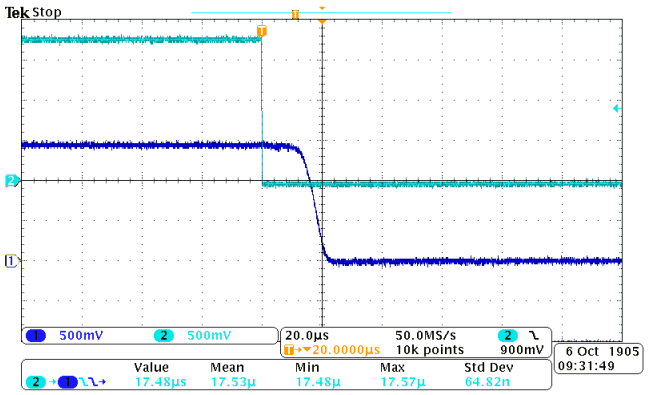
V_{IN} = 1.5 V T_A = 25°C C_{IN} = 10 µF
C_L = 1 µF R_L = 10 Ω

Figure 80. Turn-Off Response Time



V_{IN} = 1.5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 81. Turn-Off Response Time



V_{IN} = 1.5 V T_A = 25°C C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 82. Turn-Off Response Time

12 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.4 V to 5.5 V.

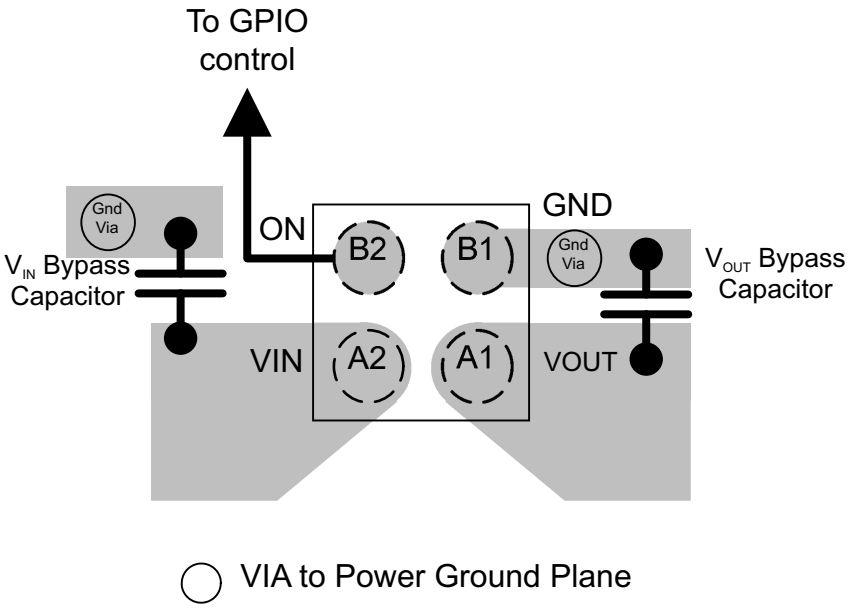
13 Layout

13.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

13.2 Layout Example

The figure below shows an example for these devices. Notice the connection to system ground between the V_{OUT} Bypass Capacitor ground and the GND pin of the load switch, this creates a ground barrier which helps to reduce the ground noise seen by the device.



13.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (5)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

14 Device and Documentation Support

14.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22910A	Click here	Click here	Click here	Click here	Click here
TPS22912C	Click here	Click here	Click here	Click here	Click here
TPS22913B	Click here	Click here	Click here	Click here	Click here
TPS22913C	Click here	Click here	Click here	Click here	Click here

14.2 Trademarks

Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

14.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22910AYZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	75	Samples
TPS22910AYZVT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	75	Samples
TPS22912CYZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78	Samples
TPS22912CYZVT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	78	Samples
TPS22913BYZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	64	Samples
TPS22913BYZVT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	64	Samples
TPS22913CYZVR	ACTIVE	DSBGA	YZV	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	76	Samples
TPS22913CYZVT	ACTIVE	DSBGA	YZV	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	76	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

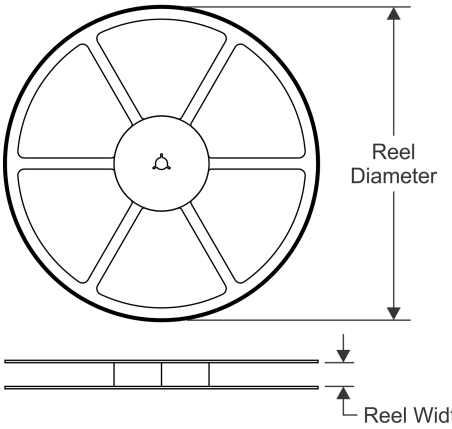
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

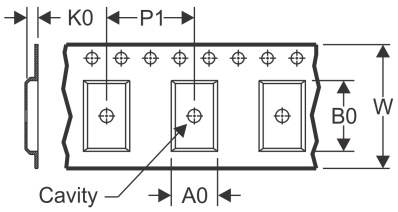
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

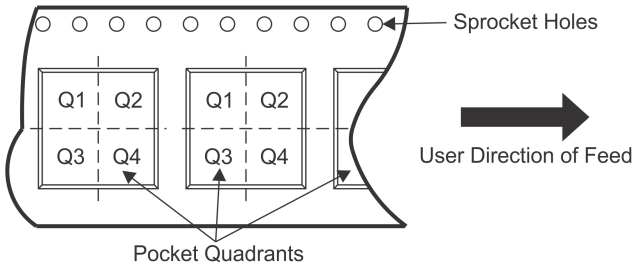


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

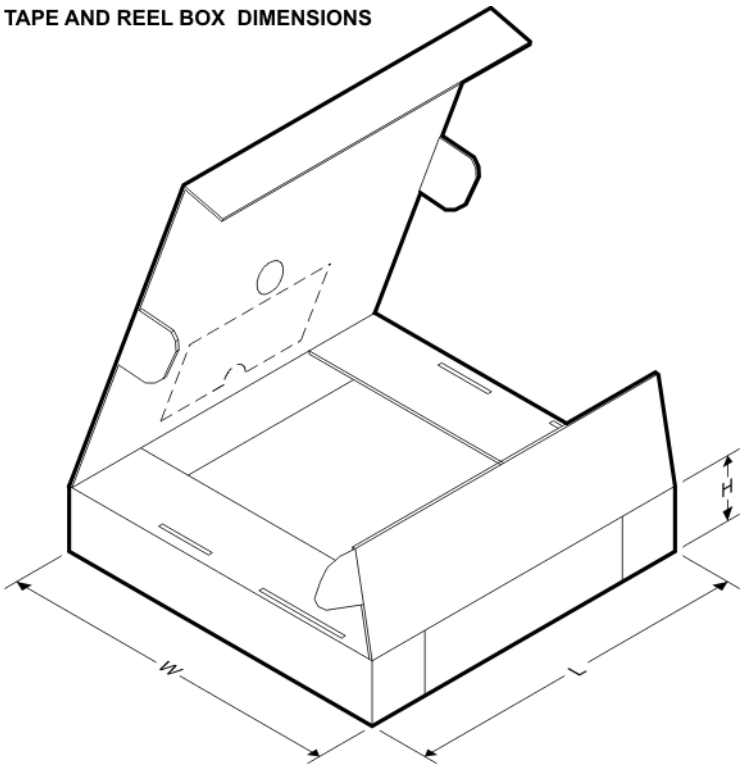
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22910AYZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22910AYZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22912CYZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22912CYZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22913BYZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22913BYZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1
TPS22913BYZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22913CYZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22913CYZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1
TPS22913CYZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

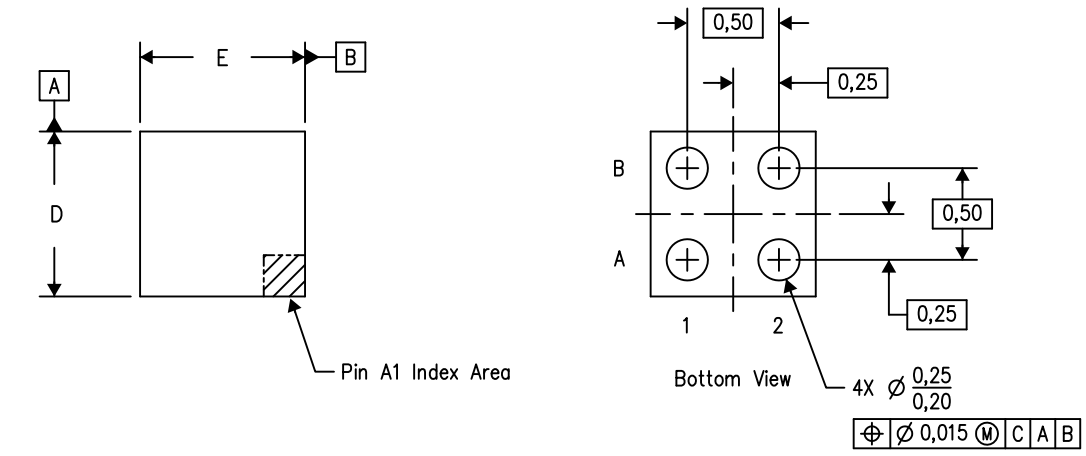
TAPE AND REEL BOX DIMENSIONS

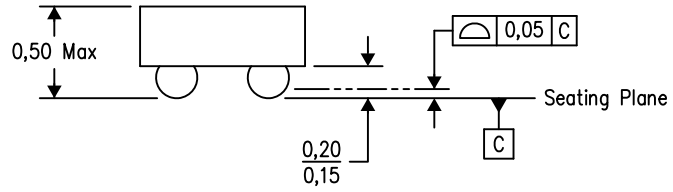


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22910AYZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22910AYZVT	DSBGA	YZV	4	250	220.0	220.0	35.0
TPS22912CYZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22912CYZVT	DSBGA	YZV	4	250	220.0	220.0	35.0
TPS22913BYZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22913BYZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0
TPS22913BYZVT	DSBGA	YZV	4	250	220.0	220.0	35.0
TPS22913CYZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22913CYZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0
TPS22913CYZVT	DSBGA	YZV	4	250	220.0	220.0	35.0

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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