# 74HC05

# Hex inverter with open-drain outputs

Rev. 3 — 8 July 2020

**Product data sheet** 

# 1. General description

The 74HC05 contains six inverters. The outputs of the 74HC05 are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. The open-drain outputs require pull-up resistors to perform correctly.

# 2. Features and benefits

- Wide operating voltage 2.0 V to 6.0 V
- CMOS input levels
- · Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- · Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

# 3. Ordering information

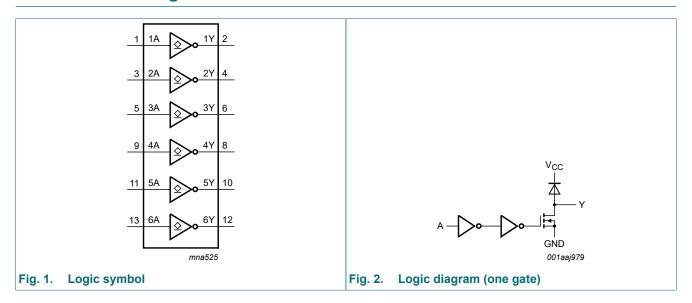
#### **Table 1. Ordering information**

Type number	Package									
	Temperature range	Name	Description	Version						
74HC05D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1						
74HC05PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1						
74HC05BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1						



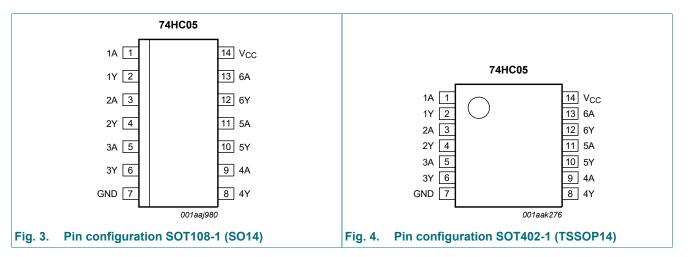
Hex inverter with open-drain outputs

# 4. Functional diagram



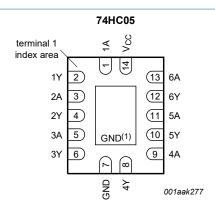
# 5. Pinning information

# 5.1. Pinning



2/13

### Hex inverter with open-drain outputs



Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

# 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	data input
1Y to 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

# 6. Functional description

#### Table 3. Function table

 $H = HIGH \text{ voltage level}; L = LOW \text{ voltage level}; Z = high-impedance OFF-state.}$ 

Input	Output
nA	nY
L	Z
Н	L

**Product data sheet** 

#### Hex inverter with open-drain outputs

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_I < -0.5 \text{ V or } V_I > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Vo	output voltage	[1]	-0.5	V <sub>CC</sub> + 0.5 V	V
Io	output current	V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	25	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	[2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V

<sup>[2]</sup> For SOT108-1 (SO14) package: P<sub>tot</sub> derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P<sub>tot</sub> derates linearly with 7.3 mW/K above 81 °C. For SOT762-1 (DHVQFN14) package: P<sub>tot</sub> derates linearly with 9.6 mW/K above 98 °C.

Hex inverter with open-drain outputs

# 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_{O}$ = 20 $\mu$ A; $V_{CC}$ = 4.5 $V$	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		$I_{O}$ = 4.0 mA; $V_{CC}$ = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{O}$ = 5.2 mA; $V_{CC}$ = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.5	-	±5.0	-	±10	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μA
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

Hex inverter with open-drain outputs

# 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

GND = 0 V; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C to	+125 °C	Unit
			Min	Тур	Max	Max (85 °C)	Max (125 °C)	
$t_{PLZ}$	LOW to OFF-state	nA to nY; see Fig. 6						
	propagation delay	V <sub>CC</sub> = 2.0 V	-	20	90	115	135	ns
		V <sub>CC</sub> = 4.5 V	-	11	18	23	27	ns
		V <sub>CC</sub> = 6.0 V	-	10	15	20	23	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nA to nY; see Fig. 6						
		V <sub>CC</sub> = 2.0 V	-	22	90	115	135	ns
		V <sub>CC</sub> = 4.5 V	-	9	18	23	27	ns
		V <sub>CC</sub> = 6.0 V	-	8	15	20	23	ns
t <sub>THL</sub>	HIGH to LOW	see Fig. 6						
	output transition	V <sub>CC</sub> = 2.0 V	-	18	75	95	110	ns
	time	V <sub>CC</sub> = 4.5 V	-	6	15	19	22	ns
		V <sub>CC</sub> = 6.0 V	-	5	13	16	19	ns
C <sub>PD</sub>	power dissipation capacitance	per inverter; $V_I$ = GND to $V_{CC}$ ; [1] $V_{CC}$ = 5.0 V	-	4	-	-	-	pF

<sup>[1]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (0.5 \times C_L \times V_O^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

 $f_o$  = output frequency in MHz;

V<sub>O</sub> = output voltage in V (output HIGH);

V<sub>CC</sub> = supply voltage in V;

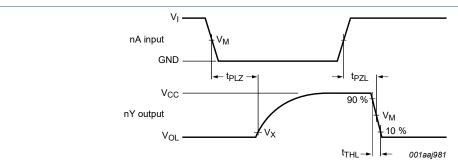
N = number of inputs switching;

 $R_L$  = load resistance in  $M\Omega$ ;

C<sub>L</sub> = load capacitance in pF;

#### Hex inverter with open-drain outputs

### 10.1. Waveforms and test circuit



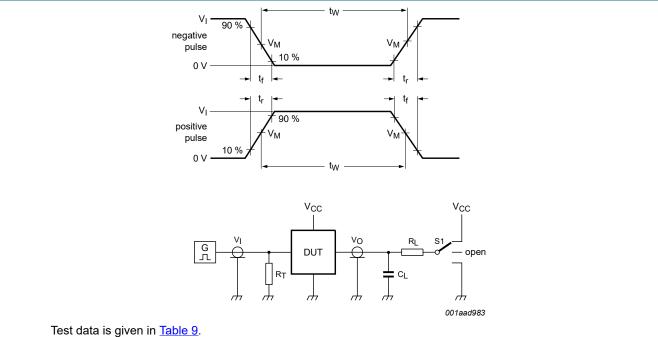
Measurement points are given in Table 8.

 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 6. The input nA to output nY propagation delays and output transition times

**Table 8. Measurement points** 

Input	Output	
V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>
0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	0.1V <sub>CC</sub>



Definitions test circuit:

 $R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

Test circuit for measuring switching times Fig. 7.

Table 9. Test data

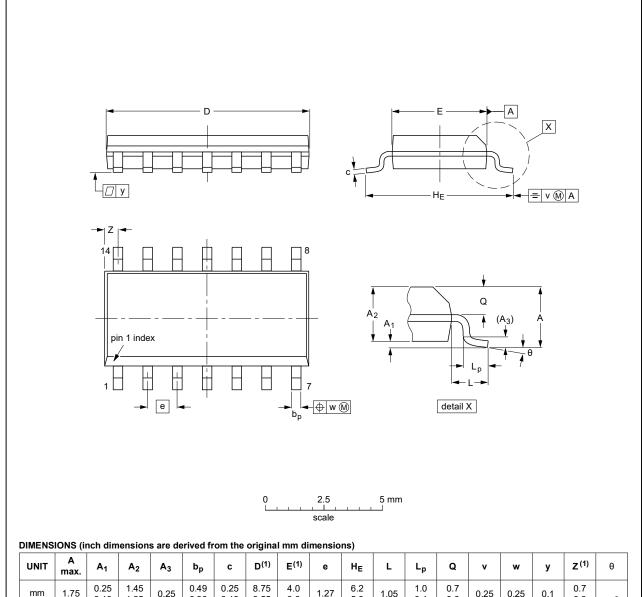
Input		Load	S1 position	
$V_l$ $t_r$ , $t_f$		CL	R <sub>L</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
V <sub>CC</sub>	6 ns	50 pF	1 kΩ	V <sub>CC</sub>

# Hex inverter with open-drain outputs

# 11. Package outline

### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

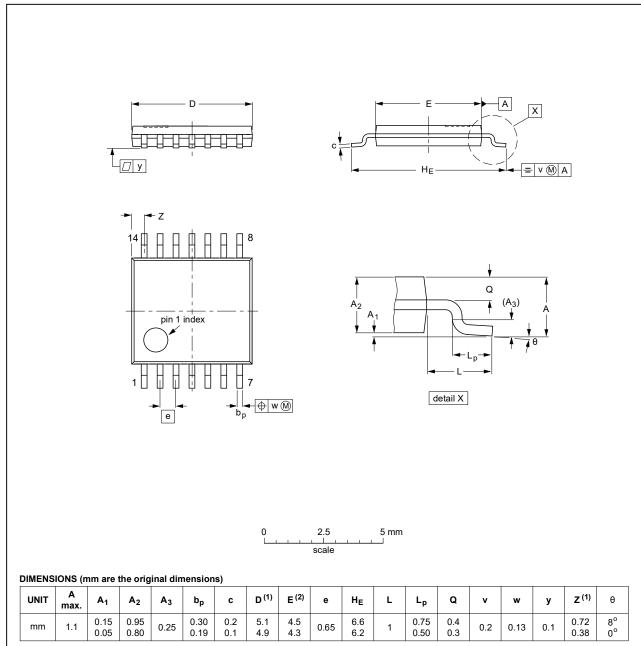
(	OUTLINE		REFER	EUROPEAN	ISSUE DATE		
	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
	SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig. 8. Package outline SOT108-1 (SO14)

### Hex inverter with open-drain outputs

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE			
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT402-1		MO-153				<del>99-12-27</del> 03-02-18	

Fig. 9. Package outline SOT402-1 (TSSOP14)

#### Hex inverter with open-drain outputs

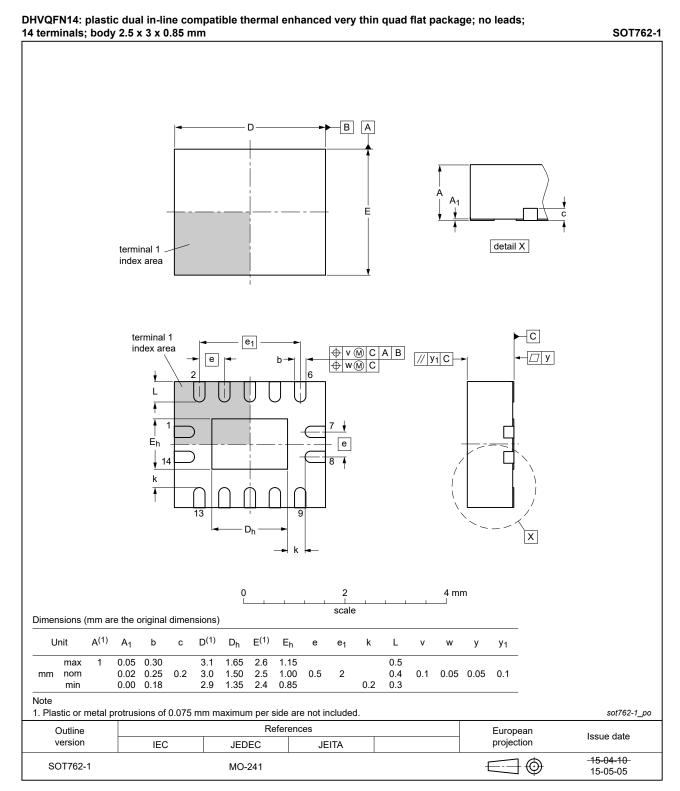


Fig. 10. Package outline SOT762-1 (DHVQFN14)

# Hex inverter with open-drain outputs

# 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC05 v.3	20200708	Product data sheet	-	74HC05 v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 1 and Section 2 updated.</li> <li>Table 4: Derating values for P<sub>tot</sub> total power dissipation have been updated.</li> <li>Table 6: Conditions for I<sub>OZ</sub> corrected.</li> <li>Package outline drawing of SOT762-1 (Fig. 10) updated.</li> </ul>				
74HC05 v.2	20090618	Product data sheet	-	74HC05 v.1	
Modifications:	Added type numbers 74HC05PW (TSSOP14 package) and 74HC05BQ (DHVQFN14 package)				
74HC05 v.1	20090427	Product data sheet	-	-	

# Hex inverter with open-drain outputs

# 14. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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# Hex inverter with open-drain outputs

# **Contents**

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	2
5.1. Pinning	2
5.2. Pin description	3
6. Functional description	3
7. Limiting values	4
8. Recommended operating conditions	4
9. Static characteristics	5
10. Dynamic characteristics	6
10.1. Waveforms and test circuit	7
11. Package outline	8
12. Abbreviations	11
13. Revision history	11
14. Legal information	12

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