MP1039

Full Bridge CCFL Controller

The Future of Analog IC Technology

DESCRIPTION

The MP1039 is a fixed operating frequency inverter controller that controls four external N-Channel power MOSFETs in a full-bridge configuration. The inverter is designed to power one or more cold cathode fluorescent lamps (CCFL) to backlight liquid crystal displays. Its full-bridge architecture converts unregulated DC input voltages to the nearly pure sine waves required to ignite and operate CCFL.

The switching frequency is set by an external resistor, and can be synchronized to an external clock to minimize the potential video display interference. The built-in burst oscillator can be synchronized with an external clock to minimize display scan interference. Burst mode or analog mode dimming is controlled with an external analog signal. Built-in fault management features include an open lamp regulator, a transformer secondary peak current regulator, and a dual-mode fault timer. The secondary over-current timeout can be shortened with external components. The MP1039 is available in TSSOP28 and SOIC28 packages.

FEATURES

- Drives Four External, Low Cost, N-Channel MOSFETs
- Programmable Fixed Operating Frequency
- Input Voltage Range of 10V to 28V
- Lamp Current and Voltage Regulation
- Full-Wave Sense Amp
- Analog and Burst Mode Dimming Control
- Integrated Burst Mode Oscillator and Modulator
- Soft-On and Soft-Off Burst Envelope
- Open Lamp Protection
- Secondary Over-Current Protection
- Dual-mode, Fault Timer
- Drives up to 20 Lamps
- Synchronization Ability for both Switching Frequency and Burst Frequency
- Available in TSSOP28 and SOIC28 Packages

APPLICATIONS

- Desktop LCD Flat Panel Displays
- Flat Panel Video Displays
- LCD TVs and Monitors

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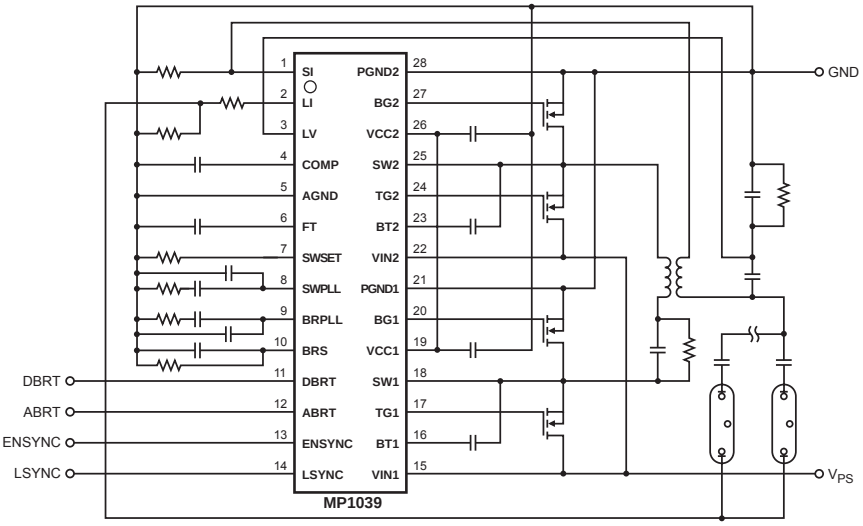
The MP1039 is covered by US Patents 6,683,422, 6,316,881, and 6,114,814. Other Patents Pending.

TYPICAL APPLICATION



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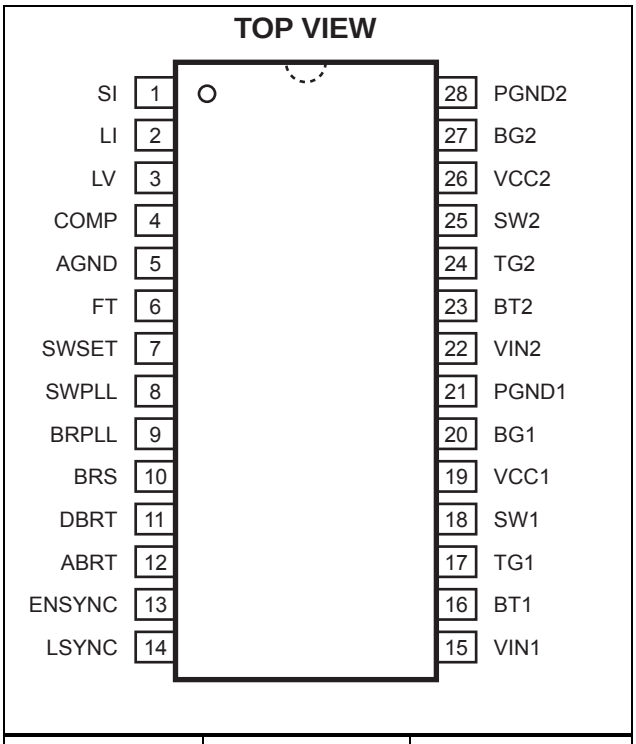
PACKAGE REFERENCE



Part Number*	Package	Temperature
MP1039EM	TSSOP28	–20°C to +85°C
MP1039EY	SOIC28	–20°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP1039EM–Z)
For RoHS compliant packaging, add suffix –LF
(eg. MP1039EM–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage $V_{IN2,}$ V_{IN1} 30V
Logic Inputs ..... –0.3V to +6.5V
Inputs SI, LI, LV ..... –3V to +3V
Junction Temperature ..... 150°C
Power Dissipation 0.6W
Junction Temperature ..... 150°C
Lead Temperature (Solder) ..... 260°C
Operating Frequency 150KHz
Storage Temperature ..... –55°C to +150°C

Recommended Operating Conditions (2)

Input Voltage $V_{IN1,}$ V_{IN2} ..... 10V to 28V
Analog Brightness Voltage V_{ABRT} ..... 0V to 1.2V
Digital Brightness Voltage V_{DBRT} ..... 0V to 1.2V
Enable Voltage V_{ENSYNC} ..... 0V to 5.0V
Operating Frequency ..... 20KHz to 100KHz
Operating Frequency (Typical) 47KHz
Operating Temperature ..... –20°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP28	82	20	°C/W
SOIC28	60	30	°C/W

Notes:
1) The device is not guaranteed to function outside of its operating conditions.
2) Exceeding these ratings may damage the device.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 17.5V, V_{BRPLL} = V_{SWPLL} = GND, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output						
Gate Pull-Down	R_{GD}			2		Ω
Gate Pull-Up	R_{GU}			9		Ω
Damper On Resistance	R_{ON}			1.0		kΩ
ENSYNC						
Threshold	V_{TH}			1.35	2.0	V
Hysteresis	V_{TH_HYS}			0.3		V
Sync Timing for Burst Oscillator						
Sync Minimum Pulse Width	$t_{SYNC(MIN)}$			1		µs
Sync Maximum Pulse Width	$t_{SYNC(MAX)}$			10		µs
Sync Rate	f_{SYNC}			200		Hz
DBRT Logic Input Threshold	V_{TH}	V_{BRS} = V_{CC}	1.8	2.1	2.3	V
DBRT Logic Input Hysteresis	V_{TH_HYS}	V_{BRS} = V_{CC}		0.4		V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = 17.5V, V_{BRPLL} = V_{SWPLL} = GND, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Lamp Frequency Sync						
LSYNC Min Pulse Width	$t_{LSYNC(MIN)}$			20		ns
LSYNC Rate (4)	f_{LSYNC}	R3 = 100kΩ		60	120	KHz
LSYNC Pulse Amplitude	V_{LSYNC}		2.5			V
Brightness Control Range						
DBRT Full Brightness	$V_{DBRT, FULL}$			0.135		V
DBRT 10% Brightness	$V_{DBRT, 10\%}$			1.34		V
ABRT Full Scale	V_{ABRT}			1.2		V
Burst Rate Generator						
Source Current	$I_{SRC(BRS)}$	V_{BRS} = 2V	120	150	180	µA
Lower Threshold	$V_{V(BRS)}$		2.2	2.35	2.5	V
Upper Threshold	$V_{P(BRS)}$		3.3	3.5	3.7	V
Supply Current						
Supply Current (Enabled)	I_{VIN}			1.7	3	mA
Supply Current (Disabled)	I_{VIN}			1	20	µA
Operating Frequency	f_0	R3 = 100kΩ		47		KHz
Accuracy of f_0				3		%
Control Input Current	I_{SWPLL}			–8		µA
Frequency Set Voltage	V_{SWSET}		1.10	1.2	1.30	V
Lamp Current Feedback						
Magnitude	$\|V_{LI}\|$	V_{ABRT} > 1.2V	1.18	1.25	1.32	V
		V_{ABRT} = 0V		0.41		V
Sine Equivalent	V_{LI}	V_{ABRT} > 1.2V		1.33		Vrms
Accuracy	V_{LI}			3		%
Input Resistance		V_{LI} < 0V		62		kΩ
Open Lamp Voltage Feedback Threshold (Peak)	$V_{TH(LV)}$		1.16	1.21	1.26	V
Secondary Peak Current Threshold	$V_{TH(SI)}$		1.16	1.21	1.26	V
Fault Timer						
Threshold	$V_{t(FT)}$		1.16	1.21	1.26	V
Sink Current	$I_{SINK(FT)}$			–1		µA
Open Lamp Source Current	$I_{SO(FT)+}$			1		µA
Secondary Over-Current Source Current	$I_{SP(FT)+}$			70		µA
Comp						
Clamp Voltage	V_{COMP}			0.56		V
Reference Current	I_{COMP+}			20		µA
Decay Current	I_{COMP-}	End of Burst		60		µA
Output (VCC1 and VCC2)						
Voltage	V_{CC}		5.5	6.0	6.5	V
Current	I_{CC}			5		mA

Note:

4) Guaranteed by design, not tested.

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PIN FUNCTIONS

Pin #	Name	Description
1	SI	Secondary Current Feedback Input. Connect a current sense resistor from the cold end of the secondary winding to ground. Connect this pin to the junction of the resistor and the secondary winding. If the voltage at SI exceeds +1.2V, a pulse of current will pull down on the COMP pin to attempt to regulate the secondary current and the Fault Timer will be started.
2	LI	Lamp Current Feedback Input. Connect this pin to the cold end of the lamp and shunt a sense resistor to ground. The sense amplifier will sink a current from the COMP pin proportional to the absolute value of the voltage at this pin. (In regulation the average of the absolute value of the voltage at this pin is determined by the voltage at the ABRT pin). A 470Ω resistor placed in series with this pin will improve ESD protection.
3	LV	Lamp Voltage Feedback Input. Connect a capacitive voltage divider from the hot end of the lamp to ground. Connect this pin to the tap on the divider and shunt a bias resistor to ground. If the voltage at LV exceeds +1.2 V, a pulse of current will pull down on the COMP pin to attempt to regulate the lamp voltage and the Fault Timer will be started.
4	COMP	Feed back Compensation Node. Connect a compensation capacitor from this pin to ground.
5	AGND	Analog Ground.
6	FT	Fault Timing. Connect a timing capacitor from this pin to AGND to set the fault timeout period.
7	SWSET	Switching Frequency Set. Connect a resistor from this pin to AGND. This resistor sets the operating frequency of the MP1039.
8	SWPLL	Switching Frequency Phase Lock Loop. SWPLL provides compensation when the operating clock is synchronized to an external clock. Connect a resistor in series with a capacitor from SWPLL to AGND. Connect a smaller capacitor directly from SWPLL to AGND. Connect only a single capacitor to AGND, if some sweeping of the operating clock can be tolerated during open lamp conditions. Connect SWPLL to AGND to force the operating clock to the selected value at all times.
9	BRPLL	Burst Frequency Phase Lock Loop. BRPLL provides compensation when the burst frequency is to be synchronized to an external clock. Connect a resistor in series with a capacitor from BRPLL to AGND. Connect a smaller capacitor directly from BRPLL to AGND. If the burst frequency is not to be synchronized to an external clock, connect BRPLL to AGND.
10	BRS	Burst Frequency Setting. If the burst frequency is to be synchronized to an external clock, connect a capacitor from BRS to AGND. If the burst rate generator is free-run and not be synchronized with an external clock, connect a resistor in parallel with a capacitor from BRS to AGND. If the burst is to be controlled by an external logic signal, connect BRS to VCC and apply the logic signal to the DBRT pin.
11	DBRT	Burst-Mode (Digital) Brightness Control Input. The voltage range of 0.12V to 1.34V at DBRT linearly sets the burst-mode duty cycle from 100% to 10%. If burst dimming is not used tie DBRT to GND. The MP1039 has negative dimming polarity on DBRT.
12	ABRT	Analog Brightness Control Input. The voltage range of 0V to 1.2V at ABRT sets 3:1 dimming range for the lamp current. If analog dimming is not used, tie ABRT to VCC.
13	ENSYNC	Enable and Sync Composite Input. Pull ENSYNC high to turn on the MP1039, pull ENSYNC low to turn it off. To synchronize the burst frequency to an external clock, apply the synchronizing clock signal with low-going pulse width of 1-10μs to this pin. Once the MP1039 has aligned the burst oscillator to the sync signal, each burst will start at the low-going edge of the sync pulse.
14	LSYNC	Lamp Frequency Synchronization Input. The synchronization clock must be greater than the frequency f_O set by the SWSET pin, but no greater than 1.4 times the value of f_O.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
15	VIN1	Input Power Rail, Side 1. Connect VIN1 directly to the drain of the side 1, top power MOSFET.
16	BT1	Output Bootstrap, Side 1. BT1 provides gate bias for the side 1 top MOSFET. Connect a capacitor from BT1 to SW1.
17	TG1	Top MOSFET Gate Output, Side 1.
18	SW1	Source of Top MOSFET, Side 1. Connect SW1 to the source of the side 1 top MOSFET and the drain of the side 1 bottom MOSFET.
19	VCC1	Linear Regulator Output and Bias Supply of Bottom Gate Driver, Side 1. VCC1 allows bypassing the bias supply for the control circuitry. Bypass VCC1 with a 1μF or larger ceramic capacitor. Connect to VCC2.
20	BG1	Bottom MOSFET Gate Output, Side 1.
21	PGND1	Power Ground, Side 1. Connect PGND1 to the source of the bottom, side 1 MOSFET.
22	VIN2	Input Power Rail, Side 2. Connect VIN2 directly to the drain of the top, side 2, external power MOSFET.
23	BT2	Output Bootstrap, Side 2. BT2 provides gate bias for the side 2 top MOSFET. Connect a capacitor from BT2 to SW2.
24	TG2	Top MOSFET Gate Output, Side 2.
25	SW2	Source of Top MOSFET, Side 2. Connect SW2 to the source of the side 2, top MOSFET and the drain of the side 2, bottom MOSFET.
26	VCC2	Voltage Rail Output, Side 2. VCC2 allows bypassing the bias supply for the control circuitry. Bypass VCC2 with a 1μF or larger ceramic capacitor. Connect to VCC1. It is an input pin.
27	BG2	Bottom MOSFET Gate Output, Side 2.
28	PGND2	Power Ground, Side 2. Connect PGND2 to the source of the bottom, side 2 MOSFET.

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OPERATION

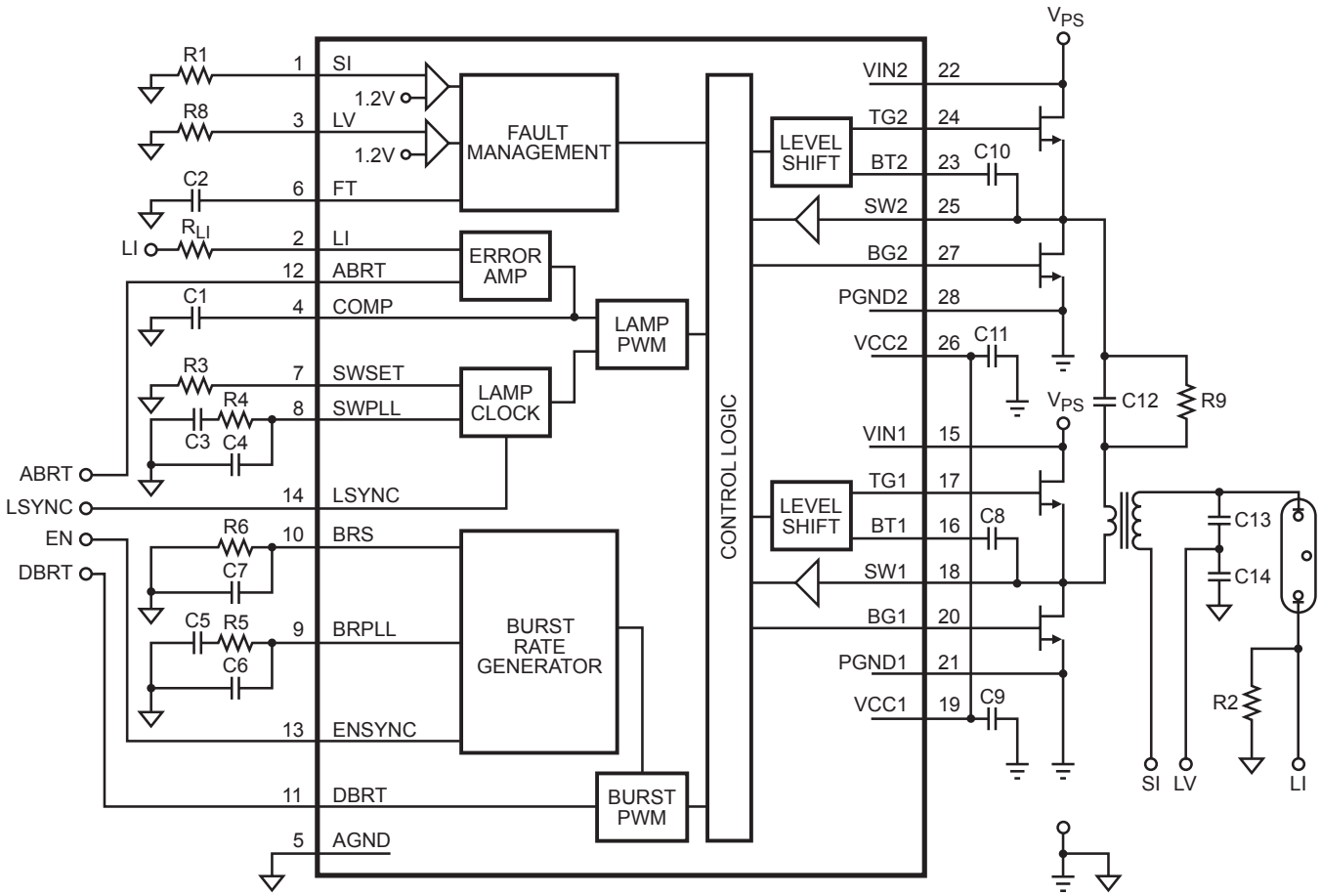

Figure 1—MP1039 Block Diagram

DESIGN INFORMATION

The MP1039 is a fixed operating frequency inverter controller specifically designed to drive a cold cathode fluorescent lamp (CCFL) used as a backlight for liquid crystal displays. Designed to run off 10V to 28V input supplies, the MP1039 can drive up to 20 lamps (140W) via four (4) external N-Channel MOSFETs. Its full bridge architecture converts unregulated DC input voltages to the nearly pure sine waves required to ignite and operate CCFLs. The Operating frequency is set by an external resistor to minimize the possibility of interference with the refresh rate of the display.

Regulated lamp current and maximum peak transformer secondary current are set by external resistors. Regulated open lamp voltage is set by an external capacitive voltage divider.

The MP1039 implements burst mode dimming of the lamp and features soft-on-soft-off control of the lamp current envelope that is virtually independent of supply voltage.

Burst frequency and duty cycle can either be determined by driving the MP1039 with an external logic signal or by choosing an external resistor and capacitor to set the burst rate and modulating the duty cycle with a DC control voltage on DBRT.

Loop gain is compensated for variations in supply voltage and the full-wave lamp current sense amplifier provides superior output pulse symmetry, loop response time, and phase margin.

The switching frequency of the MP1039 is set by an external resistor. This frequency can be synchronized to the input clock signal at the LSYNC pin.

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Careful management of limit conditions provides graceful reduction of lamp power at low supply voltages but allows the loop to recover quickly from an abrupt step in supply voltage. System fault management facilities include an on-chip open-lamp regulator, a transformer secondary peak current regulator, and a dual-mode fault timer.

By regulating the peak current in the transformer secondary winding, UL60950 can be met for most systems. When the MP1039 is regulating open lamp voltage, it ignores the burst control and runs continuously to ensure either the lamp has a chance to re-ignite or the fault timer can smoothly and accurately time out. If the MP1039 detects an open lamp condition for a time that exceeds the timer interval, it will shut down until the part is turned off and then turned on again. Similarly, the MP1039 will shut down if it detects an over-current condition in the secondary for about 2% of the open lamp timer interval. If required, the secondary over-current timeout can be shortened with external components.

FEATURE DESCRIPTION

All reference designators refer to Figure 1, unless otherwise designated.

High Efficiency Operation

There are two major power losses in a CCFL inverter: switching loss of switches and copper loss of the transformer winding. To reduce switching loss, Zero Current Switching (ZCS as described in US patent 6,114,814) or Zero Voltage Switching (ZVS) are commonly implemented.

As shown in Figure 2, ZCS and ZVS require primary current I_{PRI} lagging primary voltage V_{PRI}. With ZVS, since D1 can only conduct at the negative phase of I_{PRI}, the beginning of A & D conduction will only happen at the negative phase of I_{PRI}.

Higher phase delay will lead to higher primary RMS current and therefore higher transformer temperature. With ZCS, A & D conduction starts at the zero crossing of I_{PRI}.

The MP1039 does not utilize ZVS or ZCS. It implements fast switching to reduce switching loss and operates at the condition that I_{PRI} and V_{PRI} are in phase to reduce primary RMS current. Therefore, higher efficiency than ZVS or ZCS is achieved.

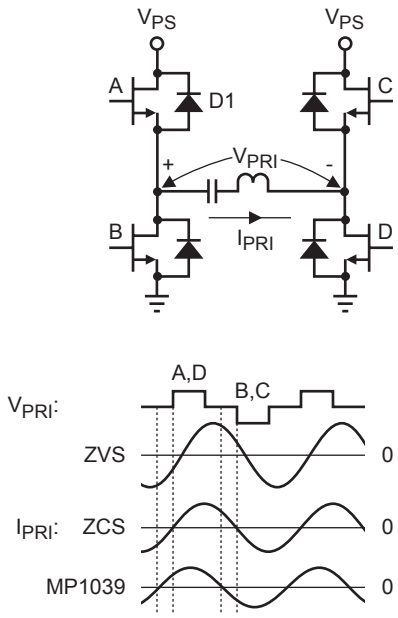

Figure 2—V_{PRI} vs. I_{PRI}

Brightness Control

The MP1039 can operate in four modes: Analog Mode, Burst Mode with a DC input, Burst Mode with an external PWM or Analog and Burst Mode. The four modes are dependent on the pin connections defined under Pin Functions.

Choosing the required burst repetition frequency can be achieved by an RC combination, as defined in component selection. The MP1039 has a soft-on and soft-off feature to reduce noise, when using burst mode dimming. Analog dimming and Burst dimming are independent of each other and may be used together to obtain a wider dimming range.

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Table 1—Function Mode

Function	Pin Connection			
	ABRT	DBRT	BRS	Ratio
Analog Mode	0 – 1.2V	GND	R6 C7	3:1
Burst Mode with DC Input Voltage	V_{CC}	0 – 1.4V	R6 C7	10:1
Burst Mode with External Source	V_{CC}	PWM	V_{CC}	Set by Customer
Analog and Burst Mode	0 – 1.2V	0 – 1.4V	R6 C7	30:1
Analog and Burst Mode with External Source	0 – 1.2V	PWM	V_{CC}	Set by Customer

Brightness Polarity
Burst: 100% duty cycle is at 0V
Analog: 1.2V is maximum brightness

Fault Protection
Open Lamp: The LV pin (#3) is used to detect whether an open lamp condition has occurred. If the voltage at LV exceeds +1.2V, a pulse of current will pull down on the COMP pin to regulate the lamp voltage. The Fault Timer will be started with a 1μA current source injecting into C2 at the FT pin, while the fault condition persists. If the voltage at the FT pin exceeds 1.2V, then the chip will shut down.

Excessive Secondary Current (Shorted Lamp): The SI pin (#1) is used to detect whether excessive secondary current has occurred. If a fault condition occurs that increases the secondary current, then the voltage at SI will be greater than 1.2V. A pulse of current will pull down on the COMP pin to regulate the secondary current. The Fault Timer will be started with a 55μA current source injecting into C2 at the FT pin, while the fault condition persists.

If the voltage at the FT pin exceeds 1.2V, then the chip will shut down and needs to be re-enabled.

Fault Timer: The timing for the fault timer will depend on the sourcing current, as described above, and the capacitor C2 on the FT pin. The user can program the time for the voltage to rise after the chip detects a “real“ fault. When a fault is triggered, then the internal voltage (V_{CC}) will collapse from 6V to 0V. If no fault is detected a 1μA current sink will keep FT to 0V.

Chip Enable
The chip has an ON/OFF function, which is controlled by the ENSYNC pin (#13). The enable signal goes directly to a Schmitt trigger. The chip will turn ON with an ENSYNC = High and OFF with an ENSYNC = Low.

The Burst waveform can be synchronized to an external reference clock. To do this, remove R6 and combine a low-going synchronization signal with the enable signal at the ENSYNC pin. The synchronizing pulses should be 1μs - 10μs wide and should occur at the desired burst repetition frequency.

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APPLICATION INFORMATION

Pin 1 (SI), R1:

Secondary Short Protection: The R1 is used for feedback to the SI pin to detect excessive secondary current. The value for R1 is calculated as 1.2V divided by the secondary peak current.

Pin 2 (LV): C13, C14 and R8:

Open Lamp protection: The regulated open lamp voltage is proportional to the C14 and C13 ratio. C13 has to be rated at 3kV and is typically between 5pF to 22pF. The value of C14 is set by the customer to achieve the required open lamp voltage detection value.

$$C14 = C13 \times 1.18 \times V_{(MAX)}rms$$

The value of bias resistor R8 is typically 10kΩ to 100kΩ (not critical).

Pin 2 (LI), R2:

Lamp Current Regulation: R2 is used for feedback to the LI pin to regulate the lamp current. The value for R2 is calculated as 1.33V divided by the lamp rms current (assuming V_{ABRT} is greater than 1.2V). For RMS 6mA lamp current, R2 value is 220Ω.

Pin 6 (FT), C2:

The C2 is used to set the fault timer. This capacitor will determine when the chip will reach the fault threshold value.

Open Lamp Time Out:

$$C2\,(nF) = \frac{t_{OPEN\,LAMP} \times 1\mu A}{1.2V}$$

For a C2 = 820nF, then the time out for open lamp will be 0.98 sec.

Secondary Overcurrent Timeout: When the MP1039 is regulating secondary overcurrent (SI feedback), the source current in the Fault Timer (FT) cap is approximately 55µA. This causes the SI timeout to be about 1/55 of the Open Lamp (LV) timeout. To reduce the SI timeout further, modify the network at the FT pin as shown in Figure 3.

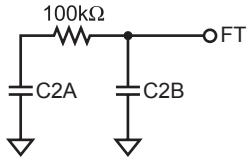

Figure 3—Timeout Adjustment

For C2B = 10nF, then the time out for secondary short will be 0.2ms.

Note: The open lamp time out will remain the same value as defined by C2A.

Pin 7 (SWSET), R3:

R3 is used to set the lamp operating clock. The value for R3 is calculated by

$$R3 = \frac{5e^9}{f_O}$$

For R3 = 100kΩ, operating clock will be 47KHz.

Pin 8 (SWPLL):

This is the lamp clock control compensation pin and needs a lag lead lag capacitor/resistor network.

Pin 9 (BRPLL):

This is the burst rate control compensation pin and needs a lag lead lag capacitor/resistor network.

Pin 4 (COMP), C1:

C1 is the feedback compensation capacitor that connects between COMP and AGND. A 1.5nF or 2.2nF cap is recommended. This cap should be X7R ceramic. The value of C1 affects the soft-on rise time and soft-off fall time.

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Pin 18 (SW1), Pin 25 (SW2), C12, R9:
SW1 and SW2 pins are used to sense the voltage at the output of the full bridge. They also are the point of access for the output dampers. SW1 and SW2 should make a Kelvin connection to the sources of the top MOSFETs and the drains of the bottom MOSFETs in the output bridge.

The primary transformer current flows through capacitor C12. Its value is typically 2.2µF. This capacitor should be ceramic and has a ripple current rating greater than the primary current. It is more optimal to use two parallel 1µF ceramic caps for minimal ESR losses. R9 is used to ensure that the bridge outputs are at 0V prior to startup. Typically R9 = 1kΩ.

Pin 16 (BT1), Pin 23 (BT2), C8, C10:
BT1 and BT2 are the bias supplies for the level shift of the upper MOSFETs. C8 and C10 should be 22nF and made of X7R ceramic material.

Pin 19 (VCC1), Pin 26 (VCC2), C9, C11:
These capacitors bypass the 6V gate supply for the bottom switches. They also supply power to the MP1039. These pins should be bypassed with a 0.47µF ceramic X7R capacitor.

Pin 13 (ENSYNC):
ENSYNC is a composite of the Enable and the Burst Oscillator Synchronization function. This pin will enable and disable the chip when the enable function is used.

To synchronize the Burst Oscillator to an external signal, remove R6 from BRS pin and apply a 1µs to 10µs pulse with a falling edge trigger and a repetition rate of 200Hz. The Burst Oscillator will then be synchronized with this signal and start a burst on its falling edge.

Pin 14 (LSYNC):
The lamp frequency can be externally synchronized by applying a signal to this pin.

The synchronization clock must be greater than the frequency f_0 set by the SWSET pin, but no greater than 1.4x the value of f_0.

Pin 11 (DBRT):
This pin is used for burst brightness control. The DC voltage on this pin will control the burst percentage on the output. The signal is filtered for optimal operation. A voltage ranging from 0 to 1.4V on DBRT will correspond to a Burst Duty Cycle of 100% to 10% respectively.

For direct Pulse Width Modulation of the burst signal, connect BRS to VCC and connect DBRT to a logic level PWM signal. Logic High is Burst On and a logic Low is Burst Off.

Pin 10 (BRS): C7, R6:
BRS is used to set the Burst frequency. C7 and R6 will set the burst frequency and the minimum burst time: $t_{MIN.}$ Set t_{MIN} to achieve the minimum required system

brightness. Ensure that t_{MIN} is long enough that the lamp does not extinguish.

These values are determined as follows:

Select a Minimum Duty Cycle, D_{MIN}, where:

$$D_{MIN} = t_{MIN} \times f_{Burst}$$

$$D_{MIN} = \frac{t_{FALL}}{(t_{FALL} + t_{RISE})}$$

If operating in Free-Running mode:

$$R6 = \frac{\frac{\left(\frac{1}{D_{MIN}} - 1\right)Vbg}{\xi} + \frac{V_P + V_V}{2}}{I_b}$$

$$R6 \sim 21.16k\left(\frac{1}{D_{MIN}} - 1\right) + 21.43k$$

For D_{MIN} = 0.1 and R6 = 212k

$$C7 = \frac{1 - D_{MIN}}{f_b \times R6 \times \gamma}$$

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For D_{MIN} = 0.1, R6 = 212k, f_b = 200Hz, then C7 = 52nf

D_{MIN} = Minimum Burst Duty Cycle

Vbg = V_P - V_V (~1.2V)

Vp = peak BRS voltage (~3.6V)

Vv = valley BRS voltage (~2.4V)

$$\gamma = \ln\left(\frac{3.6}{2.4}\right) \approx 0.405$$

Ib = BRS sink current (~150µA)

fb = burst frequency

If operating in Synchronous mode:

$$C7 = \frac{I_b \times t_{MIN}}{Vbg}$$

t_{MIN} = Minimum Burst Time

ESD Resistor

It is recommended that a resistor (R_{LI}=470Ω) be added in series with the lamp current feedback as shown in Figure 4.

The addition of this resistor helps minimize the possibility of ESD damage in case of mishandling of the IC during board level assembly and test.

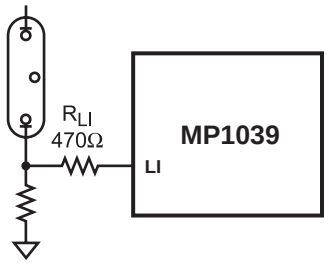

Figure 4—ESD Resistor

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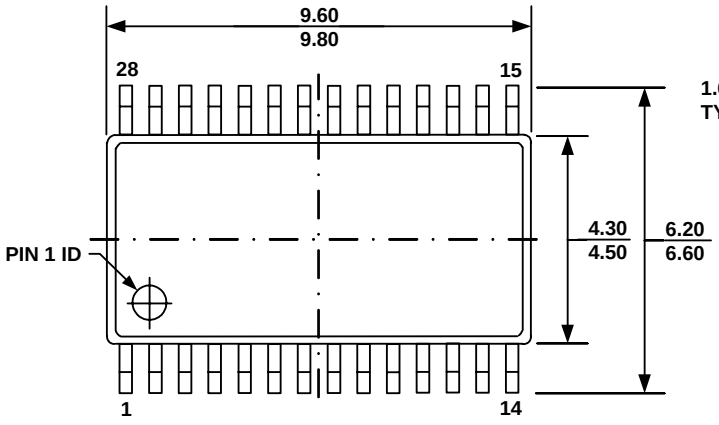
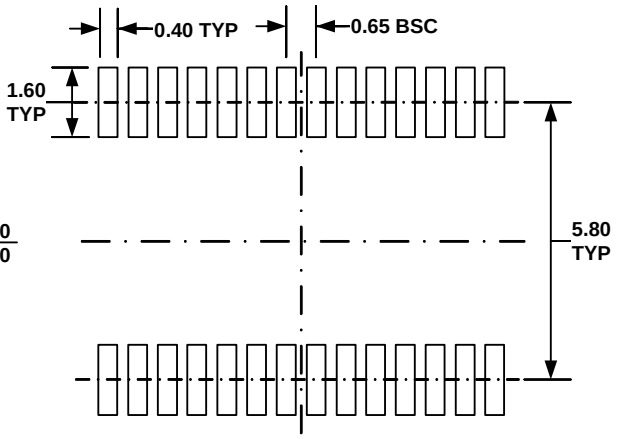
PACKAGE INFORMATION

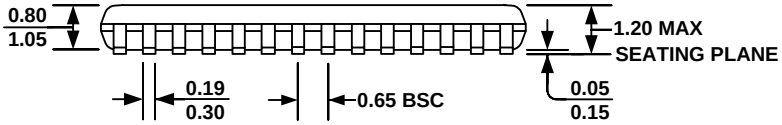
TSSOP28



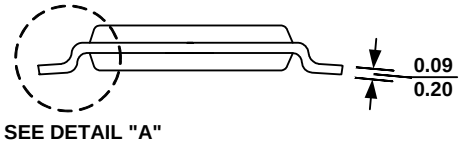
TOP VIEW



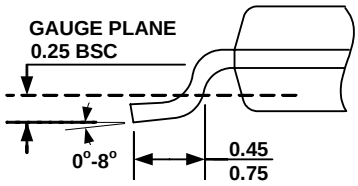
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

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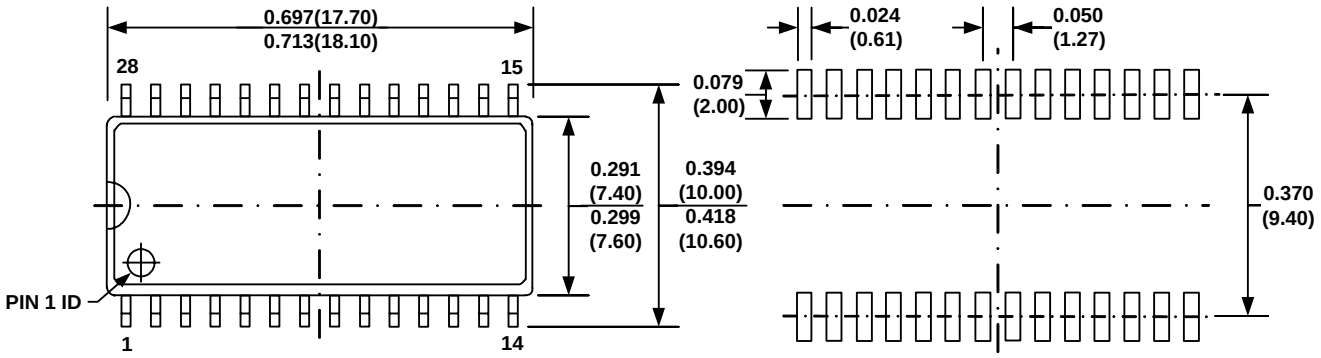
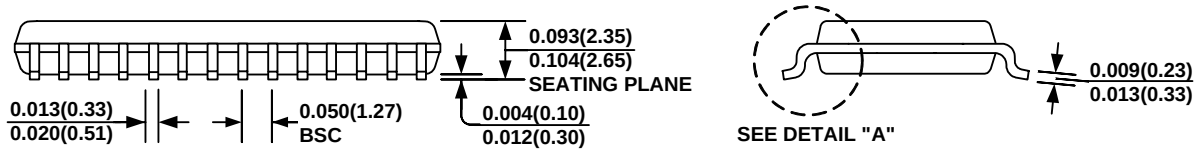
PACKAGE INFORMATION

SOIC28



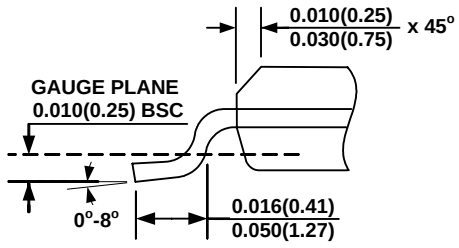
TOP VIEW

RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

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