International
IOR Rectifier

Preliminary Data Sheet No. PD60186-B

# IR2170(S)

## OVER CURRENT SENSING IC

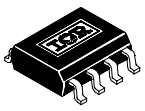
### Features

- Floating channel up to +600V
- Monolithic integration
- Overcurrent sensing through shunt resistor
- Low $I_{QBS}$ allows the boot strap power supply
- Independent fast 1µsec overcurrent trip signal
- High common mode noise immunity
- Input overvoltage protection for IGBT short circuit condition
- Open Drain outputs

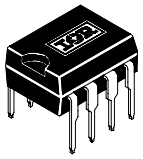
### Product Summary

| | |
|---|---|
| $V_{OFFSET}$ | 600Vmax |
| $I_{QBS}$ | 1mA |
| Overcurrent trip signal delay | 1.5usec (typ) |
| Overcurrent trip level | +/-260mV (typ.) |

### Packages



8-Lead SOIC

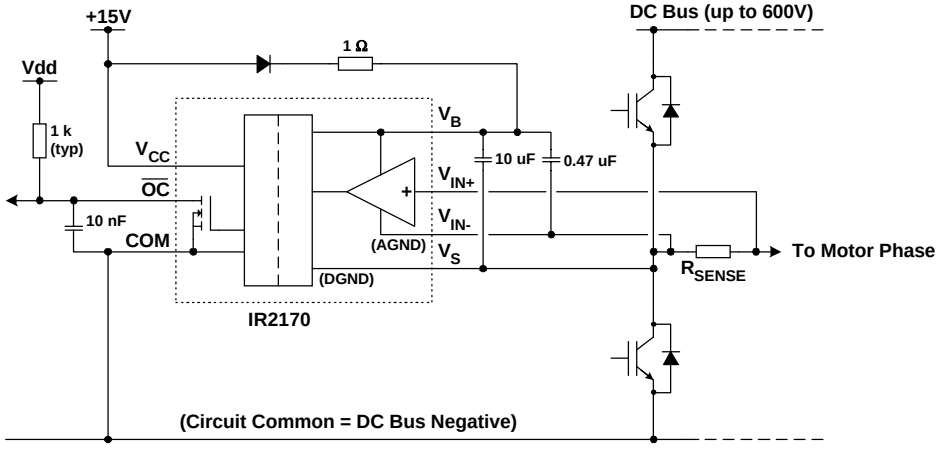


8-Lead PDIP

### Description

IR2170(S) is the monolithic over current sensing IC designed for motor drive applications. It senses the motor phase current through an external shunt resistor, detects overcurrent condition, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The dedicated overcurrent trip ($\overline{OC}$) signal facilitates IGBT short circuit protection. The OC output pulse width can be programmed by the external resistor and capacitor. The open-drain outputs make easy for any interface from 3.3V to 15V.

### Typical Application




(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_S$ | High side offset voltage | | -0.3 | 600 | V |
| $V_{BS}$ | High side floating supply voltage | | -0.3 | 25 | |
| $V_{CC}$ | Low side and logic fixed supply voltage | | -0.3 | 25 | |
| $V_{IN}$ | Maximum input voltage between $V_{IN+}$ and $V_{IN-}$ | | -5 | 5 | |
| $V_{OC}$ | Overcurrent output voltage | | COM -0.3 | VCC +0.3 | |
| $V_{IN-}$ | $V_{IN-}$ input voltage (note 1) | | $V_S$ -5 | $V_{B+}$ 0.3 | |
| dV/dt | Allowable offset voltage slew rate | | — | 50 | V/ns |
| $P_D$ | Package power dissipation @ $T_A \leq +25°C$ | 8 lead SOIC | — | .625 | W |
| | | 8 lead PDIP | — | 1.0 | |
| $Rth_{JA}$ | Thermal resistance, junction to ambient | 8 lead SOIC | — | 200 | °C/W |
| | | 8 lead PDIP | — | 125 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

Note 1: Capacitors are required between $V_B$ and Vin-, and between $V_B$ and Vs pins when bootstrap power is used. The external power supply, when used, is required between Vs and Vin-, and between $V_B$ and Vs pins.

## Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High side floating supply voltage | $V_S$ +13.0 | $V_S$ +20 | V |
| $V_S$ | High side floating supply offset voltage | note 2 | 600 | |
| $V_{OC}$ | Overcurrent output voltage | COM | VCC | |
| $V_{CC}$ | Low side and logic fixed supply voltage | 9.5 | 20 | |
| $V_{IN}$ | Input voltage between $V_{IN+}$ and $V_{IN-}$ | -260 | +260 | mV |
| $T_A$ | Ambient temperature | -40 | 125 | °C |

Note 2: Logic operation for Vs of -5 to +600V. Logic state held for Vs of -5V to -$V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

## DC Electrical Characteristics

$V_{CC}$ = $V_{BS}$ = 15V, and $T_A$ = 25°C unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{OC+}$ | Overcurrent trip positive input voltage | — | 260 | — | mV | |
| $V_{OC-}$ | Overcurrent trip negative input voltage | — | -260 | — | | |
| $I_{LK}$ | Offset supply leakage current | — | — | 50 | µA | $V_B$ = $V_S$ = 600V |
| $I_{QBS}$ | Quiescent $V_{BS}$ supply current | — | 1 | 2 | mA | $V_S$ = 0V |
| $I_{QCC}$ | Quiescent $V_{CC}$ supply current | — | — | 0.5 | | |
| $I_{OCC}$ | OC output sink current | 10 | — | — | | $V_O$ = 1V |
| | | 1 | — | — | | $V_O$ = 0.1V |

## AC Electrical Characteristics cont.

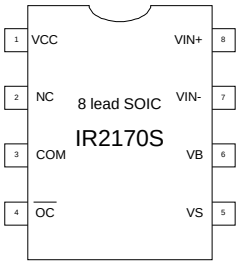
$V_{CC}$ = $V_{BS}$ = 15V, and $T_A$ = 25°C unless otherwise specified.

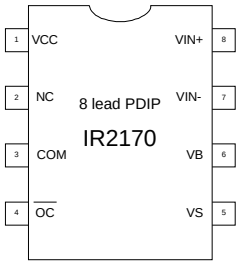
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **Proagation delay characteristics** | | | | | | |
| tdoc | Propagation delay time of OC | 1 | 1.5 | — | µsec | |
| twoc | Low true pulse width of OC | — | 1 | — | | |

## Lead Definitions

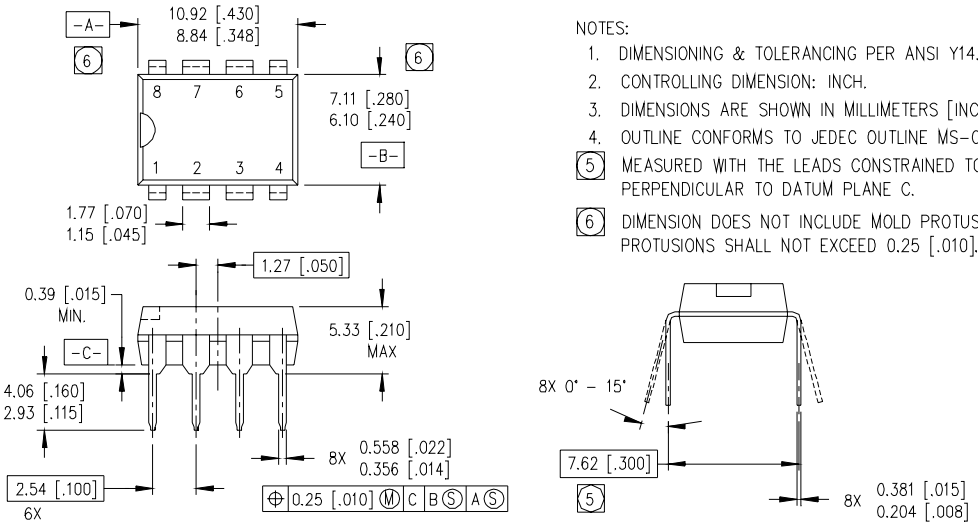
| Symbol | Description |
|---|---|
| $V_{CC}$ | Low side and logic supply voltage |
| COM | Low side logic ground |
| $V_{IN+}$ | Positive sense input |
| $V_{IN-}$ | Negative sense input |
| $V_B$ | High side supply |
| $V_S$ | High side return |
| $\overline{OC}$ | Overcurrent output (negative logic) |
| N.C. | No connection |

## Lead Assignments



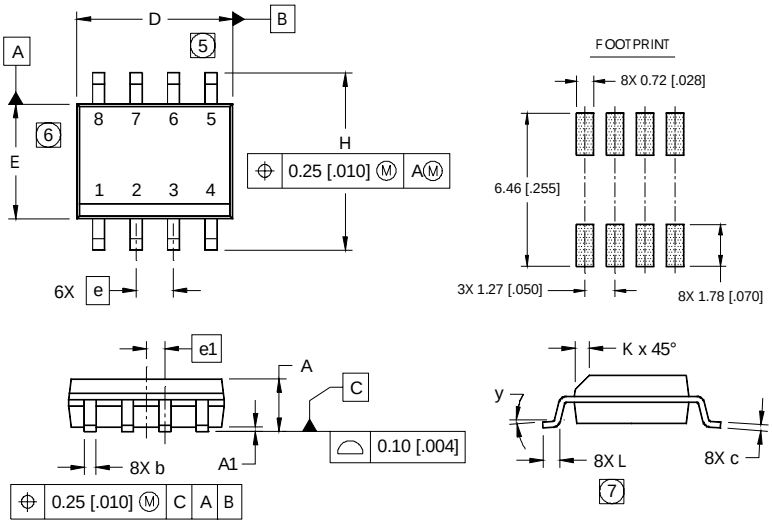
## Case outlines




NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M–1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS–001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

**8-Lead PDIP**

01-6014
01-3003 01 (MS-001AB)




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

**8-Lead SOIC**

01-6027
01-0021 11 (MS-012AA)