SBOS264A – DECEMBER 2002 – REVISED DECEMBER 2003

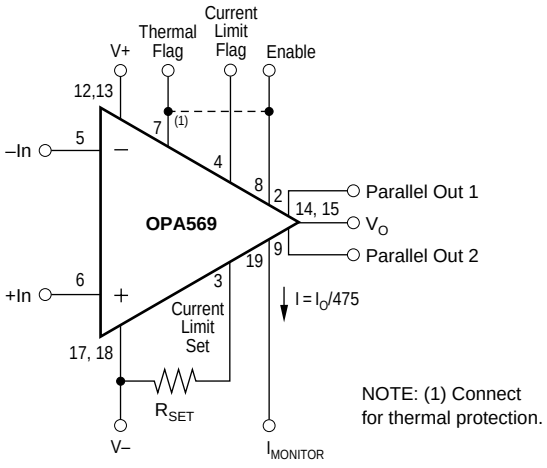
Rail-to-Rail I/O, 2A POWER AMPLIFIER

FEATURES

- **HIGH OUTPUT CURRENT: 2A**
- **OUTPUT SWINGS TO: 150mV of Rails with I_O = 2A**
- **THERMAL PROTECTION**
- **ADJUSTABLE CURRENT LIMIT**
- **TWO FLAGS: Current Limit and Temperature Warning**
- **LOW SUPPLY VOLTAGE OPERATION: 2.7V to 5.5V**
- **SHUTDOWN FUNCTION WITH OUTPUT DISABLE**
- **SMALL POWER PACKAGE: SO-20 PowerPAD™**

APPLICATIONS

- **THERMOELECTRIC COOLER DRIVER**
- **LASER DIODE PUMP DRIVER**
- **VALVE, ACTUATOR DRIVER**
- **SYNCHRO, SERVO DRIVER**
- **TRANSDUCER EXCITATION**
- **GENERAL LINEAR POWER BOOSTER FOR OP AMPS**
- **PARALLELING OPTION FOR HIGHER CURRENT APPLICATIONS**



DESCRIPTION

The OPA569 is a low-cost, high-current, operational amplifier designed for driving a wide variety of loads while operating on low-voltage supplies. It operates from either single or dual supplies for design flexibility and has rail-to-rail swing on the input and output. Typical output swing is within 150mV of the supply rails, with output current of 2A. Output swing closer to the rails is achievable with lighter loads.

The OPA569 is unity-gain stable, has low dc errors, is easy to use, and free from the phase inversion problems found in some power amplifiers. High performance is maintained at voltage swings near the output rails.

The OPA569 provides an accurate user-selected current limit that is set with an external resistor, or digitally adjusted via a Digital-to-Analog Converter.

The OPA569 output can be independently disabled using the Enable pin, saving power and protecting the load.

The $I_{MONITOR}$ pin provides a 1:475 bidirectional copy of the output current. This eliminates the need for a series current shunt resistor, allowing more voltage to be applied to the load. This pin can be used for simple monitoring, or feedback control to establish constant output current.

Two flags are provided: one for warning of thermal overstress, and one for current limit condition. The Thermal Flag pin can be connected to the Enable pin to provide a thermal shutdown solution.

Packaged in the Texas Instruments PowerPAD™ package, it is small and easy to heat-sink. The OPA569 is specified for operation over the industrial temperature range, –40°C to +85°C.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	+7.5V
Output Current	See SOA Curves
Signal Input Terminals (pins 2, 5, 6, and 9):	
Voltage(2)	(V–) – 0.5V to (V+) + 0.5V
Current(2)	±10mA
Output Short-Circuit(3)	Continuous when thermal protection enabled
Current Monitor (pin 19) Short-Circuit	Continuous
Enable Pin (pin 8)	(V–) – 0.5V to (V–) + 7.5V
PowerPAD (pins 1, 10, 11, 20, and pad)	(V–) – 0.5V to (V–) + 0.5V
Current Limit Set (pin 3)	(V–) – 0.5V to (V+) + 0.5V
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTROSTATIC DISCHARGE SENSITIVITY

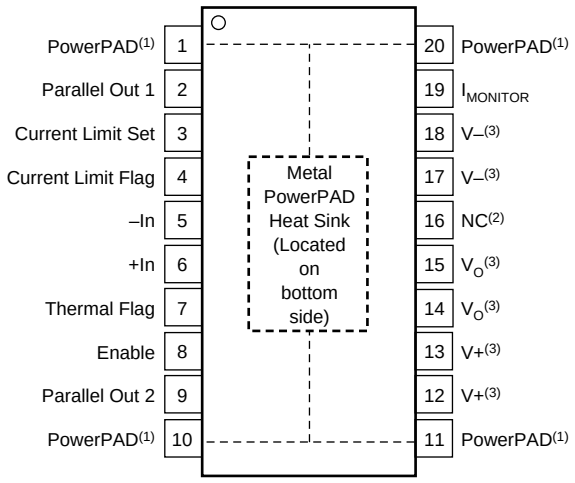
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View **SO**

OPA569



NOTES: (1) PowerPAD pins 1, 10, 11, and 20 and the PowerPAD should be connected to the most negative supply (V–) in either single or split supply configurations.
(2) NC means no internal connection.
(3) The following pin pairs must be connected together: 12 and 13; 14 and 15; 17 and 18.

PIN DESCRIPTIONS

PIN #	NAME	DESCRIPTION
1, 10, 11, 20	PowerPAD	PowerPAD Connection Pins
2	Parallel Out 1	Connection for Paralleling Multiple Amplifiers
3	Current Limit Set	Current Limit Set Pin
4	Current Limit Flag	Indicates When Part is in Current Limit (Active LOW).
5	–In	Inverting Input
6	+In	Noninverting Input
7	Thermal Flag	Indicates Thermal Stress (Active LOW)
8	Enable	Enabled HIGH. Shut down LOW.
9	Parallel Out 2	Connection for Paralleling Multiple Amplifiers
12, 13	V+	Positive Power-Supply Voltage
14, 15	V_O	Output
16	NC	No Internal Connection
17, 18	V–	Negative Power-Supply Voltage
19	$I_{MONITOR}$	Provides 1:475 Bidirectional Copy of Output Current.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_{CASE} = +25°C, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

PARAMETER		CONDITION	OPA569 MIN	OPA569 TYP	OPA569 MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	I_O = 0V, V_S = +5V		±0.5	±2	mV
vs Temperature	**dV_{OS}/dT**	**T_A = –40°C to +85°C**		**±1.3**		**µV/°C**
vs Power Supply	PSRR	V_S = +2.7V to +5.5V, V_{CM} = (V–) +0.55V		12	60	µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±1	±10	pA
vs Temperature				**(doubles every 10°C)**		
Input Offset Current	I_{OS}			±2	±10	pA
NOISE						
Input Voltage Noise Density, f = 1kHz	e_n			12		nV/√Hz
f = 0.1Hz to 10Hz				8		µVp-p
Current Noise Density, f = 1kHz	i_n			0.6		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}	Linear Operation	(V–) – 0.1		(V+) + 0.1	V
Common-Mode Rejection Ratio	CMRR	V_S = +5V, –0.1V < V_{CM} < 3.2V	80	100		dB
		V_S = +5V, –0.1V < V_{CM} < 5.1V	60	80		dB
INPUT IMPEDANCE						
Differential				10^{13} || 4.5		Ω || pF
Common-Mode				10^{13} || 9		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	0.2V < V_O < 4.8V, R_L = 1kΩ, V_S = +5V	100	126		dB
		0.3V < V_O < 4.7V, R_L = 1.15Ω, V_S = +5V		90		dB
FREQUENCY RESPONSE						
Gain Bandwidth Product	GBW			1.2		MHz
Slew Rate	SR	G = +1, V_O = 4.0V Step		1.2		V/µs
Full-Power Bandwidth[1]				See Typical Characteristics		
Settling Time: ±0.1%		G = –1, V_O = 4.0V Step		5		µs
Total Harmonic Distortion + Noise[2]	THD+N			See Typical Characteristics		
OUTPUT						
Voltage Output Swing from Rail	V_O	R_L = 1kΩ, A_{OL} > 100dB	(V–) + 0.2	(V_S) ± 0.02	(V+) – 0.2	V
		I_O = ±2A, V_S = +5V, A_{OL} > 80dB[3]	(V–) + 0.3	(V_S) ± 0.15	(V+) – 0.3	V
Maximum Continuous Current Output: dc[4]					2.4	A
Capacitive Load Drive[5]	C_{LOAD}			See Typical Characteristics		
Output Disabled						
Output Impedance				12M || 570		Ω || pF
CURRENT LIMIT						
Output Current Limit[6]		Externally Adjustable		±0.2 to ±2.2		A
Current Limit Equation				$I_{LIMIT} = I_{SET} \cdot 9800$		A
R_{SET} Equation				$R_{SET} = 9800\ (1.18V/I_{LIMIT})$		Ω
Current Limit Tolerance[7], Positive		I_{LIMIT} = 1A		±3	±10	%
Negative		I_{LIMIT} = 1A		±3	±15	%
Voltage on Current Limit Set Pin Tolerance[8]			(V–) + 1.05	(V–) + 1.18	(V–) + 1.3	V
OUTPUT CURRENT MONITOR (Pin 19)						
Output Current Monitor	I_M			$I_M = I_O/475$		A
Output Current Monitor Tolerance[9], Positive		I_O = +1A, $R_{MONITOR}$ = 400Ω		±3	±10	%
Negative		I_O = –1A, $R_{MONITOR}$ = 400Ω		±3	±15	%
Compliance Voltage Range		Linear Operation		See Discussion on Current Monitor Section		

NOTES: (1) See typical characteristic “Maximum Output Voltage vs Frequency.” (2) See the typical characteristic “Total Harmonic Distortion + Noise vs Frequency.” (3) Swing to the rail is measured in final test. Under those conditions, the A_{OL} is derived from characterization. (4) See Safe Operating Area (SOA) plots. (5) See typical characteristic, “Overshoot vs Load Capacitance.” (6) External current limit setting resistor is required. See Figure 1. (7) I_{LIMIT} is the value of the desired current limit and is equal to 9800 (I_{SET}), where I_{SET} is the current through the Current Limit Set pin (pin 3). Errors from this parameter can be calibrated out—see Applications Information section. (8) V_{SET} is a voltage reference that equals the difference between the voltage of the Current Limit Set pin and V–, and is referenced to the negative rail. Errors from this parameter can be calibrated out—see Applications Information section. (9) % Tolerance = $[(I_{OUT}/475) – I_{MONITOR}] \cdot 100/I_{MONITOR}$.

ELECTRICAL CHARACTERISTICS: V_S = +2.7V to +5.5V (Cont.)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C.**

At T_{CASE} = +25°C, R_L = 1kΩ, and connected to V_S/2, unless otherwise noted.

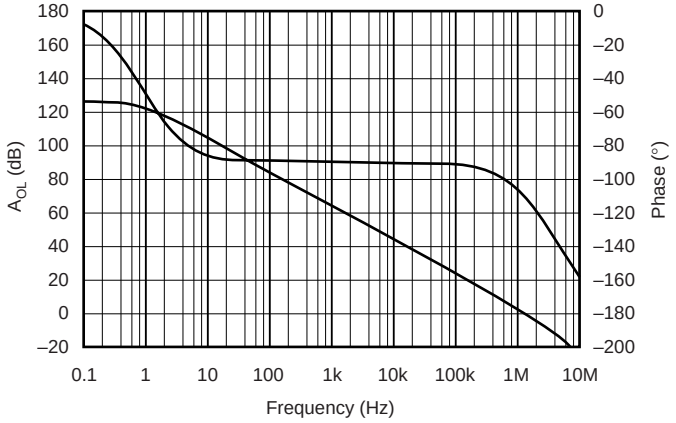
PARAMETER		CONDITION	OPA569 MIN	OPA569 TYP	OPA569 MAX	UNITS
ENABLE/SHUTDOWN INPUT (Pin 8)						
Enable Pin Bias Current		V_{SD} = 0V		0.2		µA
HIGH (Output enabled)	V_{SD}	Pin Open or Forced HIGH	(V–) + 2.5			V
LOW (Output disabled)	V_{SD}	Pin Forced LOW			(V–) + 0.8	V
Output Disable Time		R_L = 1Ω		0.5		µs
Output Enable Time		R_L = 1Ω		15		µs
THERMAL FLAG PIN (Pin 7)						
Junction Temperature:	T_J					
Alarm (Thermal Flag pin LOW)		Thermal Overstress		+147		°C
Return to Normal Operation (Thermal Flag pin HIGH)		Normal Operation		+130		°C
Thermal Flag Pin Voltage		Normal Operation $I_{pin\ 7}$ = +25µA	(V+) – 0.8V	V+		V
		During Thermal Overstress, $I_{pin\ 7}$ = –25µA		V–	(V–) + 0.8	V
CURRENT LIMIT FLAG PIN (Pin 4)						
Current Limit Flag Pin Voltage		Normal Operation, $I_{pin\ 4}$ = +25µA	(V+) – 0.8V	V+		V
		During Current Limit, $I_{pin\ 4}$ = –25µA		V–	(V–) + 0.8	V
POWER SUPPLY						
Specified Voltage Range	V_S		+2.7		+5.5	V
Operating Voltage Range			+2.7		+5.5	V
Quiescent Current(10)	I_Q	I_O = 0, I_{LIMIT} = 200mA, V_S = 5V		+3.4	+6	mA
		I_O = 0, I_{LIMIT} = 2A, V_S = 5V		+9	+11	mA
Quiescent Current in Shutdown Mode		I_O = 0, V_{SD} = 0.8V, V_S = 5V		+0.01		mA
TEMPERATURE RANGE						
Specified Range		Junction Temperature	–40		+85	°C
Operating Range		Junction Temperature	–55		+125	°C
Storage Range			–65		+150	°C
Thermal Resistance, Junction-to-Case	θ_{JC}			0.37		°C/W
Thermal Resistance, Junction-to-Ambient	θ_{JA}	2oz Trace and 9in² Copper Pad with Solder		21.5		°C/W

NOTE: (10) Quiescent current is a function of the current limit setting. See application section, “Adjustable Current Limit and Current Limit Flag Pin.”

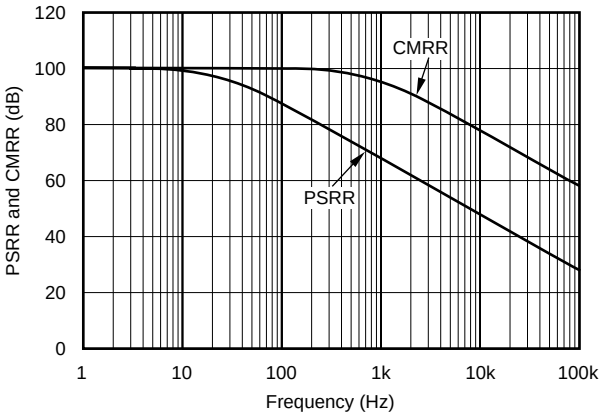
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5V, unless otherwise noted.

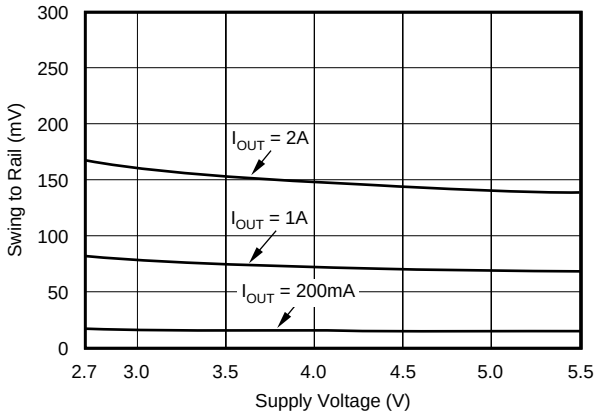
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



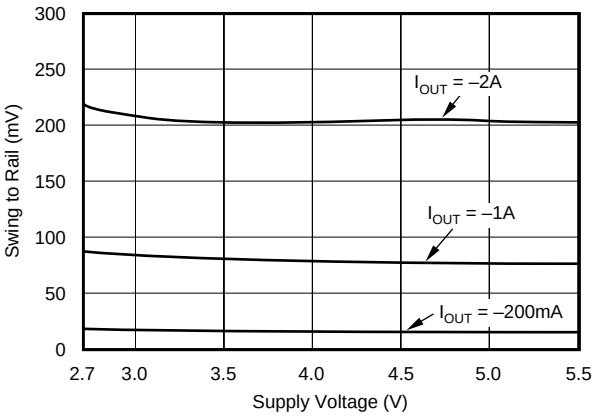
POWER-SUPPLY AND COMMON-MODE REJECTION RATIO vs FREQUENCY



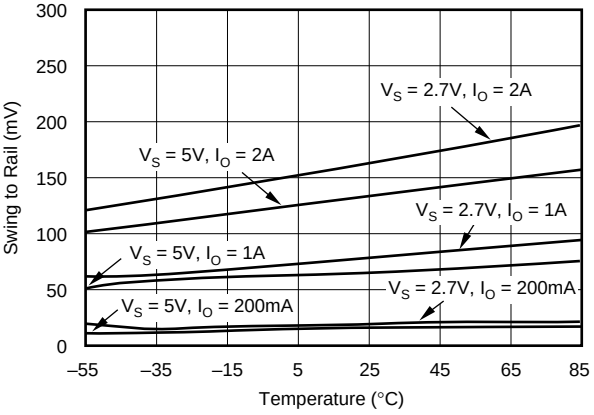
OUTPUT SWING TO POSITIVE RAIL vs SUPPLY VOLTAGE



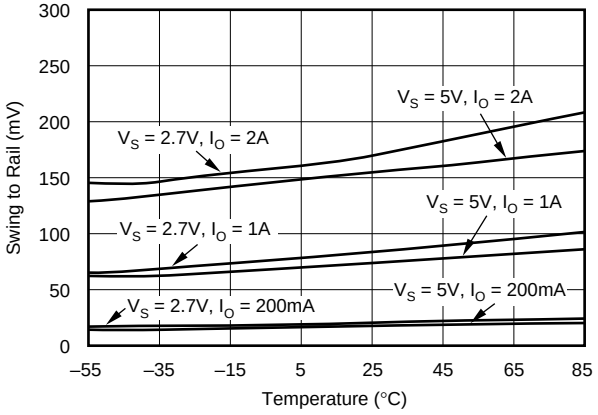
OUTPUT SWING TO NEGATIVE RAIL vs SUPPLY VOLTAGE



OUTPUT SWING TO POSITIVE RAIL vs TEMPERATURE



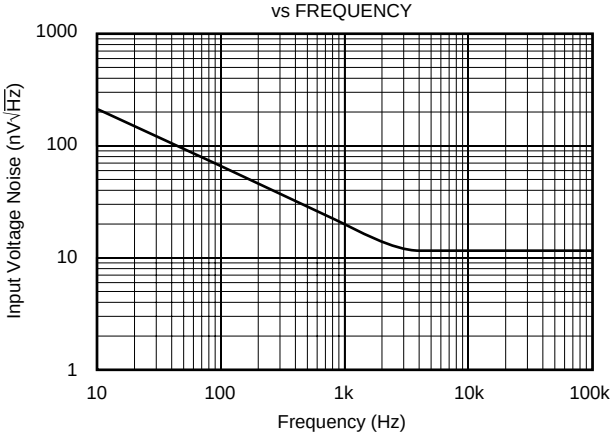
OUTPUT SWING TO NEGATIVE RAIL vs TEMPERATURE



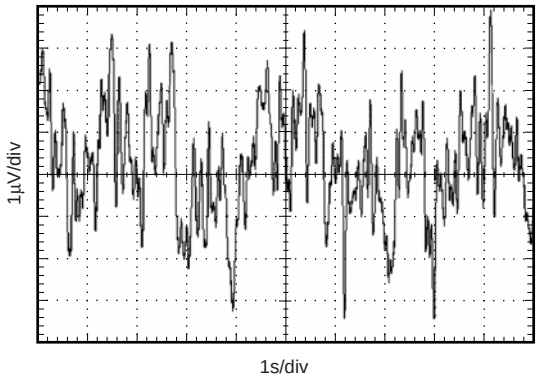
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

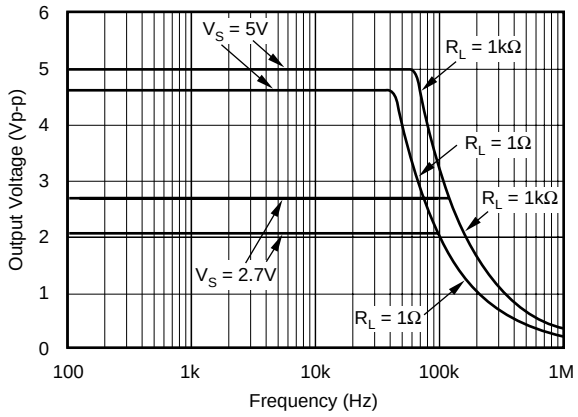
INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



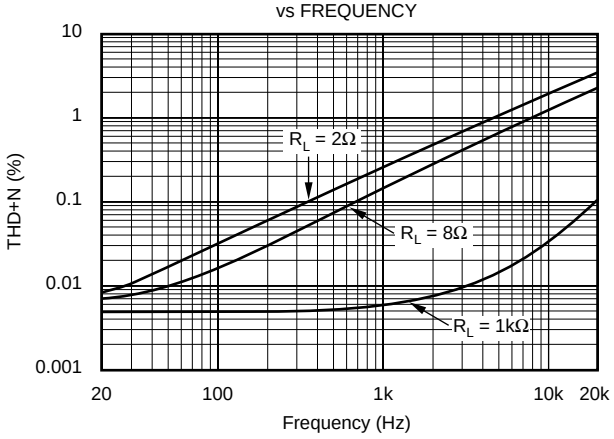
0.1Hz TO 10Hz INPUT VOLTAGE NOISE



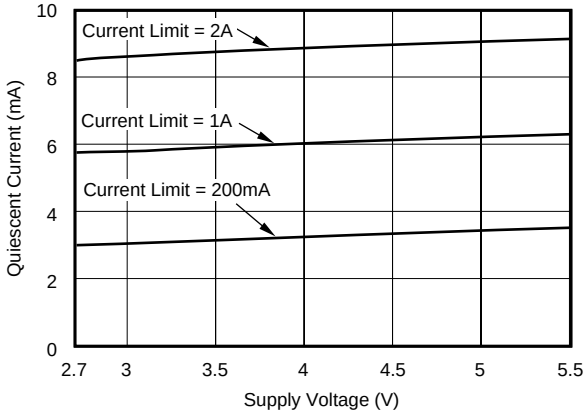
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



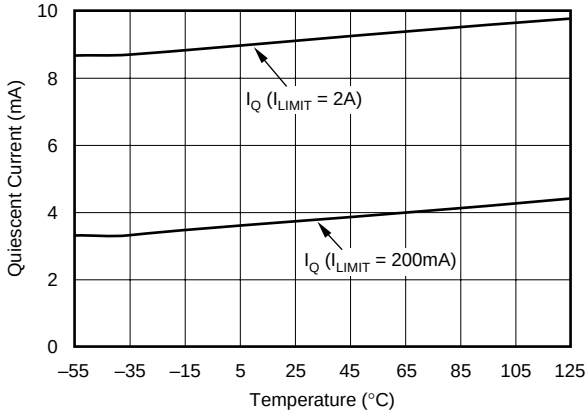
TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



QUIESCENT CURRENT vs SUPPLY VOLTAGE



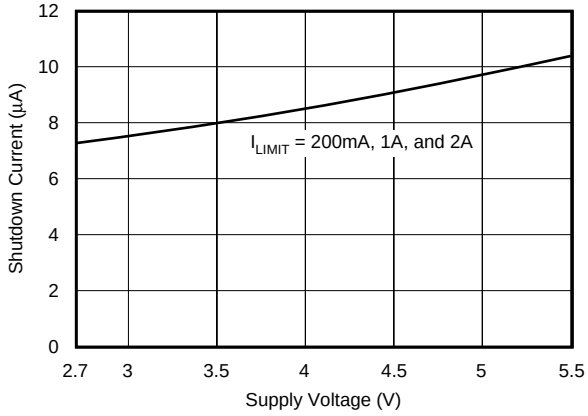
QUIESCENT CURRENT vs TEMPERATURE



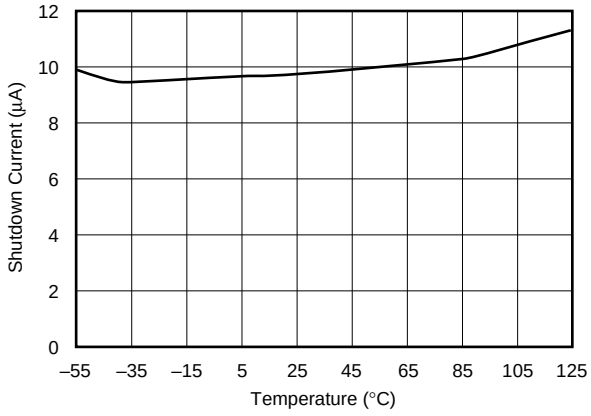
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

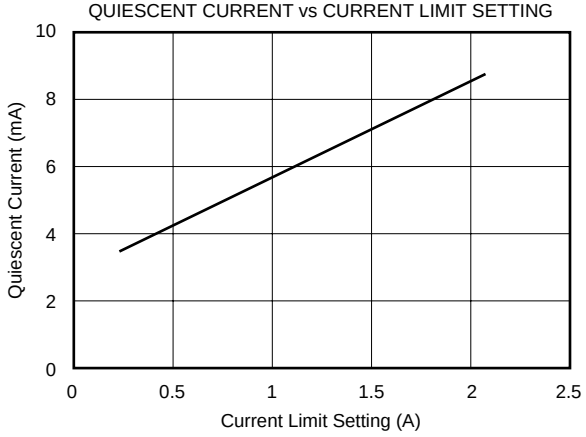
SHUTDOWN CURRENT vs SUPPLY VOLTAGE



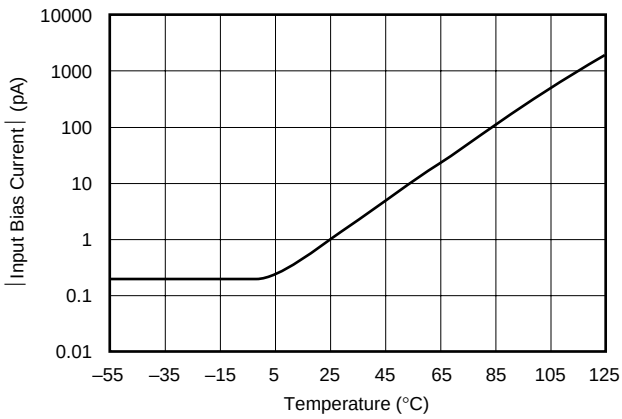
SHUTDOWN CURRENT vs TEMPERATURE



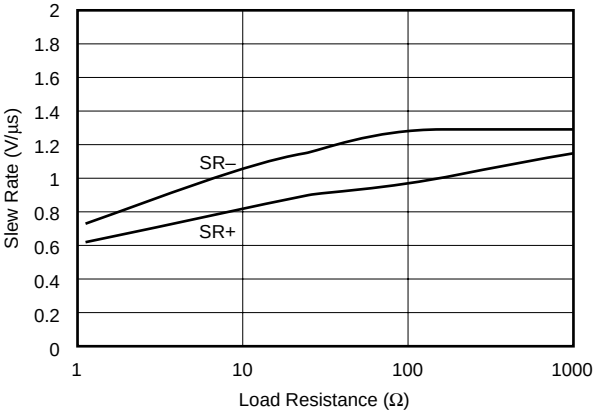
QUIESCENT CURRENT vs CURRENT LIMIT SETTING



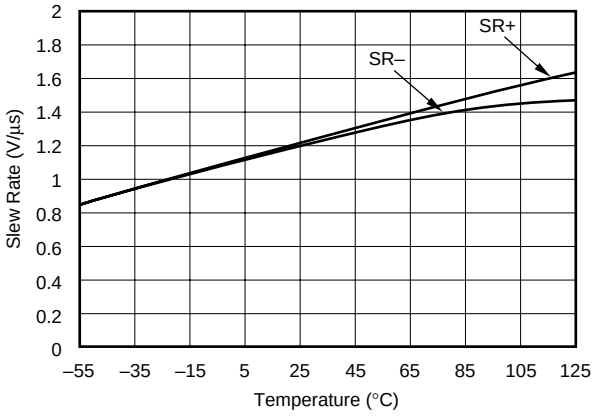
INPUT BIAS CURRENT vs TEMPERATURE



SLEW RATE vs LOAD RESISTANCE



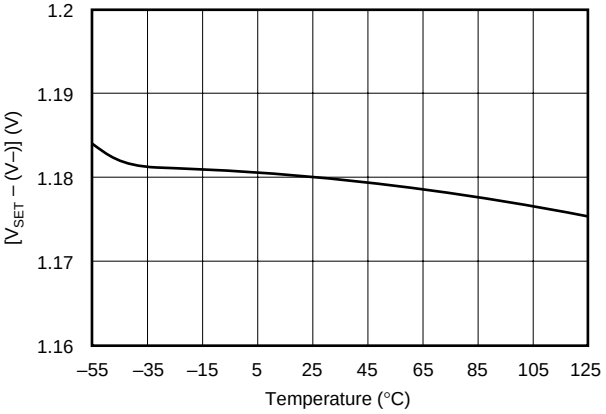
SLEW RATE vs TEMPERATURE



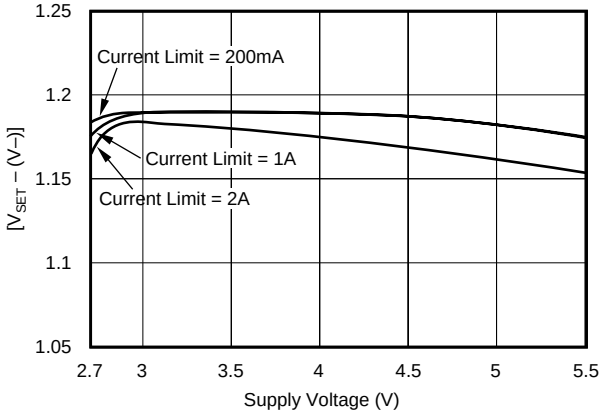
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

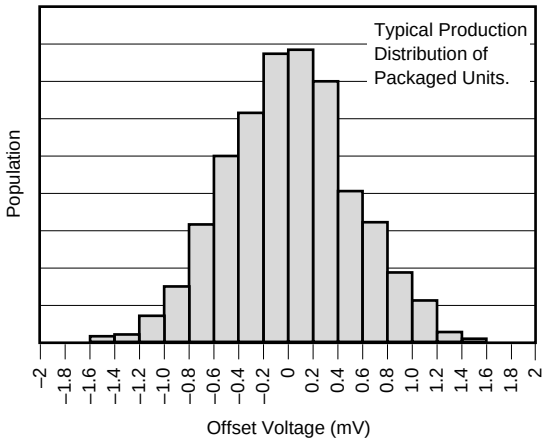
VOLTAGE ON CURRENT LIMIT SET PIN
vs TEMPERATURE



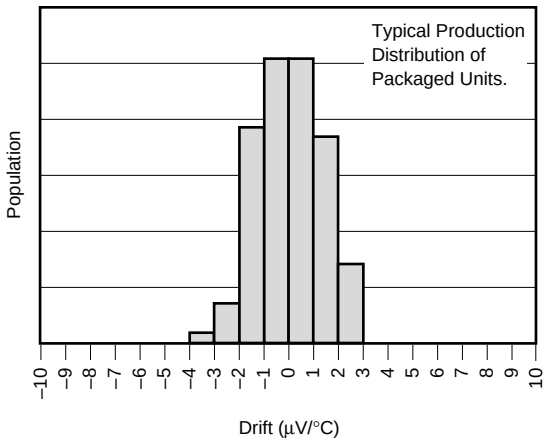
VOLTAGE ON CURRENT LIMIT SET PIN
vs SUPPLY VOLTAGE



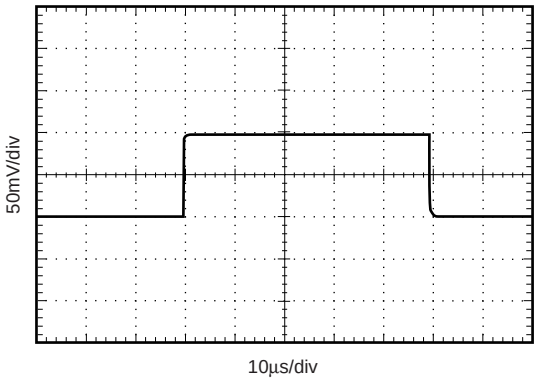
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



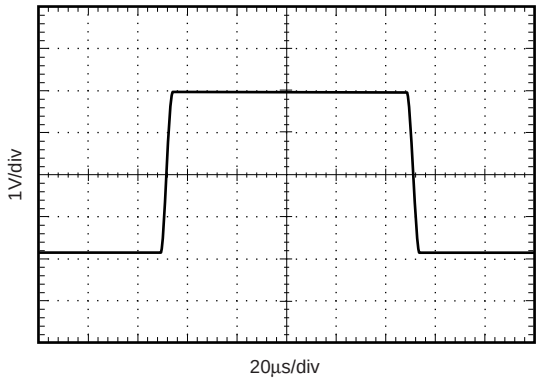
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



SMALL-SIGNAL STEP RESPONSE
(G = +1, R_L = 1kΩ)



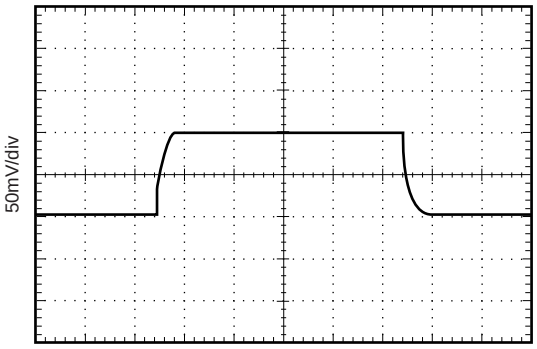
LARGE-SIGNAL STEP RESPONSE
(G = +1, R_L = 1kΩ)



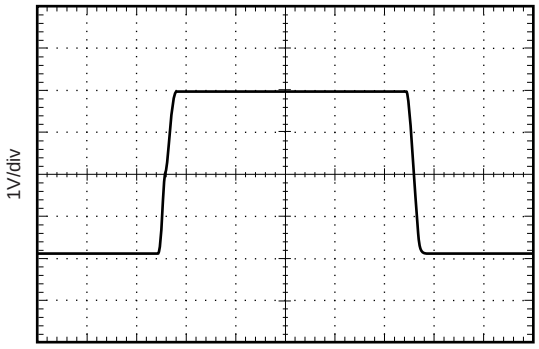
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

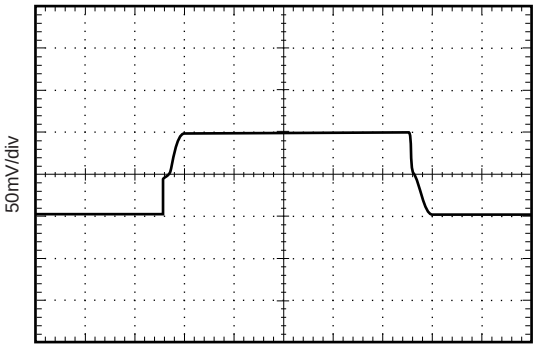
SMALL-SIGNAL STEP RESPONSE
(G = +1, R_L = 10Ω)



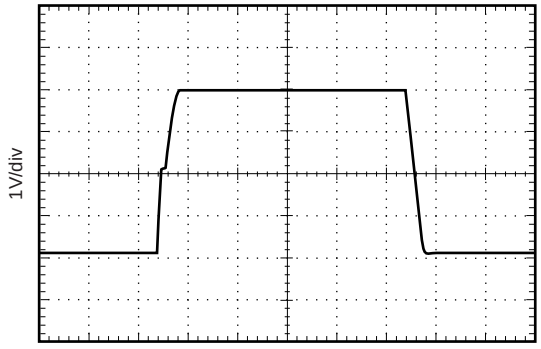
LARGE-SIGNAL STEP RESPONSE
(G = +1, R_L = 10Ω)



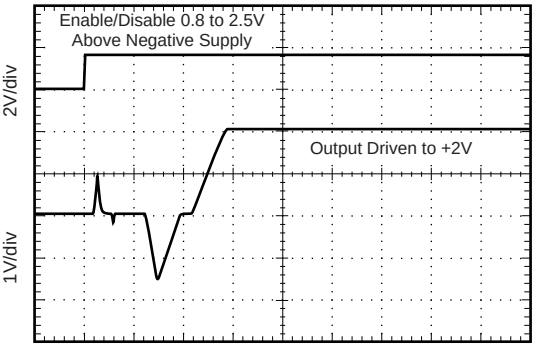
SMALL-SIGNAL STEP RESPONSE
(G = +1, R_L = 1Ω)



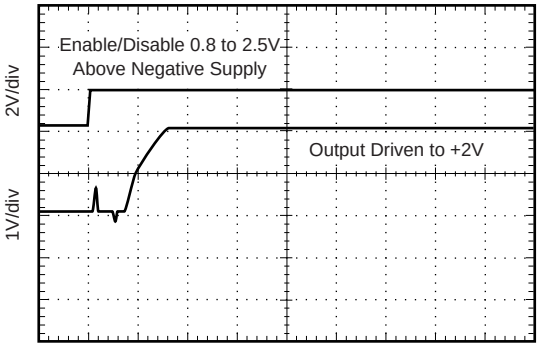
LARGE-SIGNAL STEP RESPONSE
(G = +1, R_L = 1Ω)



ENABLE
(10Ω Load)



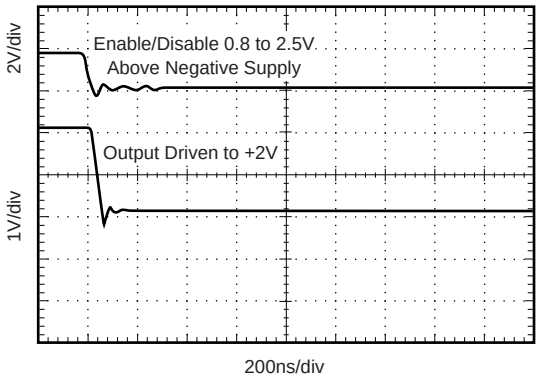
ENABLE
(1Ω Load)



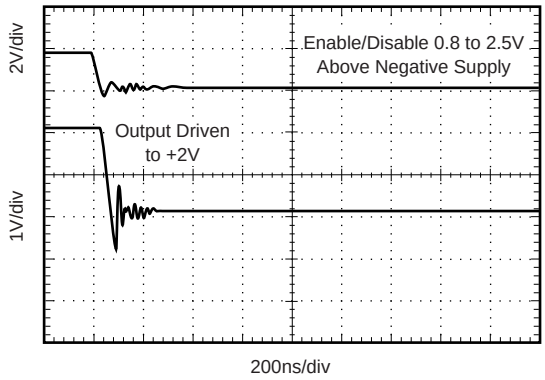
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

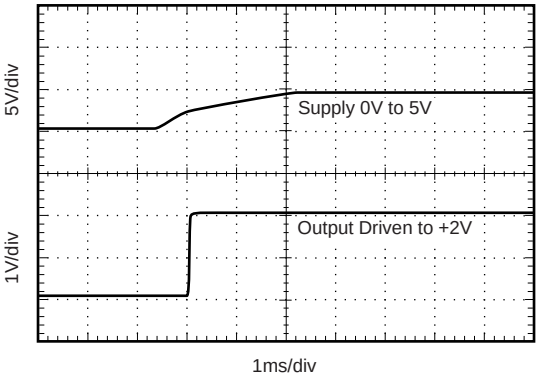
DISABLE
(10Ω Load)



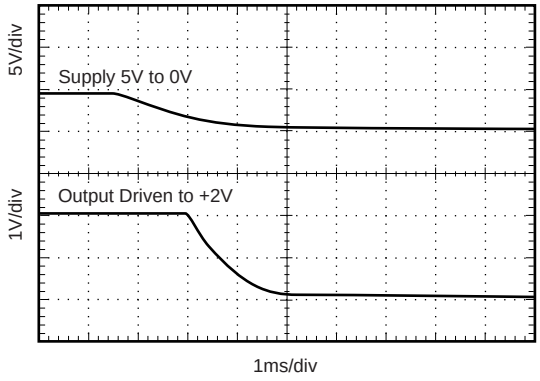
DISABLE
(1Ω Load)



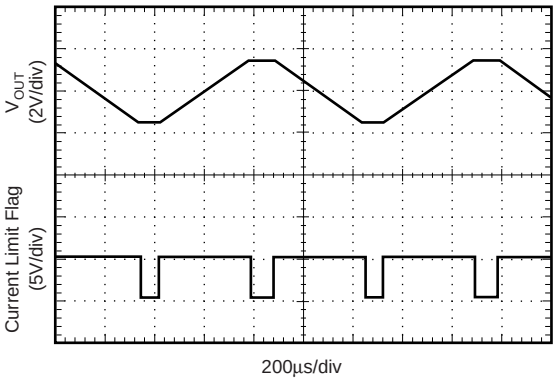
POWER ON
(1Ω Load)



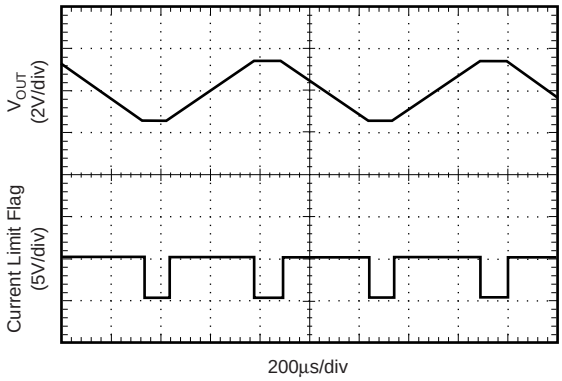
POWER OFF
(1Ω Load)



IN AND OUT OF CURRENT LIMIT TRANSIENT
(R_L = 0.75Ω, Current Limit = 2A)



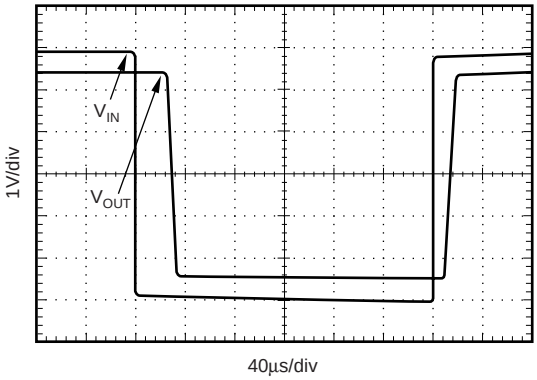
IN AND OUT OF CURRENT LIMIT TRANSIENT
(R_L = 7.5Ω, Current Limit = 200mA)



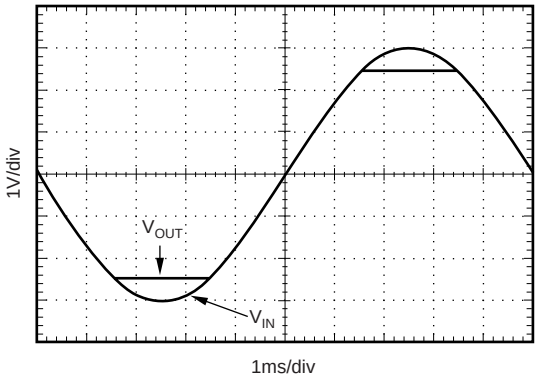
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = +5V, unless otherwise noted.

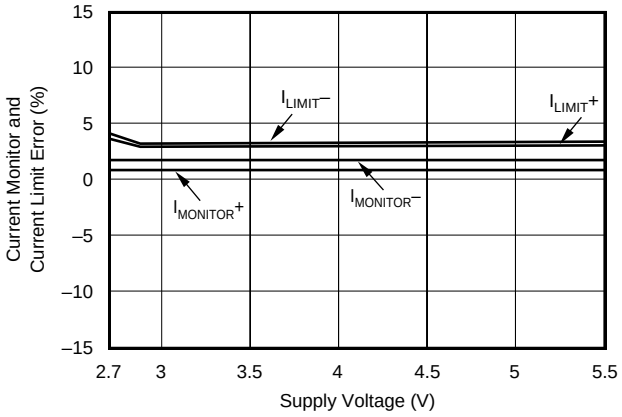
OVERLOAD RECOVERY
(G = +1)



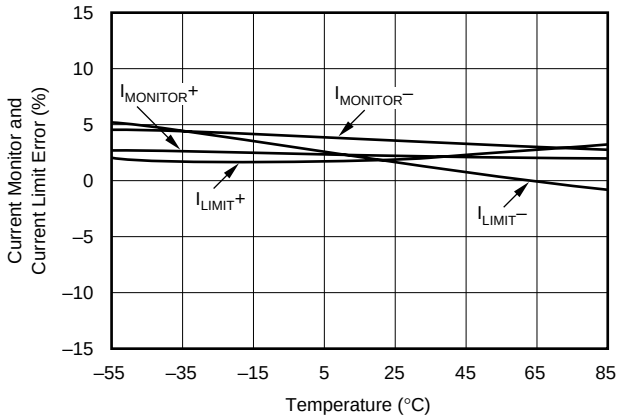
NO PHASE INVERSION WITH INPUTS
LARGER THAN SUPPLY VOLTAGE
(G = +1, R_L = 10Ω)



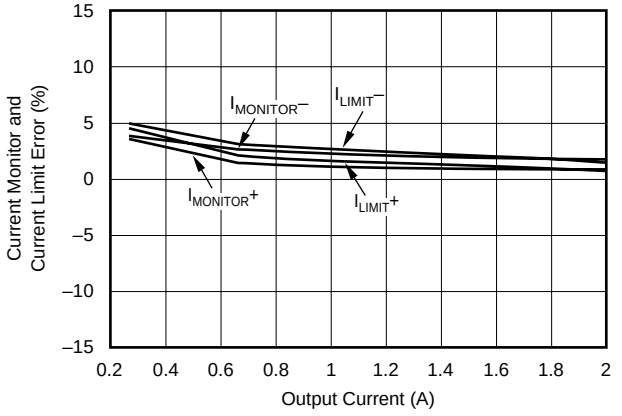
CURRENT MONITOR AND CURRENT LIMIT ERROR
vs SUPPLY VOLTAGE



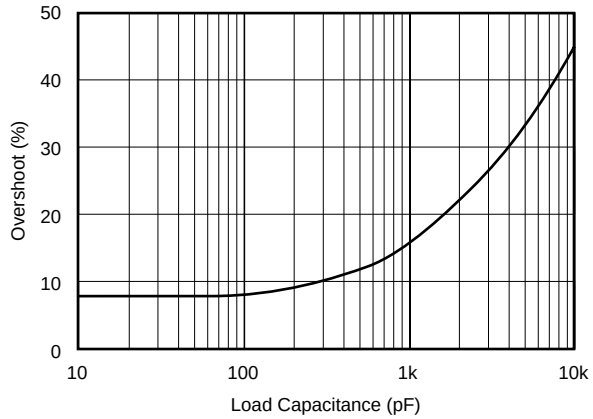
CURRENT MONITOR AND CURRENT
LIMIT ERROR vs TEMPERATURE



CURRENT MONITOR AND CURRENT LIMIT ERROR
vs OUTPUT CURRENT



OVERSHOOT vs LOAD CAPACITANCE
(G = +1, R_L = 1kΩ)



APPLICATIONS INFORMATION

BASIC CONFIGURATION

Figure 1 shows the OPA569 connected as a basic non-inverting amplifier; however, the OPA569 can be used in virtually any op amp configuration. A current limit setting resistor (R_{SET}, in Figure 1) is essential to the OPA569's operation, and cannot be omitted.

Power-supply terminals should be bypassed with low series impedance capacitors. Using a larger tantalum and smaller ceramic type in parallel is recommended. Power-supply wiring should have low series impedance.

POWER SUPPLIES

The OPA569 operates with excellent performance from a single (+2.7V to +5.5V) supply or from dual supplies. Power supply voltages do not need to be equal as long as the total voltage remains below 5.5V. Parameters that vary significantly with operating voltage are shown in the typical characteristics section.

ADJUSTABLE CURRENT LIMIT AND CURRENT LIMIT FLAG PIN

The OPA569 provides over-current protection to the load through its accurate, user-adjustable current limit (pin 3). The current limit value, I_{LIMIT}, can be set from 0.2A to 2.2A by controlling the current through the Current Limit Set pin. The current limit, I_{LIMIT}, will be 9800 I_{SET}; where I_{SET} is the current through the Current Limit Set pin. Setting the current limit requires no special power resistors. The output current does not flow through this pin.

Setting the current limit

As illustrated in Figure 2, the simplest method of setting the current limit is to connect a resistor or potentiometer between the current limit set pin and V–, the negative supply, according to the formula:

$$I_{LIMIT} = 9800 \bullet (1.18V/R_{SET})$$

Alternatively, the output current limit can be set by applying a voltage source in series with a resistance using the equation:

$$I_{LIMIT} = 9800 \bullet [(1.18V - V_{ADJUST})/R_{SET}]$$

The voltage source will be referenced to V–.

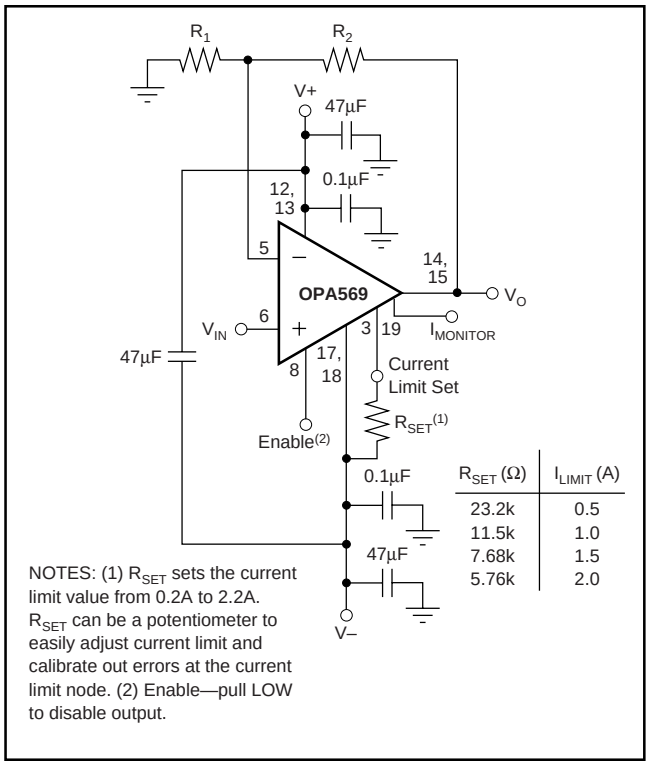


FIGURE 1. Basic Connections.

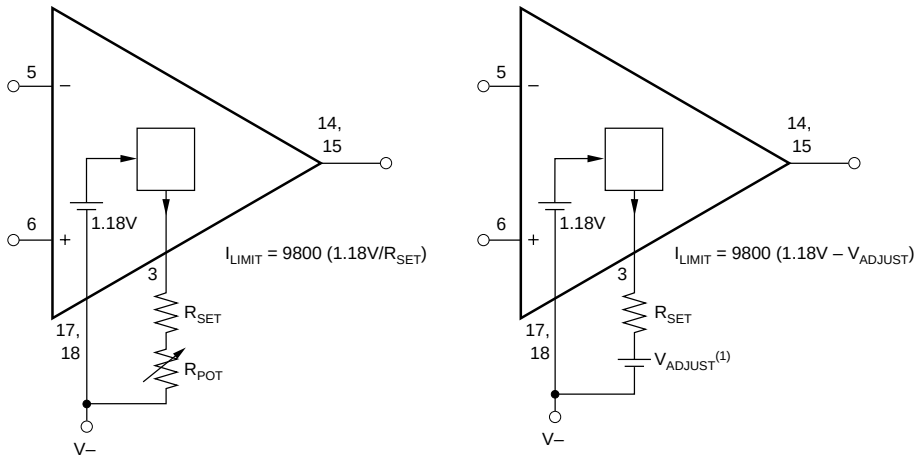


FIGURE 2. Setting the Current Limit—Resistor Method.

Current Limit Accuracy

Internally separate circuits monitor the positive and negative current limits. Each circuit output is compared to a single internal reference that is set by the user with an external resistor or a resistor/voltage source combination. The OPA569 employs a patented circuit technique to achieve an accurate and stable current limit throughout the full output range. The initial accuracy of the current limit is typically within 3%; however, due to internal matching limitations, the error can be as much as 15%. The variation of the current limit with factors such as output current level, output voltage and temperature is shown in the Typical Characteristics section.

When the accuracy of one current limit (sourcing or sinking) is more important than the other, it is possible to set its accuracy to better than 1% by adjusting the external resistor or the applied voltage. The accuracy of the other current limit will still be affected by internal matching.

Current Limit Flag Pin

The OPA569 features a Current Limit Flag pin (pin 4) that can be monitored to determine when the part is in current limit. The output signal of the current limit flag pin is compatible to standard logic in single supply applications. The output signal is a CMOS logic gate that switches from V+ to V– to indicate that the amplifier is in current limit. This flag output pin can source and sink up to 25µA. Additional parasitic capacitance between pins 3 and 4 can cause instability at the edge of the current limit. Avoid routing these traces in parallel close to each other.

Quiescent Current Dependence on the Current Limit Setting

The OPA569 is a low power amplifier, with a typical 3.4mA quiescent current (with the current limit configured for 200mA). The quiescent current varies with the current limit setting—it increases 0.5mA for each additional 200mA increase in the current limit, as shown in Figure 3.

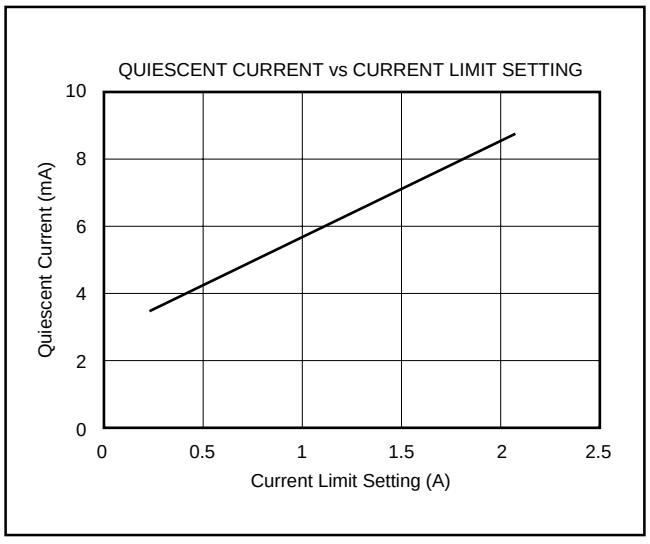


FIGURE 3. Quiescent Current vs Current Limit Setting.

CURRENT MONITOR

The OPA569 features an accurate output current monitor ($I_{MONITOR}$) without requiring the use of series resistance with the load. This increases efficiency significantly and provides better overall swing-to-supply performance.

An internal circuit creates a 1:475 copy of the output current. This copy of the output current can be monitored independently or it can be used in applications such as current control drive, setting non-symmetric positive and negative current limits or paralleling two or more devices for increased output current drive. When not being used, the Current Monitor pin may be left floating.

Some restrictions apply when using the current monitor function. When the main amplifier is sourcing current, the current monitor circuit must be sourcing current. Likewise, when the main amplifier is sinking current, the current monitor circuit must also be sinking current. Additionally, the swing on the $I_{MONITOR}$ pin is smaller than the output swing. When the amplifier is sourcing current, the voltage of the Current Monitor pin must be at least two hundred millivolts less than the output voltage of the amplifier. Conversely, when the amplifier is sinking current, the voltage of the Current Monitor pin must be at least two hundred millivolts greater than the output voltage of the amplifier. Resistive loads are able to meet these restrictions. Other types of loads may cause invalid current monitor values.

A simple way to monitor the load current and meet these requirements is to connect a resistor (with resistance less than 400 • R_L) from the $I_{MONITOR}$ pin to the same potential to which the other side of the load is connected. Another method is to use a transimpedance amplifier, as shown in Figure 4. This circuit must assure that the potential of the $I_{MONITOR}$ pin remains in the valid voltage range by connecting it to the same potential to which the load is connected—most likely ground for dual supply or mid-supply for single-supply applications.

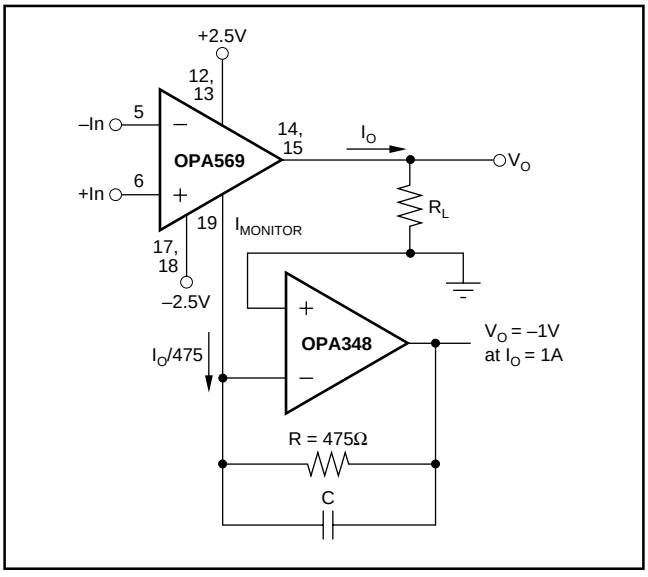


FIGURE 4. Transimpedance Amplifier to Monitor Load Current.

The accuracy of the current copy is reduced with small output currents. An internal circuit monitors the direction of the output current and enables the positive or the negative current monitoring circuitry accordingly. There is an approximate 20µs delay in the change of current direction. The switching point is near quiescent conditions and may cause current monitor inaccuracy with small output currents.

ENABLE PIN—OUTPUT DISABLE

The Enable pin can disable the OPA569 within microseconds. When disabled, the amplifier draws less than 10µA and its output enters a high-impedance state that allows multiplexing. It is important to note that when the amplifier is disabled, the Thermal Flag pin circuitry continues to operate. This feature allows use of the Thermal Flag pin output to implement thermal protection strategies. For more details, please see the section on thermal protection.

The OPA569 Enable pin has an internal pull-up circuit, so it does not have to be connected to the positive supply for normal operation. To disable the amplifier, the Enable pin must be connected to no more than (V–) + 0.8V. To enable the amplifier, either allow the Enable pin to float or connect it to at least (V–) + 2.5V.

The Enable pin is referenced to the negative supply (V–). Therefore, shutdown operation is slightly different in single-supply and dual-supply applications.

In single-supply operation, V– typically equals common ground, thus the enable/disable logic signal and the OPA569 Enable pin are referenced to the same potential. In this configuration, the logic level and the OPA569 Enable pin can simply be tied together. Disable occurs for voltage levels of less than 0.8V. The OPA569 is enabled at logic levels greater than 2.5V.

In dual-supply operation, the logic level is referenced to a logic ground. However, the OPA569 Enable pin is still referenced to V–. To disable the OPA569, the voltage level of the logic signal needs to be level-shifted. This can be done using an optocoupler, as shown in Figure 5.

Examples of output behavior during disabled and enabled conditions with various load impedances are shown in the typical characteristics section. Please note that this behavior is a function of board layout, load impedances and bypass strategies. For sensitive loads, the use of a low-pass filter or other protection strategy is recommended.

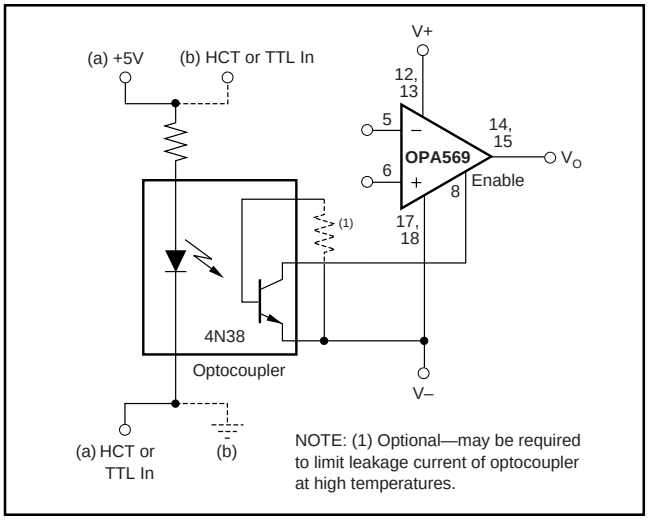


FIGURE 5. OPA569 Shutdown Configuration for Dual Supplies.

ENSURING MICROCONTROLLER COMPATIBILITY

Not all microcontrollers output the same logic state after power-up or reset. 8051-type microcontrollers, for example, output logic HIGH levels on their ports while other models power up with logic LOW levels after reset.

In configuration (a) shown in Figure 5, the enable/disable signal is applied on the cathode side of the photodiode within the optocoupler. A logic HIGH level causes the OPA569 to be enabled, and a logic LOW level disables the OPA569. In configuration (b) of Figure 5, with the logic signal applied on the anode side, a high level disables the OPA569 and a low level enables the op amp.

RAIL TO RAIL OUTPUT RANGE

The OPA569 has a class AB output stage with common source transistors that are used to achieve rail-to-rail output swing. It was designed to be able to swing closer to the rail than other existing linear amplifiers, even with high output current levels. A quick way to estimate the output swing with various output current requirements is by using the equation:

$$V_{SWING}\ [typical] = 0.1 \bullet I_O$$

Plots of the Output Swing vs Output Current, Supply Voltage, and Temperature are provided in the typical characteristics section.

RAIL TO RAIL INPUT RANGE

The input common-mode voltage range of the OPA569 extends 100mV beyond the supply rails. This is achieved by a complementary input stage with an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel input pair is active for input voltages close to the positive rail while the P-channel input pair is active for input voltages close to the negative rail. The transition point is typically at (V+) – 1.3V, and there is a small transition region around the switching point where both transistors are on. It is important to note that the two input pairs can have offsets of different signs and magnitudes. Therefore, as the transition point is crossed, the offset of the amplifier changes. This offset shift accounts for the reduced common-mode rejection ratio over the full input common-mode range.

OUTPUT PROTECTION

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 6. Schottky rectifier diodes with a 3A or greater continuous rating are recommended.

THERMAL FLAG PIN

The OPA569 has thermal sensing circuitry that provides a warning signal when the die temperature exceeds safe limits. Unless the Thermal Flag is connected to the Enable pin, when this flag is triggered, the part continues to operate even though the junction temperature exceeds 150°C. This allows maximum usable operation in very harsh conditions but degrades reliability. The Thermal Flag pin can be used to provide for orderly system shutdown before failure occurs. It can be also used to evaluate the thermal environment to determine need for and appropriate design of a shutdown mechanism.

The thermal flag output signal is from a CMOS logic gate that switches from V+ to V– to indicate that the amplifier is in thermal limit. This flag output pin can source and sink up to 25µA. The Thermal Flag pin is HIGH during normal operation. Power dissipated in the amplifier will cause the junction temperature to rise. When the junction temperature exceeds 150°C, the Thermal Flag pin will go LOW, and remain LOW until the amplifier has cooled to 130°C. Despite this hysteresis, with a method of orderly shutdown, the Thermal Flag pin can cycle on and off, depending on load and signal conditions. This limits the dissipation of the amplifier but may have an undesirable effect on the load. This temperature range exceeds the absolute maximum temperature rating and is intended to protect the device from excessive temperatures that can cause damage. Brief and infrequent excursions in this temperature range are likely to be tolerated, but are not recommended.

It is possible to connect the Thermal Flag pin directly to the Enable pin for automatic shutdown protection. When both thermal shutdown and the amplifier enable/disable functions are desired, the externally generated control signal and the Thermal Flag pin outputs should be combined with an AND gate, as shown on Figure 7. The temperature protection was designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the OPA569 in and out of thermal shutdown will degrade reliability.

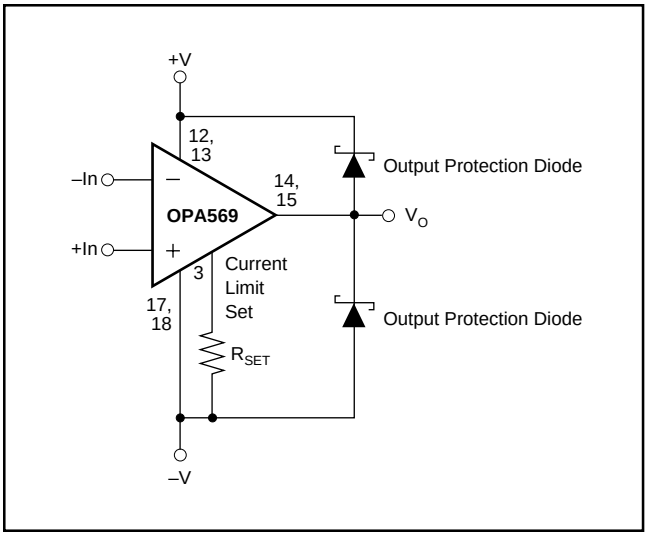


FIGURE 6. Output Protection Diode.

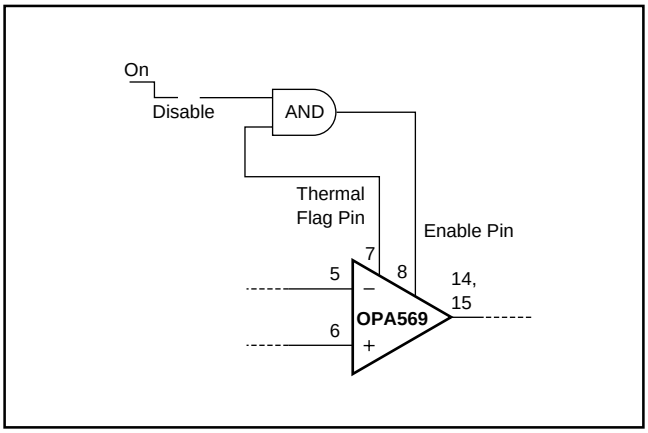


FIGURE 7. Enable/Shutdown Control Using Thermal Flag Pin and External Control Signal.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable, long term, continuous operation, the junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loading and signal conditions. For good, long-term reliability, thermal protection should trigger more than 25°C above the maximum expected ambient conditions of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

Fast transients of large output current swings (for example switching quickly from sourcing 2A to sinking 2A) may cause a glitch on the Thermal Flag pin. When switching large currents is expected, the use of extra bypass between the supplies or a low-pass filter on the Thermal Flag pin is recommended.

POWER DISSIPATION AND SAFE OPERATING AREA

Power dissipation depends on power supply, signal and load conditions. It is dominated by the power dissipation of the output transistors. For DC signals, power dissipation is equal to the product of output current, I_{OUT} and the output voltage across the conducting output transistor (V_S-V_{OUT}). Dissipation with AC signals is lower. Application Bulletin AB-039 (SBOA022) explains how to calculate or measure power dissipation with unusual signals and loads and can be found at the TI web site (www.ti.com).

Output short-circuits are particularly demanding for the amplifier because the full supply voltage is seen across the conducting transistor. It is very important to note that the temperature protection will not shut the part down in over-temperature conditions, unless the Thermal Flag pin is connected to the Enable pin; see the section on Thermal Flag.

Figure 8 shows the safe operating area at room temperature with various heatsinking efforts. Note that the safe output current decreases as (V_S – V_{OUT}) increases. Figure 9 shows the safe operating area at various temperatures with the PowerPAD being soldered to a 2 oz copper pad.

The power that can be safely dissipated in the package is related to the ambient temperature and the heatsink design. The PowerPAD package was specifically designed to provide excellent power dissipation, but board layout greatly influences the heat dissipation of the package. Refer to the “PowerPAD Thermally Enhanced Package” section for further details.

The OPA569 has a junction-to-ambient thermal resistance (θ_{JA}) value of 21.6°C/W when soldered to 2oz copper plane. This value can be further decreased to 12°C/W by the addition of forced air. Figure 10 shows the junction-to-ambient thermal resistance of the DWP-20 package.

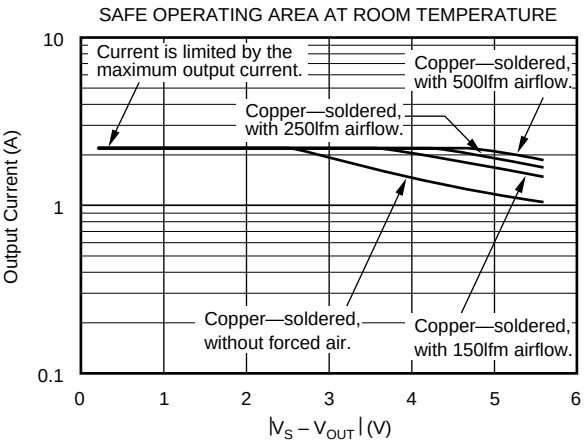


FIGURE 8. Safe Operating Area at Room Temperature.

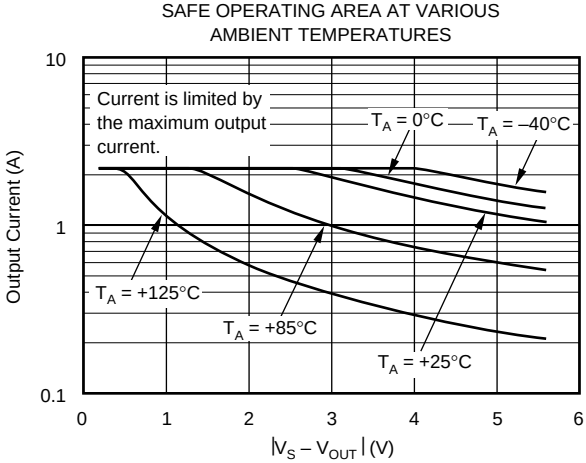


FIGURE 9. Safe Operating Area at Various Ambient Temperatures. PowerPAD soldered to a 2oz copper pad.

HEATSINKING METHOD	θ_{JA}
The part is soldered to a 2 oz copper pad under the exposed pad.	21.6
Soldered to copper pad with forced airflow (150lfm).	15.1
Soldered to copper pad with forced airflow (250lfm).	13.2
Soldered to copper pad with forced airflow (500lfm).	12.0

FIGURE 10. Junction-to-Ambient Thermal Resistance with Various Heatsinking Efforts.

Junction temperature should be kept below 125°C for reliable operation. The junction temperature can be calculated by:

$$T_J = T_A + P_D\theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CA}$

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipated (W)

θ_{JA} = Junction-to-Ambient Thermal Resistance

θ_{JC} = Junction-to-Case Thermal Resistance

θ_{CA} = Case-to-Air Thermal Resistance

The Maximum Power Dissipation vs Temperature for the heatsinking methods listed in Figure 10 is shown in Figure 11.

To appropriately determine required heatsink area, required power dissipation should be calculated and the relationship between power dissipation and thermal resistance should be considered to minimize shutdown conditions and allow for proper long-term operation (junction temperature of 125°C). Once the heatsink area has been selected, worst-case load conditions should be tested to ensure proper thermal protection.

For applications with limited board size, refer to Figure 12 for the approximate thermal resistance relative to heatsink area. Increasing the heatsink area beyond 2in^2 provides little improvement in thermal resistance. To achieve the 21.5°C/W stated in the Electrical Characteristics, a copper plane size of 9in^2 was used. The SO-20 PowerPAD package is well suited for continuous power levels, as shown in Figure 11. Higher power levels may be achieved in applications with a low on/off duty cycle.

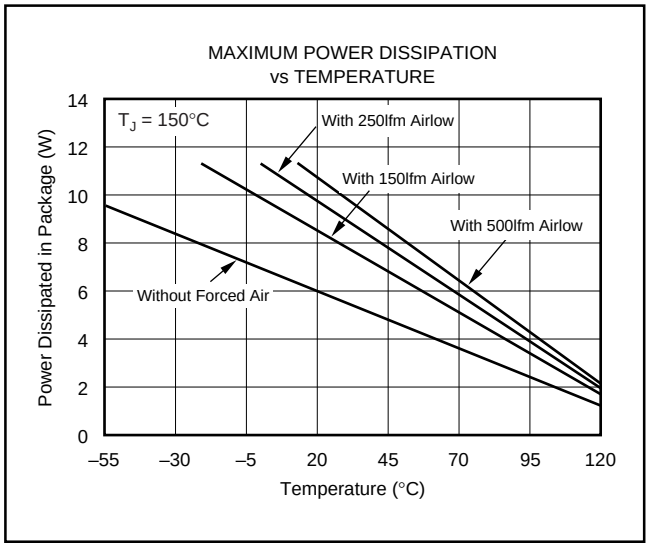


FIGURE 11. Maximum Power Dissipation vs Temperature.

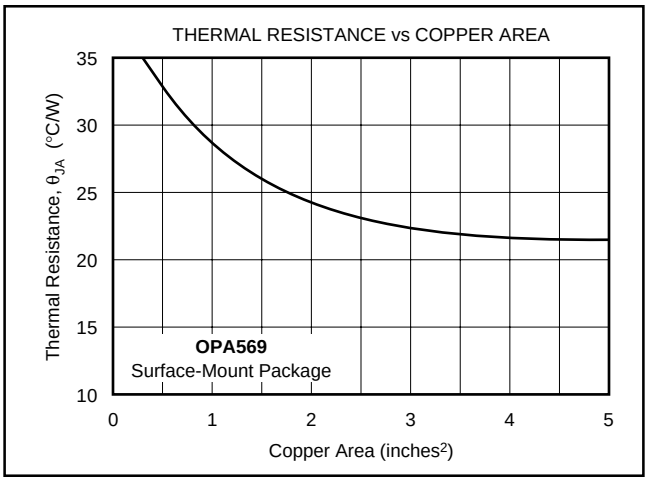


FIGURE 12. Thermal Resistance vs Circuit Board Copper Area.

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with higher impedance feedback networks (R_F > 50kΩ), it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 13. This capacitor compensates for the zero created by the feedback network impedance and the OPA569 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.

The size of the capacitor needed is estimated using the equation:

$$R_{IN} \bullet C_{IN} = R_F \bullet C_F$$

where C_{IN} is the sum of the input capacitance of the OPA569 plus the parasitic layout capacitance.

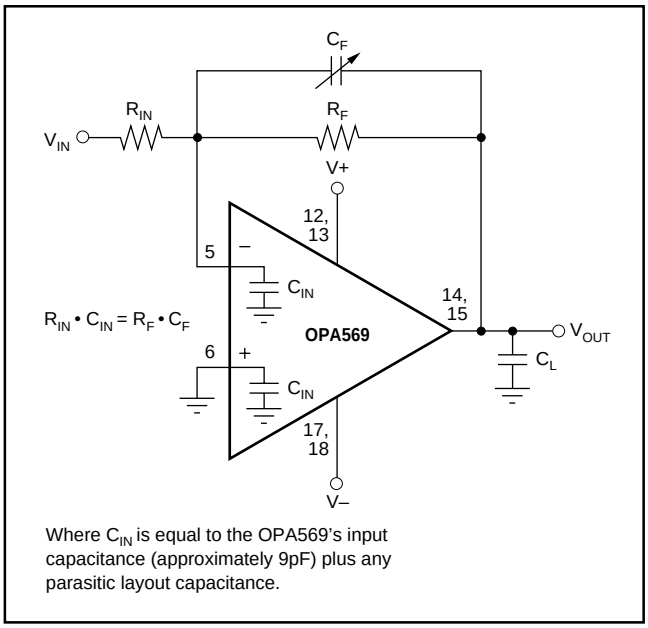


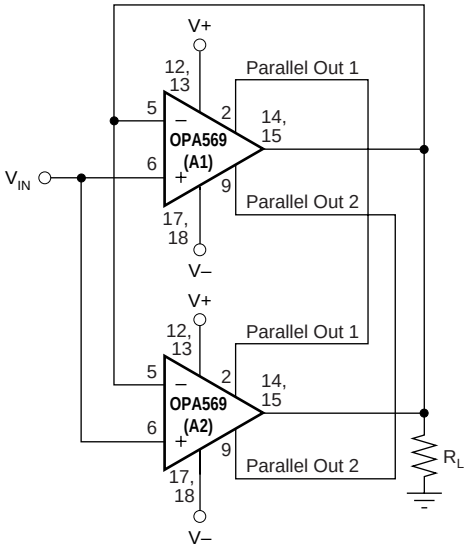
FIGURE 13. Feedback Capacitor for use with Higher Impedance Networks.

PARALLEL OPERATION

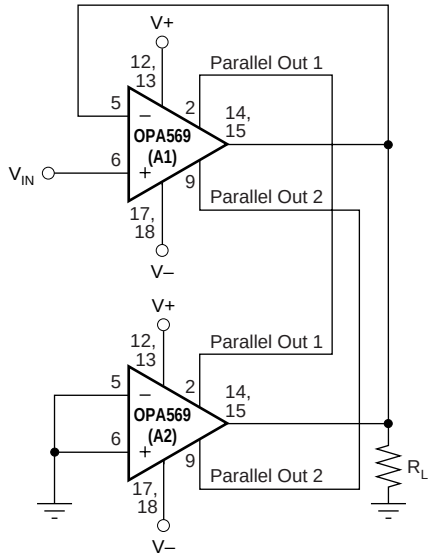
The OPA569 allows parallel operation of multiple op amps to extend output current capability or improve the output voltage swing to the rail. Special internal circuitry causes the load current to be shared equally between two (or more) op amps.

Figure 14 shows two ways to connect the input terminals. When the amplifier inputs are connected in parallel, the effective offset voltage is averaged and the bandwidth and slew rate performance are the same as that of a single amplifier. It is also possible to use one amplifier to be the "master" and connect the other inputs to a voltage within the common-mode input range of the amplifier; however, slew rate and bandwidth performance will be degraded.

For best performance, keep additional capacitance at the Parallel Out pins to a minimum and avoid routing these lines close to other lines that might see large voltage swings.



(a) Inputs connected in parallel.



(b) Amplifier A1 as "master", A2 as "slave".

FIGURE 14. Parallel Operation.

PowerPAD THERMALLY ENHANCED PACKAGE

The OPA569 uses the SO-20 PowerPAD package, a thermally enhanced, standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC, as shown in Figure 15. This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

Soldering the PowerPAD to the PCB ia always recommended, even with applications that have low power dissipation. This provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

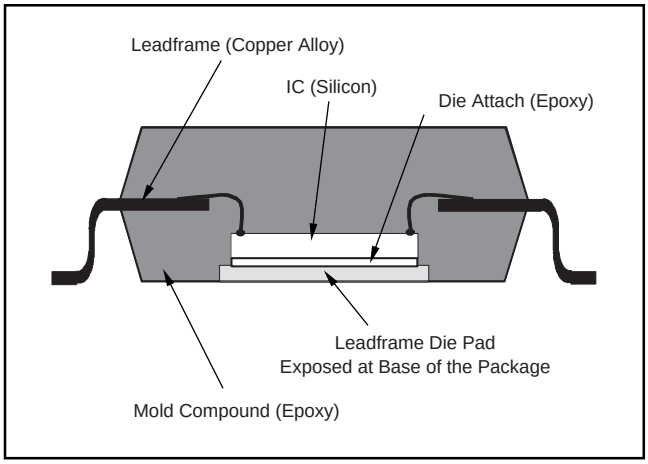


FIGURE 15. Section View of a PowerPAD Package.

PowerPAD Assembly Process

1. The PowerPAD must be connected to the most negative supply voltage of the device, which will be ground in single-supply applications and V– in split-supply applications.
2. Prepare the PCB with a top-side etch pattern, as shown in Figure 16. There should be etch for the leads as well as etch for the thermal land.
3. Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-20 PowerPAD package is 24, as shown in Figure 16.
4. It is recommended, but not required, to place a small number of additional holes under the package and outside the thermal pad area. These holes provide an additional heat path between the copper land and the ground plane. They may be larger because they are not in the area to be soldered, so wicking is not a problem. This is illustrated in Figure 16.

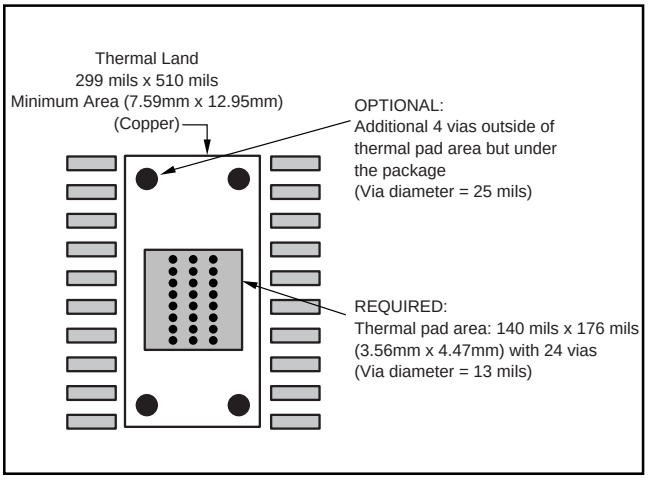


FIGURE 16. 20-Pin DWP PowerPAD PCB Etch and Via Pattern.

5. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single supply applications, and V– for split-supply applications.
6. When laying out these holes to the ground plane, do not use the typical web or spoke via connection methodology, as shown in Figure 17. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

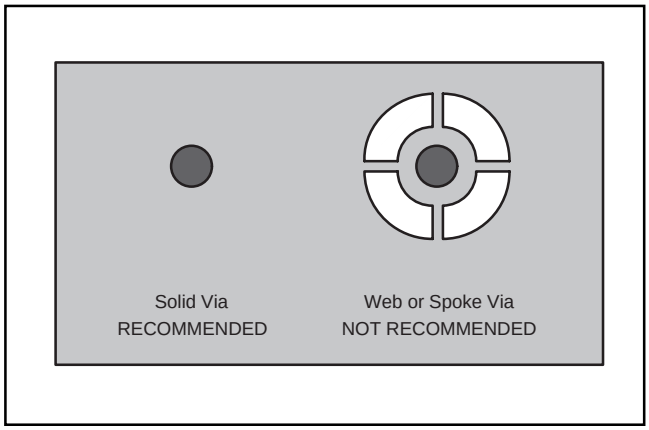


FIGURE 17. Via Connection.

7. The top-side solder mask should leave the terminals of the pad connections and the thermal pad area exposed. The thermal pad area should leave the 13 mil holes exposed. The larger holes outside the thermal pad area should be covered with solder mask.
8. Apply solder paste to the exposed thermal pad area and all of the package terminals.
9. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, please see Technical Brief SLMA002, “PowerPAD Thermally Enhanced Package,” located at www.ti.com.

LAYOUT GUIDELINES

The OPA569 is a power amplifier that requires proper layout for best performance. Figure 18 shows an example layout. Refinements to this example layout may be required based on assembly process requirements.

Keep power-supply leads as short as possible. This will keep inductance low and resistive losses at a minimum. A minimum of 18 gauge wire thickness is recommended for power-supply leads. The wire length should be less than 8 inches.

Proper power-supply bypassing with low ESR capacitors is essential to achieve good performance. A parallel combination of 100nF ceramic and 47μF tantalum bypass capacitors will provide low impedance over a wide frequency range. Bypass capacitors should be placed as close as practical to the power-supply pins of the OPA569.

PCB traces conducting high currents, such as from output to load or from the power-supply connector to the power-supply pins of the OPA569 should be kept as wide and short as possible.

The twenty-four holes in the landing pattern for the OPA569 are for the thermal vias that connect the PowerPAD of the OPA569 to the heatsink area on the PCB. The additional four larger vias further enhance the heat conduction into the heatsink area. All traces conducting high currents are very wide for lowest inductance and minimal resistive losses. Note that the negative supply (–V) pin on the OPA569 can be connected through the PowerPAD to allow for maximum trace width for high current paths.

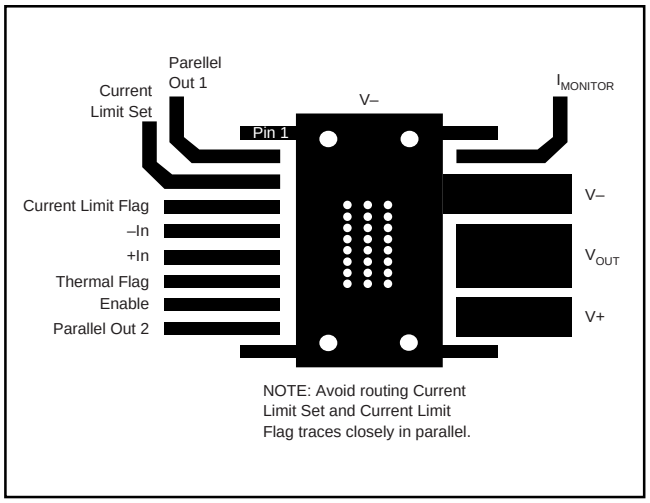


FIGURE 18. 20-Pin DWP PowerPAD PCB Etch and Via Pattern.

APPLICATION CIRCUITS

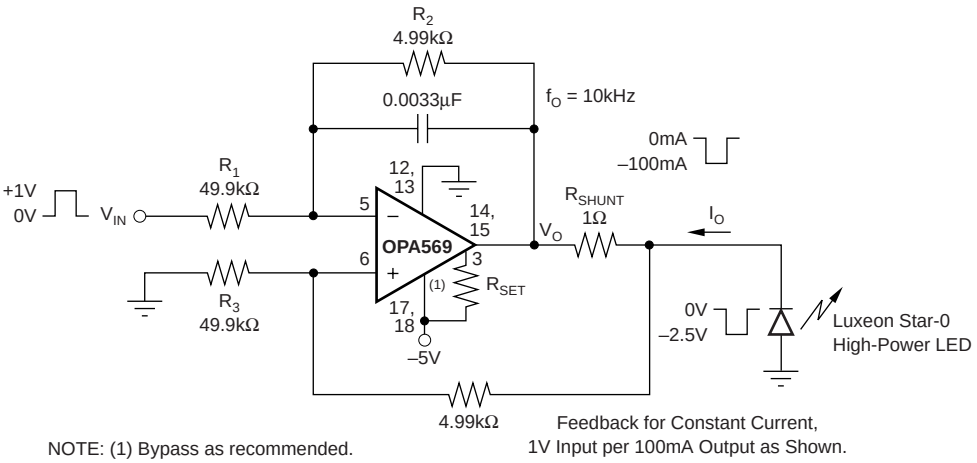


FIGURE 19. Grounded Anode LED Driver.

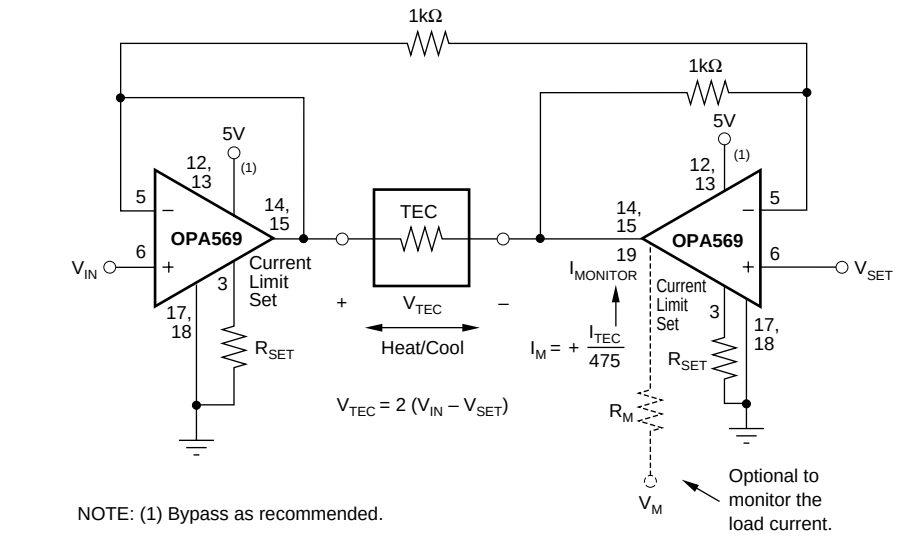


FIGURE 20. Bridge Tied Load Driver.

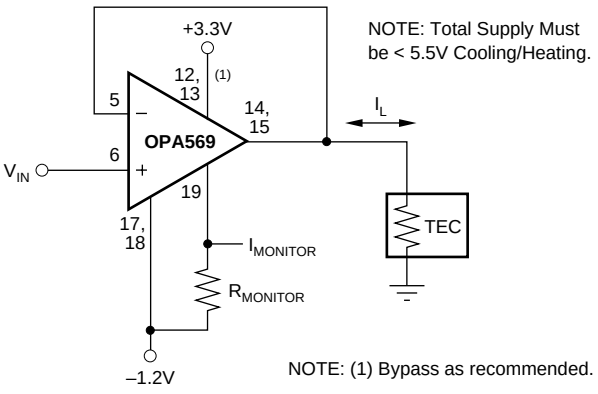
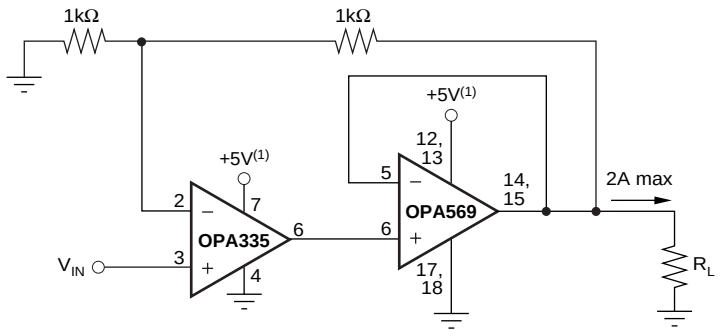
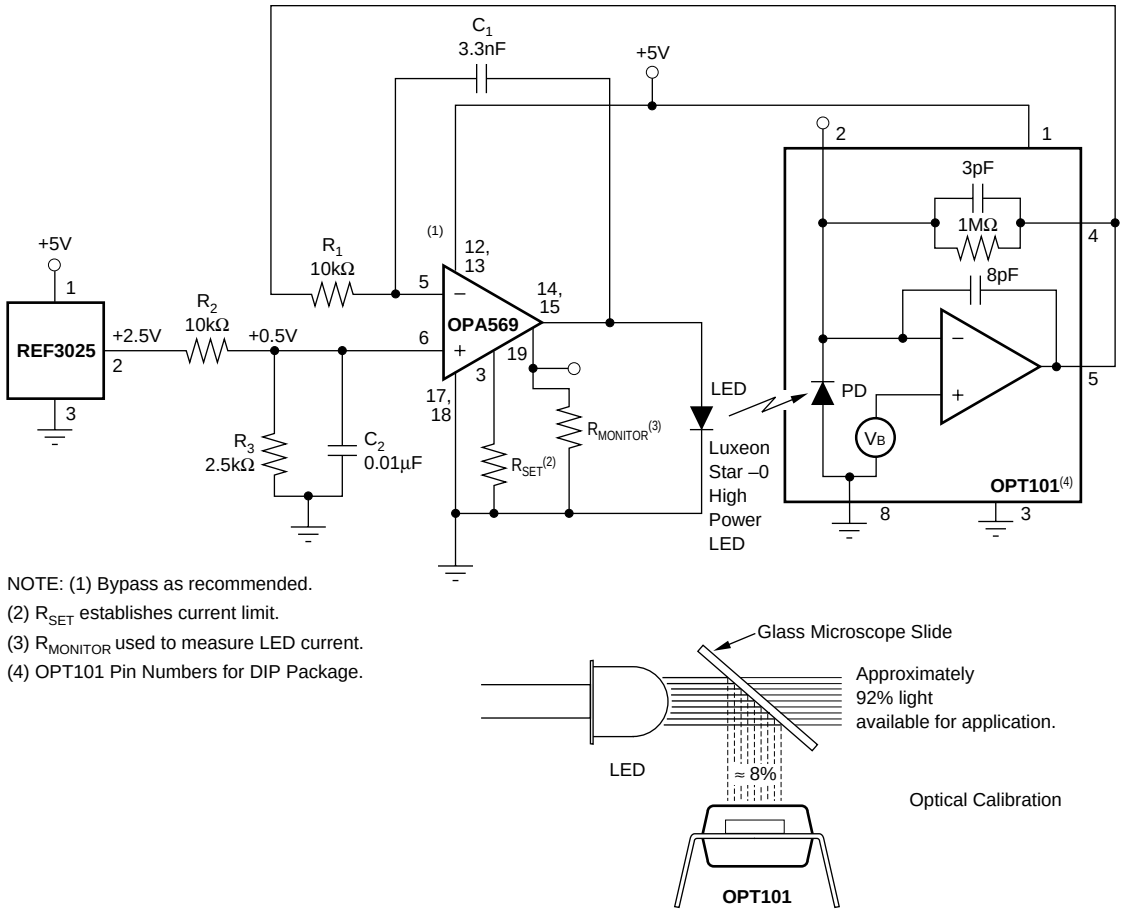


FIGURE 21. Single Power Amplifier Driving Bidirectional Current through a TEC using Asymmetrical Bipolar Power Supplies.



NOTE: (1) Bypass as recommended.

FIGURE 22. Power Booster for Precision Op Amp.



NOTE: (1) Bypass as recommended.
(2) R_{SET} establishes current limit.
(3) $R_{MONITOR}$ used to measure LED current.
(4) OPT101 Pin Numbers for DIP Package.

FIGURE 23. LED Output Regulation Circuit for Constant Optical Power.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA569AIDWP	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA569A	Samples
OPA569AIDWPG4	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA569A	Samples
OPA569AIDWPR	ACTIVE	SO PowerPAD	DWP	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	OPA569A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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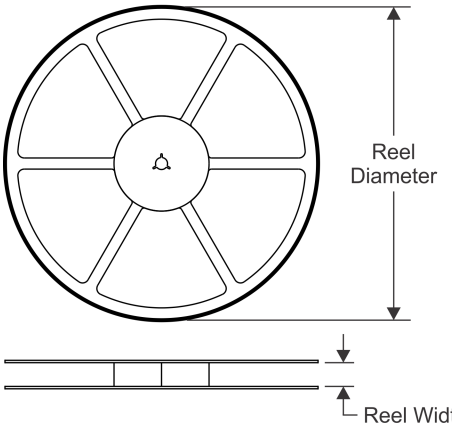
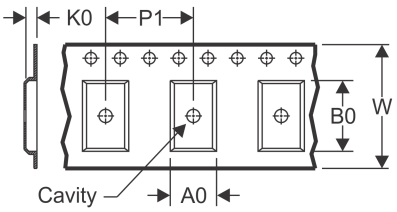
REEL DIMENSIONS

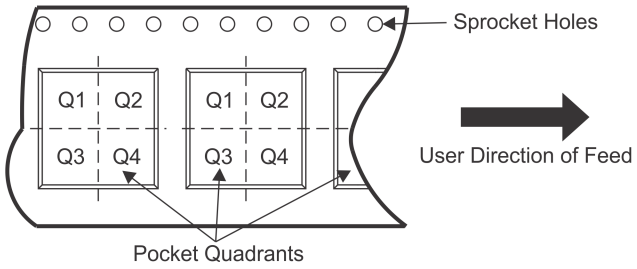


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

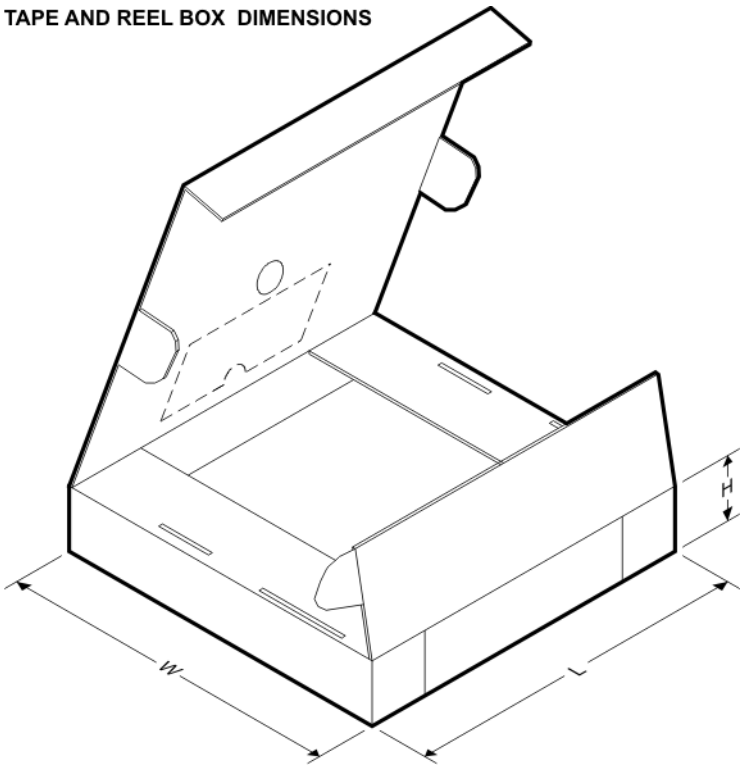
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA569AIDWPR	SO Power PAD	DWP	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

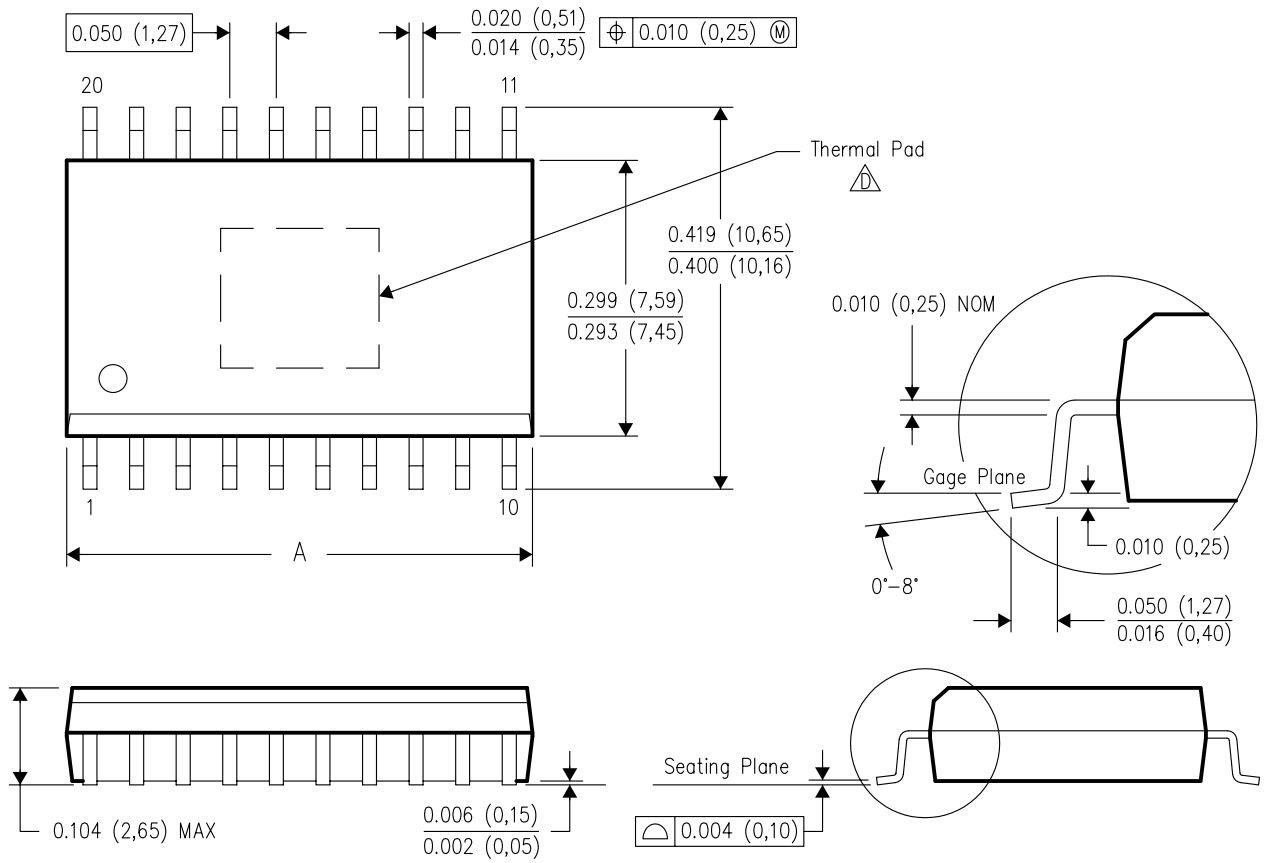


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA569AIDWPR	SO PowerPAD	DWP	20	1000	367.0	367.0	45.0

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

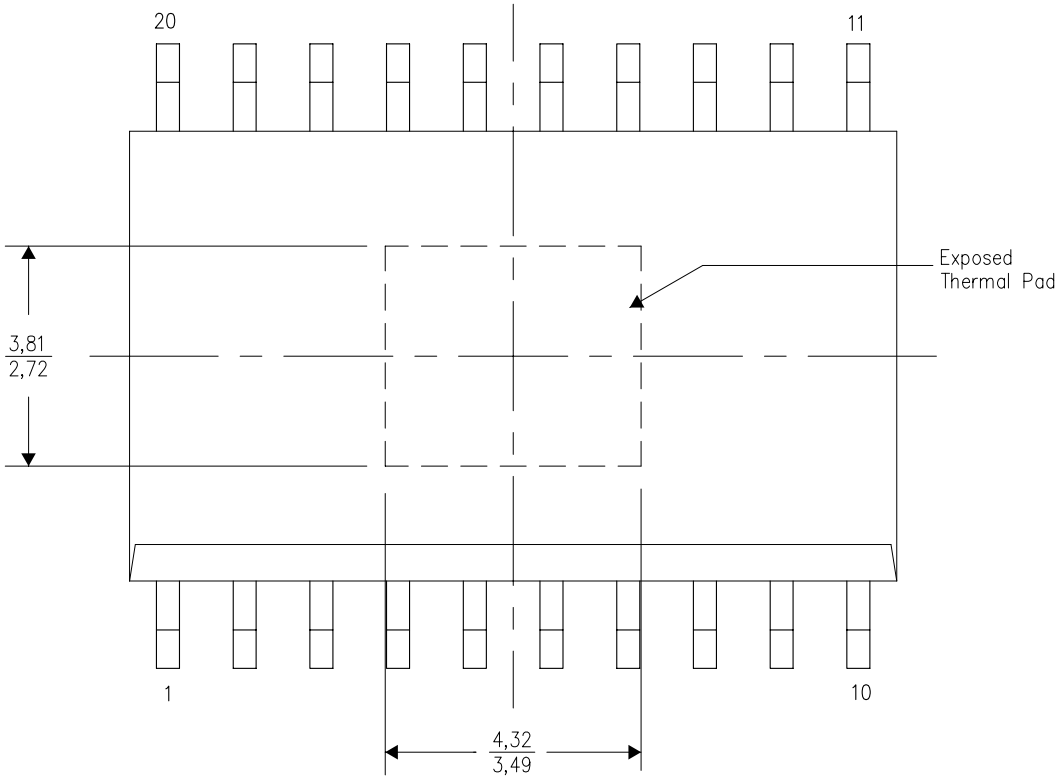
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206325–2/E 12/10

NOTE: A. All linear dimensions are in millimeters

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