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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

SEMICONDUCTOR™

NC7WZ86
TinyLogic® UHS Dual 2-Input Exclusive-OR Gate

General Description

The NC7WZ86 is a dual 2-Input Exclusive-OR Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Features

■ Space saving US8 surface mount package
■ MicroPak™ Pb-Free leadless package
■ Ultra High Speed; t_{PD} 2.9 ns typ into 50 pF at 5V V_{CC}
■ High Output Drive; ± 24 mA at 3V V_{CC}
■ Broad V_{CC} Operating Range; 1.65V to 5.5V
■ Matches the performance of LCX when operated at 3.3V
■ Power down high impedance inputs/output
■ Overvoltage tolerant inputs facilitate 5V to 3V translation
■ Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ86K8X	MAB08A	WZ86	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ86L8X	MAC08A	N7	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

Logic Symbol

IEEE/IEC
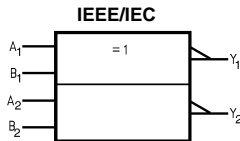
Pin Descriptions

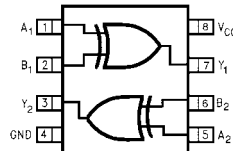| Pin Names	Description
A_n, B_n	Input
Y_n	Output

Function Table

$Y = A \oplus B$

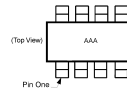| Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level   L = LOW Logic Level
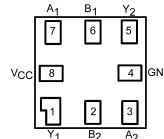
Connection Diagrams

(Top View)

Pin One Orientation Diagram

AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak

(Top Thru View)

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Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7V
DC Input Voltage (V_{IN})	−0.5V to +7V
DC Output Voltage (V_{OUT})	−0.5V to +7V
DC Input Diode Current (I_{IK})	
@V_{IN} < −0.5V	−50 mA
DC Output Diode Current (I_{OK})	
@V_{OUT} < −0.5V	−50 mA
DC Output Current (I_{OUT})	± 50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 100 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L);	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	250 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 1.8V ± 0.15V, 2.5V ±0.2V	0 ns/V to 20 ns/V
V_{CC} = 3.3V ± 0.3V	0 ns/V to 10 ns/V
V_{CC} = 5.0V ± 0.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	250° C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused input must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V		
		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output Voltage	1.65	1.55	1.65		1.55		V	V_{IN} = V_{IH}, V_{IL}	I_{OH} = −100 µA
		2.3	2.2	2.3		2.2				
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29				I_{OH} = −4 mA
		2.3	1.9	2.15		1.9				I_{OH} = −8 mA
		3.0	2.4	2.80		2.4		V		I_{OH} = −16 mA
		3.0	2.3	2.68		2.3				I_{OH} = −24 mA
		4.5	3.8	4.20		3.8				I_{OH} = −32 mA
V_{OL}	LOW Level Output Voltage	1.65		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 µA
		2.3		0.0	0.1		0.1			
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24			I_{OL} = 4 mA
		2.3		0.10	0.3		0.3			I_{OL} = 8 mA
		3.0		0.15	0.4		0.4	V		I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	0 to 5.5			±0.1		±1	µA	V_{IN} = 5.5V, GND	
I_{OFF}	Power Off Leakage Current	0.0			1		10	µA	V_{IN} or V_{OUT} = 5.5V	
I_{CC}	Quiescent Supply Current	1.65 to 5.5			1		10	µA	V_{IN} = 5.5V, GND	

AC Electrical Characteristics

| Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PLH}, t_{PHL}	Propagation Delay	1.8 ± 0.15	2.0	6.7	12.5	2.0	13.0	ns	$C_L = 15$ pF, $R_L = 1$ MΩ	Figures 1, 3
		2.5 ± 0.2	1.2	4.1	7.0	1.2	7.5			
		3.3 ± 0.3	0.8	3.0	4.8	0.8	5.2			
		5.0 ± 0.5	0.5	2.2	3.5	0.5	3.8			
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ± 0.3	1.2	3.8	5.4	1.2	5.9	ns	$C_L = 50$ pF, $R_L = 500\Omega$	Figures 1, 3
		5.0 ± 0.5	0.8	2.9	4.2	1.0	4.6			
C_{IN}	Input Capacitance	0		2.5				pF		
C_{PD}	Power Dissipation Capacitance	3.3		15				pF	(Note 3)	Figure 2
		5.0		19						

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

$I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.
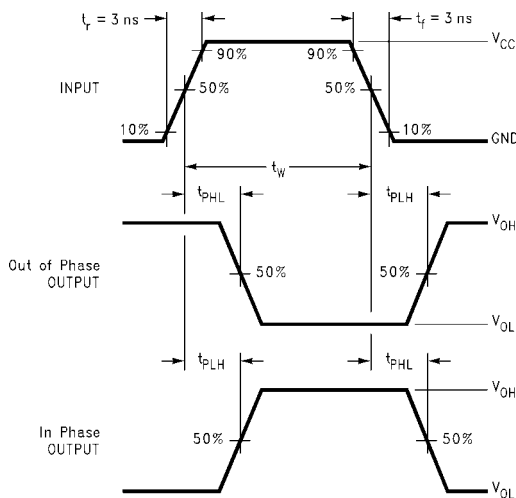
AC Loading and Waveforms
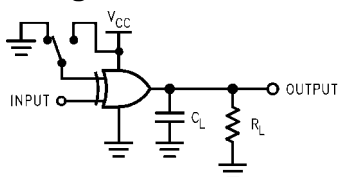
C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit
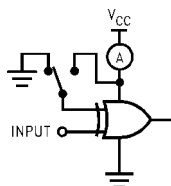
Input = AC Waveform; $t_r = t_f = 1.8$ ns;

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit
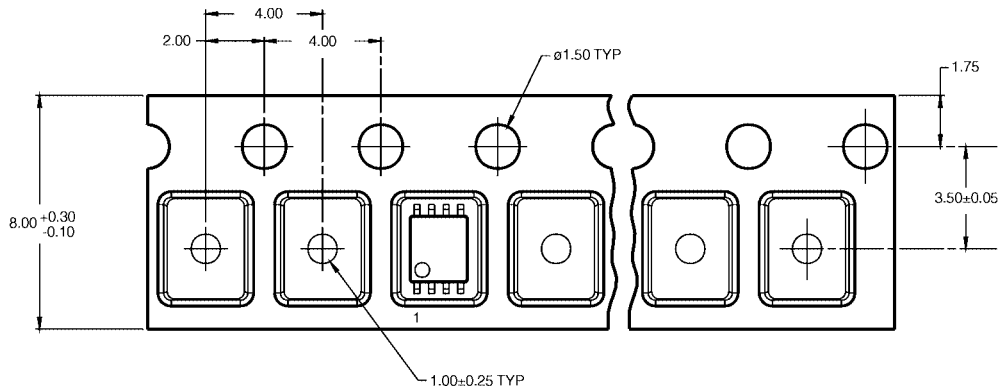

FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

| Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

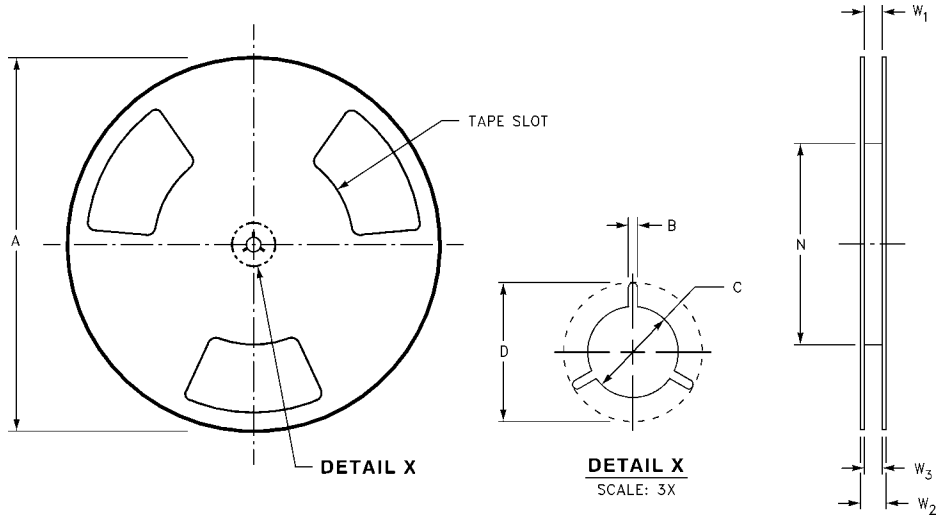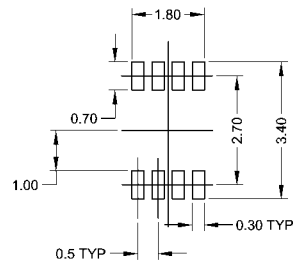**TAPE DIMENSIONS** inches (millimeters)

TAPE FORMAT for MicroPak

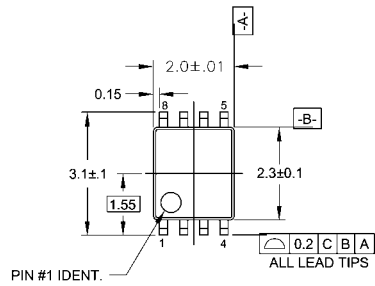| Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)
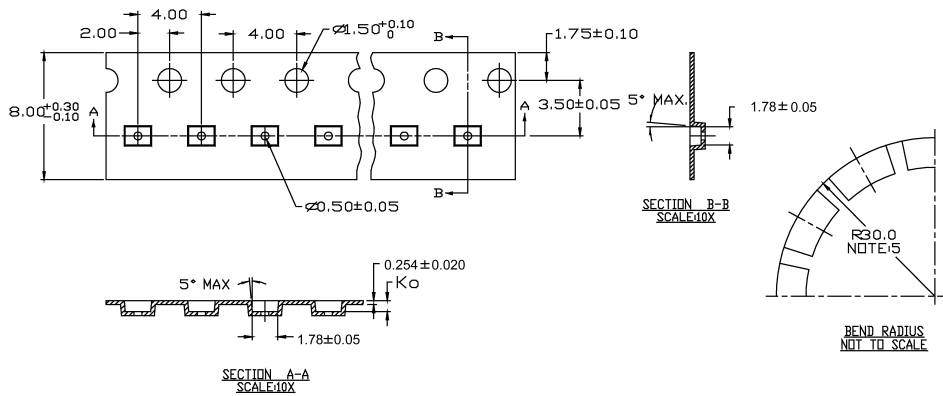
Tape and Reel Specification (Continued)
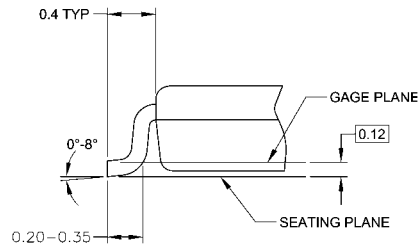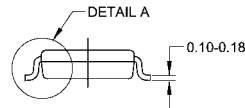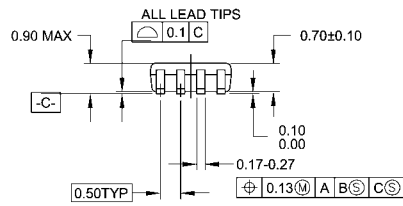
REEL DIMENSIONS inches (millimeters)

TAPE SLOT

DETAIL X

B

C

D

DETAIL X
SCALE: 3X

W₁

N

W₃

W₂

Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted

-A-

2.0±.01

0.15

8   5

-B-

3.1±.1

1.55

2.3±0.1

1   4

⌒ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1.80

0.70

1.00

2.70

3.40

0.30 TYP

0.5 TYP

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
⌒ 0.1 C

0.90 MAX

-C-

0.70±0.10

0.10
0.00

0.17-0.27

0.50TYP

⊕ 0.13 Ⓜ A BⓈ CⓈ

DETAIL A

0.10-0.18

0.4 TYP

0°-8°

GAGE PLANE

0.12

0.20−0.35

SEATING PLANE

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
   AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

2X ⌒ 0.10 C

B ▸ 1.6 A

1.6

INDEX AREA

2X ⌒ 0.10 C

TOP VIEW

(0.8)
(0.625)
(0.375)
(0.125)

(0.805)
(0.41)
(0.125)

(0.4)8X

(0.25)8X

Recommended Landpattern

0.55 MAX

∥ 0.05 C

0.05
0.00

C ⌒ 0.05 C

1.0

8X(0.09)

0.5

4 (0.1)

8   4

8X 0.35
0.25

0.15 8X
0.25

3X(0.2)

⊕ 0.10 Ⓜ C A B
0.05 Ⓜ C

BOTTOM VIEW
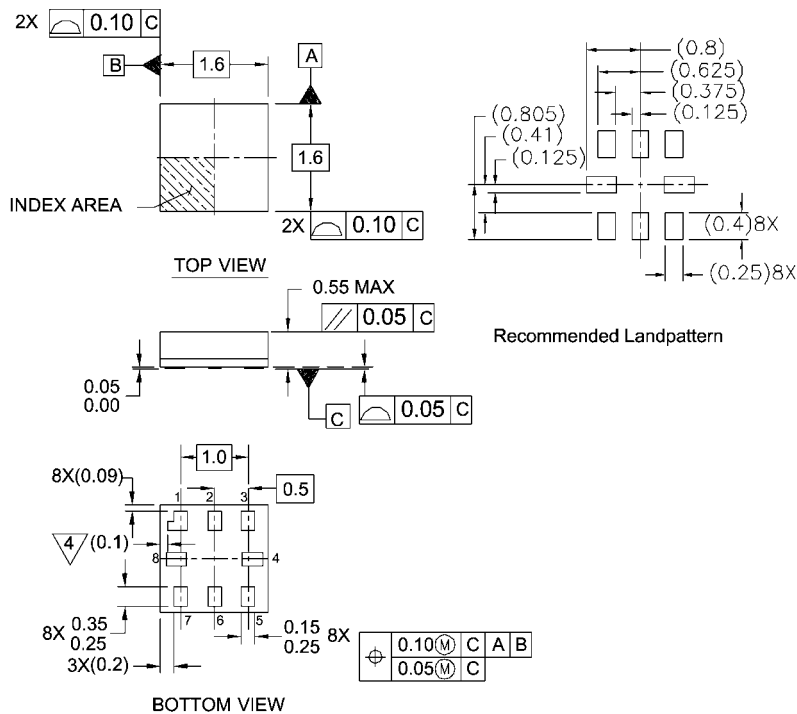
Notes:
1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

**Pb-Free 8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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