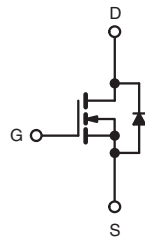
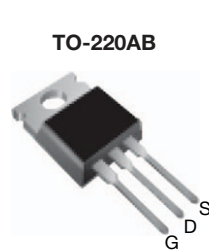


Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	500	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V	0.450
Q_g (Max.) (nC)	81	
Q_{gs} (nC)	20	
Q_{gd} (nC)	36	
Configuration	Single	



N-Channel MOSFET

FEATURES

- Lower Gate Charge Q_g Results in Simpler Drive Requirements
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage
- Compliant to RoHS Directive 2002/95/EC



APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supplies
- High Speed Power Switching

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFB13N50APbF
	SiHFB13N50A-E3
SnPb	IRFB13N50A
	SiHFB13N50A


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-Source Voltage	V_{DS}		500	V	
Gate-Source Voltage	V_{GS}		± 30		
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25$ °C	14	A	
		$T_C = 100$ °C	9.1		
Pulsed Drain Current ^a	I_{DM}		56		
Linear Derating Factor			2.0	W/°C	
Single Pulse Avalanche Energy ^b	E_{AS}		560	mJ	
Avalanche Current ^a	I_{AR}		14	A	
Repetitive Avalanche Energy ^a	E_{AR}		25	mJ	
Maximum Power Dissipation	$T_C = 25$ °C		P_D	250	W
Peak Diode Recovery dV/dt ^c			dV/dt	9.2	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}		- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d		
Mounting Torque	6-32 or M3 screw		10		lbf · in
			1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 5.7$ mH, $R_g = 25$ Ω , $I_{AS} = 14$ A, $dV/dt = 7.6$ V/ns (see fig. 12a).
- $I_{SD} \leq 14$ A, $dI/dt \leq 250$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

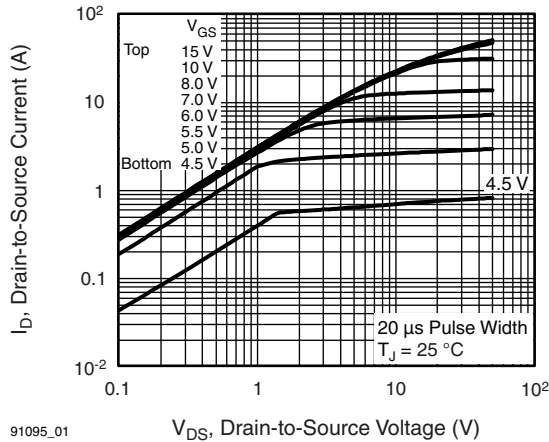
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greasd Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.50	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$	-	0.55	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 8.4\text{ A}^b$	-	-	0.450	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}$	8.1	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5	-	1910	-	pF	
Output Capacitance	C_{oss}		-	290	-		
Reverse Transfer Capacitance	C_{rss}		-	11	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2730	-	
			$V_{DS} = 400\text{ V}, f = 1.0\text{ MHz}$	-	82	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{DS} = 0\text{ V to } 400\text{ V}^c$	-	160	-		
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 14\text{ A}, V_{DS} = 400\text{ V},$ see fig. 6 and 13 ^b	-	-	81	nC
Gate-Source Charge	Q_{gs}			-	-	20	
Gate-Drain Charge	Q_{gd}			-	-	36	
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}$	$V_{DD} = 250\text{ V}, I_D = 14\text{ A},$ $R_g = 7.5\text{ }\Omega,$ see fig. 10 ^b	-	15	-	ns
Rise Time	t_r			-	39	-	
Turn-Off Delay Time	$t_{d(off)}$			-	39	-	
Fall Time	t_f			-	31	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	56		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 14\text{ A},$ $T_J = 125\text{ }^\circ\text{C}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	370	550	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	4.4	6.5	μC	
Body Diode Reverse Recovery Current	I_{RRM}		-	21	31	A	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

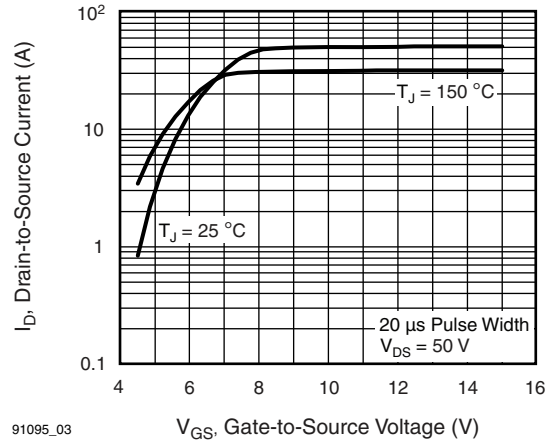
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



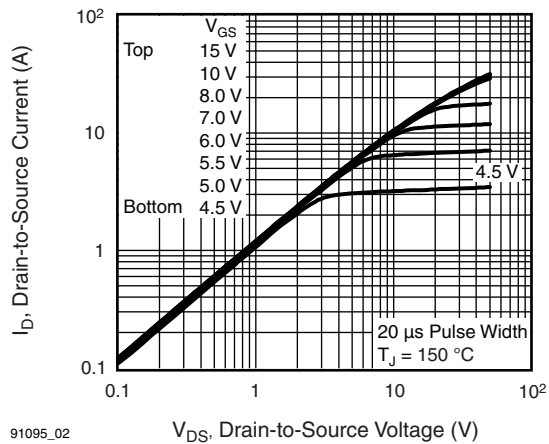
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Fig. 1 - Typical Output Characteristics



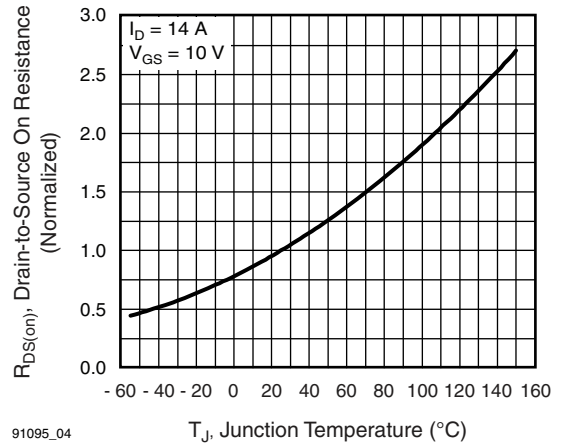
91095_03

Fig. 3 - Typical Transfer Characteristics



91095_02

Fig. 2 - Typical Output Characteristics



91095_04

Fig. 4 - Normalized On-Resistance vs. Temperature

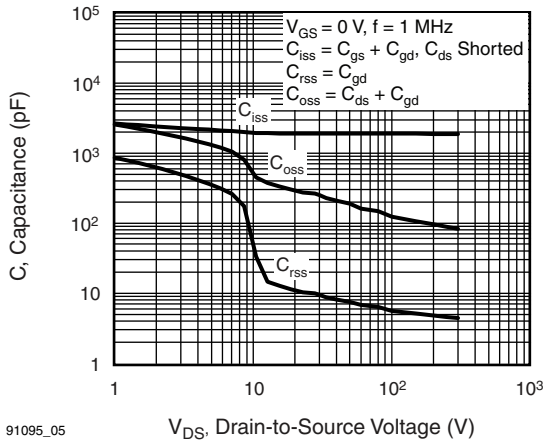


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

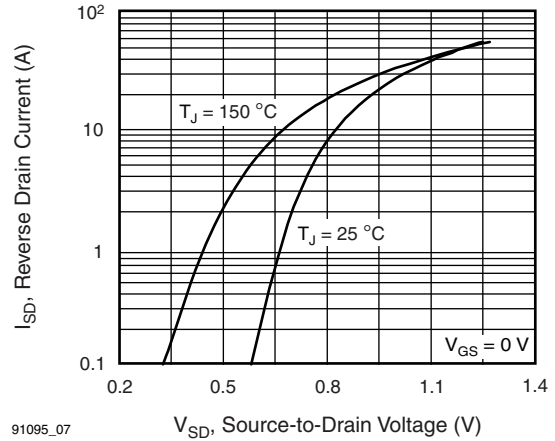


Fig. 7 - Typical Source-Drain Diode Forward Voltage

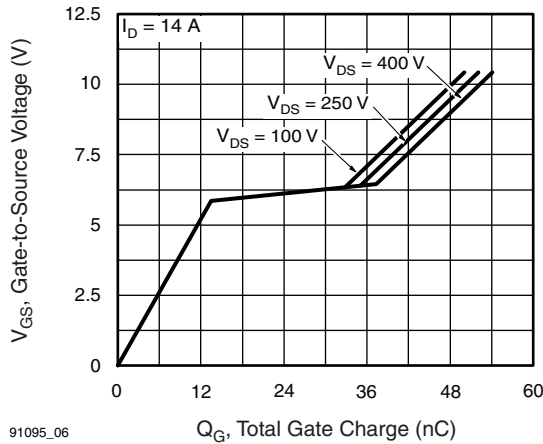


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

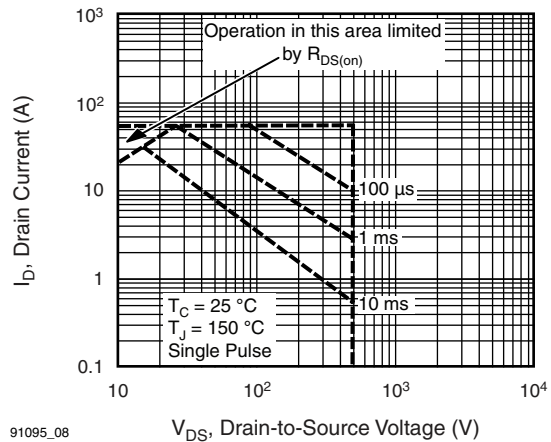
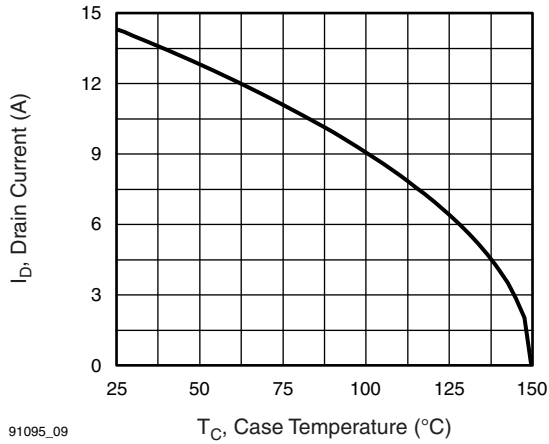


Fig. 8 - Maximum Safe Operating Area



91095_09

Fig. 9 - Maximum Drain Current vs. Case Temperature

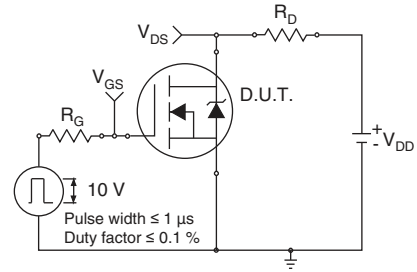


Fig. 10a - Switching Time Test Circuit

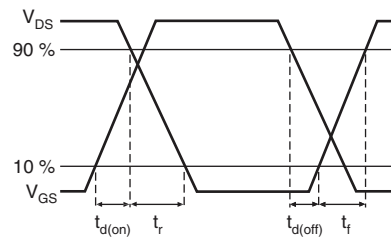
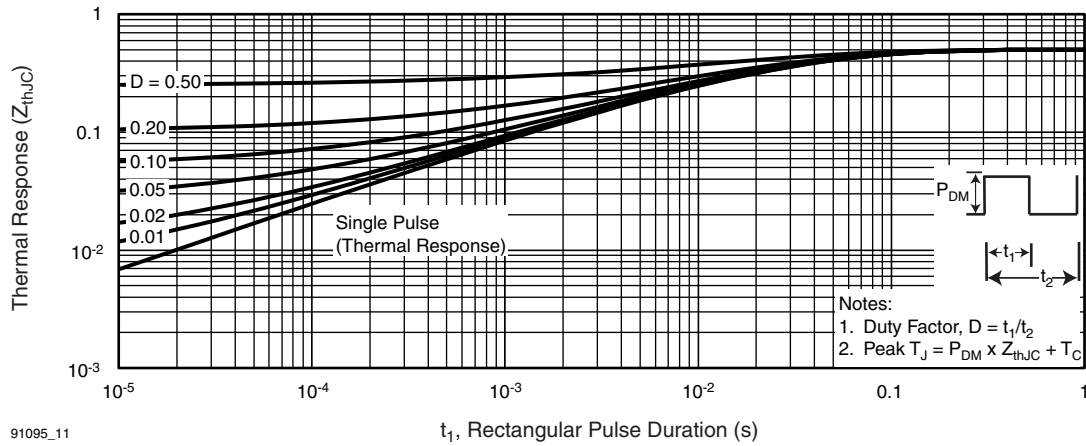


Fig. 10b - Switching Time Waveforms



91095_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

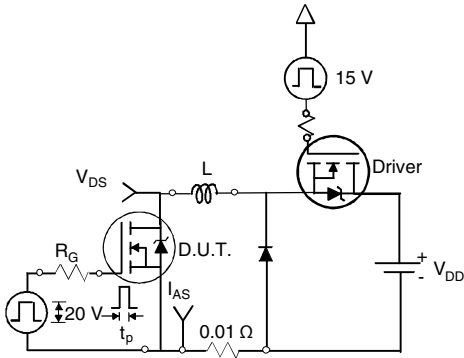


Fig. 12a - Unclamped Inductive Test Circuit

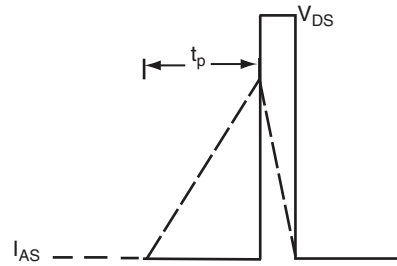


Fig. 12b - Unclamped Inductive Waveforms

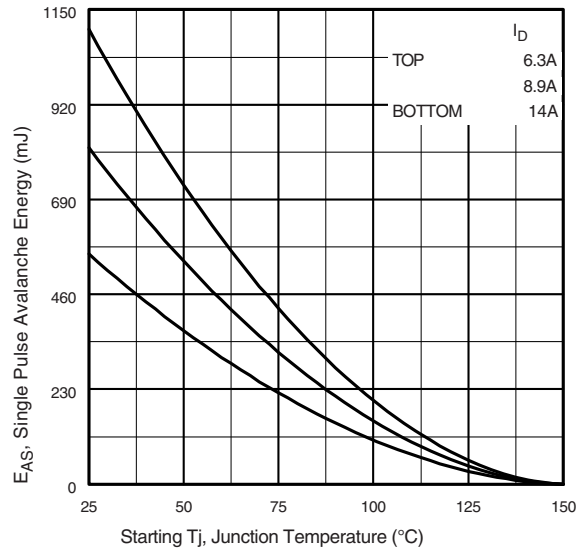


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

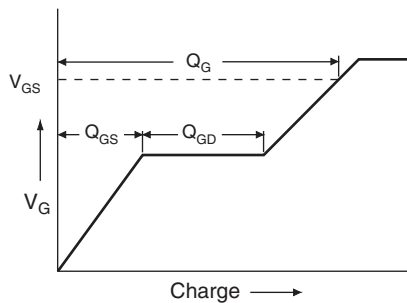


Fig. 13a - Basic Gate Charge Waveform

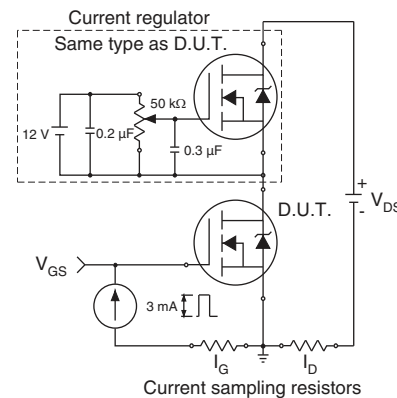
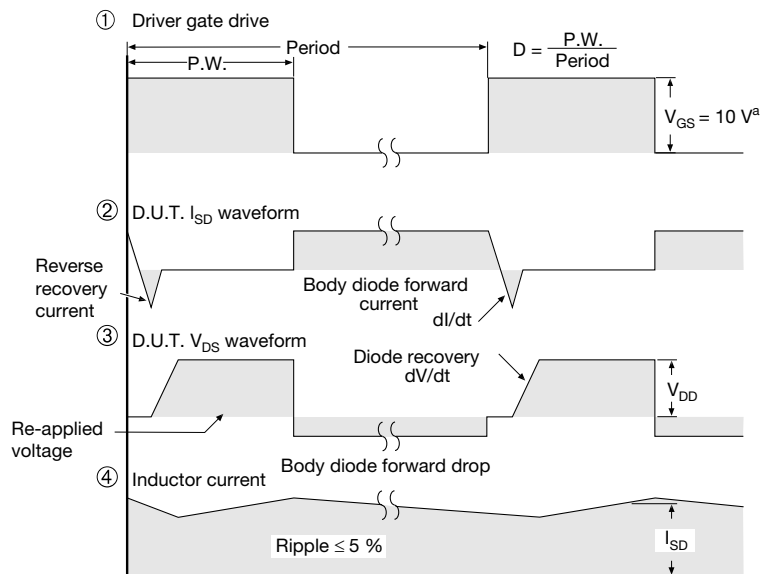
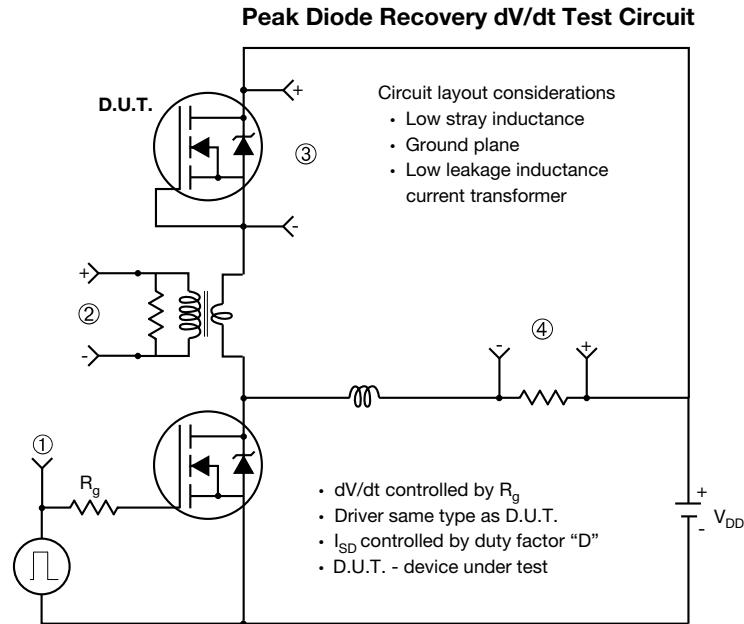


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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IRFB13N50A, SiHFB13N50A

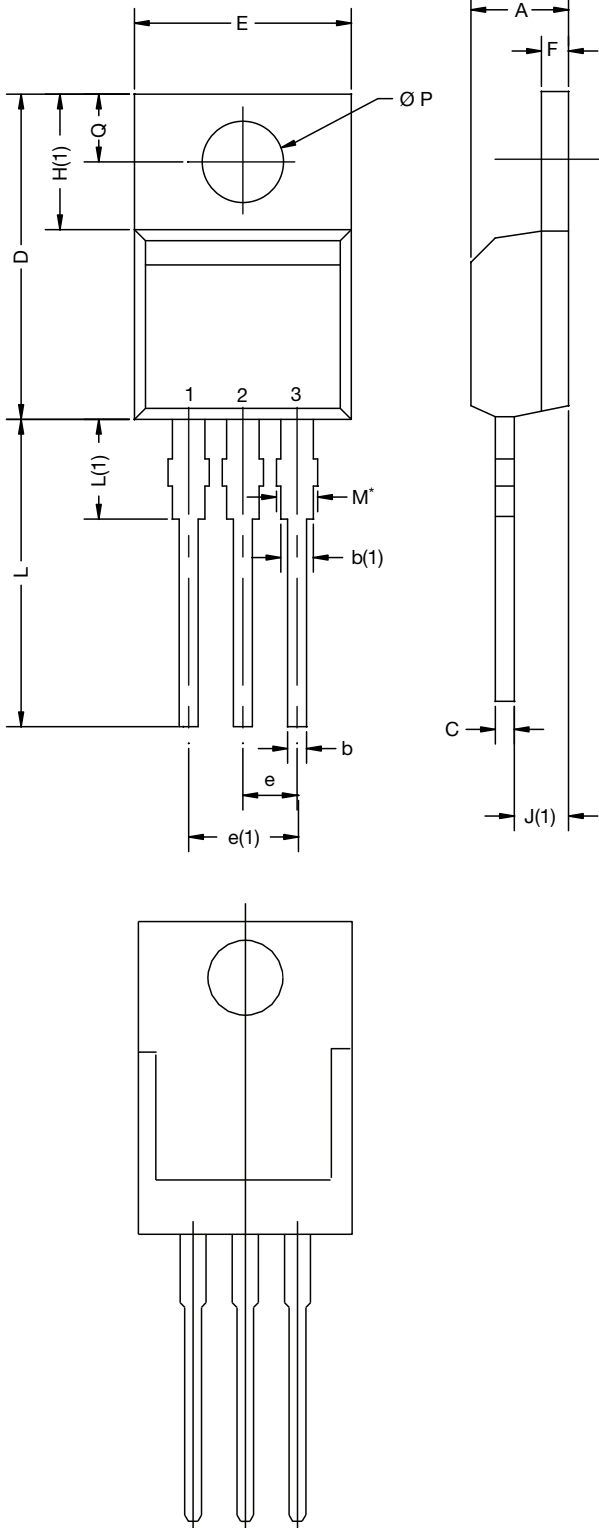
Vishay Siliconix



reliability data, see www.vishay.com/ppg?91095.



TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.14	4.70	0.163	0.185
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.32	15.86	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	0.51	1.40	0.020	0.055
H(1)	6.10	6.70	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.05	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118

ECN: X15-0339-Rev. B, 02-Nov-15
DWG: 6031

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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