

TMS320C5515 Fixed-Point Digital Signal Processor

Check for Samples: [TMS320C5515](#)

1 Fixed-Point Digital Signal Processor

1.1 Features

- **High-Performance, Low-Power, TMS320C55x™ Fixed-Point Digital Signal Processor**
 - 16.67-, 13.33-, 10-, 8.33-ns Instruction Cycle Time
 - 60-, 75-, 100-, 120-MHz Clock Rate
 - One/Two Instructions Executed per Cycle
 - Dual Multipliers [Up to 200 or 240 Million Multiply-Accumulates per Second (MMACS)]
 - Two Arithmetic/Logic Units (ALUs)
 - Three Internal Data/Operand Read Buses and Two Internal Data/Operand Write Buses
 - Software-Compatible With C55x Devices
 - Industrial Temperature Devices Available
- **320K Bytes Zero-Wait State On-Chip RAM, Composed of:**
 - 64K Bytes of Dual-Access RAM (DARAM), 8 Blocks of 4K x 16-Bit
 - 256K Bytes of Single-Access RAM (SARAM), 32 Blocks of 4K x 16-Bit
- **128K Bytes of Zero Wait-State On-Chip ROM (4 Blocks of 16K x 16-Bit)**
- **4M x 16-Bit Maximum Addressable External Memory Space (SDRAM/mSDRAM)**
- **16-/8-Bit External Memory Interface (EMIF) with Glueless Interface to:**
 - 8-/16-Bit NAND Flash, 1- and 4-Bit ECC
 - 8-/16-Bit NOR Flash
 - Asynchronous Static RAM (SRAM)
 - SDRAM/mSDRAM (1.8-, 2.5-, 2.75-, and 3.3-V)
- **Direct Memory Access (DMA) Controller**
 - Four DMA With 4 Channels Each (16-Channels Total)
- **Three 32-Bit General-Purpose Timers**
 - One Selectable as a Watchdog and/or GP
- **Two MultiMedia Card/Secure Digital (MMC/SD) Interfaces**
- **Universal Asynchronous Receiver/Transmitter (UART)**
- **Serial-Port Interface (SPI) With Four Chip-Selects**
- **Master/Slave Inter-Integrated Circuit (I²C Bus™)**
- **Four Inter-IC Sound (I²S Bus™) for Data Transport**
- **Device USB Port With Integrated 2.0 High-Speed PHY that Supports:**
 - USB 2.0 Full- and High-Speed Device
- **LCD Bridge With Asynchronous Interface**
- **Tightly-Coupled FFT Hardware Accelerator**
- **10-Bit 4-Input Successive Approximation (SAR) ADC**
- **Real-Time Clock (RTC) With Crystal Input, With Separate Clock Domain and Power Supply**
- **Four Core Isolated Power Supply Domains: Analog, RTC, CPU and Peripherals, and USB**
- **Four I/O Isolated Power Supply Domains: RTC I/O, EMIF I/O, USB PHY, and DV_{DDIO}**
- **Three integrated LDOs (DSP_LDO, ANA_LDO, and USB_LDO) to power the isolated domains: DSP Core, Analog, and USB Core, respectively**
- **Low-Power S/W Programmable Phase-Locked Loop (PLL) Clock Generator**
- **On-Chip ROM Bootloader (RBL) to Boot From NAND Flash, NOR Flash, SPI EEPROM, SPI Serial Flash or I2C EEPROM**
- **IEEE-1149.1 (JTAG) Boundary-Scan-Compatible**
- **Up to 26 General-Purpose I/O (GPIO) Pins (Multiplexed With Other Device Functions)**
- **196-Terminal Pb-Free Plastic BGA (Ball Grid Array) (ZCH Suffix)**
- **1.05-V Core (60 or 75 MHz), 1.8-V, 2.5-V, 2.75-V, or 3.3-V I/Os**
- **1.3-V Core (100, 120 MHz), 1.8-V, 2.5-V, 2.75-V, or 3.3-V I/Os**



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1.2 Applications

- **Wireless Audio Devices (Headsets, Microphones, Speakerphones)**
- **Echo Cancellation Headphones**
- **Portable Medical Devices**
- **Voice Applications**
- **Industrial Controls**
- **Fingerprint Biometrics**
- **Software Defined Radio**

1.3 Description

The device is a member of TI's TMS320C5000™ fixed-point Digital Signal Processor (DSP) product family and is designed for low-power applications.

The fixed-point DSP is based on the TMS320C55x™ DSP generation CPU processor core. The C55x™ DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, one 32-bit data read bus and two 16-bit data read buses, two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four 16-bit data reads and two 16-bit data writes in a single cycle. The device also includes four DMA controllers, each with 4 channels, providing data movement for 16-independent channel contexts without CPU intervention. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication and a 32-bit add in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the Address Unit (AU) and Data Unit (DU) of the C55x CPU.

The C55x CPU supports a variable byte width instruction set for improved code density. The Instruction Unit (IU) performs 32-bit program fetches from internal or external memory and queues instructions for the Program Unit (PU). The Program Unit decodes the instructions, directs tasks to the Address Unit (AU) and Data Unit (DU) resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instructions.

The general-purpose input and output functions along with the 10-bit SAR ADC provide sufficient pins for status, interrupts, and bit I/O for LCD displays, keyboards, and media interfaces. Serial media is supported through two MultiMedia Card/Secure Digital (MMC/SD) peripherals, four Inter-IC Sound (I2S Bus™) modules, one Serial-Port Interface (SPI) with up to 4 chip selects, one I2C multi-master and slave interface, and a Universal Asynchronous Receiver/Transmitter (UART) interface.

The device peripheral set includes an external memory interface (EMIF) that provides glueless access to asynchronous memories like EPROM, NOR, NAND, and SRAM, as well as to high-speed, high-density memories such as synchronous DRAM (SDRAM) and mobile SDRAM (mSDRAM). Additional peripherals include: a high-speed Universal Serial Bus (USB2.0) device mode only, and a real-time clock (RTC). This device also includes three general-purpose timers with one configurable as a watchdog timer, and an analog phase-locked loop (APLL) clock generator.

In addition, the device includes a tightly-coupled FFT Hardware Accelerator. The tightly-coupled FFT Hardware Accelerator supports 8 to 1024-point (in power of 2) real and complex-valued FFTs.

Furthermore, the device includes three integrated LDOs (DSP_LDO, ANA_LDO, and USB_LDO) to power different sections of the device. The DSP_LDO can provide 1.3 V or 1.05 V to the DSP core (CV_{DD}), selectable on-the-fly by software as long as operating frequency ranges are observed. To allow for lowest power operation, the programmer can shutdown the internal DSP_LDO cutting power to the DSP core (CV_{DD}) while an external supply provides power to the RTC (CV_{DDRTC} and DV_{DDRTC}). The ANA_LDO is designed to provide 1.3 V to the DSP PLL (V_{DDA_PLL}), SAR, and power management circuits (V_{DDA_ANA}). The USB_LDO provides 1.3 V to USB core digital (USB_V_{DD1P3}) and PHY circuits (USB_V_{DDA1P3}). The RTC alarm interrupt or the WAKEUP pin can re-enable the internal DSP_LDO and re-apply power to the DSP core.

The device is supported by the industry's award-winning eXpressDSPTM, Code Composer StudioTM Integrated Development Environment (IDE), DSP/BIOSTM, Texas Instruments' algorithm standard, and the industry's largest third-party network. Code Composer Studio IDE features code generation tools including a C Compiler and Linker, RTDXTM, XDS100TM, XDS510TM, XDS560TM emulation device drivers, and evaluation modules. The device is also supported by the C55x DSP Library which features more than 50 foundational software kernels (FIR filters, IIR filters, FFTs, and various math functions) as well as chip support libraries.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

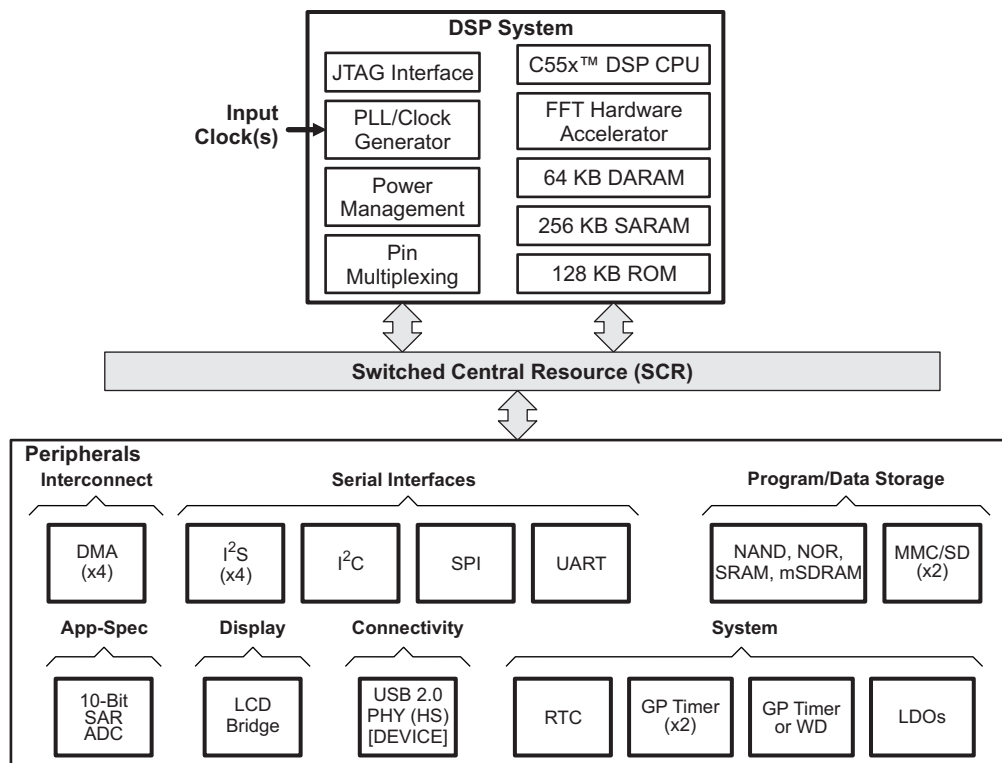


Figure 1-1. Functional Block Diagram

| | | | | | |
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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history highlights the technical changes made to the document.

Scope: Applicable updates to the TMS320C5000 device family, specifically relating to the device (Silicon Revisions 2.0) which is now in the production data (PD) stage of development have been incorporated.

| SEE | ADDITIONS/MODIFICATIONS/DELETIONS |
|--|--|
| Global | <ul style="list-style-type: none"> Added notes to clarify that CV_{DDRTC} must always be powered by an external power supply and none of the on-chip LDOs can power CV_{DDRTC}. |
| Section 2 Device Overview | Table 2-1, Characteristics of the C5515 Processor: <ul style="list-style-type: none"> Deleted Power Characterization Updated addresses for MMC/SD0 and MMC/SD1 in Table 2-4, Peripheral I/O-Space Control Registers. |
| Section 2.5 Terminal Functions | Table 2-7, RESET, Interrupts, and JTAG Terminal Functions: <ul style="list-style-type: none"> Deleted duplicate note on board design guidelines. Table 2-8, External Memory Interface (EMIF) Terminal Functions: <ul style="list-style-type: none"> Changed note for 16-bit asynchronous memory to connect EM_A[20:0] to memory address pins [21:1]. Table 2-13, USB2.0 Terminal Functions <ul style="list-style-type: none"> Added power-on information for USB_VBUS, USB_VDDA3P3, USB_VDDA1P3, and USB_VDD1P3. Table 2-20, Reserved and No Connects Terminal Functions: <ul style="list-style-type: none"> Updated RSV16 description to tie directly to V_{SS}. |
| Section 3 Device Configuration | <ul style="list-style-type: none"> Added note stating Device ID registers are reserved. Updated reset value for WU_DOUT from 0 to 1. Section 3.4, Boot Sequence: <ul style="list-style-type: none"> Added steps to set register configuration and copy boot image sections (steps 15 and 16). Changed Figure 3-2, Bootloader Software Architecture. Added reset default to pin multiplexing tables. |
| Section 4 Device Operating Conditions | Section 4.3 <ul style="list-style-type: none"> Added note for core (CV_{DD}) supply power (P). Updated ESD Stress Voltage value for HBM to > 1000 V and CDM to > 250 V. |
| Section 5.3 Power Supplies | <ul style="list-style-type: none"> Updated Section 5.3.1, Power-Supply Sequencing. |
| Section 5.5.1 PLL Device-Specific Information | Table 5-3, PLL Clock Frequency Ranges: <ul style="list-style-type: none"> Updated maximum value for PLL_LOCKTIME. |
| Section 5.8.2 Wake-Up From IDLE Electrical Data/Timing | Table 5-8, Timing Requirements for Wake-Up From IDLE: <ul style="list-style-type: none"> Changed minimum value to 30.5 μs from 10 ns. Table 5-9, Switching Characteristics Over Recommended Operating Conditions For Wake-Up From IDLE: <ul style="list-style-type: none"> Changed parameter description to, "Delay time, WAKEUP pulse complete to CPU active." Moved 2 to WAKEUP pulse complete from wake-up event high in Figure 5-14, Wake-Up From IDLE Timings. |
| Section 5.9 External Memory Interface (EMIF) | Global: <ul style="list-style-type: none"> Updated device limitations on EM_SDCLK when $DV_{DDEMIF} = 1.8$ V and 1.3 V. Added notes to timing and switching tables. |
| Section 5.11 Real-Time Clock (RTC) | <ul style="list-style-type: none"> Added to wake-up sequence in Section 5.11.1, RTC Only Mode. |
| Section 6 Device and Documentation Support | Moved documentation support to Section 7 from Section 3.6 and 3.7. |

2 Device Overview

2.1 Device Characteristics

[Table 2-1](#), provides an overview of the TMS320C5515 DSP. The tables show significant features of the device, including the capacity of on-chip RAM, the peripherals, the CPU frequency, and the package type with pin count. For more detailed information on the actual device part number and maximum device operating frequency, see [Section 6.1.2, Device and Development-Support Tool Nomenclature](#).

Table 2-1. Characteristics of the C5515 Processor

| HARDWARE FEATURES | | | C5515 |
|--|--|-------------|--|
| Peripherals Not all peripheral pins are available at the same time (for more detail, see the Device Configuration section). | External Memory Interface (EMIF) | | Asynchronous (8/16-bit bus width) SRAM, Flash (NOR, NAND), SDRAM and Mobile SDRAM (16-bit bus width) ⁽¹⁾ |
| | DMA | | Four DMA controllers each with four channels, for a total of 16 channels |
| | Timers | | 2 32-Bit General-Purpose (GP) Timers 1 Additional Timer Configurable as a 32-Bit GP Timer and/or a Watchdog |
| | UART | | 1 (with RTS/CTS flow control) |
| | SPI | | 1 with 4 chip selects |
| | I ² C | | 1 (Master/Slave) |
| | I ² S | | 4 (Two Channel, Full Duplex Communication) |
| | USB 2.0 (Device only) | | High- and Full-Speed Device |
| | MMC/SD | | 2 MMC/SD, 256 byte read/write buffer, max 50-MHz clock for SD cards, and signaling for DMA transfers |
| | LCD Bridge | | 1 (8-bit or 16-bit asynchronous parallel bus) |
| | ADC (Successive Approximation [SAR]) | | 1 (10-bit, 4-input, 16- μ s conversion time) |
| | Real-Time Clock (RTC) | | 1 (Crystal Input, Separate Clock Domain and Power Supply) |
| | FFT Hardware Accelerator | | 1 (Supports 8 to 1024-point 16-bit real and complex FFT) |
| | General-Purpose Input/Output Port (GPIO) | | Up to 26 pins (with 1 Additional General-Purpose Output (XF) and 4 Special-Purpose Outputs for Use With SAR) |
| On-Chip Memory | Size (Bytes) | | 320KB RAM, 128KB ROM |
| | Organization | | <ul style="list-style-type: none"> 64KB On-Chip Dual-Access RAM (DARAM) 256KB On-Chip Single-Access RAM (SARAM) 128KB On-Chip Single-Access ROM (SAROM) |
| JTAG BSDL_ID | JTAGID Register (Value is: 0x1B8F E02F) | | see Figure 5-45 |
| CPU Frequency | MHz | 1.05-V Core | 60 or 75 MHz |
| | | 1.3-V Core | 100 or 120 MHz |
| Cycle Time | ns | 1.05-V Core | 16.67, 13.3 ns |
| | | 1.3-V Core | 10, 8.33 ns |
| Voltage | Core (V) | | 1.05 V (60, 75 MHz) |
| | I/O (V) | | 1.3 V (100, 120 MHz) |
| LDOs | Core (V) | | 1.8 V, 2.5 V, 2.75 V, 3.3 V |
| | DSP_LDO | | 1.3 V or 1.05 V, 250 mA max current for DSP CPU (CV _{DD}) |
| | ANA_LDO | | 1.3 V, 4 mA max current for PLL (V _{DDA_PLL}), SAR, and power management circuits (V _{DDA_ANA}) |
| PLL Options | USB_LDO | | 1.3 V, 25 mA max current for USB core digital (USB_V _{DD1P3}) and PHY circuits (USB_V _{DDA1P3}) |
| | Software Programmable Multiplier | | x4 to x4099 multiplier |
| BGA Package | 10 x 10 mm | | 196-Pin BGA (ZCH) |

(1) For more information on SDRAM devices support, see [Section 5.9, External Memory Interface \(EMIF\)](#).

Table 2-1. Characteristics of the C5515 Processor (continued)

| HARDWARE FEATURES | | C5515 |
|-------------------------------|---|---------|
| Process Technology | µm | 0.09 µm |
| Product Status ⁽²⁾ | Product Preview (PP), Advance Information (AI), or Production Data (PD) | PD |

(2) PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

2.2 C55x CPU

The TMS320C5515 fixed-point digital signal processor (DSP) is based on the C55x CPU 3.3 generation processor core. The C55x DSP architecture achieves high performance and low power through increased parallelism and total focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, three data read buses (one 32-bit data read bus and two 16-bit data read buses), two 16-bit data write buses, and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four data reads and two data writes in a single cycle. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

The C55x CPU provides two multiply-accumulate (MAC) units, each capable of 17-bit x 17-bit multiplication in a single cycle. A central 40-bit arithmetic/logic unit (ALU) is supported by an additional 16-bit ALU. Use of the ALUs is under instruction set control, providing the ability to optimize parallel activity and power consumption. These resources are managed in the Address Unit (AU) and Data Unit (DU) of the C55x CPU.

The C55x DSP generation supports a variable byte width instruction set for improved code density. The Instruction Unit (IU) performs 32-bit program fetches from internal or external memory, stores them in a 128-byte Instruction Buffer Queue, and queues instructions for the Program Unit (PU). The Program Unit decodes the instructions, directs tasks to AU and DU resources, and manages the fully protected pipeline. Predictive branching capability avoids pipeline flushes on execution of conditional instruction calls.

For more detailed information on the CPU, see the *TMS320C55x CPU 3.0 CPU Reference Guide* (literature number [SWPU073](#)).

The C55x core of the device can address 16M bytes of unified data and program space. It also addresses 64K words of I/O space and includes three types of on-chip memory: 128 KB read-only memory (ROM), 256 KB single-access random access memory (SARAM), 64 KB dual-access random access memory (DARAM). The memory map is shown in [Figure 2-1](#).

2.2.1 On-Chip Dual-Access RAM (DARAM)

The DARAM is located in the byte address range 000000h – 00FFFFh and is composed of eight blocks of 4K words each (see [Table 2-2](#)). Each DARAM block can perform two accesses per cycle (two reads, two writes, or a read and a write). The DARAM can be accessed by the internal program, data, or DMA buses.

Table 2-2. DARAM Blocks

| CPU BYTE ADDRESS RANGE | DMA CONTROLLER BYTE ADDRESS RANGE | MEMORY BLOCK |
|---------------------------|--------------------------------------|------------------------|
| 000000h – 001FFFh | 0001 0000h – 0001 1FFFh | DARAM 0 ⁽¹⁾ |
| 002000h – 003FFFh | 0001 2000h – 0001 3FFFh | DARAM 1 |
| 004000h – 005FFFh | 0001 4000h – 0001 5FFFh | DARAM 2 |
| 006000h – 007FFFh | 0001 6000h – 0001 7FFFh | DARAM 3 |
| 008000h – 009FFFh | 0001 8000h – 0001 9FFFh | DARAM 4 |
| 00A000h – 00BFFFh | 0001 A000h – 0001 BFFFh | DARAM 5 |
| 00C000h – 00DFFFh | 0001 C000h – 0001 DFFFh | DARAM 6 |
| 00E000h – 00FFFFh | 0001 E000h – 0001 FFFFh | DARAM 7 |

(1) The first 192 bytes are reserved for memory-mapped registers (MMRs). See [Figure 2-1, Memory Map Summary](#).

2.2.2 On-Chip Single-Access RAM (SARAM)

The SARAM is located at the byte address range 010000h – 04FFFFh and is composed of 32 blocks of 4K words each (see [Table 2-3](#)). Each SARAM block can perform one access per cycle (one read or one write). SARAM can be accessed by the internal program, data, or DMA buses. SARAM is also accessed by the USB and LCD DMA buses.

Table 2-3. SARAM Blocks

| CPU BYTE ADDRESS RANGE | DMA/USB CONTROLLER BYTE ADDRESS RANGE | MEMORY BLOCK |
|---------------------------|--|-------------------------|
| 010000h – 011FFFh | 0009 0000h – 0009 1FFFh | SARAM 0 |
| 012000h – 013FFFh | 0009 2000h – 0009 3FFFh | SARAM 1 |
| 014000h – 015FFFh | 0009 4000h – 0009 5FFFh | SARAM 2 |
| 016000h – 017FFFh | 0009 6000h – 0009 7FFFh | SARAM 3 |
| 018000h – 019FFFh | 0009 8000h – 0009 9FFFh | SARAM 4 |
| 01A000h – 01BFFFh | 0009 A000h – 0009 BFFFh | SARAM 5 |
| 01C000h – 01DFFFh | 0009 C000h – 0009 DFFFh | SARAM 6 |
| 01E000h – 01FFFFh | 0009 E000h – 0009 FFFFh | SARAM 7 |
| 020000h – 021FFFh | 000A 0000h – 000A 1FFFh | SARAM 8 |
| 022000h – 023FFFh | 000A 2000h – 000A 3FFFh | SARAM 9 |
| 024000h – 025FFFh | 000A 4000h – 000A 5FFFh | SARAM 10 |
| 026000h – 027FFFh | 000A 6000h – 000A 7FFFh | SARAM 11 |
| 028000h – 029FFFh | 000A 8000h – 000A 9FFFh | SARAM 12 |
| 02A000h – 02BFFFh | 000A A000h – 000A BFFFh | SARAM 13 |
| 02C000h – 02DFFFh | 000A C000h – 000A DFFFh | SARAM 14 |
| 02E000h – 02FFFFh | 000A E000h – 000A FFFFh | SARAM 15 |
| 030000h – 031FFFh | 000B 0000h – 000B 1FFFh | SARAM 16 |
| 032000h – 033FFFh | 000B 2000h – 000B 3FFFh | SARAM 17 |
| 034000h – 035FFFh | 000B 4000h – 000B 5FFFh | SARAM 18 |
| 036000h – 037FFFh | 000B 6000h – 000B 7FFFh | SARAM 19 |
| 038000h – 039FFFh | 000B 8000h – 000B 9FFFh | SARAM 20 |
| 03A000h – 03BFFFh | 000B A000h – 000B BFFFh | SARAM 21 |
| 03C000h – 03DFFFh | 000B C000h – 000B DFFFh | SARAM 22 |
| 03E000h – 03FFFFh | 000B E000h – 000B FFFFh | SARAM 23 |
| 040000h – 041FFFh | 000C 0000h – 000C 1FFFh | SARAM 24 |
| 042000h – 043FFFh | 000C 2000h – 000C 3FFFh | SARAM 25 |
| 044000h – 045FFFh | 000C 4000h – 000C 5FFFh | SARAM 26 |
| 046000h – 047FFFh | 000C 6000h – 000C 7FFFh | SARAM 27 |
| 048000h – 049FFFh | 000C 8000h – 000C 9FFFh | SARAM 28 |
| 04A000h – 04BFFFh | 000C A000h – 000C BFFFh | SARAM 29 |
| 04C000h – 04DFFFh | 000C C000h – 000C DFFFh | SARAM 30 |
| 04E000h – 04FFFFh | 000C E000h – 000C FFFFh | SARAM 31 ⁽¹⁾ |

(1) SARAM31 (byte address range: 0x4E000 – 0x4EFFF) is reserved for the bootloader. After the boot process is complete, this memory space can be used.

2.2.3 On-Chip Read-Only Memory (ROM)

The zero-wait-state ROM is located at the byte address range FE0000h – FFFFFFFh. The ROM is composed of four 16K-word blocks, for a total of 128K bytes of ROM. The ROM address space can be mapped by software to the external memory or to the internal ROM.

The standard device includes a Bootloader program resident in the ROM.

When the MPNMC bit field of the ST3 status register is cleared (by default), the byte address range FE0000h – FFFFFFFh is reserved for the on-chip ROM. When the MPNMC bit field of the ST3 status register is set through software, the on-chip ROM is disabled and not present in the memory map, and byte address range FE0000h – FFFFFFFh is unmapped. A hardware reset always clears the MPNMC bit, so it is not possible to disable the ROM at reset. However, the software reset instruction does not affect the MPNMC bit. The ROM can be accessed by the program and data buses. Each on-chip ROM block is a one cycle per word access memory.

2.2.4 External Memory

The external memory space of the device is located at the byte address range 050000h – FFFFFFFh. The external memory space is divided into five chip select spaces: one dedicated to SDRAM and mobile SDRAM (EMIF CS0 or CS[1:0] space), and the remainder (EMIF CS2 through CS5 space) dedicated to asynchronous devices including flash. Each chip select space has a corresponding chip select pin (called EM_CSx) that is activated during an access to the chip select space.

The external memory interface (EMIF) provides the means for the DSP to access external memories and other devices including: mobile single data rate (SDR) synchronous dynamic RAM (SDRAM and mSDRAM), NOR Flash, NAND Flash, and asynchronous static RAM (SRAM). Before accessing external memory, you must configure the EMIF through its memory-mapped registers.

The EMIF provides a configurable 16- or 8-bit data bus, an address bus width of up to 21-bits, and 5 dedicated chip selects, along with memory control signals. To maximize power savings, the I/O pins of the EMIF can be operated at an independent voltage from the other I/O pins on the device.

2.2.5 I/O Memory

The device includes a 64K byte I/O space for the memory-mapped registers of the DSP peripherals and system registers used for idle control, status monitoring and system configuration. I/O space is separate from program/memory space and is accessed with separate instruction opcodes or via the DMA's.

[Table 2-4](#) lists the memory-mapped registers of the device. Note that not all addresses in the 64K byte I/O space are used; these addresses should be treated as RESERVED and not accessed by the CPU nor DMA. For the expanded tables of each peripheral, see [Section 5, Peripheral Information and Electrical Specifications](#) of this document.

Some of the DMA controllers have access to the I/O-Space memory-mapped registers of the following peripherals registers: I2C, UART, I2S, MMC/SD, EMIF, USB, and SAR ADC.

Before accessing any peripheral memory-mapped register, make sure the peripheral being accessed is not held in reset via the Peripheral Reset Control Register (PRCR) and its internal clock is enabled via the Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2).

Table 2-4. Peripheral I/O-Space Control Registers

| WORD ADDRESS | PERIPHERAL |
|---|----------------------------------|
| 0x0000 – 0x0004 | Idle Control |
| 0x0005 – 0x000D through 0x0803 – 0x0BFF | Reserved |
| 0x0C00 – 0x0C7F | DMA0 |
| 0x0C80 – 0x0CFF | Reserved |
| 0x0D00 – 0x0D7F | DMA1 |
| 0x0D80 – 0x0DFF | Reserved |
| 0x0E00 – 0x0E7F | DMA2 |
| 0x0E80 – 0x0EFF | Reserved |
| 0x0F00 – 0x0F7F | DMA3 |
| 0x0F80 – 0x0FFF | Reserved |
| 0x1000 – 0x10DD | EMIF |
| 0x10EE – 0x10FF through 0x1300 – 0x17FF | Reserved |
| 0x1800 – 0x181F | Timer0 |
| 0x1820 – 0x183F | Reserved |
| 0x1840 – 0x185F | Timer1 |
| 0x1860 – 0x187F | Reserved |
| 0x1880 – 0x189F | Timer2 |
| 0x1900 – 0x197F | RTC |
| 0x1980 – 0x19FF | Reserved |
| 0x1A00 – 0x1A6C | I2C |
| 0x1A6D – 0x1AFF | Reserved |
| 0x1B00 – 0x1B1F | UART |
| 0x1B80 – 0x1BFF | Reserved |
| 0x1C00 – 0x1CFF | System Control |
| 0x1D00 – 0x1FFF through 0x2600 – 0x27FF | Reserved |
| 0x2800 – 0x2840 | I2S0 |
| 0x2900 – 0x2940 | I2S1 |
| 0x2A00 – 0x2A40 | I2S2 |
| 0x2B00 – 0x2B40 | I2S3 |
| 0x2C41 – 0x2DFF | Reserved |
| 0x2E00 – 0x2E40 | LCD |
| 0x2E41 – 0x2FFF | Reserved |
| 0x3000 – 0x300F | SPI |
| 0x3010 – 0x39FF | Reserved |
| 0x3A00 – 0x3A7F | MMC/SD0 |
| 0x3A80 – 0x3AFF | Reserved |
| 0x3B00 – 0x3B7F | MMC/SD1 |
| 0x3B80 – 0x6FFF | Reserved |
| 0x7000 – 0x70FF | SAR and Analog Control Registers |
| 0x7100 – 0x7FFF | Reserved |
| 0x8000 – 0xFFFF | USB |

2.3 Memory Map Summary

The device provides 16M bytes of total memory space composed of on-chip RAM, on-chip ROM, and external memory space supporting a variety of memory types. The on-chip, dual-access RAM allows two accesses to a given block during the same cycle. There are 8 blocks of 8K bytes of dual-access RAM. The on-chip, single-access RAM allows one access to a given block per cycle. In addition, there are 32 blocks of 8K bytes of single-access RAM.

The remainder of the memory map is divided into five external spaces, and on-chip ROM. Each external space has a chip select decode signal (called $\overline{\text{EM_CS0}}$, $\overline{\text{EM_CS[2:5]}}$) that indicates an access to the selected space. The external memory interface (EMIF) supports access to asynchronous memories such as SRAM, NAND, or NOR and Flash, and mobile single data rate (mSDR) and single data rate (SDR) SDRAM.

The DSP memory is accessible by different master modules within the DSP, including the C55x CPU, the four DMA controllers, LCD, and the CDMA of USB (see [Figure 2-1](#)).

| CPU BYTE ADDRESS ^(A) | DMA/USB/LCD BYTE ADDRESS ^(A) | MEMORY BLOCKS | | BLOCK SIZE |
|---------------------------------|---|--------------------------------------|--------------------------|--|
| 000000h | 0001 0000h | MMR (Reserved) ^(B) | | |
| 0000C0h | 0001 00C0h | DARAM ^(D) | | 64K Minus 192 Bytes |
| 010000h | 0009 0000h | SARAM | | 256K Bytes |
| 050000h | 0100 0000h | External-CS0 Space ^{(C)(E)} | | 8M Minus 320K Bytes SDRAM/mSDRAM |
| 800000h | 0200 0000h | External-CS2 Space ^(C) | | 4M Bytes Asynchronous |
| C00000h | 0300 0000h | External-CS3 Space ^(C) | | 2M Bytes Asynchronous |
| E00000h | 0400 0000h | External-CS4 Space ^(C) | | 1M Bytes Asynchronous |
| F00000h | 0500 0000h | External-CS5 Space ^(C) | | 1M Minus 128K Bytes Asynchronous |
| FE0000h | 050E 0000h | ROM (if MPNMC=0) | Reserved (if MPNMC=1) | Unmapped (if MPNMC=1) 128K Bytes ROM (if MPNMC=0) |
| FFFFFFh | 050F FFFFh | | | |

- A. Address shown represents the first byte address in each block.
- B. The first 192 bytes are reserved for memory-mapped registers (MMRs).
- C. Reading/Writing to/from unmapped returns zeros.
- D. The USB and LCD controllers do not have access to DARAM.
- E. The CS0 space can be accessed by CS0 *only* or by CS0 *and* CS1.

Figure 2-1. Memory Map Summary

2.4 Pin Assignments

Extensive pin multiplexing is used to accommodate the largest number of peripheral functions in the smallest possible package. Pin multiplexing is controlled using software programmable register settings. For more information on pin muxing, see [Section 3.7, Multiplexed Pin Configurations](#) of this document.

2.4.1 Pin Map (Bottom View)

Figure 2-2 shows the bottom view of the package pin assignments.

| | | | | | | | | | | | | | | |
|---|---------------------|---------------------|------------------------|-------------------------|------------------------|---------------------|---------------------|---------------------|-------------------------------|--|---|--|---|---|
| P | EM_DQM1 | DVDDDEMIF | DVDDIO | LCD_CS0_E0/ SPI_CS0 | LCD_RW_WRB/ SPI_CS2 | LCD_D[0]/ SPI_RX | LCD_D[2]/ GP[12] | DVDDIO | LCD_D[5]/ GP[15] | LCD_D[7]/ GP[17] | LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0 | LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX | LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS | LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX |
| N | EM_A[15]/ GP[21] | EM_SDCKE | LCD_EN_RDB/ SPI_CLK | LCD_CS1_EN1/ SPI_CS1 | LCD_RS/ SPI_CS3 | LCD_D[1]/ SPI_TX | LCD_D[3]/ GP[13] | LCD_D[4]/ GP[14] | LCD_D[6]/ GP[16] | LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK | LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX | LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK | LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX | DVDDIO |
| M | EM_A[14] | EM_D[5] | EM_SDCLK | EM_CS3 | EMU1 | TCK | TDO | XF | TRST | MMC0_D1/ I2S0_RX/ GP[3] | MMC0_CMD/ I2S0_FS/ GP[1] | MMC1_D1/ I2S1_RX/ GP[9] | MMC1_CLK/ I2S1_CLK/ GP[6] | MMC1_D0/ I2S1_DX/ GP[8] |
| L | EM_A[13] | EM_A[10] | EM_D[12] | EM_D[4] | CVDD | EMU0 | TDI | TMS | MMC0_D0/ I2S0_DX/ GP[2] | MMC0_CLK/ I2S0_CLK/ GP[0] | MMC0_D3/ GP[5] | MMC0_D2/ GP[4] | MMC1_D3/ GP[11] | MMC1_CMD/ I2S1_FS/ GP[7] |
| K | EM_A[12]/ (CLE) | EM_A[11]/ (ALE) | EM_D[14] | EM_D[13] | EM_D[6] | EM_WAIT3 | DVDDIO | VSS | VSS | CVDD | VSS | DVDDIO | VSS | MMC1_D2/ GP[10] |
| J | EM_A[8] | EM_A[9] | EM_A[20]/ GP[26] | EM_D[15] | DVDDDEMIF | CVDD | VSS | VSS | VSS | RSV1 | RSV2 | USB_VBUS | USB_VDD1P3 | USB_DM |
| H | EM_WE | EM_A[7] | EM_D[7] | EM_WAIT5 | DVDDDEMIF | VSS | DVDDDEMIF | CVDD | USB_VSSA1P3 | USB_VDDA1P3 | USB_VSSA3P3 | USB_VDDA3P3 | USB_VSS1P3 | USB_DP |
| G | EM_WAIT4 | EM_A[18]/ GP[24] | EM_D[0] | EM_A[19]/ GP[25] | DVDDDEMIF | VSS | VSS | USB_VDDPLL | USB_R1 | USB_VSSREF | USB_VSSPLL | USB_VDDOSC | USB_MXI | USB_MXO |
| F | EM_A[6] | EM_A[17]/ GP[23] | EM_D[2] | EM_D[9] | DVDDDEMIF | CVDD | DVDDIO | DVDDRTC | VSS | VSS | USB_VSSOSC | USB_LDOO | LDOI | LDOI |
| E | EM_A[2] | EM_A[16]/ GP[22] | EM_D[8] | EM_OE | EM_D[1] | DVDDDEMIF | INT1 | WAKEUP | VSS | DSP_LDOO | VSS | VSS | VSS | VSS |
| D | EM_A[5] | EM_A[3] | EM_D[10] | EM_D[3] | EM_WAIT2 | RESET | VSS | RTC_CLKOUT | VSSA_PLL | GPAIN0 | VSS | DSP_LDO_EN | RSV16 | RSV3 |
| C | EM_A[4] | EM_A[1] | EM_CS4 | EM_D[11] | EM_CS2 | INT0 | CLK_SEL | CVDDRTC | VSSRTC | VDDA_PLL | GPAIN3 | RSV0 | RSV5 | RSV4 |
| B | EM_BA[1] | EM_A[0] | EM_CS0 | EM_SDCAS | EM_DQM0 | EM_RW | SCL | SDA | RTC_XI | VSSA_ANA | GPAIN2 | LDOI | BG_CAP | VSSA_ANA |
| A | EM_BA[0] | DVDDDEMIF | EM_CS5 | EM_CS1 | DVDDDEMIF | EM_SDRAS | CLKOUT | CLKIN | RTC_XO | VDDA_ANA | GPAIN1 | ANA_LDOO | VSS | VSS |

Figure 2-2. Pin Map

2.5 Terminal Functions

The terminal functions tables ([Table 2-5](#) through [Table 2-22](#)) identify the external signal names, the associated pin (ball) numbers along with the mechanical package designator, the pin type, whether the pin has any internal pullup or pulldown resistors or bus-holders, and a functional pin description. For more detailed information on device configuration, peripheral selection, multiplexed/shared pins, and debugging considerations, see [Section 3](#), *Device Configuration*.

For proper device operation, external pullup/pulldown resistors may be required on some pins. [Section 3.8.1](#), *Pullup/Pulldown Resistors*, discusses situations where external pullup/pulldown resistors are required.

2.5.1 Oscillator and PLL Terminal Functions

Table 2-5. Oscillator and PLL Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------------|-----|----------------------------|--|--|
| CLKOUT | A7 | O/Z | – DV _{DDIO} BH | <p>DSP clock output signal. For debug purposes, the CLKOUT pin can be used to tap different clocks within the system clock generator. The SRC bits in the CLKOUT Control Source Register (CCSSR) can be used to specify the CLKOUT pin source. Additionally, the slew rate of the CLKOUT pin can be controlled by the Output Slew Rate Control Register (OSRCR) [0x1C16].</p> <p>The CLKOUT pin is enabled/disabled through the CLKOFF bit in the CPU ST3_55 register. When disabled, the CLKOUT pin is placed in high-impedance (Hi-Z). At reset the CLKOUT pin is enabled until the beginning of the boot sequence, when the on-chip Bootloader sets CLKOFF = 1 and the CLKOUT pin is disabled (Hi-Z). For more information on the ST3_55 register, see the <i>TMS320C55x 3.0 CPU Reference Guide</i> (literature number: SWPU073).</p> <p>Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin.</p> |
| CLKIN | A8 | I | – DV _{DDIO} BH | <p>Input clock. This signal is used to input an external clock when the 32-KHz on-chip oscillator is not used as the DSP clock (pin CLK_SEL = 1). For boot purposes, the CLKIN frequency is assumed to be either 11.2896, 12, or 12.288 MHz.</p> <p>The CLK_SEL pin (C7) selects between the 32-KHz crystal clock or CLKIN.</p> <p>When the CLK_SEL pin is low, this pin should be tied to ground (V_{SS}). When CLK_SEL is high, this pin should be driven by an external clock source.</p> <p>If CLK_SEL is high, this pin is used as the reference clock for the clock generator and during bootup the bootloader bypasses the PLL and assumes the CLKIN frequency is one of the following frequencies: 11.2896-, 12-, or 12.288-MHz. With these frequencies in mind, the bootloader sets the SPI clock rates at 500 KHz and the I2C clock rate at 400 KHz.</p> |
| CLK_SEL | C7 | I | – DV _{DDIO} BH | <p>Clock input select. This pin selects between the 32-KHz crystal clock or CLKIN.</p> <p>0 = 32-KHz on-chip oscillator drives the RTC timer and the system clock generator while CLKIN is ignored.</p> <p>1 = CLKIN drives the system clock generator and the 32-KHz on-chip oscillator drives only the RTC timer.</p> <p>This pin is not allowed to change during device operation; it must be tied high or low at the board.</p> |
| V _{DDA_PLL} | C10 | PWR | see Section 4.2 , ROC | <p>1.3-V Analog PLL power supply for the system clock generator (PLLOUT ≤ 120 MHz).</p> <p>This signal can be powered from the ANA_LDOO pin.</p> |
| V _{SSA_PLL} | D9 | GND | see Section 4.2 , ROC | Analog PLL ground for the system clock generator. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1](#), *Pullup/Pulldown Resistors*.
- (4) Specifies the operating I/O supply voltage for each signal

2.5.2 RTC Terminal Functions

Table 2-6. Real-Time Clock (RTC) Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------|-----|----------------------------|--------------------------|--|
| RTC_XO | A9 | O/Z | – CV _{DDRTC} | Real-time clock oscillator output. This pin operates at the RTC core voltage, CV _{DDRTC} , and supports a 32.768-kHz crystal. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV _{DDRTC} and RTC_XO to floating or grounded. A voltage must still be applied to CV _{DDRTC} by an external power source (see Section 4.2, Recommended Operating Conditions). None of the on-chip LDOs can power CV _{DDRTC} . Note: When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible. |
| RTC_XI | B9 | I | – CV _{DDRTC} | Real-time clock oscillator input. If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CV _{DDRTC} and RTC_XO to ground (V _{SS}). A voltage must still be applied to CV _{DDRTC} by an external power source (see Section 4.2, Recommended Operating Conditions). None of the on-chip LDOs can power CV _{DDRTC} . Note: When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible. |
| RTC_CLKOUT | D8 | O/Z | – DV _{DDRTC} | Real-time clock output pin. This pin operates at DV _{DDRTC} voltage. The RTC_CLKOUT pin is enabled/disabled through the RTCCLKOUTEN bit in the RTC Power Management Register (RTCPMGT). At reset, the RTC_CLKOUT pin is disabled (high-impedance [Hi-Z]). |
| WAKEUP | E8 | I/O/Z | – DV _{DDRTC} | The pin is used to WAKEUP the core from idle condition. This pin defaults to an input at CV _{DDRTC} powerup, but can also be configured as an active-low open-drain output signal to wakeup an external device from an RTC alarm. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

2.5.3 RESET, Interrupts, and JTAG Terminal Functions

Table 2-7. RESET, Interrupts, and JTAG Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--|-----|-------------------------|---------------------------------|---|
| RESET | | | | |
| XF | M8 | O/Z | – DV _{DDIO} BH | <p>External Flag Output. XF is used for signaling other processors in multiprocessor configurations or XF can be used as a fast general-purpose output pin.</p> <p>XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. For more information on the ST1_55 register, see the <i>TMS320C55x 3.0 CPU Reference Guide</i> (literature number: SWPU073).</p> <p>For XF pin behavior at reset, see Section 5.7.2, Pin Behaviors at Reset.</p> <p>Note: This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin. XF pin is ONLY in the Hi-Z state when doing boundary scan. Therefore, external termination is probably not required for most applications.</p> |
| $\overline{\text{RESET}}$ | D6 | I | IPU DV _{DDIO} BH | <p>Device reset. $\overline{\text{RESET}}$ causes the DSP to terminate execution and loads the program counter with the contents of the reset vector. When $\overline{\text{RESET}}$ is brought to a high level, the reset vector in ROM at FFFF00h forces the program execution to branch to the location of the on-chip ROM bootloader.</p> <p>$\overline{\text{RESET}}$ affects the various registers and status bits.</p> <p>The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register but will be forced ON when $\overline{\text{RESET}}$ is asserted.</p> |
| JTAG | | | | |
| [For more detailed information on emulation header design guidelines, see the <i>XDS560 Emulator Technical Reference</i> (literature number: SPRU589).] | | | | |
| TMS | L8 | I | IPU DV _{DDIO} BH | <p>IEEE standard 1149.1 test mode select. This serial control input is clocked into the TAP controller on the rising edge of TCK.</p> <p>If the emulation header is located greater than 6 inches from the device, TMS must be buffered. In this case, the input buffer for TMS needs a pullup resistor connected to DV_{DDIO} to hold the signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested. For board design guidelines related to the emulation header, see the <i>XDS560 Emulator Technical Reference</i> (literature number: SPRU589).</p> <p>The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.</p> |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

Table 2-7. RESET, Interrupts, and JTAG Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ^{(1) (2)} | OTHER ^{(3) (4)} | DESCRIPTION |
|--------------------------|-----|-------------------------|---------------------------------|--|
| TDO | M7 | O/Z | – DV _{DDIO} BH | <p>IEEE standard 1149.1 test data output. The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. TDO is in the high-impedance (Hi-Z) state except when the scanning of data is in progress.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (literature number: SPRU589).</p> <p>If the emulation header is located greater than 6 inches from the device, TDO must be buffered.</p> <p>Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. TDO pin will be Hi-Z whenever not doing emulation/boundary scan, so an external pullup is highly recommended.</p> |
| TDI | L7 | I | IPU DV _{DDIO} BH | <p>IEEE standard 1149.1 test data input. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.</p> <p>If the emulation header is located greater than 6 inches from the device, TDI must be buffered. In this case, the input buffer for TDI needs a pullup resistor connected to DV_{DDIO} to hold this signal at a known value when the emulator is not connected. A resistor value of 4.7 kΩ or greater is suggested.</p> <p>The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.</p> |
| TCK | M6 | I | IPU DV _{DDIO} BH | <p>IEEE standard 1149.1 test clock. TCK is normally a free-running clock signal with a 50% duty cycle. The changes on input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.</p> <p>If the emulation header is located greater than 6 inches from the device, TCK must be buffered.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (literature number: SPRU589).</p> <p>The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.</p> |
| $\overline{\text{TRST}}$ | M9 | I | IPD DV _{DDIO} BH | <p>IEEE standard 1149.1 reset signal for test and emulation logic. $\overline{\text{TRST}}$, when high, allows the IEEE standard 1149.1 scan and emulation logic to take control of the operations of the device. If $\overline{\text{TRST}}$ is not connected or is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. The device will not operate properly if this reset pin is never asserted low.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (literature number: SPRU589).</p> <p>It is recommended that an external pulldown resistor be used in addition to the IPD -- especially if there is a long trace to an emulation header.</p> |
| EMU1 | M5 | I/O/Z | IPU DV _{DDIO} BH | <p>Emulator 1 pin. EMU1 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic.</p> <p>An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 μsec. A 4.7-kΩ resistor is suggested for most applications.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (literature number: SPRU589).</p> <p>The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.</p> |

Table 2-7. RESET, Interrupts, and JTAG Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------------------|-----|-------------------------|---------------------------------|---|
| EMU0 | L6 | I/O/Z | IPU DV _{DDIO} BH | <p>Emulator 0 pin. When $\overline{\text{TRST}}$ is driven low and then high, the state of the EMU0 pin is latched and used to connect the JTAG pins (TCK, TMS, TDI, TDO) to either the IEEE1149.1 Boundary-Scan TAP (when the latched value of EMU0 = 0) or to the DSP Emulation TAP (when the latched value of EMU0 = 1). Once $\overline{\text{TRST}}$ is high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output by way of the emulation logic.</p> <p>An external pullup to DV_{DDIO} is required to provide a signal rise time of less than 10 μsec. A 4.7-kΩ resistor is suggested for most applications.</p> <p>For board design guidelines related to the emulation header, see the <i>XDS560 Emulator</i> Technical Reference (literature number: SPRU589).</p> <p>The IPU resistor on this pin can be enabled or disabled via the PDINHIBR2 register.</p> |
| EXTERNAL INTERRUPTS | | | | |
| $\overline{\text{INT1}}$ | E7 | I | IPU DV _{DDIO} BH | External interrupt inputs ($\overline{\text{INT1}}$ and $\overline{\text{INT0}}$). These pins are maskable via their specific Interrupt Mask Register (IMR1, IMR0) and the interrupt mode bit. The pins can be polled and reset by their specific Interrupt Flag Register (IFR1, IFR0). |
| $\overline{\text{INT0}}$ | C6 | I | IPU DV _{DDIO} BH | The IPU resistor on these pins can be enabled or disabled via the PDINHIBR2 register. |

2.5.4 EMIF Terminal Functions

Table 2-8. External Memory Interface (EMIF) Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--|-----|----------------------------|-----------------------------------|---|
| EMIF FUNCTIONAL PINS: ASYNC (NOR, SRAM, and NAND) | | | | |
| | | | | Note: When accessing 8-bit Asynchronous memory: <ul style="list-style-type: none"> Connect EM_A[20:0] to memory address pins [22:2] Connect EM_BA[1:0] to memory address pins [1:0] For 16-bit Asynchronous memory: <ul style="list-style-type: none"> Connect EM_A[20:0] to memory address pins [21:1] Connect EM_BA[1] to memory address pin [0] |
| EM_A[20]/GP[26] | J3 | I/O/Z | IPD DV _{DDEMIF} BH | This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 20. Mux control via the A20_MODE bit in the EBSR (see Figure 3-3). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[19]/GP[25] | G4 | I/O/Z | IPD DV _{DDEMIF} BH | This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 19. Mux control via the A19_MODE bit in the EBSR (see Figure 3-3). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[18]/GP[24] | G2 | I/O/Z | IPD DV _{DDEMIF} BH | This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 18. Mux control via the A18_MODE bit in the EBSR (see Figure 3-3). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[17]/GP[23] | F2 | I/O/Z | IPD DV _{DDEMIF} BH | This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 17. Mux control via the A17_MODE bit in the EBSR (see Figure 3-3). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[16]/GP[22] | E2 | I/O/Z | IPD DV _{DDEMIF} BH | This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 16. Mux control via the A16_MODE bit in the EBSR (see Figure 3-3). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[15]/GP[21] | N1 | I/O/Z | IPD DV _{DDEMIF} BH | This pin is multiplexed between EMIF and GPIO. For EMIF, this pin is the EMIF external address pin 15. Mux control via the A15_MODE bit in the EBSR (see Figure 3-3). The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[14] | M1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 14. |
| EM_A[13] | L1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 13. |
| EM_A[12]/(CLE) | K1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 12. When interfacing with NAND Flash, this pin also acts as Command Latch Enable (CLE). |
| EM_A[11]/(ALE) | K2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 11. When interfacing with NAND Flash, this pin also acts as Address Latch Enable (ALE). |
| EM_A[10] | L2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 10. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

Table 2-8. External Memory Interface (EMIF) Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE⁽¹⁾ (2) | OTHER⁽³⁾ (4) | DESCRIPTION |
|-----------------------------|------------|-----------------------------------|--------------------------------|--|
| EM_A[9] | J2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 9. |
| EM_A[8] | J1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 8. |
| EM_A[7] | H2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 7. |
| EM_A[6] | F1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 6. |
| EM_A[5] | D1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 5. |
| EM_A[4] | C1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 4. |
| EM_A[3] | D2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 3. |
| EM_A[2] | E1 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 2. |
| EM_A[1] | C2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 1. |
| EM_A[0] | B2 | I/O/Z | DV _{DDEMIF} BH | This pin is the EMIF external address pin 0. |
| EM_D[15] | J4 | I/O/Z | DV _{DDEMIF} BH | EMIF 16-bit bi-directional bus. |
| EM_D[14] | K3 | | | |
| EM_D[13] | K4 | | | |
| EM_D[12] | L3 | | | |
| EM_D[11] | C4 | | | |
| EM_D[10] | D3 | | | |
| EM_D[9] | F4 | | | |
| EM_D[8] | E3 | | | |
| EM_D[7] | H3 | | | |
| EM_D[6] | K5 | | | |
| EM_D[5] | M2 | | | |
| EM_D[4] | L4 | | | |
| EM_D[3] | D4 | | | |
| EM_D[2] | F3 | | | |
| EM_D[1] | E5 | | | |
| EM_D[0] | G3 | | | |
| $\overline{\text{EM_CS5}}$ | A3 | O/Z | DV _{DDEMIF} BH | EMIF chip select 5 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM). Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_CS4}}$ | C3 | O/Z | DV _{DDEMIF} BH | EMIF chip select 4 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM). Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_CS3}}$ | M4 | O/Z | DV _{DDEMIF} BH | EMIF NAND chip select 3 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM). Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |

Table 2-8. External Memory Interface (EMIF) Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|-----------------------------|-----|----------------------------|----------------------------|---|
| $\overline{\text{EM_CS2}}$ | C5 | O/Z | DV _{DDEMIF} BH | EMIF NAND chip select 2 output for use with asynchronous memories (i.e., NOR flash, NAND flash, or SRAM). Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_WE}}$ | H1 | O/Z | DV _{DDEMIF} BH | EMIF asynchronous memory write enable output Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_OE}}$ | E4 | O/Z | DV _{DDEMIF} BH | EMIF asynchronous memory read enable output Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| EM_R $\overline{\text{W}}$ | B6 | O/Z | DV _{DDEMIF} BH | EMIF asynchronous read/write output Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| EM_DQM1 | P1 | O/Z | DV _{DDEMIF} BH | EMIF asynchronous data write strobes and byte enables or EMIF SDRAM and mSDRAM data mask bits. |
| EM_DQM0 | B5 | O/Z | DV _{DDEMIF} BH | Note: These pins may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pins. |
| EM_BA[1] | B1 | O/Z | DV _{DDEMIF} BH | EMIF asynchronous bank address |
| EM_BA[0] | A1 | O/Z | DV _{DDEMIF} BH | 16-bit wide memory: EM_BA[1] forms the device address[0] and BA[0] forms device address [23]. 8-bit wide memory: EM_BA[1] forms the device address[1] and BA[0] forms device address [0]. EMIF SDRAM and mSDRAM bank address. Note: These pins may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pins. |
| EM_WAIT5 | H4 | I | DV _{DDEMIF} BH | EMIF wait state extension input 5 for $\overline{\text{EM_CS5}}$ Note: This pin may consume static power through the input buffer if not externally driven. Prevent current drain by externally terminating the pin. |
| EM_WAIT4 | G1 | I | DV _{DDEMIF} BH | EMIF wait state extension input 4 for $\overline{\text{EM_CS4}}$ Note: This pin may consume static power through the input buffer if not externally driven. Prevent current drain by externally terminating the pin. |
| EM_WAIT3 | K6 | I | DV _{DDEMIF} BH | EMIF wait state extension input 3 for $\overline{\text{EM_CS3}}$ Note: This pin may consume static power through the input buffer if not externally driven. Prevent current drain by externally terminating the pin. |
| EM_WAIT2 | D5 | I | DV _{DDEMIF} BH | EMIF wait state extension input 2 for $\overline{\text{EM_CS2}}$ Note: This pin may consume static power through the input buffer if not externally driven. Prevent current drain by externally terminating the pin. |

Table 2-8. External Memory Interface (EMIF) Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--|-----|----------------------------|----------------------------|---|
| EMIF FUNCTIONAL PINS: SDRAM and mSDRAM ONLY | | | | |
| $\overline{\text{EM_CS1}}$ | A4 | O/Z | DV _{DDEMIF} BH | EMIF SDRAM/mSDRAM chip select 1 output Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_CS0}}$ | B3 | O/Z | DV _{DDEMIF} BH | EMIF SDRAM/mSDRAM chip select 0 output Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| EM_SDCLK | M3 | O/Z | DV _{DDEMIF} BH | EMIF SDRAM/mSDRAM clock Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| EM_SDCKE | N2 | O/Z | DV _{DDEMIF} BH | EMIF SDRAM/mSDRAM clock enable Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_SDRAS}}$ | A6 | O/Z | DV _{DDEMIF} BH | EMIF SDRAM/mSDRAM row address strobe Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |
| $\overline{\text{EM_SDCAS}}$ | B4 | O/Z | DV _{DDEMIF} BH | EMIF SDRAM/mSDRAM column strobe Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. |

2.5.5 I2C Terminal Functions

Table 2-9. Inter-Integrated Circuit (I2C) Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------|-----|----------------------------|--------------------------|--|
| I2C | | | | |
| SCL | B7 | I/O/Z | DV _{DDIO} BH | This pin is the I2C clock output. Per the I2C standard, an external pullup is required on this pin. |
| SDA | B8 | I/O/Z | DV _{DDIO} BH | This pin is the I2C bidirectional data signal. Per the I2C standard, an external pullup is required on this pin. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

2.5.6 I2S0 – I2S3 Terminal Functions

Table 2-10. Inter-IC Sound (I2S0 – I2S3) Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|---------------------------------|-----|----------------------------|---------------------------------|---|
| Interface 0 (I2S0) | | | | |
| MMC0_D0/ I2S0_DX/ GP[2] | L9 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 transmit data output I2S0_DX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC0_CLK/ I2S0_CLK/ GP[0] | L10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 clock input/output I2S0_CLK. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC0_D1/ I2S0_RX/ GP[3] | M10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 receive data input I2S0_RX. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC0_CMD/ I2S0_FS/ GP[1] | M11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC0, I2S0, and GPIO. For I2S, it is I2S0 frame synchronization input/output I2S0_FS. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| Interface 1 (I2S1) | | | | |
| MMC1_D0/ I2S1_DX/ GP[8] | M14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For I2S, it is I2S1 transmit data output I2S1_DX. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_CLK/ I2S1_CLK/ GP[6] | M13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For I2S, it is I2S1 clock input/output I2S1_CLK. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D1/ I2S1_RX/ GP[9] | M12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For I2S, it is I2S1 receive data input I2S1_RX. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_CMD/ I2S1_FS/ GP[7] | L14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S2, and GPIO. For I2S, it is I2S1 frame synchronization input/output I2S1_FS. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
 (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
 (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
 (4) Specifies the operating I/O supply voltage for each signal

Table 2-10. Inter-IC Sound (I2S0 – I2S3) Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--|-----|----------------------------|---------------------------------|--|
| Interface 2 (I2S2) | | | | |
| LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX | P12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 transmit data output I2S2_DX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D8]/ I2S2_CLK/ GP[18]/ SPI_CLK | N10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 clock input/output I2S2_CLK. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX | N11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For I2S, it is I2S2 receive data input I2S2_RX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0 | P11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, and GPIO. For I2S, it is I2S2 frame synchronization input/output I2S2_FS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| Interface 3 (I2S3) | | | | |
| LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX | P14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 transmit data output I2S3_DX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK | N12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 clock input/output I2S3_CLK. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX | N13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 receive data input I2S3_RX. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS | P13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For I2S, it is I2S3 frame synchronization input/output I2S3_FS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |

2.5.7 SPI Terminal Functions

Table 2-11. Serial Peripheral Interface (SPI) Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|---|-----|----------------------------|---------------------------------|--|
| Serial Port Interface (SPI) | | | | |
| LCD_CS0_E0/ SPI_CS0 | P4 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0. |
| LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0 | P11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS0. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_CS1_E1/ SPI_CS1 | N4 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS1. |
| LCD_RW_WRB/ SPI_CS2 | P5 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS2. |
| LCD_RS/ SPI_CS3 | N5 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI chip select SPI_CS3. |
| LCD_EN_RDB/ SPI_CLK | N3 | O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin. This pin is ONLY in the Hi-Z state when doing boundary scan. Therefore, external termination is probably not required for most applications. |
| LCD_D8/ I2S2_CLK/ GP[18]/ SPI_CLK | N10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is clock output SPI_CLK. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[1]/ SPI_TX | N6 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output. |
| LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX | P12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. Mux control via the PPMODE bits in the EBSR. For SPI, this pin is SPI transmit data output. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[0]/ SPI_RX | P6 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. Mux control via the PPMODE bits in the EBSR. For SPI this pin is SPI receive data input. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
 (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
 (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
 (4) Specifies the operating I/O supply voltage for each signal

Table 2-11. Serial Peripheral Interface (SPI) Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|---|-----|----------------------------|---------------------------------|---|
| LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX | N11 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI.</p> <p>Mux control via the PPMODE bits in the EBSR.</p> <p>For SPI this pin is SPI receive data input.</p> <p>The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.</p> |

2.5.8 UART Terminal Functions

Table 2-12. UART Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--|-----|----------------------------|---------------------------------|--|
| UART | | | | |
| LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX | N13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. When used by UART, it is the receive data input UART_RXD. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX | P14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. In UART mode, it is the transmit data output UART_TXD. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS | P13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. In UART mode, it is the clear to send input UART_CTS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK | N12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. In UART mode, it is the ready to send output UART_RTS. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
 (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
 (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
 (4) Specifies the operating I/O supply voltage for each signal

2.5.9 USB 2.0 Terminal Functions

Table 2-13. USB2.0 Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------|-----|----------------------------|---|--|
| USB 2.0 | | | | |
| USB_MXI | G13 | I | USB_VDDOSC | 12-MHz crystal oscillator input. When the USB peripheral is not used, USB_MXI should be connected to ground (V _{SS}). When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V _{IH} requirement (see Section 4.2, Recommended Operating Conditions). The USB_MXO is left unconnected and the USB_VSSOSC signal is connected to board ground (V _{SS}). |
| USB_MXO | G14 | O/Z | USB_VDDOSC | 12-MHz crystal oscillator output. When the USB peripheral is not used, USB_MXO should be left unconnected. When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V _{IH} requirement (see Section 4.2, Recommended Operating Conditions). The USB_MXO is left unconnected and the USB_VSSOSC signal is connected to board ground (V _{SS}). |
| USB_VDDOSC | G12 | S | see Section 4.2, ROC | 3.3-V power supply for USB oscillator. When the USB peripheral is not used, USB_VDDOSC should be connected to ground (V _{SS}). |
| USB_VSSOSC | F11 | S | see Section 4.2, ROC | Ground for USB oscillator. When using a 12-MHz crystal, this pin is a local ground for the crystal and must not be connected to the board ground (See Figure 5-7). When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V _{IH} requirement (see Section 4.2, Recommended Operating Conditions). The USB_MXO is left unconnected and the USB_VSSOSC signal is connected to board ground (V _{SS}). |
| USB_VBUS | J12 | A I/O | see Section 4.2, ROC | USB power detect. 5-V input that signifies that VBUS is connected. This signal must be powered on in the order listed in Section 5.3.1, Power-Supply Sequencing . When the USB peripheral is not used, the USB_VBUS signal should be connected to ground (V _{SS}). |
| USB_DP | H14 | A I/O | USB_VDDA3P3 | USB bi-directional Data Differential signal pair [positive/negative]. |
| USB_DM | J14 | A I/O | USB_VDDA3P3 | When the USB peripheral is not used, the USB_DP and USB_DM signals should both be tied to ground (V _{SS}). |
| USB_R1 | G9 | A I/O | USB_VDDA3P3 | External resistor connect. Reference current output. This must be connected via a 10-kΩ ±1% resistor to USB_VSSREF and be placed as close to the device as possible. When the USB peripheral is not used, the USB_R1 signal should be connected via a 10-kΩ resistor to USB_VSSREF. |
| USB_VSSREF | G10 | GND | see Section 4.2, ROC | Ground for reference current. This must be connected via a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral is not used, the USB_VSSREF signal should be connected directly to ground (V _{SS}). |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
(4) Specifies the operating I/O supply voltage for each signal

Table 2-13. USB2.0 Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------|-----|----------------------------|---|---|
| USB_VDDA3P3 | H12 | S | see Section 4.2 , ROC | Analog 3.3 V power supply for USB PHY. This signal must be powered on in the order listed in Section 5.3.1 , <i>Power-Supply Sequencing</i> . When the USB peripheral is not used, the USB_VDDA3P3 signal should be connected to ground (V _{SS}). |
| USB_VSSA3P3 | H11 | GND | see Section 4.2 , ROC | Analog ground for USB PHY. |
| USB_VDDA1P3 | H10 | S | see Section 4.2 , ROC | Analog 1.3 V power supply for USB PHY. [For high-speed sensitive analog circuits] This signal must be powered on in the order listed in Section 5.3.1 , <i>Power-Supply Sequencing</i> . When the USB peripheral is not used, the USB_VDDA1P3 signal should be connected to ground (V _{SS}). |
| USB_VSSA1P3 | H9 | GND | see Section 4.2 , ROC | Analog ground for USB PHY [For high speed sensitive analog circuits]. |
| USB_VDD1P3 | J13 | S | see Section 4.2 , ROC | 1.3-V digital core power supply for USB PHY. This signal must be powered on in the order listed in Section 5.3.1 , <i>Power-Supply Sequencing</i> . When the USB peripheral is not used, the USB_VDD1P3 signal should be connected to ground (V _{SS}). |
| USB_VSS1P3 | H13 | GND | see Section 4.2 , ROC | Digital core ground for USB phy. |
| USB_VDDPLL | G8 | S | see Section 4.2 , ROC | 3.3 V USB Analog PLL power supply. When the USB peripheral is not used, the USB_VDDPLL signal should be connected to ground (V _{SS}). |
| USB_VSSPLL | G11 | GND | see Section 4.2 , ROC | USB Analog PLL ground. |

2.5.10 LCD Bridge Terminal Functions

Table 2-14. LCD Bridge Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--|-----|----------------------------|---------------------------------|--|
| LCD_EN_RDB/ SPI_CLK | N3 | O/Z | DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge and SPI.</p> <p>For LCD Bridge, this pin is either LCD Bridge read/write enable (MPU68 mode) or read strobe (MPU80 mode).</p> <p>Mux control via the PPMODE bits in the EBSR.</p> <p>Note: This pin may consume static power if configured as Hi-Z and not pulled high or low. Prevent current drain by externally terminating the pin.</p> |
| LCD_CS0_E0/ SPI_CS0 | P4 | I/O/Z | DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge and SPI.</p> <p>For LCD Bridge, this pin is either LCD Bridge chip select 0 (MPU68 and MPU80 modes) or enable 0 (HD44780 mode).</p> <p>Mux control via the PPMODE bits in the EBSR.</p> |
| LCD_CS1_E1/ SPI_CS1 | N4 | I/O/Z | DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge and SPI.</p> <p>For LCD Bridge, this pin is either LCD Bridge chip select 1 (MPU68 and MPU80 modes) or enable 1 (HD44780 mode).</p> <p>Mux control via the PPMODE bits in the EBSR.</p> |
| LCD_RW_WRB/ SPI_CS2 | P5 | I/O/Z | DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge and SPI.</p> <p>For LCD, this pin is either LCD Bridge read/write select (HD44780 and MPU68 modes) or write strobe (MPU80 mode).</p> <p>Mux control via the PPMODE bits in the EBSR.</p> |
| LCD_RS/ SPI_CS3 | N5 | I/O/Z | DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge and SPI.</p> <p>For LCD, this pin is the LCD Bridge address set-up.</p> <p>Mux control via the PPMODE bits in the EBSR.</p> |
| LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX | P14 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.</p> <p>For LCD Bridge, it is LCD data pin 15.</p> <p>Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.</p> |
| LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX | N13 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.</p> <p>For LCD Bridge, it is LCD data pin 14.</p> <p>Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.</p> |
| LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS | P13 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3.</p> <p>For LCD Bridge, it is LCD data pin 13.</p> <p>Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.</p> |
| LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK | N12 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between LCD Bridge, I2S2, and GPIO.</p> <p>For LCD Bridge, it is LCD data pin 12.</p> <p>Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register.</p> |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

Table 2-14. LCD Bridge Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE⁽¹⁾ (2) | OTHER⁽³⁾ (4) | DESCRIPTION |
|--|------------|-----------------------------------|---------------------------------|--|
| LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX | P12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 11. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX | N11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 10. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0 | P11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 9. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK | N10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For LCD Bridge, it is LCD data pin 8. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[7]/ GP[17] | P10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 7. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[6]/ GP[16] | N9 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 6. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[5]/ GP[15] | P9 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 5. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[4]/ GP[14] | N8 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 4. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[3]/ GP[13] | N7 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 3. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[2]/ GP[12] | P7 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For LCD Bridge, it is LCD data pin 2. Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[1]/ SPI_TX | N6 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, it is LCD data pin 1. Mux control via the PPMODE bits in the EBSR. |
| LCD_D[0]/ SPI_RX | P6 | I/O/Z | DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and SPI. For LCD Bridge, it is LCD data pin 0. Mux control via the PPMODE bits in the EBSR. |

2.5.11 MMC/SD Terminal Functions

Table 2-15. MMC1/SD Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|---------------------------------|-----|----------------------------|---------------------------------|---|
| MMC/SD | | | | |
| MMC1_CLK/ I2S1_CLK/ GP[6] | M13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For MMC/SD, this is the MMC1 data clock output MMC1_CLK. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_CMD/ I2S1_FS/ GP[7] | L14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For MMC/SD, this is the MMC1 command I/O output MMC1_CMD. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D3/ GP[11] | L13 | I/O/Z | IPD DV _{DDIO} BH | The MMC1_D3 and MMC1_D2 pins are multiplexed between MMC1 and GPIO. The MMC1_D1 and MMC1_D0 pins are multiplexed between MMC1, I2S1, and GPIO. In MMC/SD mode, all these pins are the MMC1 nibble wide bi-directional data bus. Mux control via the SP1MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D2/ GP[10] | K14 | I/O/Z | IPD DV _{DDIO} BH | |
| MMC1_D1/ I2S1_RX/ GP[9] | M12 | I/O/Z | IPD DV _{DDIO} BH | |
| MMC1_D0/ I2S1_DX/ GP[8] | M14 | I/O/Z | IPD DV _{DDIO} BH | |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

Table 2-16. MMC0/SD Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|---------------------------------|-----|----------------------------|---------------------------------|---|
| MMC/SD | | | | |
| MMC0_CLK/ I2S0_CLK/ GP[0] | L10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC0, I2S0, and GPIO. For MMC/SD, this is the MMC0 data clock output MMC0_CLK. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC0_CMD/ I2S0_FS/ GP[1] | M11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC0, I2S0, and GPIO. For MMC/SD, this is the MMC0 command I/O output MMC0_CMD. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC0_D3/ GP[5] | L11 | I/O/Z | IPD DV _{DDIO} BH | The MMC0_D3 and MMC0_D2 pins are multiplexed between MMC0 and GPIO. The MMC0_D1 and MMC0_D0 pins are multiplexed between MMC0, I2S0, and GPIO. In MMC/SD mode, these pins are the MMC0 nibble wide bi-directional data bus. Mux control via the SP0MODE bits in the EBSR. The IPD resistor on these pins can be enabled or disabled via the PDINHIBR1 register. |
| MMC0_D2/ GP[4] | L12 | I/O/Z | IPD DV _{DDIO} BH | |
| MMC0_D1/ I2S0_RX/ GP[3] | M10 | I/O/Z | IPD DV _{DDIO} BH | |
| MMC0_D0/ I2S0_DX/ GP[2] | L9 | I/O/Z | IPD DV _{DDIO} BH | |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

2.5.12 SAR ADC Terminal Functions

Table 2-17. 10-Bit SAR ADC Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|----------------|-----|----------------------------|--------------------------|---|
| SAR ADC | | | | |
| GPAIN0 | D10 | I/O | V _{DDA_ANA} | GPAIN0: General -Purpose Output and Analog Input pin 0. This pin is demuxed internally into ADC Channels 0, 1, & 2. GPAIN0 can also be used as a general-purpose open-drain output. This pin is unique among the GPAIN pins in that it is the only pin that is 3.6 V-tolerant to support measuring a battery voltage. GPAIN0 can accommodate input voltages from 0 V to 3.6 V; although, the ADC is unable to accept signals greater than V _{DDA_ANA} without clamping. ADC Channel 1 is capable of switching in an internal resistor divider that has a divide ratio of approximately 1/8. |
| GPAIN1 | A11 | I/O | V _{DDA_ANA} | GPAIN1: General -Purpose Output and Analog Input pin 1. This pin is connected to ADC Channel 3. GPAIN1 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN1 can accommodate input voltages from 0 V to V _{DDA_ANA} . Note: If the ANA_LDO is used to supply power to V _{DDA_ANA} , this pin must not be used as a general-purpose output (driving high) since the max current capability (see the I _{SD} parameter in Section 4.3, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature) of the ANA_LDO can be exceeded. Doing so may result in the on-chip power-on reset (POR) resetting the chip. |
| GPAIN2 | B11 | I/O | V _{DDA_ANA} | GPAIN2: General -Purpose Output and Analog Input pin 2. This pin is connected to ADC Channel 4. GPAIN2 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN2 can accommodate input voltages from 0 V to V _{DDA_ANA} . Note: If the ANA_LDO is used to supply power to V _{DDA_ANA} , this pin must not be used as a general-purpose output (driving high) since the max current capability (see the I _{SD} parameter in Section 4.3, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip. |
| GPAIN3 | C11 | I/O | V _{DDA_ANA} | GPAIN3: General -Purpose Output and Analog Input pin 3. This pin is connected to ADC Channel 5. GPAIN3 can be used as a general-purpose output if certain requirements are met (see the following note). GPAIN3 can accommodate input voltages from 0 V to V _{DDA_ANA} . Note: If the ANA_LDO is used to supply power to V _{DDA_ANA} , this pin must not be used as a general-purpose output (driving high) since the max current capability (see the I _{SD} parameter in Section 4.3, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature) of the ANA_LDO can be exceeded. Doing so may result in the on-chip POR resetting the chip. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

2.5.13 GPIO Terminal Functions

Table 2-18. GPIO Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|-------------------------------------|-----|----------------------------|---------------------------------|---|
| General-Purpose Input/Output | | | | |
| XF | M8 | O/Z | – DV _{DDIO} BH | <p>External Flag Output. XF is used for signaling other processors in multiprocessor configurations or XF can be used as a fast general-purpose output pin.</p> <p>XF is set high by the BSET XF instruction and XF is set low by the BCLR XF instruction or by writing to bit 13 of the ST1_55 register. For more information on the ST1_55 register, see the <i>TMS320C55x 3.0 CPU Reference Guide</i> (literature number: SWPU073).</p> <p>For XF pin behavior at reset, see Section 5.7.2, Pin Behaviors at Reset.</p> <p>Note: This pin may consume static power if configured as Hi-Z and not externally pulled low or high. Prevent current drain by externally terminating the pin. XF pin is ONLY in the Hi-Z state when doing boundary scan. Therefore, external termination is probably not required for most applications.</p> |
| MMC0_CLK/ I2S0_CLK/ GP[0] | L10 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC0, I2S0, and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 0 (GP[0]).</p> <p>Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.</p> |
| MMC0_CMD/ I2S0_FS/ GP[1] | M11 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC0, I2S0, and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 1 (GP[1]).</p> <p>Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.</p> |
| MMC0_D0/ I2S0_DX/ GP[2] | L9 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC0, I2S0, and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 2 (GP[2]).</p> <p>Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.</p> |
| MMC0_D1/ I2S0_RX/ GP[3] | M10 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC0, I2S0, and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 3 (GP[3]).</p> <p>Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.</p> |
| MMC0_D2/ GP[4] | L12 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC0 and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 4 (GP[4]).</p> <p>Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.</p> |
| MMC0_D3/ GP[5] | L11 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC0 and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 5 (GP[5]).</p> <p>Mux control via the SP0MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register.</p> |
| MMC1_CLK/ I2S1_CLK/ GP[6] | M13 | I/O/Z | IPD DV _{DDIO} BH | <p>This pin is multiplexed between MMC1, I2S1, and GPIO.</p> <p>For GPIO, it is general-purpose input/output pin 6 (GP[6]).</p> <p>Mux control via the SP1MODE bits in the EBSR.</p> |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
- (4) Specifies the operating I/O supply voltage for each signal

Table 2-18. GPIO Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|--------------------------------|-----|----------------------------|---------------------------------|---|
| MMC1_CMD/ I2S1_FS/ GP[7] | L14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 7 (GP[7]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D0/ I2S1_DX/ GP[8] | M14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 8 (GP[8]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D1/ I2S1_RX/ GP[9] | M12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1, I2S1, and GPIO. For GPIO, it is general-purpose input/output pin 9 (GP[9]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D2/ GP[10] | K14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1 and GPIO. For GPIO, it is general-purpose input/output pin 10 (GP[10]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| MMC1_D3/ GP[11] | L13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between MMC1 and GPIO. For GPIO, it is general-purpose input/output pin 11 (GP[11]). Mux control via the SP1MODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR1 register. |
| LCD_D[2]/ GP[12] | P7 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 12 (GP[12]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[3]/ GP[13] | N7 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 13 (GP[13]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[4]/ GP[14] | N8 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 14 (GP[14]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[5]/ GP[15] | P9 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 15 (GP[15]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[6]/ GP[16] | N9 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 16 (GP[16]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[7]/ GP[17] | P10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 17 (GP[17]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |

Table 2-18. GPIO Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE⁽¹⁾ (2) | OTHER⁽³⁾ (4) | DESCRIPTION |
|--|------------|-----------------------------------|----------------------------------|--|
| LCD_D8]/ I2S2_CLK/ GP[18]/ SPI_CLK | N10 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge and GPIO. For GPIO, it is general-purpose input/output pin 18 (GP[18]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0 | P11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, and GPIO. For GPIO, it is general-purpose input/output pin 19 (GP[19]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX | N11 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO and SPI. For GPIO, it is general-purpose input/output pin 20 (GP[20]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| EM_A[15]/GP[21] | N1 | I/O/Z | IPD DV _{DDEMF} BH | This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 21 (GP[21]). Mux control via the A15_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[16]/GP[22] | E2 | I/O/Z | IPD DV _{DDEMF} BH | This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 22 (GP[22]). Mux control via the A16_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[17]/GP[23] | F2 | I/O/Z | IPD DV _{DDEMF} BH | This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 23 (GP[23]). Mux control via the A17_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[18]/GP[24] | G2 | I/O/Z | IPD DV _{DDEMF} BH | This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 24 (GP[24]). Mux control via the A18_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[19]/GP[25] | G4 | I/O/Z | IPD DV _{DDEMF} BH | This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 25 (GP[25]). Mux control via the A19_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| EM_A[20]/GP[26] | J3 | I/O/Z | IPD DV _{DDEMF} BH | This pin is multiplexed between EMIF and GPIO. For GPIO, it is general-purpose input/output pin 26 (GP[26]). Mux control via the A20_MODE bit in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR2 register. |
| LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX | P12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, I2S2, GPIO, and SPI. For GPIO, it is general-purpose input/output pin 27 (GP[27]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK | N12 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 28 (GP[28]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |

Table 2-18. GPIO Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|---|-----|----------------------------|---------------------------------|--|
| LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS | P13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 29 (GP[29]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX | N13 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 30 (GP[30]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |
| LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX | P14 | I/O/Z | IPD DV _{DDIO} BH | This pin is multiplexed between LCD Bridge, UART, GPIO, and I2S3. For GPIO, it is general-purpose input/output pin 31 (GP[31]). Mux control via the PPMODE bits in the EBSR. The IPD resistor on this pin can be enabled or disabled via the PDINHIBR3 register. |

2.5.14 Regulators and Power Management Terminal Functions

Table 2-19. Regulators and Power Management Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|-------------------|---------------------|----------------------------|--------------------------|--|
| Regulators | | | | |
| DSP_LDOO | E10 | S | | DSP_LDO output. When enabled, this output provides a regulated 1.3 V or 1.05 V output and up to 250 mA of current (see the I _{SD} parameter in Section 4.3 , Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature). The DSP_LDO is intended to supply current to the digital core circuits only (CV _{DD}) and not external devices. For proper device operation, the external decoupling capacitor of this pin should be 5µF ~ 10µF. For more detailed information, see Section 5.3.4 , Power-Supply Decoupling. When disabled, this pin is in the high-impedance (Hi-Z) state. |
| LDOI | F14, F13, B12 | S | | LDO inputs. For proper device operation, LDOI must always be powered. The LDOI pins must be connected to the same power supply source with a voltage range of 1.8 V to 3.6 V. These pins supply power to the internal LDOs, the bandgap reference generator circuits, and serve as the I/O supply for some input pins. |
| DSP_LDO_EN | D12 | I | LDOI | DSP_LDO enable input. This signal is not intended to be dynamically switched. 0 = DSP_LDO is enabled. The internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal. 1 = DSP_LDO is disabled. The internal POR voltage monitoring is also disabled. The internal POWERGOOD signal is forced high and the external reset signal on the RESET pin (D6) is the only source of the device reset. Note, the device's internal reset signal is generated as the logical AND of the RESET pin and the internal POWERGOOD signal. |
| USB_LDOO | F12 | S | | USB_LDO output. This output provides a regulated 1.3 V output and up to 25 mA of current (see the I _{SD} parameter in Section 4.3 , Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature). For proper device operation, this pin must be connected to a 1 µF ~ 2 µF decoupling capacitor to V _{SS} . For more detailed information, see Section 5.3.4 , Power-Supply Decoupling. This LDO is intended to supply power to the USB_ V _{DD1P3} , USB_ V _{DDA1P3} pins and not external devices. |
| ANA_LDOO | A12 | S | | ANA_LDO output. This output provides a regulated 1.3 V output and up to 4 mA of current (see the I _{SD} parameter in Section 4.3 , Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature). For proper device operation, this pin must be connected to an ~ 1.0 µF decoupling capacitor to V _{SS} . For more detailed information, see Section 5.3.4 , Power-Supply Decoupling. This LDO is intended to supply power to the V _{DDA_ANA} and V _{DDA_PLL} pins and not external devices. |
| BG_CAP | B13 | A, I/O | | Bandgap reference filter signal. For proper device operation, this pin needs to be bypassed with a 0.1 µF capacitor to analog ground (V _{SSA_ANA}). This external capacitor provides filtering for stable reference voltages & currents generated by the bandgap circuit. The bandgap produces the references for use by the System PLL, SAR, and POR circuits. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
- (2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
- (3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1](#), Pullup/Pulldown Resistors.
- (4) Specifies the operating I/O supply voltage for each signal

2.5.15 Reserved and No Connects Terminal Functions

Table 2-20. Reserved and No Connects Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|-----------------|-----|----------------------------|--------------------------|---|
| Reserved | | | | |
| RSV0 | C12 | I | – LDOI | Reserved. For proper device operation, this pin must be tied directly to V _{SS} . |
| RSV1 | J10 | PWR | | Reserved. For proper device operation, this pin must be tied directly to CV _{DD} . |
| RSV2 | J11 | PWR | | Reserved. For proper device operation, this pin must be tied directly to CV _{DD} . |
| RSV3 | D14 | I | – LDOI | Reserved. For proper device operation, this pin must be tied directly to V _{SS} . |
| RSV4 | C14 | I | – LDOI | Reserved. For proper device operation, this pin must be tied directly to V _{SS} . |
| RSV5 | C13 | I | – LDOI | Reserved. For proper device operation, this pin must be tied directly to V _{SS} . |
| RSV16 | D13 | I | – LDOI | Reserved. For proper device operation, this pin must be directly tied to V _{SS} . |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive IO-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1, Pullup/Pulldown Resistors](#).
(4) Specifies the operating I/O supply voltage for each signal

2.5.16 Supply Voltage Terminal Functions

Table 2-21. Supply Voltage Terminal Functions

| SIGNAL NAME NO. | | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|------------------------|-----|----------------------------|---------------------------------------|---|
| SUPPLY VOLTAGES | | | | |
| CV _{DD} | F6 | PWR | | 1.05-V Digital Core supply voltage (60 or 75 MHz) 1.3-V Digital Core supply voltage (100 or 120 MHz) |
| | H8 | | | |
| | J6 | | | |
| | K10 | | | |
| | L5 | | | |
| DV _{DDIO} | F7 | PWR | | 1.8-V, 2.5-V, 2.75-V, or 3.3-V I/O power supply for non-EMIF and non-RTC I/Os The DV _{DDIO} must always be powered for proper operation. |
| | K7 | | | |
| | K12 | | | |
| | N14 | | | |
| | P3 | | | |
| DV _{DDEMIF} | P8 | PWR | | 1.8-V, 2.5-V, 2.75-V, or 3.3-V EMIF I/O power supply Note: When EMIF is not used, it is permissible to ground the DV _{DDEMIF} supply pins if the following conditions are all met: <ul style="list-style-type: none"> At least one DV_{DDEMIF} package ball (A2, A5, E6, F5, G5, H5, H7, J5, P2) is grounded. The others must be either floating or grounded. All signal pins that use DV_{DDEMIF} as their I/O supply voltage (i.e., all pins listed in Table 2-8, External Memory Interface Terminal Functions), regardless of multiplexing options, are either: <ul style="list-style-type: none"> all grounded all floating (not driven by any external source), or any combination of grounded or floating. |
| | A2 | | | |
| | A5 | | | |
| | E6 | | | |
| | F5 | | | |
| | G5 | | | |
| | H5 | | | |
| | H7 | | | |
| CV _{DDRTC} | C8 | PWR | | 1.05-V thru 1.3-V RTC digital core and RTC oscillator power supply. Note: The CV _{DDRTC} must always be powered by an external power source even though RTC is not used. CV _{DDRTC} cannot be powered by any of the on-chip LDOs. |
| | | | | |
| DV _{DDRTC} | F8 | PWR | | 1.8-V, 2.5-V, 2.75-V, or 3.3-V I/O power supply for RTC_CLOCKOUT and WAKEUP pins. Note: The DV _{DDRTC} can be tied to ground (V _{SS}) when the RTC_CLKOUT and WAKEUP pins are not permanently used. In this case, the WAKEUP pin must be configured as output by software (see Table 5-24 , <i>RTCPMGT Register Bit Descriptions</i>). |
| V _{DDA_PLL} | C10 | PWR | see Section 4.2 , ROC | 1.3-V Analog PLL power supply for the system clock generator (PLLOUT ≤ 120 MHz). This signal can be powered from the ANA_LDOO pin. |
| USB_V _{DDPLL} | G8 | S | see Section 4.2 , ROC | 3.3 V USB Analog PLL power supply. When the USB peripheral is not used, the USB_V _{DDPLL} signal should be connected to ground (V _{SS}). |
| USB_V _{DD1P3} | J13 | S | see Section 4.2 , ROC | 1.3-V digital core power supply for USB PHY. When the USB peripheral is not used, the USB_V _{DD1P3} signal should be connected to ground (V _{SS}). |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1](#), *Pullup/Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 2-21. Supply Voltage Terminal Functions (continued)

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|-------------------------|-----|----------------------------|---|---|
| USB_V _{DDA1P3} | H10 | S | see Section 4.2 , ROC | Analog 1.3 V power supply for USB PHY. [For high-speed sensitive analog circuits] When the USB peripheral is not used, the USB_V _{DDA1P3} signal should be connected to ground (V _{SS}). |
| USB_V _{DDA3P3} | H12 | S | see Section 4.2 , ROC | Analog 3.3 V power supply for USB PHY. When the USB peripheral is not used, the USB_V _{DDA3P3} signal should be connected to ground (V _{SS}). |
| USB_V _{DDOSC} | G12 | S | see Section 4.2 , ROC | 3.3-V power supply for USB oscillator. When the USB peripheral is not used, USB_V _{DDOSC} should be connected to ground (V _{SS}). |
| V _{DDA_ANA} | A10 | PWR | | 1.3-V supply for power management and 10-bit SAR ADC This signal can be powered from the ANA_LDOO pin. |

2.5.17 Ground Terminal Functions

Table 2-22. Ground Terminal Functions

| SIGNAL NAME | NO. | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|-------------------------|-----|----------------------------|---|---|
| V _{SS} | A13 | GND | | Ground pins |
| | A14 | | | |
| | D7 | | | |
| | D11 | | | |
| | E9 | | | |
| | E11 | | | |
| | E12 | | | |
| | E13 | | | |
| | E14 | | | |
| | F9 | | | |
| | F10 | | | |
| | G6 | | | |
| | G7 | | | |
| | H6 | | | |
| | J7 | | | |
| | J8 | | | |
| | J9 | | | |
| | K8 | | | |
| | K9 | | | |
| | K11 | | | |
| | K13 | | | |
| V _{SSRTC} | C9 | GND | | Ground for RTC oscillator. When using a 32.768-KHz crystal, this pin is a local ground for the crystal and must not be connected to the board ground (See Figure 5-4 and Figure 5-5). When not using RTC and the crystal is not populated on the board, this pin is connected to the board ground. |
| V _{SSA_PLL} | D9 | GND | see Section 4.2 , ROC | Analog PLL ground for the system clock generator. |
| USB_V _{SSPLL} | G11 | GND | see Section 4.2 , ROC | USB Analog PLL ground. |
| USB_V _{SS1P3} | H13 | GND | see Section 4.2 , ROC | Digital core ground for USB phy. |
| USB_V _{SSA1P3} | H9 | GND | see Section 4.2 , ROC | Analog ground for USB PHY [For high speed sensitive analog circuits]. |
| USB_V _{SSA3P3} | H11 | GND | see Section 4.2 , ROC | Analog ground for USB PHY. |
| USB_V _{SSOSC} | F11 | S | see Section 4.2 , ROC | Ground for USB oscillator. |

- (1) I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground, A = Analog signal, BH = Bus Holder
(2) Input pins of type I, I/O, and I/O/Z are required to be driven at all times. To achieve the lowest power, these pins must not be allowed to float. When they are configured as input or high-impedance state, and not driven to a known state, they may cause an excessive I/O-supply current. Prevent this current by externally terminating it or enabling IPD/IPU, if applicable.
(3) IPD = Internal pulldown, IPU = Internal pullup. For more detailed information on pullup/pulldown resistors and situations where external pullup/pulldown resistors are required, see [Section 3.8.1](#), *Pullup/Pulldown Resistors*.
(4) Specifies the operating I/O supply voltage for each signal

Table 2-22. Ground Terminal Functions (continued)

| SIGNAL NAME NO. | | TYPE ⁽¹⁾ (2) | OTHER ⁽³⁾ (4) | DESCRIPTION |
|------------------------|------------|----------------------------|---|--|
| USB_V _{SSREF} | G10 | GND | see Section 4.2 , ROC | Ground for reference current. This must be connected via a 10-kΩ ±1% resistor to USB_R1. When the USB peripheral <i>is not</i> used, the USB_V _{SSREF} signal should be connected directly to ground (V _{SS}). |
| V _{SSA_ANA} | B10 B14 | GND | | Ground pins for power management (POR & Bandgap circuits) and 10-bit SAR ADC |

3 Device Configuration

3.1 System Registers

The system registers in [Table 3-1](#) configure the device and monitor its status.

Table 3-1. Idle Control, Status, and System Registers

| CPU WORD ADDRESS | ACRONYM | Register Description | COMMENTS |
|------------------|------------------------|--|-------------------------------------|
| 0001h | ICR | Idle Control Register | |
| 0002h | ISTR | Idle Status Register | |
| 1C00h | EBSR | External Bus Selection Register | see Section 3.6.1 . |
| 1C02h | PCGCR1 | Peripheral Clock Gating Control Register 1 | |
| 1C03h | PCGCR2 | Peripheral Clock Gating Control Register 2 | |
| 1C04h | PSRCR | Peripheral Software Reset Counter Register | |
| 1C05h | PRCR | Peripheral Reset Control Register | |
| 1C14h | TIAFR | Timer Interrupt Aggregation Flag Register | |
| 1C16h | ODSCR | Output Drive Strength Control Register | |
| 1C17h | PDINHIBR1 | Pull-Down Inhibit Register 1 | |
| 1C18h | PDINHIBR2 | Pull-Down Inhibit Register 2 | |
| 1C19h | PDINHIBR3 | Pull-Down Inhibit Register 3 | |
| 1C1Ah | DMA0CESR1 | DMA0 Channel Event Source Register 1 | |
| 1C1Bh | DMA0CESR2 | DMA0 Channel Event Source Register 2 | |
| 1C1Ch | DMA1CESR1 | DMA1 Channel Event Source Register 1 | |
| 1C1Dh | DMA1CESR2 | DMA1 Channel Event Source Register 2 | |
| 1C26h | ECDR | EMIF Clock Divider Register | |
| 1C28h | RAMSLPMDCNTLR1 | DARAM Sleep Mode Control Register 1 | |
| 1C2Ah | RAMSLPMDCNTLR2 | SARAM Sleep Mode Control Register 2 | |
| 1C2Bh | RAMSLPMDCNTLR3 | SARAM Sleep Mode Control Register 3 | |
| 1C2Ch | RAMSLPMDCNTLR4 | SARAM Sleep Mode Control Register 4 | |
| 1C2Dh | RAMSLPMDCNTLR5 | SARAM Sleep Mode Control Register 5 | |
| 1C30h | DMAIFR | DMA Interrupt Flag Aggregation Register | |
| 1C31h | DMAIER | DMA Interrupt Enable Register | |
| 1C32h | USBSR | USB System Control Register | |
| 1C33h | ESCR | EMIF System Control Register | |
| 1C36h | DMA2CESR1 | DMA2 Channel Event Source Register 1 | |
| 1C37h | DMA2CESR2 | DMA2 Channel Event Source Register 2 | |
| 1C38h | DMA3CESR1 | DMA3 Channel Event Source Register 1 | |
| 1C39h | DMA3CESR2 | DMA3 Channel Event Source Register 2 | |
| 1C3Ah | CLKSTOP | Peripheral Clock Stop Request/Acknowledge Register | |
| 1C40h | DIEIDR0 ⁽¹⁾ | Die ID Register 0 | |
| 1C41h | DIEIDR1 ⁽¹⁾ | Die ID Register 1 | |
| 1C42h | DIEIDR2 ⁽¹⁾ | Die ID Register 2 | |
| 1C43h | DIEIDR3 ⁽¹⁾ | Die ID Register 3 | |
| 1C44h | DIEIDR4 ⁽¹⁾ | Die ID Register 4 | |
| 1C45h | DIEIDR5 ⁽¹⁾ | Die ID Register 5 | |
| 1C46h | DIEIDR6 ⁽¹⁾ | Die ID Register 6 | |
| 1C47h | DIEIDR7 ⁽¹⁾ | Die ID Register 7 | |
| 7004h | LDOCNTL | LDO Control Register | see Figure 3-1 . |

(1) This register is reserved.

3.2 Power Considerations

The device provides several means of managing power consumption.

To minimize power consumption, the device divides its circuits into nine main isolated supply domains:

- LDO (LDOs and Bandgap Power Supply)
- Analog POR, SAR, and PLL (V_{DDA_ANA} and V_{DDA_PLL})
- RTC Core (CV_{DDRTC}) — **Note:** CV_{DDRTC} must always be powered by an external power source and none of the on-chip LDOs can be used to power CV_{DDRTC} .
- Digital Core (CV_{DD})
- USB Core (USB_V_{DD1P3} and USB_V_{DDA1P3})
- USB PHY and USB PLL (USB_V_{DDOSC} , USB_V_{DDA3P3} , and USB_V_{DDPLL})
- EMIF I/O (DV_{DDEMF})
- RTC I/O (DV_{DDRTC})
- Rest of the I/O (DV_{DDIO})

3.2.1 LDO Configuration

The device includes three Low-Dropout Regulators (LDOs) which can be used to regulate the power supplies of the analog PLL and SAR ADC/Power Management (ANA_LDO), Digital Core (DSP_LDO), and USB Core (USB_LDO).

These LDOs are controlled by a combination of pin configuration and register settings. For more detailed information see the following sections.

3.2.1.1 LDO Inputs

The LDO pins (B12, F13, F14) provide power to the internal Analog LDO, DSP LDO, USB LDO, the bandgap reference generator, and some I/O input pins, and can range from 1.8 V to 3.6 V. The bandgap provides accurate voltage and current references to the POR, LDOs, PLL, and SAR; therefore, for proper device operation, power **must** always be applied to the LDO pins even if the LDO outputs are **not** used.

3.2.1.2 LDO Outputs

The ANA_LDOO pin (A12) is the output of the internal ANA_LDO and can provide regulated 1.3 V power of up to 4 mA. The ANA_LDOO pin is intended to be connected, on the board, to the V_{DDA_ANA} and V_{DDA_PLL} pins to provide a regulated 1.3 V to the 10-bit SAR ADC, Power Management Circuits, and System PLL. V_{DDA_ANA} and V_{DDA_PLL} may be powered by this LDO output, which is recommended, to take advantage of the device's power management techniques, or by an external power supply. The ANA_LDO cannot be disabled individually (see [Section 3.2.1.3, LDO Control](#)).

The DSP_LDOO pin (E10) is the output of the internal DSP_LDO and provides software-selectable regulated 1.3 V or regulated 1.05 V power of up to 250 mA. The DSP_LDOO pin is intended to be connected, on the board, to the CV_{DD} pins. In this configuration, the DSP_LDO_EN pin should be tied to the board V_{SS} , thus enabling the DSP_LDO. Optionally, the CV_{DD} pins may be powered by an external power supply; in this configuration the DSP_LDO_EN pin should be tied (high) to LDO pin, disabling DSP_LDO. The DSP_LDO_EN also affects how reset is generated to the chip (for more details, see the DSP_LDO_EN pin description in [Table 2-19, Regulators and Power Management Terminal Functions](#)). When the DSP_LDO is disabled, its output pin is in a high-impedance state. Note: DSP_LDO_EN is **not** intended to be changed dynamically.

The USB_LDOO pin (F12) is the output of the internal USB_LDO and provides regulated 1.3 V, software-switchable (on/off) power of up to 25 mA. The USB_LDOO pin is intended to be connected, on the board, to the USB_V_{DD1P3} and USB_V_{DDA1P3} pins to provide power to portions of the USB. Optionally, the USB_V_{DD1P3} and USB_V_{DDA1P3} may be powered by an external power supply and the USB_LDO can be left disabled. When the USB_LDO is disabled, its output pin is in a high-impedance state.

3.2.1.3 LDO Control

All three LDOs can be simultaneously disabled via software by writing to either the BG_PD bit or the LDO_PD bit in the RTCPMGT register (see [Figure 5-26](#)). When the LDOs are disabled via this mechanism, the only way to re-enable them is by asserting the WAKEUP signal pin (which must also have been previously enabled to allow wakeup), or by a previously enabled and configured RTC alarm, or by cycling power to the CV_{DDRTC} pin. **Note:** CV_{DDRTC} must be externally powered. None of the on-chip LDOs can be used to power CV_{DDRTC}.

ANA_LDO: The ANA_LDO is only disabled by the BG_PD and the LDO_PD mechanism described above. Otherwise, it is always enabled.

DSP_LDO: The DSP_LDO can be statically disabled by the $\overline{\text{DSP_LDO_EN}}$ pin as described in [Section 3.2.1.2, LDO Outputs](#). It can be also dynamically disabled via the BG_PD and the LDO_PD mechanism described above. The DSP_LDO can change its output voltage dynamically by software via the DSP_LDO_V bit in the LDOCNTL register (see [Figure 3-1](#)). The DSP_LDO output voltage is set to 1.3 V at reset.

USB_LDO: The USB_LDO can be independently and dynamically enabled or disabled by software via the USB_LDO_EN bit in the LDOCNTL register (see [Figure 3-1](#)). The USB_LDO is disabled at reset.

[Table 3-3](#) shows the ON/OFF control of each LDO and its register control bit configurations.

| | | | |
|----------|----------|-----------|------------|
| 15 | Reserved | | 8 |
| R-0 | | | |
| 7 | 2 | 1 | 0 |
| Reserved | | DSP_LDO_V | USB_LDO_EN |
| R-0 | | | |

Table 3-2. LDOCNTL Register Bit Descriptions

Table 3-3. LDO Controls Matrix

| RTCPMGT Register (0x1930) | | LDOCNTL Register (0x7004) | <u>DSP_LDO_EN</u> (Pin D12) | ANA_LDO | DSP_LDO | USB_LDO |
|------------------------------|------------|------------------------------|--------------------------------|---------|---------|---------|
| BG_PD Bit | LDO_PD Bit | USB_LDO_EN Bit | | | | |
| 1 | Don't Care | Don't Care | Don't Care | OFF | OFF | OFF |
| Don't Care | 1 | Don't Care | Don't Care | OFF | OFF | OFF |
| 0 | 0 | 0 | Low | ON | ON | OFF |
| 0 | 0 | 0 | High | ON | OFF | OFF |
| 0 | 0 | 1 | Low | ON | ON | ON |

3.3 Clock Considerations

The system clock, which is used by the CPU and most of the DSP peripherals, is controlled by the system clock generator. The system clock generator features a software-programmable PLL multiplier and several dividers. The clock generator accepts an input reference clock from the CLKIN pin or the output clock of the 32.768-KHz real-time clock (RTC) oscillator. The selection of the input reference clock is based on the state of the CLK_SEL pin. The CLK_SEL pin is required to be statically tied high or low and cannot change dynamically after reset.

In addition, the DSP requires a reference clock for USB applications. The USB reference clock is generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins.

The USB reference clock is not required if the USB peripheral is not being used. To completely disable the USB oscillator, connect the USB_MXI pin to ground (V_{SS}) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_V_{DDOSC} and USB_V_{SSOSC}) should also be connected to ground.

The RTC oscillator generates a clock when a 32.768-KHz crystal is connected to the RTC_XI and RTC_XO pins. The 32.768-KHz crystal can be disabled if CLKIN is used as the clock source for the DSP. However, when the RTC oscillator is disabled, the RTC peripheral will not operate and the RTC registers (I/O address range 1900h – 197Fh) will not be accessible. This includes the RTC power management register (RTCPMGT) which controls the RTCLKOUT and WAKEUP pins. To disable the RTC oscillator, connect the RTC_XI pin to CV_{DDRTC} and the RTC_XO pin to ground.

For more information on crystal specifications for the RTC oscillator and the USB oscillator, see [Section 5.4](#), *External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins*.

3.3.1 Clock Configurations After Device Reset

After reset, the on-chip Bootloader programs the system clock generator based on the input clock selected via the CLK_SEL pin. If CLK_SEL = 0, the Bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-kHz RTC oscillator clock by 375). If CLK_SEL = 1, the Bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin. In this case, the CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, or 12.288 MHz. While the bootloader tries to boot from the USB, the clock generator will be programmed to output approximately 36 MHz.

3.3.1.1 Device Clock Frequency

After the boot process is complete, the user is allowed to re-program the system clock generator to bring the device up to the desired clock frequency and the desired peripheral clock state (clock gating or not). The user must adhere to various clock requirements when programming the system clock generator. For more information, see [Section 5.5](#), *Clock PLLs*.

Note: The on-chip Bootloader allows for DSP registers to be configured during the boot process. However, this feature **must not** be used to change the output frequency of the system clock generator during the boot process. Timer0 is also used by the bootloader to allow for 200 ms of BG_CAP settling time. The bootloader register modification feature **must not** modify the Timer0 registers.

3.3.1.2 Peripheral Clock State

The clock and reset state of each of peripheral is controlled through a set of system registers. The peripheral clock gating control registers (PCGCR1 and PCGCR2) are used to enable and disable peripheral clocks. The peripheral software reset counter register (PSRCR) and the peripheral reset control register (PRCR) are used to assert and de-assert peripheral reset signals.

At hardware reset, all of the peripheral clocks are off to conserve power. After hardware reset, the DSP boots via the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. In other words, it reads each peripheral looking for a valid boot image file. At that time, the individual peripheral clocks will be enabled for the query and then disabled again when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be off and all domains in the ICR, except the CPU domain, will be idled.

3.3.1.3 USB Oscillator Control

The USB oscillator is controlled through the USB system control register (USBSCR). To enable the oscillator, the USBOSCDIS and USBOSCBIASDIS bits must be cleared to 0. The user must wait until the USB oscillator stabilizes before proceeding with the USB configuration. The USB oscillator stabilization time is typically 100 μ s, with a 10 ms maximum (**Note:** the startup time is highly dependent on the ESR and capacitive load on the crystal).

3.4 Boot Sequence

The boot sequence is a process by which the device's on-chip memory is loaded with program and data sections from an external image file (in flash memory, for example). The boot sequence also allows, optionally, for some of the device's internal registers to be programmed with predetermined values. The boot sequence is started automatically after each device reset. For more details on device reset, see [Section 5.7, Reset](#).

There are several methods by which the memory and register initialization can take place. Each of these methods is referred to as a boot mode. At reset, the device cycles through different boot modes until an image is found with a valid boot signature. The on-chip Bootloader allows the DSP registers to be configured during the boot process, if the optional register configuration section is present in the boot image (see [Figure 3-2](#)). For more information on the boot modes supported, see [Section 3.4.1, Boot Modes](#).

The device Bootloader follows the following steps as shown in [Figure 3-2](#)

1. Immediately after reset, the CPU fetches the reset vector from 0xFFFF00. MP/MC is 0 by default, so 0xFFFF00 is mapped to internal ROM. The PLL is in bypass mode.
2. Set CLKOUT slew rate control to slow slew rate.
3. Idle all peripherals, MPORT and HWA.
4. If CLK_SEL = 0, the Bootloader powers up the PLL and sets its output frequency to 12.288 MHz (with a 375x multiplier using VP = 749, VS = 0, input divider disabled, output divide-by-8 enabled, and output divider enabled with VO = 0). If CLK_SEL = 1, the Bootloader keeps the PLL bypassed.
5. Apply manufacturing trim to the bandgap references.
6. Disable CLKOUT.
7. Test for NOR boot on all asynchronous CS spaces ($\overline{\text{EM_CS}}[2:5]$) with 16-bit access:
 - (a) Check the first 2 bytes read from boot signature.
 - (b) If the boot signature is not valid, go to step 8.
 - (c) Set Register Configuration, if present in boot image.
 - (d) Attempt NOR boot, go to step 17.
8. Test for NAND boot on all asynchronous CS spaces ($\overline{\text{EM_CS}}[2:5]$) with 8-bit access:
 - (a) Check the first 2 bytes read from boot table for a boot signature match.
 - (b) If the boot signature is not valid, go to step 9.
 - (c) Set Register Configuration, if present in boot image.
 - (d) Attempt NAND boot, go to step 17.
9. Test for 16-bit and 24-bit SPI EEPROM boot on SPI_CS[0] with 500-KHz clock rate and for Parallel Port Mode on External bus Selection Register set to 5, then set to 6:
 - (a) Check the first 2 bytes read from boot table for a boot signature match using 16-bit address mode.
 - (b) If the boot signature is not valid, read the first 2 bytes again using 24-bit address mode.
 - (c) If the boot signature is not valid from either case (16-bit and 24-bit address modes), go to step 10.
 - (d) Set Register Configuration, if present in boot image.
 - (e) Attempt SPI Serial Memory boot, go to step 17.
10. Test for I2C EEPROM boot with a 7-bit slave address 0x50 and 400-kHz clock rate.
 - (a) Check the first 2 bytes read from boot table for a boot signature match.
 - (b) If the boot signature is not valid, go to step 11.
 - (c) Set Register Configuration, if present in boot image.
 - (d) Attempt I2C EEPROM boot, go to step 17.
11. Test for MMC/SD boot — **For more information on MMC/SD boot, contact your local sales representative.**
12. Set the PLL output to approximately 36 MHz. If CLK_SEL = 1, CLKIN multiplied by 3x, ; if CLK_SEL = 0, CLKIN is multiplied by 1125x.
13. Test for USB boot — **For more information on USB boot, contact your local sales representative.**

14. If the boot signature is **not** valid, then go back to step 14 and repeat.
15. Set register configuration.
16. Copy boot image sections to system memory.
17. Enable TIMER0 to start counting 200 ms.
18. Ensure a minimum of 200 ms has elapsed since step 17 before proceeding to execute the bootloaded code.
19. Jump to the entry point specified in the boot image.

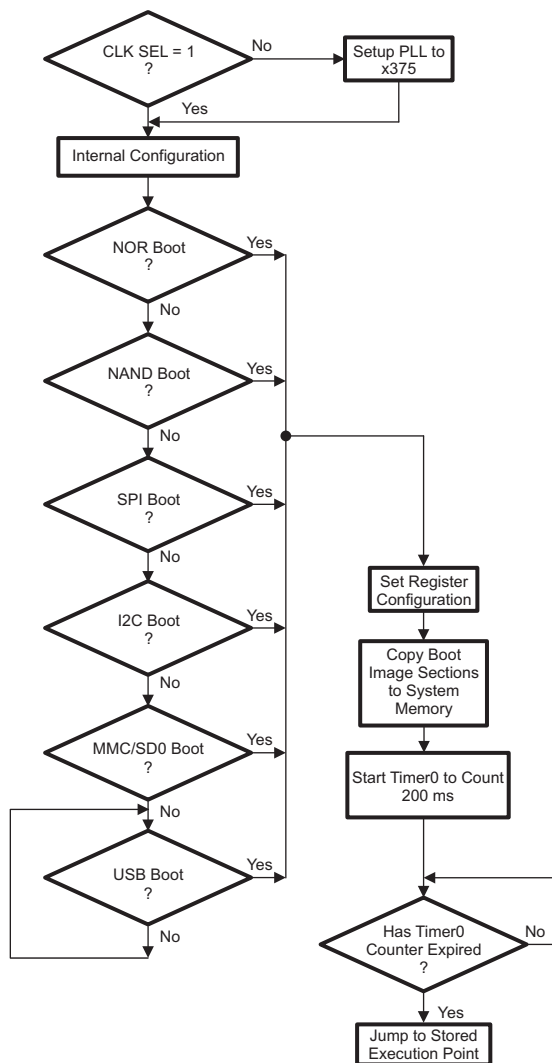


Figure 3-2. Bootloader Software Architecture

3.4.1 Boot Modes

The device DSP supports the following boot modes in the following device order: NOR Flash, NAND Flash, SPI 16-bit EEPROM, SPI 24-bit Flash, I2C EEPROM, and MMC/SD card. The boot mode is determined by checking for a valid boot signature on each supported boot device. The first boot device with a valid boot signature will be used to load and execute the user code. If none of the supported boot devices have a valid boot signature, the Bootloader goes into an endless loop checking the USB boot mode and the device must be reset to look for another valid boot image in the supported boot modes.

Note: For detailed information on MMC/SD and USB boot modes, contact your local sales representative.

3.4.2 Boot Configuration

After reset, the on-chip Bootloader programs the system clock generator based on the input clock selected via the CLK_SEL pin. If CLK_SEL = 0, the Bootloader programs the system clock generator and sets the system clock to 12.288 MHz (multiply the 32.768-KHz RTC oscillator clock by 375). If CLK_SEL = 1, the Bootloader bypasses the system clock generator altogether and the system clock is driven by the CLKIN pin.

Note:

- When CLK_SEL = 1, the CLKIN frequency is expected to be 11.2896 MHz, 12.0 MHz, or 12.288 MHz.
- The on-chip Bootloader allows for DSP registers to be configured during the boot process. However, this feature must not be used to change the output frequency of the system clock generator during the boot process. Timer0 is also used by the bootloader to allow for 200 ms of BG_CAP settling time. The bootloader register modification feature **must not** modify the Timer0 registers.

After hardware reset, the DSP boots via the bootloader code in ROM. During the boot process, the bootloader queries each peripheral to determine if it can boot from that peripheral. At that time, the individual peripheral clocks will be enabled for the query and then disabled when the bootloader is finished with the peripheral. By the time the bootloader releases control to the user code, all peripheral clocks will be "off" and all domains in the ICR, except the CPU domain, will be idled.

3.4.3 DSP Resources Used By the Bootloader

The Bootloader uses SARAM block 31 for the storing of temporary data. This block of memory is reserved during the boot process. However, after the boot process is complete, it can be used by the user application.

3.5 Configurations at Reset

Some device configurations are determined at reset. The following subsections give more details.

3.5.1 Device and Peripheral Configurations at Device Reset

Table 3-4 summarizes the device boot and configuration pins that are required to be statically tied high, tied low, or left unconnected during device operation. For proper device operation, a device reset should be initiated after changing any of these pin functions.

Table 3-4. Default Functions Affected by Device Configuration Pins

| CONFIGURATION PINS | SIGNAL NO. | IPU/IPD | FUNCTIONAL DESCRIPTION |
|--------------------|------------|---------|---|
| DSP_LDO_EN | D12 | – | <p>DSP_LDO enable input. This signal is not intended to be dynamically switched. 0 = DSP_LDO is enabled. The internal DSP LDO is enabled to regulate power on the DSP_LDOO pin at either 1.3 V or 1.05 V according to the LDO_DSP_V bit in the LDOCNTL register, see Figure 3-1). At power-on-reset, the internal POR monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO voltage is above a minimum threshold voltage. The internal device reset is generated by the AND of POWERGOOD and the RESET pin. 1 = DSP_LDO is disabled and the DSP_LDOO pin is in high-impedance (Hi-Z). The internal voltage monitoring on the DSP_LDOO is bypassed and the internal POWERGOOD signal is immediately set high. The RESET pin (D6) will act as the sole reset source for the device. If an external power supply is used to provide power to CV_{DD}, then DSP_LDO_EN should be tied to LDOI, DSP_LDOO should be left unconnected, and the RESET pin must be asserted appropriately for device initialization after powerup.</p> <p>Note: to pullup this pin, connect it to the same supply as LDOI pins.</p> |
| CLK_SEL | C7 | – | <p>Clock input select. 0 = 32-KHz on-chip oscillator drives the RTC timer and the system clock generator. CLKIN is ignored. 1 = CLKIN drives the system clock generator and the 32-KHz on-chip oscillator drives only the RTC timer.</p> <p>This pin is not allowed to change during device operation; it must be tied to DV_{DDIO} or GND at the board.</p> |

For proper device operation, external pullup/pulldown resistors may be required on these device configuration pins. For discussion on situations where external pullup/pulldown resistors are required, see Section 3.8.1, *Pullup/Pulldown Resistors*.

This device also has RESERVED pins that need to be configured correctly for proper device operation (statically tied high, tied low, or left unconnected at all times). For more details on these pins, see Table 2-20, *Reserved and No Connects Terminal Functions*.

3.6 Configurations After Reset

The following sections provide details on configuring the device after reset. Multiplexed pin functions are selected by software after reset. For more details on multiplexed pin function control, see [Section 3.7, Multiplexed Pin Configurations](#).

3.6.1 External Bus Selection Register (EBSR)

The External Bus Selection Register (EBSR) determines the mapping of the LCD controller, I2S2, I2S3, UART, SPI, and GPIO signals to 21 signals of the external parallel port pins. It also determines the mapping of the I2S or MMC/SD ports to serial port 1 pins and serial port 2 pins. The EBSR register is located at port address 0x1C00. Once the bit fields of this register are changed, the routing of the signals takes place on the next CPU clock cycle.

Additionally, the EBSR controls the function of the upper bits of the EMIF address bus. Pins EM_A[20:15]/GP[26:21] can be individually configured as GPIO pins through the Axx_MODE bits. When Axx_MODE = 1, the EM_A[xx] pin functions as a GPIO pin. When Axx_MODE = 0, the EM_A[xx] pin retains its EMIF functionality.

Before modifying the values of the external bus selection register, you must clock gate all affected peripherals through the Peripheral Clock Gating Control Register. After the external bus selection register has been modified, you must reset the peripherals before using them through the Peripheral Software Reset Counter Register.

Figure 3-3. External Bus Selection Register (EBSR) [1C00h]

| | | | | | | | | | | | | | | | |
|----------|--|----------|--|----------|--|----------|--|----------|--|----------|--|----------|--|----------|--|
| 15 | | 14 | | 12 | | 11 | | 10 | | 9 | | 8 | | | |
| Reserved | | PPMODE | | | | SP1MODE | | | | SP0MODE | | | | | |
| R-0 | | R/W-000 | | | | R/W-00 | | | | R/W-00 | | | | | |
| 7 | | 6 | | 5 | | 4 | | 3 | | 2 | | 1 | | 0 | |
| Reserved | | Reserved | | A20_MODE | | A19_MODE | | A18_MODE | | A17_MODE | | A16_MODE | | A15_MODE | |
| R-0 | | R-0 | | R/W-0 | | R/W-0 | | R/W-0 | | R/W-0 | | R/W-0 | | R/W-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 3-5. EBSR Register Bit Descriptions

| BIT | NAME | DESCRIPTION |
|-------|----------|---|
| 15 | RESERVED | Reserved. Read-only, writes have no effect. |
| 14:12 | PPMODE | Parallel Port Mode Control Bits. These bits control the pin multiplexing of the LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] pins on the parallel port. For more details, see Table 3-6, LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing . 000 = Mode 0 (16-bit LCD Controller). All 21 signals of the LCD Bridge module are routed to the 21 external signals of the parallel port. 001 = Mode 1 (SPI, GPIO, UART, and I2S2). 7 signals of the SPI module, 6 GPIO signals, 4 signals of the UART module and 4 signals of the I2S2 module are routed to the 21 external signals of the parallel port. 010 = Mode 2 (8-bit LCD Controller and GPIO). 8-bits of pixel data of the LCD Controller module and 8 GPIO are routed to the 21 external signals of the parallel port. 011 = Mode 3 (8-bit LCD Controller, SPI, and I2S3). 8-bits of pixel data of the LCD Controller module, 4 signals of the SPI module, and 4 signals of the I2S3 module are routed to the 21 external signals of the parallel port. 100 = Mode 4 (8-bit LCD Controller, I2S2, and UART). 8-bits of pixel data of the LCD Controller module, 4 signals of the I2S2 module, and 4 signals of the UART module are routed to the 21 external signals of the parallel port. 101 = Mode 5 (8-bit LCD Controller, SPI, and UART). 8-bits of pixel data of the LCD Controller module, 4 signals of the SPI module, and 4 signals of the UART module are routed to the 21 external signals of the parallel port. 110 = Mode 6 (SPI, I2S2, I2S3, and GPIO). 7 signals of the SPI module, 4 signals of the I2S2 module, 4 signals of the I2S3 module, and 6 GPIO are routed to the 21 external signals of the parallel port. 111 = Reserved. |

Table 3-5. EBSR Register Bit Descriptions (continued)

| BITS | NAME | DESCRIPTION |
|-------|----------|--|
| 11:10 | SP1MODE | Serial Port 1 Mode Control Bits. The bits control the pin multiplexing of the MMC1, I2S1, and GPIO pins on serial port 1. For more details, see Table 3-7, MMC1, I2S1, and GP[11:6] Pin Multiplexing . 00 = Mode 0 (MMC/SD1). All 6 signals of the MMC/SD1 module are routed to the 6 external signals of the serial port 1. 01 = Mode 1 (I2S1 and GP[11:10]). 4 signals of the I2S1 module and 2 GP[11:10] signals are routed to the 6 external signals of the serial port 1. 10 = Mode 2 (GP[11:6]). 6 GPIO signals (GP[11:6]) are routed to the 6 external signals of the serial port 1. 11 = Reserved. |
| 9:8 | SP0MODE | Serial Port 0 Mode Control Bits. The bits control the pin multiplexing of the MMC0, I2S0, and GPIO pins on serial port 0. For more details, see Section 3.7.1.3, MMC0, I2S0, and GP[5:0] Pin Multiplexing . 00 = Mode 0 (MMC/SD0). All 6 signals of the MMC/SD0 module are routed to the 6 external signals of the serial port 0. 01 = Mode 1 (I2S0 and GP[5:0]). 4 signals of the I2S0 module and 2 GP[5:4] signals are routed to the 6 external signals of the serial port 0. 10 = Mode 2 (GP[5:0]). 6 GPIO signals (GP[5:0]) are routed to the 6 external signals of the serial port 0. 11 = Reserved. |
| 7 | RESERVED | Reserved. Read-only, writes have no effect. |
| 6 | RESERVED | Reserved. Read-only, writes have no effect. |
| 5 | A20_MODE | A20 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 20 (EM_A[20]) and general-purpose input/output pin 26 (GP[26]) pin functions. 0 = Pin function is EMIF address pin 20 (EM_A[20]). 1 = Pin function is general-purpose input/output pin 26 (GP[26]). |
| 4 | A19_MODE | A19 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 19 (EM_A[19]) and general-purpose input/output pin 25 (GP[25]) pin functions. 0 = Pin function is EMIF address pin 19 (EM_A[19]). 1 = Pin function is general-purpose input/output pin 25 (GP[25]). |
| 3 | A18_MODE | A18 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 18 (EM_A[18]) and general-purpose input/output pin 24 (GP[24]) pin functions. 0 = Pin function is EMIF address pin 18 (EM_A[18]). 1 = Pin function is general-purpose input/output pin 24 (GP[24]). |
| 2 | A17_MODE | A17 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 17 (EM_A[17]) and general-purpose input/output pin 23 (GP[23]) pin functions. For more details, see Table 3-8, EM_A[20:16] and GP[26:21] Pin Multiplexing . 0 = Pin function is EMIF address pin 17 (EM_A[17]). 1 = Pin function is general-purpose input/output pin 23 (GP[23]). |
| 1 | A16_MODE | A16 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 16 (EM_A[16]) and general-purpose input/output pin 22 (GP[22]) pin functions. For more details, see Table 3-8, EM_A[20:16] and GP[26:21] Pin Multiplexing . 0 = Pin function is EMIF address pin 16 (EM_A[16]). 1 = Pin function is general-purpose input/output pin 22 (GP[22]). |
| 0 | A15_MODE | A15 Pin Mode Bit. This bit controls the pin multiplexing of the EMIF address 15 (EM_A[15]) and general-purpose input/output pin 21 (GP[21]) pin functions. For more details, see Table 3-8, EM_A[20:16] and GP[26:21] Pin Multiplexing . 0 = Pin function is EMIF address pin 15 (EM_A[15]). 1 = Pin function is general-purpose input/output pin 21 (GP[21]). |

3.6.2 LDO Control Register [7004h]

When the DSP_LDO is enabled by the $\overline{\text{DSP_LDO_EN}}$ pin [D12], by default, the DSP_LDOO voltage is set to 1.3 V. The DSP_LDOO voltage can be programmed to be either 1.05 V or 1.3 V via the DSP_LDO_V bit (bit 1) in the LDO Control Register (LDOCNTL).

At reset, the USB_LDO is turned off. The USB_LDO can be enabled via the USBLDOEN bit (bit 0) in the LDOCNTL register.

For more detailed information on the LDOs, see [Section 3.2.1 LDO Configuration](#).

3.6.3 EMIF and USB System Control Registers (ESCR and USBSCR) [1C33h and 1C32h]

After reset, by default, the CPU performs 16-bit accesses to the EMIF and USB registers and data space. To perform 8-bit accesses to the EMIF data space, the user must set the BYTEMODE bits to 01b for the "high byte" or 10b for the "low byte" in the EMIF System Control Register (ESCR). Similarly, the BYTEMODE bits in the USB System Control Register (USBSCR) must also be configured for byte access.

3.6.4 Peripheral Clock Gating Control Registers (PCGCR1 and PCGCR2) [1C02h and 1C03h]

After hardware reset, the DSP executes the on-chip bootloader from ROM. As the bootloader executes, it selectively enables the clock of the peripheral being queried for a valid boot. If a valid boot source is not found, the bootloader disables the clock to that peripheral and moves on to the next peripheral in the boot order. After the boot process is complete, all of the peripheral clocks will be off and all domains in the ICR, except for the CPU domain, will be idled (this includes the MPORT and HWA). The user must enable the clocks to the peripherals and CPU ports that are going to be used. The peripheral clock gating control registers (PCGCR1 and PCGCR2) are used to enable and disable the peripheral clocks.

3.6.5 Pullup/Pulldown Inhibit Registers (PDINHIBR1/2/3) [1C17h, 1C18h, and 1C19h, respectively]

Each internal pullup and pulldown (IPU/IPD) resistor on the device DSP, except for the IPD on $\overline{\text{TRST}}$, can be individually controlled through the IPU/IPD registers (PDINHIBR1 [1C17h], PDINHIBR2 [1C18h], and PDINHIBR3 [1C19h]). To minimize power consumption, internal pullup or pulldown resistors should be disabled in the presence of an external pullup or pulldown resistor or external driver. [Section 3.8.1, Pullup/Pulldown Resistors](#), describes other situations in which an pullup and pulldown resistors are required.

When CV_{DD} is powered down, pullup and pulldown resistors will be forced disabled and an internal bus-holder will be enabled. For more detailed information, see [Section 5.3.2, Digital I/O Behavior When Core Power \(\$\text{CV}_{\text{DD}}\$ \) is Down](#).

3.6.6 Output Slew Rate Control Register (OSRCR) [1C16h]

To provide the lowest power consumption setting, the DSP has configurable slew rate control on the EMIF and CLKOUT output pins. The output slew rate control register (OSRCR) is used to set a subset of the device I/O pins, namely CLKOUT and EMIF pins, to either fast or slow slew rate. The slew rate feature is implemented by staging/delaying turn-on times of the parallel p-channel drive transistors and parallel n-channel drive transistors of the output buffer. In the slow slew rate configuration, the delay is longer, but ultimately the same number of parallel transistors are used to drive the output high or low. Thus, the drive strength is ultimately the same. The slower slew rate control can be used for power savings and has the greatest effect at lower DV_{DDIO} and $\text{DV}_{\text{DDEMIF}}$ voltages.

3.7 Multiplexed Pin Configurations

The device DSP uses pin multiplexing to accommodate a larger number of peripheral functions in the smallest possible package, providing the ultimate flexibility for end applications. The external bus selection register (EBSR) controls all the pin multiplexing functions on the device.

3.7.1 Pin Multiplexing Details

This section discusses how to program the external bus selection register (EBSR) to select the desired peripheral functions and pin muxing. See the individual pin mux sections for pin muxing details for a specific muxed pin. After changing any of the pin mux control registers, it will be necessary to reset the peripherals that are affected.

3.7.1.1 LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing [EBSR.PPMODE Bits]

The LCD Controller, SPI, UART, I2S2, I2S3, and GPIO signal muxing is determined by the value of the PPMODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see [Table 3-6](#).

Table 3-6. LCD Controller, SPI, UART, I2S2, I2S3, and GP[31:27, 20:18] Pin Multiplexing

| PDINHIBR3 REGISTER BIT FIELDS ⁽¹⁾ | PIN NAME | EBSR PPMODE BITS | | | | | | |
|---|------------------------------------|------------------------|----------|------------|------------|------------|------------|----------|
| | | MODE 0 | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 |
| | | 000 (Reset Default) | 001 | 010 | 011 | 100 | 101 | 110 |
| | LCD_EN_RDB/SPI_CLK | LCD_EN_RDB | SPI_CLK | LCD_EN_RDB | LCD_EN_RDB | LCD_EN_RDB | LCD_EN_RDB | SPI_CLK |
| | LCD_D[0]/SPI_RX | LCD_D[0] | SPI_RX | LCD_D[0] | LCD_D[0] | LCD_D[0] | LCD_D[0] | SPI_RX |
| | LCD_D[1]/SPI_TX | LCD_D[1] | SPI_TX | LCD_D[1] | LCD_D[1] | LCD_D[1] | LCD_D[1] | SPI_TX |
| P2PD | LCD_D[2]/GP[12] | LCD_D[2] | GP[12] | LCD_D[2] | LCD_D[2] | LCD_D[2] | LCD_D[2] | GP[12] |
| P3PD | LCD_D[3]/GP[13] | LCD_D[3] | GP[13] | LCD_D[3] | LCD_D[3] | LCD_D[3] | LCD_D[3] | GP[13] |
| P4PD | LCD_D[4]/GP[14] | LCD_D[4] | GP[14] | LCD_D[4] | LCD_D[4] | LCD_D[4] | LCD_D[4] | GP[14] |
| P5PD | LCD_D[5]/GP[15] | LCD_D[5] | GP[15] | LCD_D[5] | LCD_D[5] | LCD_D[5] | LCD_D[5] | GP[15] |
| P6PD | LCD_D[6]/GP[16] | LCD_D[6] | GP[16] | LCD_D[6] | LCD_D[6] | LCD_D[6] | LCD_D[6] | GP[16] |
| P7PD | LCD_D[7]/GP[17] | LCD_D[7] | GP[17] | LCD_D[7] | LCD_D[7] | LCD_D[7] | LCD_D[7] | GP[17] |
| P8PD | LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK | LCD_D[8] | I2S2_CLK | GP[18] | SPI_CLK | I2S2_CLK | SPI_CLK | I2S2_CLK |
| P9PD | LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0 | LCD_D[9] | I2S2_FS | GP[19] | SPI_CS0 | I2S2_FS | SPI_CS0 | I2S2_FS |
| P10PD | LCD_D[10]/I2S2_RX/GP[20]/SPI_RX | LCD_D[10] | I2S2_RX | GP[20] | SPI_RX | I2S2_RX | SPI_RX | I2S2_RX |
| P11PD | LCD_D[11]/I2S2_DX/GP[27]/SPI_TX | LCD_D[11] | I2S2_DX | GP[27] | SPI_TX | I2S2_DX | SPI_TX | I2S2_DX |
| P12PD | LCD_D[12]/UART_RTS/GP[28]/I2S3_CLK | LCD_D[12] | UART_RTS | GP[28] | I2S3_CLK | UART_RTS | UART_RTS | I2S3_CLK |
| P13PD | LCD_D[13]/UART_CTS/GP[29]/I2S3_FS | LCD_D[13] | UART_CTS | GP[29] | I2S3_FS | UART_CTS | UART_CTS | I2S3_FS |
| P14PD | LCD_D[14]/UART_RXD/GP[30]/I2S3_RX | LCD_D[14] | UART_RXD | GP[30] | I2S3_RX | UART_RXD | UART_RXD | I2S3_RX |
| P15PD | LCD_D[15]/UART_TXD/GP[31]/I2S3_DX | LCD_D[15] | UART_TXD | GP[31] | I2S3_DX | UART_TXD | UART_TXD | I2S3_DX |
| | LCD_CS0_E0/SPI_CS0 | LCD_CS0_E0 | SPI_CS0 | LCD_CS0_E0 | LCD_CS0_E0 | LCD_CS0_E0 | LCD_CS0_E0 | SPI_CS0 |
| | LCD_CS1_E1/SPI_CS1 | LCD_CS1_E1 | SPI_CS1 | LCD_CS1_E1 | LCD_CS1_E1 | LCD_CS1_E1 | LCD_CS1_E1 | SPI_CS1 |
| | LCD_RW_WRB/SPI_CS2 | LCD_RW_WRB | SPI_CS2 | LCD_RW_WRB | LCD_RW_WRB | LCD_RW_WRB | LCD_RW_WRB | SPI_CS2 |
| | LCD_RS/SPI_CS3 | LCD_RS | SPI_CS3 | LCD_RS | LCD_RS | LCD_RS | LCD_RS | SPI_CS3 |

(1) The pin names with PDINHIBR3 register bit field references can have the pulldown resistor enabled or disabled via this register.

3.7.1.2 MMC1, I2S1, and GP[11:6] Pin Multiplexing [EBSR.SP1MODE Bits]

The MMC1, I2S1, and GPIO signal muxing is determined by the value of the SP1MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see [Table 3-7](#).

Table 3-7. MMC1, I2S1, and GP[11:6] Pin Multiplexing

| PDINHIBR1 REGISTER BIT FIELDS ⁽¹⁾ | PIN NAME | EBSR SP1MODE BITS | | |
|--|-------------------------|-----------------------|----------|--------|
| | | MODE 0 | MODE 1 | MODE 2 |
| | | 00 (Reset Default) | 01 | 10 |
| S10PD | MMC1_CLK/I2S1_CLK/GP[6] | MMC1_CLK | I2S1_CLK | GP[6] |
| S11PD | MMC1_CMD/I2S1_FS/GP[7] | MMC1_CMD | I2S1_FS | GP[7] |
| S12PD | MMC1_D0/I2S1_DX/GP[8] | MMC1_D0 | I2S1_DX | GP[8] |
| S13PD | MMC1_D1/I2S1_RX/GP[9] | MMC1_D1 | I2S1_RX | GP[9] |
| S14PD | MMC1_D2/GP[10] | MMC1_D2 | GP[10] | GP[10] |
| S15PD | MMC1_D3/GP[11] | MMC1_D3 | GP[11] | GP[11] |

(1) The pin names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled via this register.

3.7.1.3 MMC0, I2S0, and GP[5:0] Pin Multiplexing [EBSR.SP0MODE Bits]

The MMC0, I2S0, and GPIO signal muxing is determined by the value of the SP0MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see [Table 3-8](#).

Table 3-8. MMC0, I2S0, and GP[5:0] Pin Multiplexing

| PDINHIBR1 REGISTER BIT FIELDS ⁽¹⁾ | PIN NAME | EBSR SP0MODE BITS | | |
|--|-------------------------|-----------------------|----------|--------|
| | | MODE 0 | MODE 1 | MODE 2 |
| | | 00 (Reset Default) | 01 | 10 |
| S00PD | MMC0_CLK/I2S0_CLK/GP[0] | MMC0_CLK | I2S0_CLK | GP[0] |
| S01PD | MMC0_CMD/I2S0_FS/GP[1] | MMC0_CMD | I2S0_FS | GP[1] |
| S02PD | MMC0_D0/I2S0_DX/GP[2] | MMC0_D0 | I2S0_DX | GP[2] |
| S03PD | MMC0_D1/I2S0_RX/GP[3] | MMC0_D1 | I2S0_RX | GP[3] |
| S04PD | MMC0_D2/GP[4] | MMC0_D2 | GP[4] | GP[4] |
| S05PD | MMC0_D3/GP[5] | MMC0_D3 | GP[5] | GP[5] |

(1) The pin names with PDINHIBR1 register bit field references can have the pulldown register enabled or disabled via this register.

3.7.1.4 EMIF EM_A[20:15] and GP[26:21] Pin Multiplexing [EBSR.Axx_MODE bits]

The EMIF Address and GPIO signal muxing is determined by the value of the A20_MODE, A19_MODE, A18_MODE, A17_MODE, A16_MODE, and A15_MODE bit fields in the External Bus Selection Register (EBSR) register. For more details on the actual pin functions, see [Table 3-9](#).

Table 3-9. EM_A[20:16] and GP[26:21] Pin Multiplexing

| PIN NAME | Axx_MODE BIT | |
|-----------------|--------------|--------|
| | 0 | 1 |
| EM_A[15]/GP[21] | EM_A[15] | GP[21] |
| EM_A[16]/GP[22] | EM_A[16] | GP[22] |
| EM_A[17]/GP[23] | EM_A[17] | GP[23] |
| EM_A[18]/GP[24] | EM_A[18] | GP[24] |
| EM_A[19]/GP[25] | EM_A[19] | GP[25] |
| EM_A[20]/GP[26] | EM_A[20] | GP[26] |

3.8 Debugging Considerations

3.8.1 Pullup/Pulldown Resistors

Proper board design should ensure that input pins to the device DSP always be at a valid logic level and not floating. This may be achieved via pullup/pulldown resistors. The DSP features internal pullup (IPU) and internal pulldown (IPD) resistors on many pins, including all GPIO pins, to eliminate the need, unless otherwise noted, for external pullup/pulldown resistors.

An external pullup/pulldown resistor may need to be used in the following situations:

- **Configuration Pins:** An external pullup/pulldown resistor is recommended to set the desired value/state (see the configuration pins listed in [Table 3-4, Default Functions Affected by Device Configuration Pins](#)). Note that some configuration pins must be connected directly to ground or to a specific supply voltage.
- **Other Input Pins:** If the IPU/IPD does not match the desired value/state, use an external pullup/pulldown resistor to pull the signal to the opposite rail.

For the configuration pins (listed in [Table 3-4, Default Functions Affected by Device Configuration Pins](#)), if they are both routed out and in a high-impedance state (not driven), it is strongly recommended that an external pullup/pulldown resistor be implemented. In addition, applying external pullup/pulldown resistors on the configuration pins adds convenience to the user in debugging and flexibility in switching operating modes.

When an external pullup or pulldown resistor is used on a pin, the pin's internal pullup or pulldown resistor should be disabled through the Pullup/Pulldown Inhibit Registers (PDINHIBR1/2/3) [1C17h, 1C18h, and 1C19h, respectively] to minimize power consumption.

Tips for choosing an external pullup/pulldown resistor:

- Consider the total amount of current that may pass through the pullup or pulldown resistor. Make sure to include the leakage currents of all the devices connected to the net, as well as any internal pullup or pulldown (IPU/IPD) resistors.
- Decide a target value for the net. For a pulldown resistor, this should be below the lowest V_{IL} level of all inputs connected to the net. For a pullup resistor, this should be above the highest V_{IH} level of all inputs on the net. A reasonable choice would be to target the V_{OL} or V_{OH} levels for the logic family of the limiting device; which, by definition, have margin to the V_{IL} and V_{IH} levels.
- Select a pullup/pulldown resistor with the largest possible value; but, which can still ensure that the net will reach the target pulled value when maximum current from all devices on the net is flowing through the resistor. The current to be considered includes leakage current plus, any other internal and external pullup/pulldown resistors on the net.
- For bidirectional nets, there is an additional consideration which sets a lower limit on the resistance value of the external resistor. Verify that the resistance is small enough that the weakest output buffer can drive the net to the opposite logic level (including margin).
- Remember to include tolerances when selecting the resistor value.
- For pullup resistors, also remember to include tolerances on the DV_{DD} rail.

For most systems, a 1-k Ω resistor can be used to oppose the IPU/IPD while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For most systems, a 20-k Ω resistor can be used to compliment the IPU/IPD on the configuration pins while meeting the above criteria. Users should confirm this resistor value is correct for their specific application.

For more detailed information on input current (I_I), and the low-/high-level input voltages (V_{IL} and V_{IH}) for the device DSP, see [Section 4.3, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature](#).

For the internal pullup/pulldown resistors for all device pins, see the peripheral/system-specific terminal functions table in [Section 2.5](#).

3.8.2 Bus Holders

The device has special I/O bus-holder structures to ensure pins are not left floating when CV_{DD} power is removed while I/O power is applied. When CV_{DD} is "ON", the bus-holders are disabled and the internal pullups or pulldowns, if applicable, function normally. But when CV_{DD} is "OFF" and the I/O supply is "ON", the bus-holders become enabled and any applicable internal pullups and pulldowns are disabled.

The bus-holders are weak drivers on the pin and, for as long as CV_{DD} is "OFF" and I/O power is "ON", they hold the last state on the pin. If an external device is strongly driving the device I/O pin to the opposite state then the bus-holder will flip state to match the external driver and DC current will stop.

This bus-holder feature prevents unnecessary power consumption when CV_{DD} is "OFF" and I/O supply is "ON". For example, current caused by undriven pins (input buffer oscillation) and/or DC current flowing through pullups or pulldowns.

If external pullup or pulldown resistors are implemented, then care should be taken that those pullup/pulldown resistors can exceed the internal bus-holder's max current and thereby cause the bus-holder to flip state to match the state of the external pullup or pulldown. Otherwise, DC current will flow unnecessarily. When CV_{DD} power is applied, the bus holders are disabled (for further details on bus holders, see [Section 5.3.2, Digital I/O Behavior When Core Power \(\$CV_{DD}\$ \) is Down](#)).

3.8.3 CLKOUT Pin

For debug purposes, the DSP includes a CLKOUT pin which can be used to tap different clocks within the clock generator. The SRC bits of the CLKOUT Control Source Register (CCSSR) can be used to specify the source for the CLKOUT pin.

Note: The bootloader disables the CLKOUT pin via CLKOFF bit in the ST3_55 CPU register.

For more information on the ST3_55 CPU register, see the *TMS320C55x 3.0 CPU Reference Guide* (literature number: [SWPU073](#)).

4 Device Operating Conditions

For the device maximum operating frequency, see [Section 6.1.2, Device and Development-Support Tool Nomenclature](#).

4.1 Absolute Maximum Ratings Over Operating Case Temperature Range (Unless Otherwise Noted)⁽¹⁾

| | | |
|--|--|---|
| Supply voltage ranges: | Digital Core (CV _{DD} , CV _{DDRTC} , USB_V _{DD1P3}) ⁽²⁾ | –0.5 V to 1.7 V |
| | I/O, 1.8 V, 2.5 V, 2.75 V, 3.3 V (DV _{DDIO} , DV _{DDEMI} , DV _{DDRTC}) 3.3V USB supplies USB PHY (USB_V _{DDOSC} , USB_V _{DDPLL} , USB_V _{DDA3P3}) ⁽²⁾ | –0.5 V to 4.2 V |
| | LDO1 | –0.5 V to 4.2 V |
| | Analog, 1.3 V (V _{DDA_PLL} , USB_V _{DDA1P3} , V _{DDA_ANA}) ⁽²⁾ | –0.5 V to 1.7 V |
| Input and Output voltage ranges: | V _I I/O, All pins with DV _{DDIO} or DV _{DDEMI} or USB_V _{DDOSC} or USB_V _{DDPLL} or USB_V _{DDA3P3} as supply source | –0.5 V to 4.2 V |
| | V _O I/O, All pins with DV _{DDIO} or DV _{DDEMI} or USB_V _{DDOSC} or USB_V _{DDPLL} or USB_V _{DDA3P3} as supply source | –0.5 V to 4.2 V |
| | RTC_XI and RTC_XO | –0.5 V to 1.7 V |
| | USB_V _{BUS} Input | –0.5 V to 5.5 V |
| | V _I and V _O , GPAIN[0] | –0.5 V to 4.2 V |
| | V _I and V _O , GPAIN[3:1] | –0.5 V to 1.7 V |
| | V _O , BG_CAP | –0.5 V to 1.7 V |
| | ANA_LDOO, DSP_LDOO, and USB_LDOO | –0.5 V to 1.7 V |
| Operating case temperature ranges, T _C : | Commercial Temperature (default) | –10°C to 70°C |
| | Industrial Temperature | –40°C to 85°C |
| Storage temperature range, T _{stg} | (default) | –65°C to 150°C |
| Device Operating Life Power-On Hours (POH) ⁽³⁾ | DSP Operating Frequency (SYSCLK) ≤100 MHz | <70 °C ≥70 °C - ≤85 °C |
| | DSP Operating Frequency (SYSCLK): >100 MHz - ≤120 MHz | <70 °C ≥70 °C - ≤85 °C |
| | | 100,000 POH 100,000 POH 100,000 POH 80,000 POH |
| | | |
| ESD Stress Voltage ⁽⁴⁾ | Human Body Model (HBM) ⁽⁵⁾ | > 1000 V |
| | Charged Device Model (CDM) ⁽⁶⁾ | > 250 V |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to V_{SS}.
- (3) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
- (4) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
- (5) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001-2010. JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500 V HBM is possible if necessary precautions are taken. Pins listed as 1000 V may actually have higher performance.
- (6) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.

4.2 Recommended Operating Conditions

| | | | | MIN | NOM | MAX | UNIT |
|--------------------------------|--|---|----------------------|------------------------|------|----------------------------|------|
| Core Supplies | CV _{DD} | Supply voltage, Digital Core | 60 or 75 MHz | 0.998 | 1.05 | 1.15 | V |
| | | | 100 or 120 MHz | 1.24 | 1.3 | 1.43 | V |
| | CV _{DDRTC} | Supply voltage, RTC and RTC OSC | 32.768 KHz | 0.998 | | 1.43 | V |
| | USB_V _{DD1P3} | Supply voltage, Digital USB | | 1.24 | 1.3 | 1.43 | V |
| | USB_V _{DDA1P3} | Supply voltage, 1.3 V Analog USB | | 1.24 | 1.3 | 1.43 | V |
| | V _{DDA_ANA} | Supply voltage, 1.3 V SAR and Pwr Mgmt | | 1.24 | 1.3 | 1.43 | V |
| | V _{DDA_PLL} | Supply voltage, System PLL | | 1.24 | 1.3 | 1.43 | V |
| I/O Supplies | DV _{DDIO} DV _{DDMIF} DV _{DDRTC} | Supply voltage, I/O, 3.3 V | | 2.97 | 3.3 | 3.63 | V |
| | | Supply voltage, I/O, 2.75 V | | 2.48 | 2.75 | 3.02 | V |
| | | Supply voltage, I/O, 2.5 V | | 2.25 | 2.5 | 2.75 | V |
| | | Supply voltage, I/O, 1.8 V | | 1.65 | 1.8 | 1.98 | V |
| | USB_V _{DDOSC} | Supply voltage, I/O, 3.3 V USB OSC | | 2.97 | 3.3 | 3.63 | V |
| | USB_V _{DDA3P3} | Supply voltage, I/O, 3.3 V Analog USB PHY | | 2.97 | 3.3 | 3.63 | V |
| | LDO1 | Supply voltage, Analog Pwr Mgmt and LDO Inputs | | 1.8 | | 3.6 | V |
| | | | | | | | |
| GND | V _{SS} | Supply ground, Digital I/O | | | | | |
| | V _{SSRTC} | Supply ground, RTC | | | | | |
| | USB_V _{SSOSC} | Supply ground, USB OSC | | | | | |
| | USB_V _{SSPLL} | Supply ground, USB PLL | | | | | |
| | USB_V _{SSA3P3} | Supply ground, 3.3 V Analog USB PHY | | 0 | 0 | 0 | V |
| | USB_V _{SSA1P3} | Supply ground, USB 1.3 V Analog USB PHY | | | | | |
| | USB_V _{SSREF} | Supply ground, USB Reference Current | | | | | |
| | V _{SSA_PLL} | Supply ground, System PLL | | | | | |
| | USB_V _{SS1P3} | Supply ground, 1.3 V Digital USB PHY | | | | | |
| | V _{SSA_ANA} | Supply ground, SAR and Pwr Mgmt | | | | | |
| V _{IH} ⁽¹⁾ | | High-level input voltage, 3.3, 2.75, 2.5, 1.8 V I/O (except GPAIN[3:0] pins) ⁽²⁾ | | 0.7 * DV _{DD} | | DV _{DD} + 0.3 | V |
| V _{IL} ⁽¹⁾ | | Low-level input voltage, 3.3, 2.75, 2.5, 1.8 V I/O (except GPAIN[3:0] pins) ⁽²⁾ | | -0.3 | | 0.3 * DV _{DD} | V |
| V _{IN} | | Input voltage, GPAIN0 pin ⁽³⁾ | | -0.3 | | 3.6 | V |
| | | Input voltage, GPAIN[3:1] pins | | -0.3 | | V _{DDA_ANA} + 0.3 | V |
| T _c | | Operating case temperature | Default (Commercial) | -10 | | 70 | °C |
| | | | (Industrial) | -40 | | 85 | °C |
| F _{SYSCLK} | | DSP Operating Frequency (SYSCLK) | 1.05 V | 0 | | 60 or 75 ⁽⁴⁾ | MHz |
| | | | 1.3 V | 0 | | 100 or 120 ⁽⁴⁾ | MHz |

(1) DV_{DD} refers to the pin I/O supply voltage. To determine the I/O supply voltage for each pin, see [Section 2.5, Terminal Functions](#).

(2) The I2C pin SDA and SCL do not feature fail-safe I/O buffers. These pin could potentially draw current when the DV_{DDIO} is powered down. Due to the fact that different voltage devices can be connected to I2C bus and the I2C inputs are LVCMOS, the level of logic 0 (low) and logic 1 (high) are not fixed and depend on DV_{DDIO}.

(3) The GNDON bit in the SARPINCTRL register should be set to "1" before SAR channels 0, 1, or 2 are enabled via the CHSEL bit in the SARCTRL register, when V_{IN} greater than V_{DDA_ANA}.

(4) For the device maximum operating frequency, see [Section 6.1.2, Device and Development-Support Tool Nomenclature](#).

4.3 Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature (Unless Otherwise Noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|---|---|--|----------------------------|-------------------------|----------------------------|------|
| V _{OH} | Full speed: USB_DN and USB_DP ⁽²⁾ | | 2.8 | USB_V _{DDA3P3} | | V |
| | High speed: USB_DN and USB_DP ⁽²⁾ | | 360 | | 440 | mV |
| | High-level output voltage, 3.3, 2.75, 2.5, 1.8 V I/O (except GPAIN[3:0] pins) | IO = I _{OH} | 0.8 * DV _{DD} | | | V |
| | High-level output voltage, GPAIN[3:1] pins | IO = I _{OH} | 0.8 * V _{DDA_ANA} | | | V |
| V _{OL} | Full speed: USB_DN and USB_DP ⁽²⁾ | | 0.0 | | 0.3 | V |
| | High speed: USB_DN and USB_DP ⁽²⁾ | | –10 | | 10 | mV |
| | Low-level output voltage, 3.3, 2.75, 2.5, 1.8V I/O (except I2C and GPAIN[3:0] pins) | IO = I _{OL} | | | 0.2 * DV _{DD} | V |
| | Low-level output voltage, I2C pins ⁽³⁾ | V _{DD} > 2 V, I _{OL} = 3 mA | 0 | | 0.4 | V |
| | Low-level output voltage, GPAIN[3:0] pins | IO = I _{OL} | | | 0.2 * V _{DDA_ANA} | V |
| V _{HYS} | Input hysteresis ⁽⁴⁾ | DV _{DD} = 3.3 V | | 162 | | mV |
| | | DV _{DD} = 2.5 V | | 141 | | mV |
| | | DV _{DD} = 1.8 V | | 122 | | mV |
| V _{LDO} | USB_LDOO voltage | | 1.24 | 1.3 | 1.43 | V |
| | ANA_LDOO voltage | | 1.24 | 1.3 | 1.43 | V |
| | DSP_LDOO voltage | DSP_LDO_V bit in the LDOCNTL register = 1 | 1.24 | 1.3 | 1.43 | V |
| | | DSP_LDO_V bit in the LDOCNTL register = 0 | 0.998 | 1.05 | 1.15 | V |
| I _{SD} | DSP_LDO shutdown current ⁽⁵⁾ | LDOl = V _{MIN} | 250 | | | mA |
| | ANA_LDO shutdown current ⁽⁵⁾ | LDOl = V _{MIN} | 4 | | | mA |
| | USB_LDO shutdown current ⁽⁵⁾ | LDOl = V _{MIN} | 25 | | | mA |
| I _{ILPU} ⁽⁶⁾⁽⁷⁾ | Input current [DC] (except WAKEUP, I2C, and GPAIN[3:0] pins) | Input only pin, internal pulldown or pullup disabled | –5 | | +5 | μA |
| | | DV _{DD} = 3.3 V with internal pullup enabled ⁽⁸⁾ | | –59 to –161 | | μA |
| | | DV _{DD} = 2.5 V with internal pullup enabled ⁽⁸⁾ | | –31 to –93 | | μA |
| | | DV _{DD} = 1.8 V with internal pullup enabled ⁽⁸⁾ | | –14 to –44 | | μA |
| I _{IHPD} ⁽⁶⁾⁽⁷⁾ | Input current [DC] (except WAKEUP, I2C, and GPAIN[3:0] pins) | Input only pin, internal pulldown or pullup disabled | –5 | | +5 | μA |
| | | DV _{DD} = 3.3 V with internal pulldown enabled ⁽⁸⁾ | | 52 to 158 | | μA |
| | | DV _{DD} = 2.5 V with internal pulldown enabled ⁽⁸⁾ | | 27 to 83 | | μA |
| | | DV _{DD} = 1.8 V with internal pulldown enabled ⁽⁸⁾ | | 11 to 35 | | μA |
| I _{IH} / I _{IL} ⁽⁷⁾ | Input current [DC], ALL pins | V _I = V _{SS} to DV _{DD} with internal pullups and pulldowns disabled. | –5 | | +5 | μA |

(1) For test conditions shown as MIN, MAX, or TYP, use the appropriate value specified in the recommended operating conditions table.

(2) The USB I/Os adhere to the Universal Bus Specification Revision 2.0 (USB2.0 spec).

(3) V_{DD} is the voltage to which the I2C bus pullup resistors are connected.

(4) Applies to all input pins except WAKEUP, I2C pins, GPAIN[3:0], RTC_XI, and USB_MXI.

(5) I_{SD} is the amount of current the LDO is ensured to deliver before shutting down to protect itself.

(6) I_I applies to input-only pins and bi-directional pins. For input-only pins, I_I indicates the input leakage current. For bi-directional pins, I_I indicates the input leakage current and off-state (Hi-Z) output leakage current.

(7) When CV_{DD} power is "ON", the pin bus-holders are disabled. For more detailed information, see [Section 5.3.2, Digital I/O Behavior When Core Power \(CV_{DD}\) is Down](#).

(8) Applies only to pins with an internal pullup (IPU) or pulldown (IPD) resistor.

**Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature
(Unless Otherwise Noted) (continued)**

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP | MAX | UNIT |
|-------------------|--|--|---|-------|-----|------|------|
| $I_{OH}^{(7)}$ | High-level output current [DC] | All Pins (except USB, EMIF, CLKOUT, and GPAIN[3:0] pins) | | -4 | | | mA |
| | | EMIF pins | $DV_{DD} = 3.3\text{ V}$ | -6 | | | mA |
| | | | $DV_{DD} = 1.8\text{ V}$ | -5 | | | mA |
| | | CLKOUT pin | $DV_{DD} = 3.3\text{ V}$ | -6 | | | mA |
| | | | $DV_{DD} = 1.8\text{ V}$ | -4 | | | mA |
| | | GPAIN[3:1] pins | $DV_{DD} = V_{DDA_ANA} = 1.3\text{ V}$, External Regulator ⁽⁹⁾ | -4 | | | mA |
| $I_{OL}^{(7)}$ | Low-level output current [DC] | (GPAIN0 is open-drain and cannot drive high) | | -100 | | | μA |
| | | All Pins (except USB, EMIF, CLKOUT, and GPAIN[3:0] pins) | | | | +4 | mA |
| | | EMIF pins | $DV_{DD} = 3.3\text{ V}$ | | | +6 | mA |
| | | | $DV_{DD} = 1.8\text{ V}$ | | | +5 | mA |
| | | CLKOUT pin | $DV_{DD} = 3.3\text{ V}$ | | | +6 | mA |
| | | | $DV_{DD} = 1.8\text{ V}$ | | | +4 | mA |
| $I_{OZ}^{(10)}$ | I/O Off-state output current | All Pins (except USB and GPAIN[3:0]) | | -10 | | +10 | μA |
| | | GPAIN[3:0] pins | | -10 | | +10 | μA |
| $I_{OLBH}^{(11)}$ | Bus Holder pull low current when CV_{DD} is powered "OFF" | Supply voltage, I/O, 3.3 V | | | | 2.2 | mA |
| | | Supply voltage, I/O, 2.75 V | | | | 1.6 | mA |
| | | Supply voltage, I/O, 2.5 V | | | | 1.4 | mA |
| | | Supply voltage, I/O, 1.8 V | | | | 0.72 | mA |
| $I_{OHBH}^{(11)}$ | Bus Holder pull high current when CV_{DD} is powered "OFF" | Supply voltage, I/O, 3.3 V | | -1.3 | | | mA |
| | | Supply voltage, I/O, 2.75 V | | -0.97 | | | mA |
| | | Supply voltage, I/O, 2.5 V | | -0.83 | | | mA |
| | | Supply voltage, I/O, 1.8 V | | -0.46 | | | mA |

(9) When the ANA_LDO supplies V_{DDA_ANA} , it is not recommended to use the GPAIN[3:1] signals for general-purpose outputs (driving high). The I_{SD} parameter of the ANA_LDO is too low to drive any realistic load on the GPAIN[3:1] pins while also supplying the PLL through V_{DDA_PLL} and the SAR through V_{DDA_ANA} .

(10) I_{OZ} applies to output-only pins, indicating off-state (Hi-Z) output leakage current.

(11) This parameter specifies the maximum strength of the Bus Holder and is needed to calculate the minimum strength of external pull-ups and pull-downs.

**Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature
(Unless Otherwise Noted) (continued)**

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|----------------|---|---|-----|------|-----|--------|
| P | Core (CV _{DD}) supply power ⁽¹²⁾ | Active, CV _{DD} = 1.3 V, DSP clock = 100 or 120 MHz, Clock source = RTC on-chip Oscillator Room Temp (25 °C), 75% DMAC + 25% ADD (typical sine wave data switching) | | 0.22 | | mW/MHz |
| | | Active, CV _{DD} = 1.05 V, DSP clock = 60 or 75 MHz, Clock source = RTC on-chip Oscillator Room Temp (25 °C), 75% DMAC + 25% ADD (typical data switching) | | 0.15 | | mW/MHz |
| | | Active, CV _{DD} = 1.3 V, DSP clock = 100 or 120 MHz, Clock source = RTC on-chip Oscillator Room Temp (25 °C), 75% DMAC + 25% NOP (typical sine wave data switching) | | 0.22 | | mW/MHz |
| | | Active, CV _{DD} = 1.05 V, DSP clock = 60 or 75 MHz, Clock source = RTC on-chip Oscillator Room Temp (25 °C), 75% DMAC + 25% NOP (typical data switching) | | 0.14 | | mW/MHz |
| | | Standby, CV _{DD} = 1.3 V, Master clock disabled, Clock source = RTC on-chip Oscillator Room Temp (25 °C), DARAM and SARAM in active mode | | 0.44 | | mW |
| | | Standby, CV _{DD} = 1.05 V, Master clock disabled, Clock source = RTC on-chip Oscillator Room Temp (25 °C), DARAM and SARAM in active mode | | 0.26 | | mW |
| | | Standby, CV _{DD} = 1.3 V, Master clock disabled, Clock source = RTC on-chip Oscillator Room Temp (25 °C), DARAM in retention and SARAM in active mode | | 0.40 | | mW |
| | | Standby, CV _{DD} = 1.05 V, Master clock disabled, Clock source = RTC on-chip Oscillator Room Temp (25 °C), DARAM in retention and SARAM in active mode | | 0.23 | | mW |
| | | Standby, CV _{DD} = 1.3 V, Master clock disabled, Clock source = RTC on-chip Oscillator Room Temp (25 °C), DARAM in active mode and SARAM in retention | | 0.28 | | mW |
| | | Standby, CV _{DD} = 1.05 V, Master clock disabled, Clock source = RTC on-chip Oscillator Room Temp (25 °C), DARAM in active mode and SARAM in retention | | 0.15 | | mW |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| I | Analog PLL (V _{DDA_PLL}) supply current | V _{DDA_PLL} = 1.3 V Room Temp (25 °C), Phase detector = 170 kHz, VCO = 120 MHz | | 0.7 | | mA |
| | SAR Analog (V _{DDA_ANA}) supply current | V _{DDA_ANA} = 1.3 V, SAR clock = 2 MHz, Temp (70 °C) | | | 1 | mA |
| C _I | Input capacitance | | | | 4 | pF |
| C _O | Output capacitance | | | | 4 | pF |

(12) Measured under the following conditions:

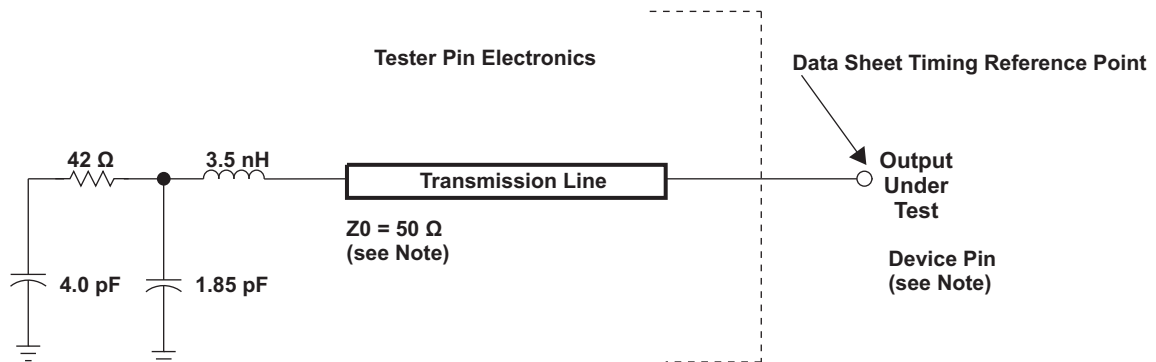
- At room temperature using units representative of a typical process.
- I/O pins are properly terminated.

The actual current draw varies across manufacturing processes and is highly application-dependent.

For more details on core and I/O activity, as well as information relevant to board power supply design, see *Estimating Power Consumption on the TMS320C5504/05/14/15/32/33/34/35 DSPs* (literature number [SPRABM0](#)).

5 Peripheral Information and Electrical Specifications

5.1 Parameter Information



NOTE: The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns) from the data sheet timings.

Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

Figure 5-1. 3.3-V Test Load Circuit for AC Timing Measurements

The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

5.1.1 1.8-V, 2.5-V, 2.75-V, and 3.3-V Signal Transition Levels

All rise and fall transition timing parameters are referenced to V_{IL} MAX and V_{IH} MIN for input clocks, V_{OL} MAX and V_{OH} MIN for output clocks.

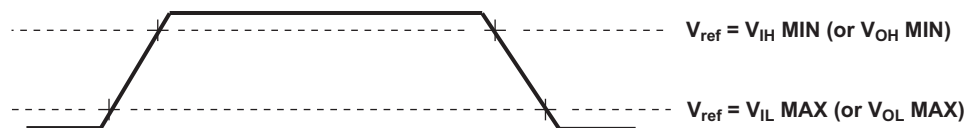


Figure 5-2. Rise and Fall Transition Time Voltage Reference Levels

5.1.2 3.3-V Signal Transition Rates

All timings are tested with an input edge rate of 4 volts per nanosecond (4 V/ns).

5.1.3 Timing Parameters and Board Routing Analysis

The timing parameter values specified in this data manual do *not* include delays by board routing. As a good board design practice, such delays must *always* be taken into account. Timing values may be adjusted by increasing/decreasing such delays. TI recommends utilizing the available I/O buffer information specification (IBIS) models to analyze the timing characteristics correctly. To properly use IBIS models to attain accurate timing analysis for a given system, see the *Using IBIS Models for Timing Analysis* application report (literature number [SPRA839](#)). If needed, external logic hardware such as buffers may be used to compensate any timing differences.

5.2 Recommended Clock and Control Signal Transition Behavior

All clocks and control signals **must** transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

5.3 Power Supplies

The device includes four core voltage-level supplies (CV_{DD} , CV_{DDRTC} , USB_V_{DD1P3} , USB_V_{DDA1P3}), and several I/O supplies (DV_{DDIO} , DV_{DDEMI} , DV_{DDRTC} , USB_V_{DDOSC} , and USB_V_{DDA3P3}), as well as several analog supplies ($LDO1$, V_{DDA_PLL} , V_{DDA_ANA} , and USB_V_{DDPLL}).

Note: CV_{DDRTC} must be externally powered. None of the on-chip LDOs can be used to power CV_{DDRTC} .

Some TI power-supply devices include features that facilitate power sequencing—for example, Auto-Track and Slow-Start/Enable features. For more information regarding TI's power management products and suggested devices to power TI DSPs, visit www.ti.com/processorpower.

5.3.1 Power-Supply Sequencing

The device includes four core voltage-level supplies (CV_{DD} , CV_{DDRTC} , USB_V_{DD1P3} , USB_V_{DDA1P3}), and several I/O supplies including DV_{DDIO} , DV_{DDEMI} , DV_{DDRTC} , USB_V_{DDOSC} , and USB_V_{DDA3P3} .

If the DSP_LDO is disabled ($\overline{DSP_LDO_EN} = \text{high}$) and an external regulator supplies power to the CPU Core (CV_{DD}), the external reset signal (\overline{RESET}) must be held asserted until all of the supply voltages reach their valid operating ranges.

Note: the external reset signal on the \overline{RESET} pin must be held low until all of the power supplies reach their operating voltage conditions.

The I/O design allows either the core supplies (CV_{DD} , CV_{DDRTC} , USB_V_{DD1P3} , USB_V_{DDA1P3}) or the I/O supplies (DV_{DDIO} , DV_{DDEMI} , DV_{DDRTC} , USB_V_{DDOSC} , and USB_V_{DDA3P3}) to be powered up for an indefinite period of time while the other supply is not powered if the following constraints are met:

1. All maximum ratings and recommended operating conditions are satisfied.
2. All warnings about exposure to maximum rated and recommended conditions, particularly junction temperature are satisfied. These apply to power transitions as well as normal operation.
3. Bus contention while core supplies are powered must be limited to 100 hours over the projected lifetime of the device.
4. Bus contention while core supplies are powered down does not violate the absolute maximum ratings.

If the USB subsystem is used, the subsystem must be powered up in the following sequence:

1. USB_V_{DDA1P3} and USB_V_{DD1P3}
2. USB_V_{DDA3P3}
3. USB_V_{BUS}

If the USB subsystem is not used, the following can be powered off:

- USB Core
 - USB_V_{DD1P3}
 - USB_V_{DDA1P3}
- USB PHY and I/O Level Supplies
 - USB_V_{DDOSC}
 - USB_V_{DDA3P3}
 - USB_V_{DDPLL}

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when the voltage is below that range, either stable or while in transition.

5.3.2 Digital I/O Behavior When Core Power (CV_{DD}) is Down

With some exceptions (listed below), all digital I/O pins on the device have special features to allow powering down of the Digital Core Domain (CV_{DD}) without causing I/O contentions or floating inputs at the pins (see [Figure 5-3](#)). The device asserts the internal signal called HHV high when power has been removed from the Digital Core Domain (CV_{DD}). Asserting the internal HHV signal causes the following conditions to occur in any order:

- All output pin strong drivers to go to the high-impedance (Hi-Z) state
- Weak bus holders to be enabled to hold the pin at a valid high or low
- The internal pullups or pulldowns (IPUs/IPDs) on the I/O pins will be disabled

The exception pins that **do not** have this special feature are:

- Pins driven by the CV_{DDRTC} Power Domain [This power domain is "Always On"; therefore, the pins driven by CV_{DDRTC} *do not* need these special features]:
 - RTC_XI, RTC_XO, RTC_CLKOUT, and WAKEUP
- USB Pins:
 - USB_DP, USB_DM, USB_R1, USB_VBUS, USB_MXI, and USB_MXO
- Pins for the Analog Block:
 - GPAIN[3:0], $\overline{DSP_LDO_EN}$, and BG_CAP

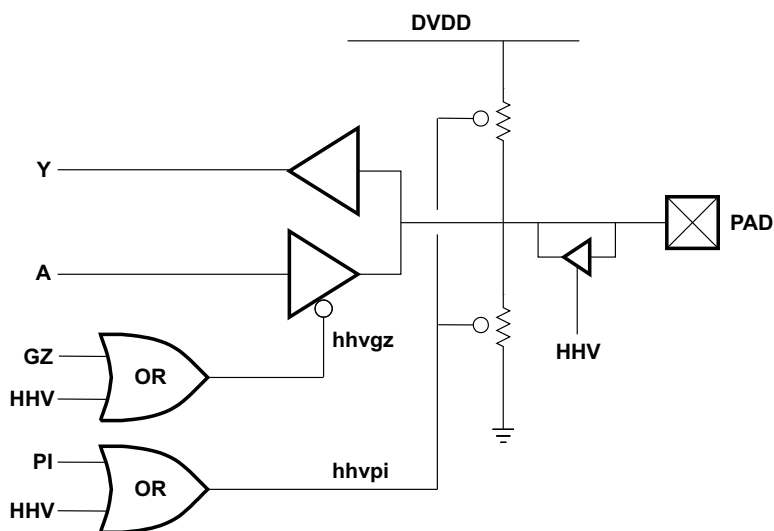


Figure 5-3. Bus Holder I/O Circuit

NOTE

[Figure 5-3](#) shows both a pullup and pulldown but pins only have one, not both.

PI = Pullup/Pulldown Inhibit

GZ = Output Enable (active low)

HHV = Described in [Section 5.3.2](#)

5.3.3 Power-Supply Design Considerations

Core and I/O supply voltage regulators should be located close to the DSP (or DSP array) to minimize inductance and resistance in the power delivery path. Additionally, when designing for high-performance applications utilizing the device, the PC board should include separate power planes for core, I/O, V_{DDA_ANA} and V_{DDA_PLL} (which can share the same PCB power plane), and ground; all bypassed with high-quality low-ESL/ESR capacitors.

5.3.4 Power-Supply Decoupling

In order to properly decouple the supply planes from system noise, place capacitors (caps) as close as possible to the device. These caps need to be no more than 1.25 cm maximum distance from the device power pins to be effective. Physically smaller caps, such as 0402, are better but need to be evaluated from a yield/manufacturing point-of-view. Parasitic inductance limits the effectiveness of the decoupling capacitors, therefore physically smaller capacitors should be used while maintaining the largest available capacitance value.

Larger caps for each supply can be placed further away for bulk decoupling. Large bulk caps (on the order of 10 μ F) should be furthest away, but still as close as possible. Large caps for each supply should be placed outside of the BGA footprint.

As with the selection of any component, verification of capacitor availability over the product's production lifetime should be considered.

The recommended decoupling capacitance for the DSP core supplies should be 1 μ F in parallel with 0.01- μ F capacitor per supply pin.

5.3.5 LDO Input Decoupling

The LDO inputs should follow the same decoupling guidelines as other power-supply pins above.

5.3.6 LDO Output Decoupling

The LDO circuits implement a voltage feedback control system which has been designed to optimize gain and stability tradeoffs. As such, there are design assumptions for the amount of capacitance on the LDO outputs. For proper device operation, the following external decoupling capacitors should be used when the on-chip LDOs are enabled:

- ANA_LDOO – 1 μ F
- DSP_LDOO – 5 μ F ~ 10 μ F
- USB_LDOO – 1 μ F ~ 2 μ F

5.4 External Clock Input From RTC_XI, CLKIN, and USB_MXI Pins

The device DSP includes two options to provide an external clock input to the system clock generator:

- Use the on-chip real-time clock (RTC) oscillator with an external 32.768-kHz crystal connected to the RTC_XI and RTC_XO pins.
- Use an external 11.2896-, 12.0-, or 12.288-MHz LVCMOS clock input fed into the CLKIN pin that operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.5-, 2.75-, or 3.3-V).

The CLK_SEL pin determines which input is used as the clock source for the system clock generator. For more details, see [Section 3.5.1, Device and Peripheral Configurations at Device Reset](#). The crystal for the RTC oscillator is not required if CLKIN is used as the system reference clock; however, the RTC must still be powered by an external power source. None of the on-chip LDOs can power CV_{DDRTC}. The RTC registers starting at I/O address 1900h will not be accessible without an RTC clock. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. [Section 5.4.1, Real-Time Clock \(RTC\) On-Chip Oscillator With External Crystal](#) provides more details on using the RTC on-chip oscillator with an external crystal. [Section 5.4.2, CLKIN Pin With LVCMOS-Compatible Clock Input](#) provides details on using an external LVCMOS-compatible clock input fed into the CLKIN pin.

Additionally, the USB requires a reference clock generated using a dedicated on-chip oscillator with a 12-MHz external crystal connected to the USB_MXI and USB_MXO pins. The USB reference clock is not required if the USB peripheral is not being used. [Section 5.4.3, USB On-Chip Oscillator With External Crystal](#) provides details on using the USB on-chip oscillator with an external crystal.

5.4.1 Real-Time Clock (RTC) On-Chip Oscillator With External Crystal

The on-chip oscillator requires an external 32.768-kHz crystal connected across the RTC_XI and RTC_XO pins, along with two load capacitors, as shown in [Figure 5-4](#). The external crystal load capacitors must be connected only to the RTC oscillator ground pin (V_{SSRTC}). **Do not** connect to board ground (V_{SS}). Position the V_{SS} lead on the board between RTC_XI and RTC_XO as a shield to reduce direct capacitance between RTC_XI and RTC_XO leads on the board. The CV_{DDRTC} pin can be connected to the same power supply as CV_{DD}, or may be connected to a different supply that meets the recommended operating conditions (see [Section 4.2, Recommended Operating Conditions](#)), if desired.

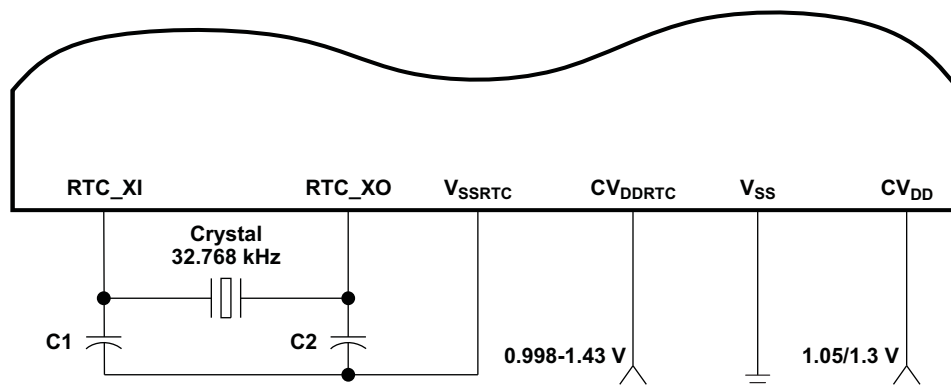


Figure 5-4. 32.768-kHz RTC Oscillator

The crystal should be in fundamental-mode function, and parallel resonant, with a maximum effective series resistance (ESR) specified in [Table 5-1](#). The load capacitors, C1 and C2, are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitors values are usually approximately twice the value of the crystal's load capacitance, CL, which is specified in the crystal manufacturer's datasheet and should be chosen such that the equation is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (RTC_XI and RTC_XO) and to the V_{SSRTC} pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-1. Input Requirements for Crystal on the 32.768-kHz RTC Oscillator

| PARAMETER | MIN | NOM | MAX | UNIT |
|--|-----|--------|-----|------|
| Start-up time (from power up until oscillating at stable frequency of 32.768-kHz) ⁽¹⁾ | 0.2 | | 2 | sec |
| Oscillation frequency | | 32.768 | | kHz |
| ESR | | | 100 | kΩ |
| Maximum shunt capacitance | | | 1.6 | pF |
| Maximum crystal drive | | | 1.0 | μW |

(1) The startup time is highly dependent on the ESR and the capacitive load of the crystal.

5.4.2 CLKIN Pin With LVCMOS-Compatible Clock Input (Optional)

Note: If CLKIN is not used, the pin **must** be tied low.

A LVCMOS-compatible clock input of a frequency less than 24 MHz can be fed into the CLKIN pin for use by the DSP system clock generator. The external connections are shown in [Figure 5-5](#) and [Figure 5-6](#). The bootloader assumes that the CLKIN pin is connected to the LVCMOS-compatible clock source with a frequency of 11.2896-, 12.0-, or 12.288-MHz. These frequencies were selected to support boot mode peripheral speeds of 500 KHz for SPI and 400 KHz for I2C. These clock frequencies are achieved by dividing the CLKIN value by 25 for SPI and by 32 for I2C. If a faster external clock is input, then these boot modes will run at faster clock speeds. If the system design utilizes faster peripherals or these boot modes are not used, CLKIN values higher than 12.288 MHz can be used. **Note:** The CLKIN pin operates at the same voltage as the DV_{DDIO} supply (1.8-, 2.5-, 2.75-, or 3.3-V).

In this configuration the RTC oscillator can be optionally disabled by connecting RTC_XI to CV_{DDRTC} and RTC_XO to ground (V_{SS}). However, when the RTC oscillator is disabled the RTC registers starting at I/O address 1900h will not be accessible. This includes the RTC Power Management Register which provides control to the on-chip LDOs and WAKEUP and RTC_CLKOUT pins. **Note:** the RTC must still be powered by an external power source even if the RTC oscillator is disabled. None of the on-chip LDOs can power CV_{DDRTC}.

For more details on the RTC on-chip oscillator, see [Section 5.4.1, Real-Time Clock \(RTC\) On-Chip Oscillator With External Crystal](#).

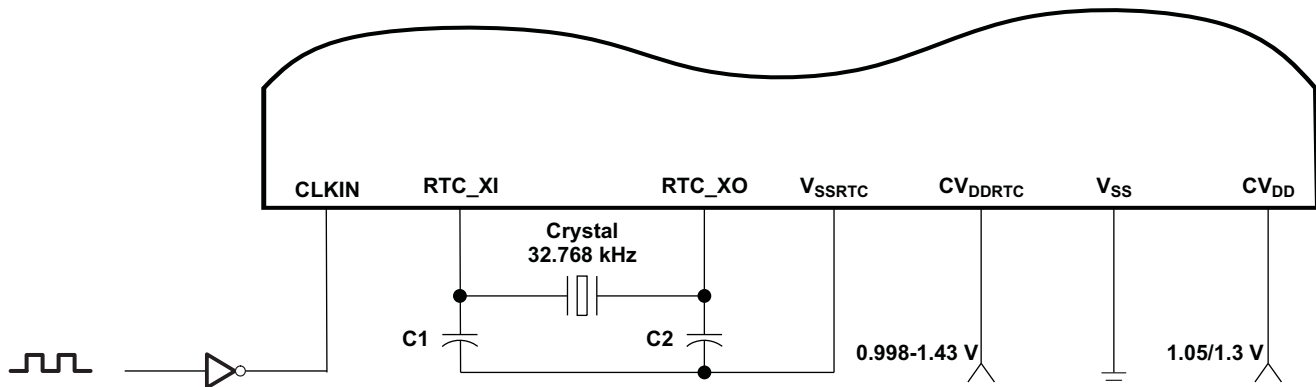


Figure 5-5. LVC MOS-Compatible Clock Input With RTC Oscillator Enabled

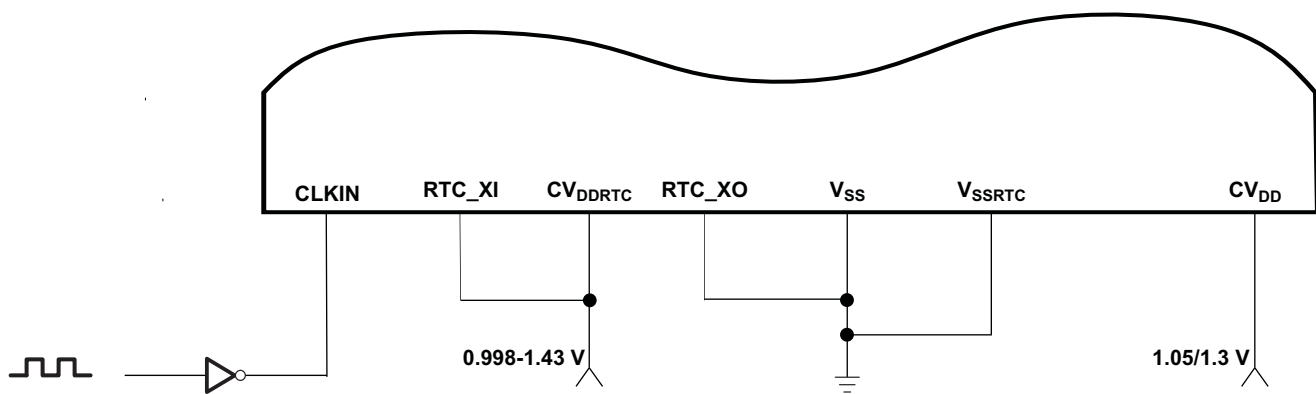


Figure 5-6. LVC MOS-Compatible Clock Input With RTC Oscillator Disabled

5.4.3 USB On-Chip Oscillator With External Crystal (Optional)

When using the USB, the USB on-chip oscillator requires an external 12-MHz crystal connected across the USB_MXI and USB_MXO pins, along with two load capacitors, as shown in [Figure 5-7](#). The external crystal load capacitors must be connected only to the USB oscillator ground pin (USB_VSSOSC). **Do not** connect to board ground (VSS). The USB_VDDOSC pin can be connected to the same power supply as USB_VDDA3P3.

The USB on-chip oscillator can be permanently disabled, via tie-offs, if the USB peripheral is not being used. To permanently disable the USB oscillator, connect the USB_MXI pin to ground (VSS) and leave the USB_MXO pin unconnected. The USB oscillator power pins (USB_VDDOSC and USB_VSSOSC) should also be connected to ground, as shown in [Figure 5-8](#).

When using an external 12-MHz oscillator, the external oscillator clock signal should be connected to the USB_MXI pin and the amplitude of the oscillator clock signal must meet the V_{IH} requirement (see [Section 4.2, Recommended Operating Conditions](#)). The USB_MXO is left unconnected and the USB_VSSOSC signal is connected to board ground (VSS).

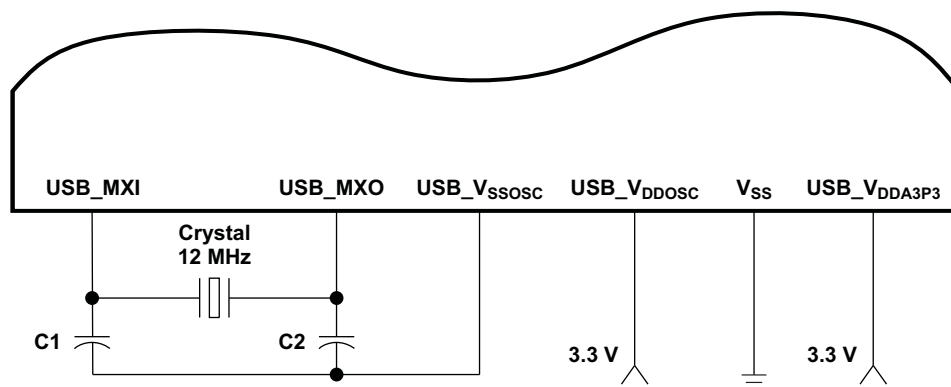


Figure 5-7. 12-MHz USB Oscillator

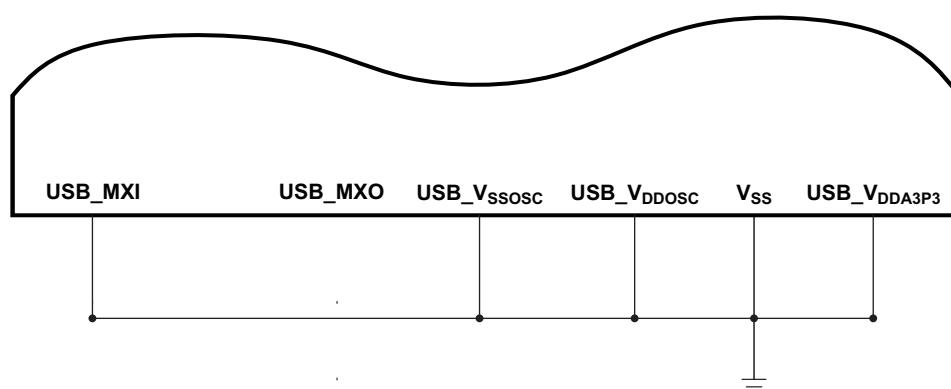


Figure 5-8. Connections when USB Oscillator is Permanently Disabled

The crystal should be in fundamental-mode operation, and parallel resonant, with a maximum effective series resistance (ESR) specified in [Table 5-2](#). The load capacitors, C1 and C2 are the total capacitance of the circuit board and components, excluding the IC and crystal. The load capacitor value is usually approximately twice the value of the crystal's load capacitance, CL, which is specified in the crystal manufacturer's datasheet and should be chosen such that the equation below is satisfied. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator pins (USB_MXI and USB_MXO) and to the USB_VSSOSC pin.

$$C_L = \frac{C_1 C_2}{(C_1 + C_2)}$$

Table 5-2. Input Requirements for Crystal on the 12-MHz USB Oscillator

| PARAMETER | MIN | NOM | MAX | UNIT |
|--|-----|-------|------|------|
| Start-up time (from power up until oscillating at stable frequency of 12 MHz) ⁽¹⁾ | | 0.100 | 10 | ms |
| Oscillation frequency | | 12 | | MHz |
| ESR | | | 100 | Ω |
| Frequency stability ⁽²⁾ | | | ±100 | ppm |
| Maximum shunt capacitance | | | 5 | pF |
| Maximum crystal drive | | | 330 | μW |

(1) The startup time is highly dependent on the ESR and the capacitive load of the crystal.

(2) If the USB is used, a 12-MHz, ±100-ppm crystal is recommended.

5.5 Clock PLLs

The device DSP uses a software-programmable PLL to generate frequencies required by the CPU, DMA, and peripherals. The reference clock for the PLL is taken from either the CLKIN pin or the RTC on-chip oscillator (as specified through the CLK_SEL pin).

5.5.1 PLL Device-Specific Information

There is a minimum and maximum operating frequency for CLKIN, PLLOUT, and the system clock (SYSCLK). The system clock generator must be configured not to exceed any of these constraints documented in this section (certain combinations of external clock inputs, internal dividers, and PLL multiply ratios are not supported).

Table 5-3. PLL Clock Frequency Ranges

| CLOCK SIGNAL NAME | CV _{DD} = 1.05 V V _{DDA_PLL} = 1.3 V | | CV _{DD} = 1.3 V V _{DDA_PLL} = 1.3 V | | UNIT |
|----------------------|---|-------------------------|--|-------------------------|------|
| | MIN | MAX | MIN | MAX | |
| CLKIN ⁽¹⁾ | | 11.2896 12 12.288 | | 11.2896 12 12.288 | MHz |
| RTC Clock | | 32.768 | | 32.768 | KHz |
| PLLIN | 32.768 | 170 | 32.768 | 170 | KHz |
| PLLOUT | 60 | 120 | 60 | 120 | MHz |
| SYSCLK | 0.032768 | 60 or 75 | 0.032768 | 100 or 120 | MHz |
| PLL_LOCKTIME | | 4 | | 4 | ms |

(1) These CLKIN values are used when the CLK_SEL pin = 1.

The PLL has lock time requirements that must be followed. The PLL lock time is the amount of time needed for the PLL to complete its phase-locking sequence.

5.5.2 Clock PLL Considerations With External Clock Sources

If the CLKIN pin is used to provide the reference clock to the PLL, to minimize the clock jitter a single clean power supply should power both the device and the external clock oscillator circuit. The minimum CLKIN rise and fall times should also be observed. For the input clock timing requirements, see [Section 5.5.3, Clock PLL Electrical Data/Timing \(Input and Output Clocks\)](#).

Rise/fall times, duty cycles (high/low pulse durations), and the load capacitance of the external clock source must meet the device requirements in this data manual (see [Section 4.3, Electrical Characteristics Over Recommended Ranges of Supply Voltage and Operating Temperature](#), and [Section 5.5.3, Clock PLL Electrical Data/Timing \(Input and Output Clocks\)](#)).

5.5.3 Clock PLL Electrical Data/Timing (Input and Output Clocks)

Table 5-4. Timing Requirements for CLKIN^{(1) (2)} (see Figure 5-9)

| NO. | | CV _{DD} = 1.05 V | | | CV _{DD} = 1.3 V | | | UNIT |
|-----|--|----------------------------------|------------------------------------|-----|----------------------------------|------------------------------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| 1 | t _{c(CLKIN)} Cycle time, external clock driven on CLKIN | | 88.577, 83.333, or 81.380 | | | 88.577, 83.333, or 81.380 | | ns |
| 2 | t _{w(CLKINH)} Pulse width, CLKIN high | 0.466 * t _{c(CLKIN)} | | | 0.466 * t _{c(CLKIN)} | | | ns |
| 3 | t _{w(CLKINL)} Pulse width, CLKIN low | 0.466 * t _{c(CLKIN)} | | | 0.466 * t _{c(CLKIN)} | | | ns |
| 4 | t _{t(CLKIN)} Transition time, CLKIN | | | 4 | | | 4 | ns |

- (1) The CLKIN frequency and PLL multiply factor should be chosen such that the resulting clock frequency is within the specific range for CPU operating frequency.
- (2) The reference points for the rise and fall transitions are measured at V_{IL} MAX and V_{IH} MIN.

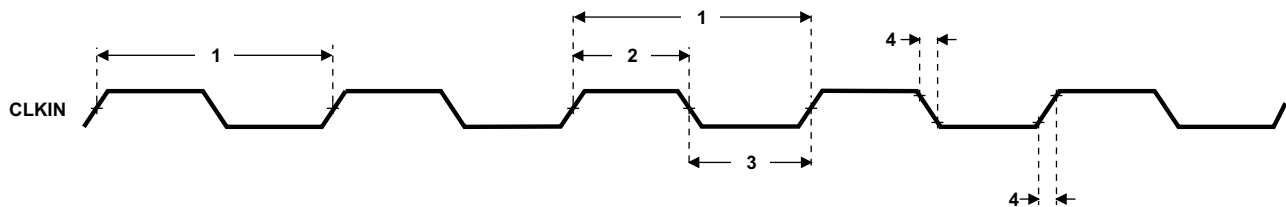


Figure 5-9. CLKIN Timing

Table 5-5. Switching Characteristics Over Recommended Operating Conditions for CLKOUT^{(1) (2)} (see Figure 5-10)

| NO. | PARAMETER | CV _{DD} = 1.05 V V _{DDA_PLL} = 1.3 V | | CV _{DD} = 1.3 V V _{DDA_PLL} = 1.3 V | | UNIT |
|-----|--|---|-------------------|--|-----------|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | t _{c(CLKOUT)} Cycle time, CLKOUT | P | 16.67 or 13.33 | P | 10 or 8.3 | ns |
| 2 | t _{w(CLKOUTH)} Pulse duration, CLKOUT high | 0.466 * t _{c(CLKOUT)} | | 0.466 * t _{c(CLKOUT)} | | ns |
| 3 | t _{w(CLKOUTL)} Pulse duration, CLKOUT low | 0.466 * t _{c(CLKOUT)} | | 0.466 * t _{c(CLKOUT)} | | ns |
| 4 | t _{t(CLKOUTR)} Transition time (rise), CLKOUT | | 5 | | 5 | ns |
| 5 | t _{t(CLKOUTF)} Transition time (fall), CLKOUT | | 5 | | 5 | ns |

- (1) The reference points for the rise and fall transitions are measured at V_{OL} MAX and V_{OH} MIN.
- (2) P = 1/SYSCLK clock frequency in nanoseconds (ns). For example, when SYSCLK frequency is 100 MHz, use P = 10 ns.

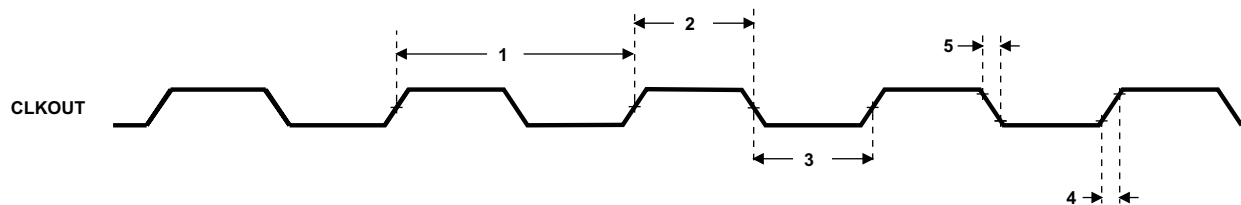


Figure 5-10. CLKOUT Timing

5.6 Direct Memory Access (DMA) Controller

The DMA controller is used to move data among internal memory, external memory, and peripherals without intervention from the CPU and in the background of CPU operation.

The DSP includes a total of four DMA controllers. Aside from the DSP resources they can access, all four DMA controllers are identical.

The DMA controller has the following features:

- Operation that is independent of the CPU.
- Four channels, which allow the DMA controller to keep track of the context of four independent block transfers.
- Event synchronization. DMA transfers in each channel can be made dependent on the occurrence of selected events.
- An interrupt for each channel. Each channel can send an interrupt to the CPU on completion of the programmed transfer.
- Ping-Pong mode allows the DMA controller to keep track of double buffering context without CPU intervention.
- A dedicated clock idle domain. The four device DMA controllers can be put into a low-power state by independently turning off their input clocks.

5.6.1 DMA Channel Synchronization Events

The DMA controllers allow activity in their channels to be synchronized to selected events. The DSP supports 20 separate synchronization events and each channel can be tied to separate sync events independent of the other channels. Synchronization events are selected by programming the CHnEVT field in the DMA_n channel event source registers (DMA_nCESR1 and DMA_nCESR2).

5.7 Reset

The device has two main types of reset: hardware reset and software reset.

Hardware reset is responsible for initializing all key states of the device. It occurs whenever the $\overline{\text{RESET}}$ pin is asserted or when the internal power-on-reset (POR) circuit deasserts an internal signal called POWERGOOD. The device's internal POR is a voltage comparator that monitors the DSP_LDOO pin voltage and generates the internal POWERGOOD signal when the DSP_LDO is enabled externally by the $\overline{\text{DSP_LDO_EN}}$ pin. POWERGOOD is asserted when the DSP_LDOO voltage is above a minimum threshold voltage provided by the bandgap. When the DSP_LDO is disabled ($\overline{\text{DSP_LDO_EN}}$ is high), the internal voltage comparator becomes inactive, and the POWERGOOD signal logic level is immediately set high. The $\overline{\text{RESET}}$ pin and the POWERGOOD signal are internally combined with a logical AND gate to produce an (active low) hardware reset (see [Figure 5-11](#), *Power-On Reset Timing Requirements* and [Figure 5-12](#), *Reset Timing Requirements*).

There are two types of software reset: the CPU's software reset instruction and the software control of the peripheral reset signals. For more information on the CPU's software reset instruction, see the *TMS320C55x CPU 3.0 CPU Reference Guide* (literature number: [SWPU073](#)). In all the device documentation, all references to "reset" refer to hardware reset. Any references to software reset will explicitly state software reset.

The device RTC has one additional type of reset, a power-on-reset (POR) for the registers in the RTC core. This POR monitors the voltage of CV_{DDRTC} and resets the RTC registers when power is first applied to the RTC core.

5.7.1 Power-On Reset (POR) Circuits

The device includes two power-on reset (POR) circuits, one for the RTC (RTC POR) and another for the rest of the chip (MAIN POR).

5.7.1.1 RTC Power-On Reset (POR)

The RTC POR ensures that the flip-flops in the CV_{DDRTC} power domain have an initial state upon powerup. In particular, the RTCNOPWR register is reset by this POR and is used to indicate that the RTC time registers need to be initialized with the current time and date when power is first applied.

5.7.1.2 Main Power-On Reset (POR)

The device includes an analog power-on reset (POR) circuit that keeps the DSP in reset until specific voltages have reached predetermined levels. When the DSP_LDO is enabled externally by the $\overline{\text{DSP_LDO_EN}}$ pin, the output of the POR circuit, POWERGOOD, is held low until the following conditions are satisfied:

- LDO1 is powered and the bandgap is active for at least approximately 8 ms
- VDD_ANA is powered for at least approximately 4 ms
- DSP_LDOO is above a threshold of approximately 950 mV (see **Note**.)

Note: The POR comparator has hysteresis, so the threshold voltage becomes approximately 850 mV after POWERGOOD signal is set high.

Once these conditions are met, the internal POWERGOOD signal is set high. The POWERGOOD signal is internally combined with the $\overline{\text{RESET}}$ pin signal, via an AND-gate, to produce the DSP subsystem's global reset. This global reset is the hardware reset for the whole chip, except the RTC. When the global reset is deasserted (high), the boot sequence starts. For more detailed information on the boot sequence, see [Section 3.4](#), *Boot Sequence*.

When the DSP_LDO is disabled ($\overline{\text{DSP_LDO_EN}}$ pin = 1), the voltage monitoring on the DSP_LDOO pin is de-activated and the POWERGOOD signal is immediately set high. The $\overline{\text{RESET}}$ pin will be the sole source of hardware reset.

5.7.1.3 Reset Pin ($\overline{\text{RESET}}$)

The device can receive an external reset signal on the $\overline{\text{RESET}}$ pin. As specified above in [Section 5.7.1.2, Main Power-On Reset](#), the $\overline{\text{RESET}}$ pin is combined with the internal POWERGOOD signal, that is generated by the MAIN POR, via an AND-gate. The output of the AND gate provides the hardware reset to the chip. The $\overline{\text{RESET}}$ pin may be tied high and the MAIN POR can provide the hardware reset in case DSP_LDO is enabled ($\overline{\text{DSP_LDO_EN}} = 0$), but an external hardware reset must be provided via the $\overline{\text{RESET}}$ pin when the DSP_LDO is disabled ($\overline{\text{DSP_LDO_EN}} = 1$).

Once the hardware reset is applied, the system clock generator is enabled and the DSP starts the boot sequence. For more information on the boot sequence, see [Section 3.4, Boot Sequence](#).

5.7.2 Pin Behavior at Reset

During normal operation, pins are controlled by the respective peripheral selected in the External Bus Selection Register (EBSR) register. During power-on reset and reset, the behavior of the output pins changes and is categorized as follows:

- **High Group:** $\overline{\text{EM_CS4}}$, $\overline{\text{EM_CS5}}$, $\overline{\text{EM_CS2}}$, $\overline{\text{EM_CS3}}$, EM_DQM0, EM_DQM1, $\overline{\text{EM_OE}}$, $\overline{\text{EM_WE}}$, LCD_RS/SPI_CS3, EM_SDCAS, EM_SDRAS
- **Low Group:** LCD_EN_RDB/SPI_CLK, EM_R $\overline{\text{W}}$, MMC0_CLK/I2S0_CLK/GP[0], MMC1_CLK/I2S1_CLK/GP[6], EM_SDCLK
- **Z Group:** EM_D[15:0], EMU[1:0], SCL, SDA, LCD_D[0]/SPI_RX, LCD_D[1]/SPI_TX, LCD_D[10]/I2S2_RX/GP[20]/SPI_RX, LCD_D[11]/I2S2_DX/GP[27]/SPI_TX, LCD_D[12]/I2S2_RTS/GP[28]/I2S3_CLK, LCD_D[13]/I2S2_CTS/GP[29]/I2S3_RS, LCD_D[14]/I2S2_RXD/GP[30]/I2S3_RX, LCD_D[15]/I2S2_TXD/GP[31]/I2S3_DX, LCD_D[2]/GP[12], LCD_D[3]/GP[13], LCD_D[4]/GP[14], LCD_D[5]/GP[15], LCD_D[6]/GP[16], LCD_D[7]/GP[17], LCD_D[8]/I2S2_CLK/GP[18]/SPI_CLK, LCD_D[9]/I2S2_FS/GP[19]/SPI_CS0, RTC_CLKOUT, MMC0_CMD/I2S0_FS/GP[1], MMC0_D0/I2S0_DX/GP[2], MMC0_D1/I2S0_RX/GP[3], MMC0_D2/GP[4], MMC0_D3/GP[5], MMC1_CMD/I2S1_FS/GP[7], MMC1_D0/I2S1_DX/GP[8], MMC1_D1/I2S1_RX/GP[9], MMC1_D2/GP[10], MMC1_D3/GP[11], TDO, WAKEUP
- **CLKOUT Group:** CLKOUT, LCD_CS1_E1/SPI_CS1
- **SYNCH 0→1 Group:** LCD_CS0_E0/SPI_CS0, LCD_RW_WRB/SPI_CS2, EM_SDCKE
- **SYNCH 1→0 Group:** $\overline{\text{EM_CS0}}$, $\overline{\text{EM_CS1}}$
- **SYNCH X→1 Group:** EM_BA[1:0], XF
- **SYNCH X→0 Group:** EM_A[20:0]

5.7.3 Reset Electrical Data/Timing

Table 5-6. Timing Requirements for Reset⁽¹⁾ (see Figure 5-11 and Figure 5-12)

| NO. | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | UNIT |
|-----|--|---------------------------|-----|--------------------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| 1 | t _{w(RSTL)} Pulse duration, $\overline{\text{RESET}}$ low | 3P | | 3P | | ns |

(1) P = 1/SYSCLK clock frequency in ns. For example, if SYSCLK = 12 MHz, use P = 83.3 ns. In IDLE3 mode the system clock generator is bypassed and the SYSCLK frequency is equal to either CLKIN or the RTC clock frequency depending on CLK_SEL.

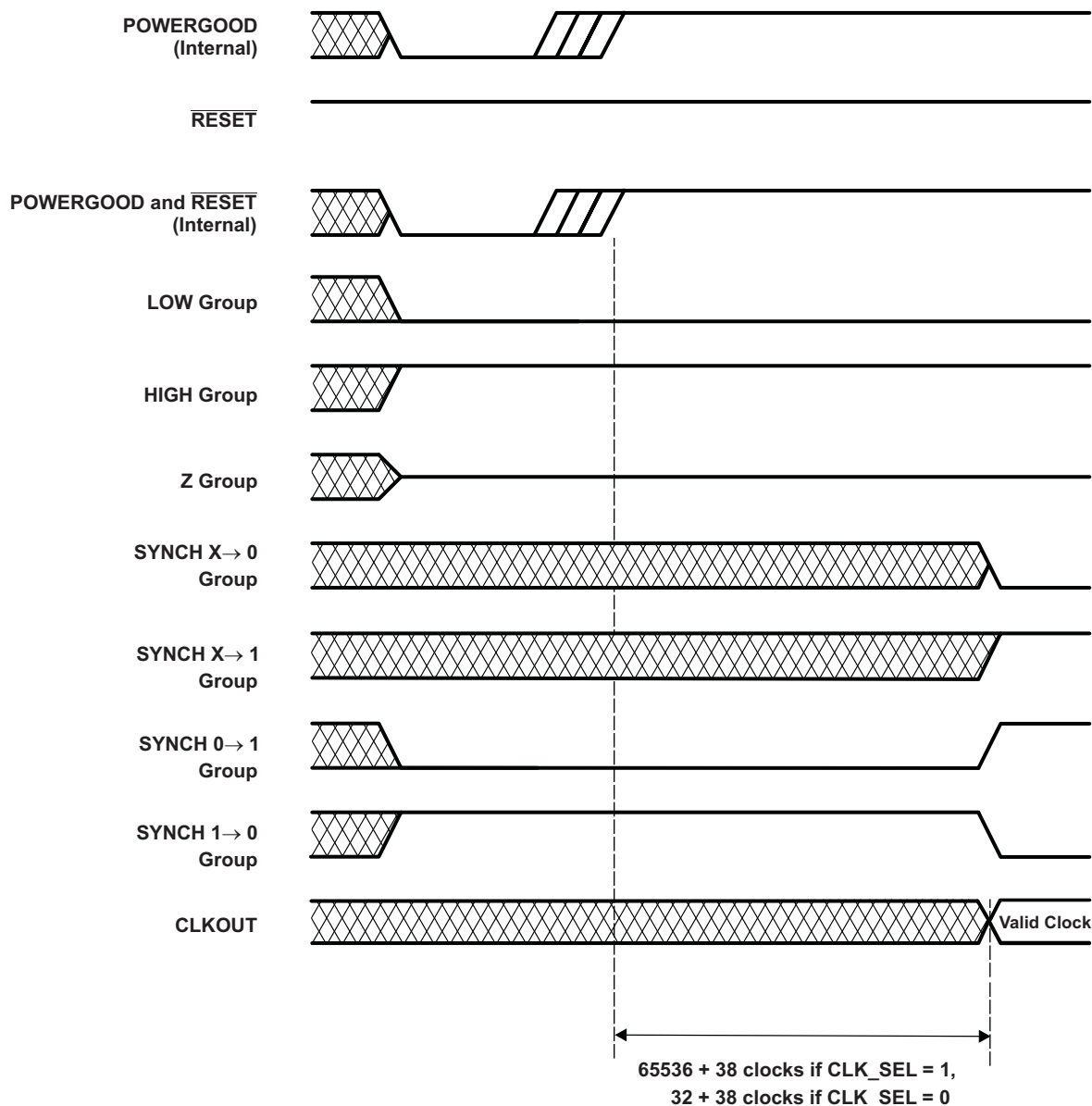


Figure 5-11. Power-On Reset Timing Requirements

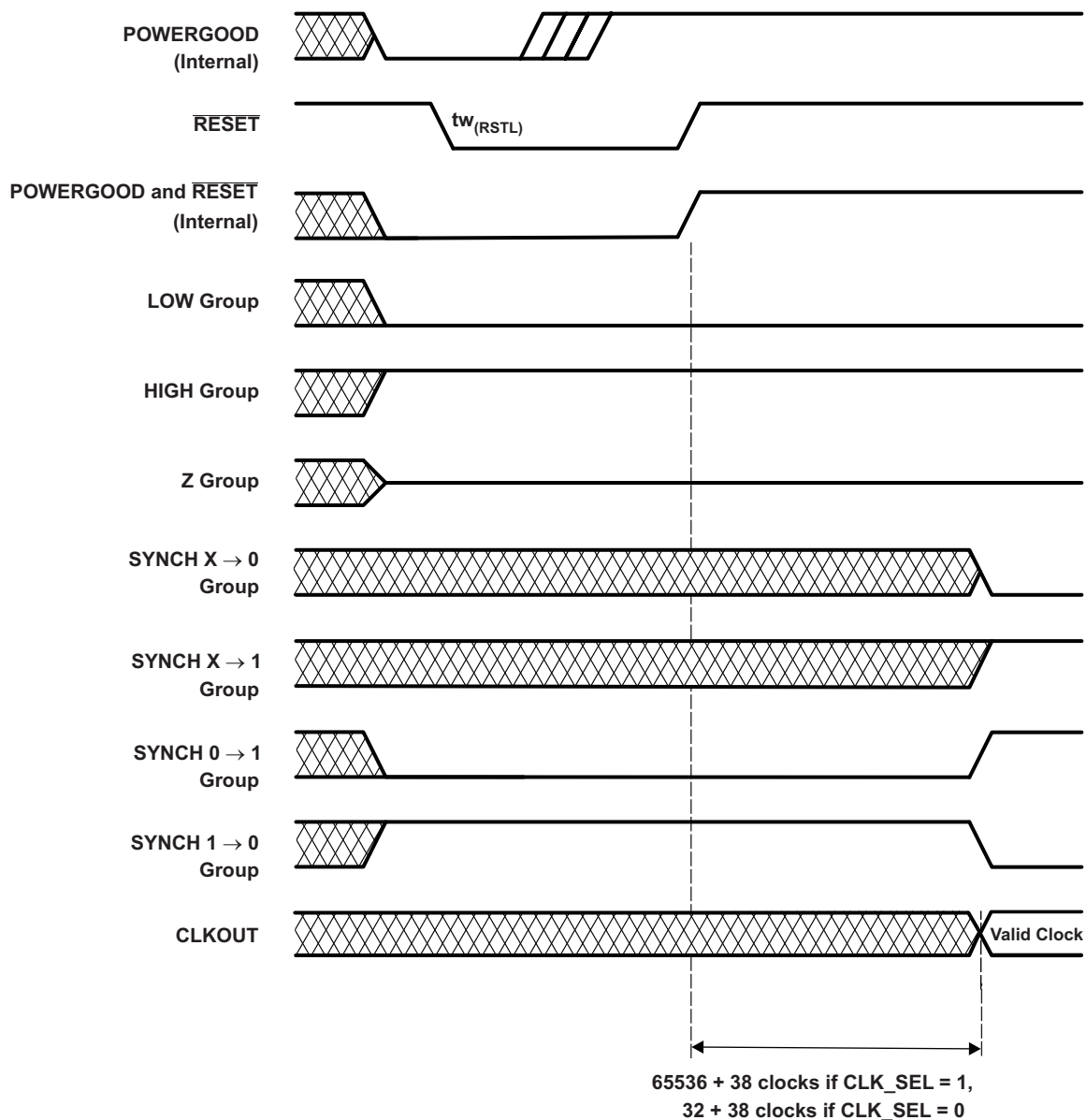


Figure 5-12. Reset Timing Requirements

5.8 Wake-up Events, Interrupts, and XF

The device has a number of interrupts to service the needs of its peripherals. The interrupts can be selectively enabled or disabled.

5.8.1 Interrupts Electrical Data/Timing

Table 5-7. Timing Requirements for Interrupts⁽¹⁾ (see Figure 5-13)

| NO. | | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|----------------------|---|---|-----|------|
| | | | MIN | MAX | |
| 1 | t _{w(INTH)} | Pulse duration, interrupt high CPU active | 2P | | ns |
| 2 | t _{w(INTL)} | Pulse duration, interrupt low CPU active | 2P | | ns |

(1) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns. For example, when the CPU core is clocked at 120 MHz, use P = 8.3 ns.

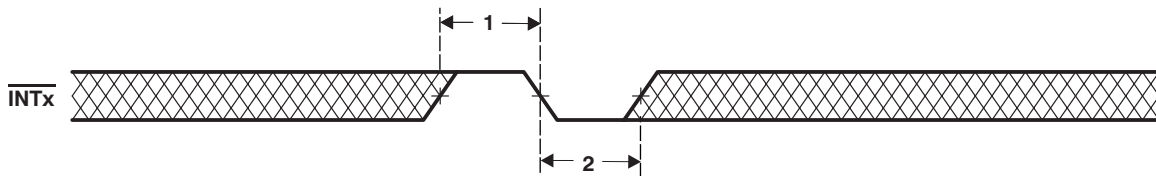


Figure 5-13. External Interrupt Timings

5.8.2 Wake-Up From IDLE Electrical Data/Timing

Table 5-8. Timing Requirements for Wake-Up From IDLE (see Figure 5-14)

| NO. | | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|----------------------|---|---|-----|------|
| | | | MIN | MAX | |
| 1 | t _{w(WKPL)} | Pulse duration, WAKEUP or $\overline{\text{INTx}}$ low, SYSCLKDIS = 1 | 30.5 | | μs |

Table 5-9. Switching Characteristics Over Recommended Operating Conditions For Wake-Up From IDLE⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (see Figure 5-14)

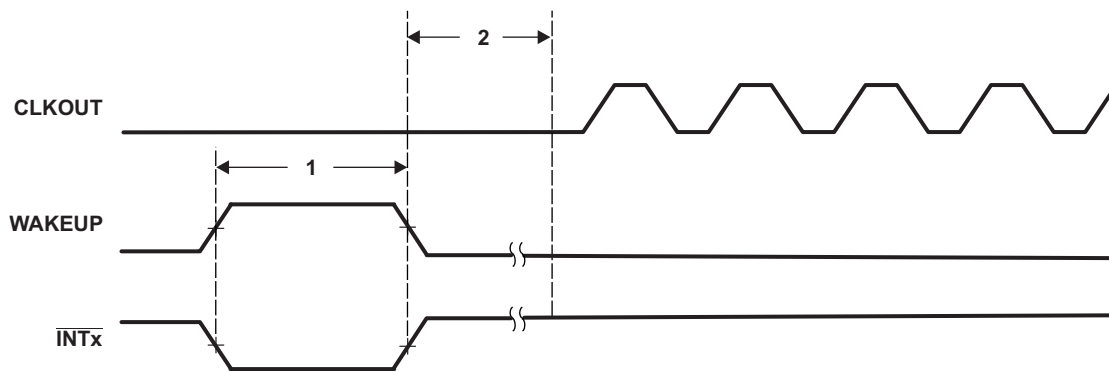
| NO. | PARAMETER | | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | | UNIT |
|-----|--------------------------------|---|--|---|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| 2 | t _{d(WKEVTH-C KLGEN)} | Delay time, WAKEUP pulse complete to CPU active | IDLE3 Mode with SYSCLKDIS = 1, WAKEUP or $\overline{\text{INTx}}$ event, CLK_SEL = 1 | D | | | ns |
| | | | IDLE3 Mode with SYSCLKDIS = 1, WAKEUP or $\overline{\text{INTx}}$ event, CLK_SEL = 0 | C | | | ns |
| | | | IDLE2 Mode; $\overline{\text{INTx}}$ event | 3P | | | ns |

(1) D = 1/ External Clock Frequency (CLKIN).

(2) C = 1/RTCCLK = 30.5 μs. RTCCLK is the clock output of the 32.768-kHz RTC oscillator.

(3) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(4) Assumes the internal LDOs are used with a 0.1μF bandgap capacitor.



- A. INT[1:0] can only be used as a wake-up event for IDLE3 and IDLE2 modes.
- B. RTC interrupt (internal signal) can be used as wake-up event for IDLE3 and IDLE2 modes.
- C. Any unmasked interrupt can be used to exit the IDLE2 mode.
- D. CLKOUT reflects either the CPU clock, SAR, USB PHY, or PLL clock dependent on the setting of the CLOCKOUT Clock Source Register. For this diagram, CLKOUT refers to the CPU clock.

Figure 5-14. Wake-Up From IDLE Timings

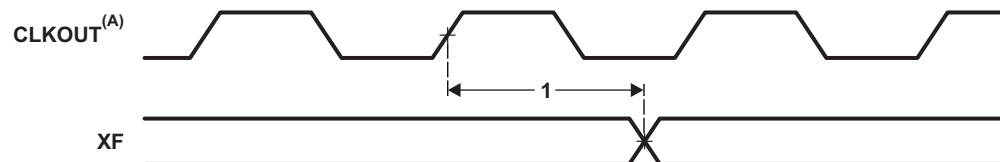
5.8.3 XF Electrical Data/Timing

Table 5-10. Switching Characteristics Over Recommended Operating Conditions For XF⁽¹⁾ (2)
(see [Figure 5-15](#))

| NO. | PARAMETER | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|---|---|------|------|
| | | MIN | MAX | |
| 1 | t _{d(XF)} Delay time, CLKOUT high to XF high | 0 | 10.2 | ns |

(1) P = 1/SYSCLK clock frequency in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) C = 1/RTCCLK = 30.5 μs. RTCCLK is the clock output of the 32.768-kHz RTC oscillator.



- A. CLKOUT reflects either the CPU clock, SAR, USB PHY, or PLL clock dependent on the setting of the CLOCKOUT Clock Source Register. For this diagram, CLKOUT refers to the CPU clock.

Figure 5-15. XF Timings

5.9 External Memory Interface (EMIF)

The device supports several memories and external device interfaces, including: NOR Flash, NAND Flash, SRAM, Non-Mobile SDRAM, and Mobile SDRAM (mSDRAM).

Note: The device can support non-mobile SDRAM under certain circumstances. The device also always uses mobile SDRAM initialization, but it is able to support SDRAM memories that ignore the BA0 and BA1 pins for the 'load mode register' command. During the mobile SDRAM initialization, the device issues the 'load mode register' initialization command to two different addresses that differ in only the BA0 and BA1 address bits. These registers are the Extended Mode register and the Mode register. The Extended mode register exists only in mSDRAM and not in non-mSDRAM. If a non-mobile SDRAM memory ignores bits BA0 and BA1, the second loaded register value overwrites the first, leaving the desired value in the Mode register and the non-mobile SDRAM will work with the device.

The EMIF provides an 8-bit or 16-bit data bus, an address bus width up to 21 bits, and 6 chip selects, along with memory control signals.

The EM_A[20:15] address signals are multiplexed with the GPIO peripheral and controlled by the External Bus Selection Register (EBSR). For more detail on the pin muxing, see the [Section 3.6.1, External Bus Selection Register \(EBSR\)](#).

5.9.1 EMIF Asynchronous Memory Support

The EMIF supports asynchronous:

- SRAM memories
- NAND Flash memories
- NOR Flash memories

The EMIF data bus can be configured for both 8- or 16-bit width. The device supports up to 21 address lines and four external wait/interrupt inputs. Up to four asynchronous chip selects are supported by EMIF (EM_CS[5:2]).

Each chip select has the following individually programmable attributes:

- Data bus width
- Read cycle timings: setup, hold, strobe
- Write cycle timings: setup, hold, strobe
- Bus turn around time
- Extended Wait Option With Programmable Timeout
- Select Strobe Option
- NAND flash controller supports 1-bit and 4-bit ECC calculation on blocks of 512 bytes

5.9.2 EMIF Non-Mobile and Mobile Synchronous DRAM Memory Supported

The EMIF supports 16-bit non-mobile and mobile single data rate (SDR) SDRAM in addition to the asynchronous memories listed in [Section 5.9.1, EMIF Asynchronous Memory Support](#). The supported SDRAM and mobile SDRAM configurations are:

- One, two, and four bank SDRAM/mSDRAM devices
- Supports devices with eight, nine, ten, and eleven column addresses
- CAS latency of two or three clock cycles
- 16-bit data-bus width
- 3.3/2.75/2.5/1.8 -V LVCMOS interface that is separate from the rest of the chip I/Os.
- One (EM_CS0) or two (EM_CS[1:0]) chip selects

Additionally, the SDRAM/mSDRAM interface of EMIF supports placing the SDRAM/mSDRAM in "Self-Refresh" and "Powerdown Modes". Self-Refresh mode allows the SDRAM/mSDRAM to be put into a low-power state while still retaining memory contents; since the SDRAM/mSDRAM will continue to refresh itself even without clocks from the DSP. Powerdown mode achieves even lower power, except the DSP must periodically wake the SDRAM/mSDRAM up and issue refreshes if data retention is required. To achieve the lowest power consumption, the SDRAM/mSDRAM interface has configurable slew rate on the EMIF pins.

The device has limitations to the clock frequency on the EM_SDCLK pin based on the CV_{DD} and DV_{DDEMIF} .

- The clock frequency on the EM_SDCLK pin can be configured either as SYSCLK (DSP Operating Frequency) or SYSCLK/2 via bit 0 of the ECDR Register (0x1C26h)
- When $CV_{DD} = 1.3$ V and $DV_{DDEMIF} = 3.3$ V, 2.75 V, or 2.5 V, the max clock frequency on the EM_SDCLK pin is limited to 100 MHz ($EM_SDCLK \leq 100$ MHz). Therefore, if $SYSCLK \leq 100$ MHz, the EM_SDCLK can be configured either as SYSCLK or SYSCLK/2, but if $SYSCLK > 100$ MHz, the EM_SDCLK must be configured as SYSCLK/2.
- When $CV_{DD} = 1.05$ V, and $DV_{DDEMIF} = 3.3$ V, 2.75 V, or 2.5 V, the max clock frequency on the EM_SDCLK pin is limited to 60 MHz ($EM_SDCLK \leq 60$ MHz). Therefore, if $SYSCLK \leq 60$ MHz, the EM_SDCLK can be configured as either SYSCLK or SYSCLK/2, but if $SYSCLK > 60$ MHz, the EM_SDCLK must be configured as SYSCLK/2.
- When $DV_{DDEMIF} = 1.8$ V, regardless of the CV_{DD} voltage, the clock frequency on the EM_SDCLK pin must be configured as SYSCLK/2 and ≤ 50 MHz.

5.9.3 EMIF Peripheral Register Descriptions

Table 5-11 shows the EMIF registers.

Table 5-11. External Memory Interface (EMIF) Peripheral Registers⁽¹⁾

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|---------|--|
| 1000h | REV | Revision Register |
| 1001h | STATUS | Status Register |
| 1004h | AWCCR1 | Asynchronous Wait Cycle Configuration Register 1 |
| 1005h | AWCCR2 | Asynchronous Wait Cycle Configuration Register 2 |
| 1008h | SDCR1 | SDRAM/mSDRAM Configuration Register 1 |
| 1009h | SDCR2 | SDRAM/mSDRAM Configuration Register 2 |
| 100Ch | SDRCR | SDRAM/mSDRAM Refresh Control Register |
| 1010h | ACS2CR1 | Asynchronous CS2 Configuration Register 1 |
| 1011h | ACS2CR2 | Asynchronous CS2 Configuration Register 2 |
| 1014h | ACS3CR1 | Asynchronous CS3 Configuration Register 1 |
| 1015h | ACS3CR2 | Asynchronous CS3 Configuration Register 2 |
| 1018h | ACS4CR1 | Asynchronous CS4 Configuration Register 1 |
| 1019h | ACS4CR2 | Asynchronous CS4 Configuration Register 2 |
| 101Ch | ACS5CR1 | Asynchronous CS5 Configuration Register 1 |
| 101Dh | ACS5CR2 | Asynchronous CS5 Configuration Register 2 |
| 1020h | SDTIMR1 | SDRAM/mSDRAM Timing Register 1 |
| 1021h | SDTIMR2 | SDRAM/mSDRAM Timing Register 2 |
| 103Ch | SDSRETR | SDRAM/mSDRAM Self Refresh Exit Timing Register |
| 1040h | EIRR | EMIF Interrupt Raw Register |
| 1044h | EIMR | EMIF Interrupt Mask Register |
| 1048h | EIMSR | EMIF Interrupt Mask Set Register |

(1) Before reading or writing to the EMIF registers, be sure to set the BYTEMODE bits to 00b in the EMIF system control register to enable word accesses to the EMIF registers.

Table 5-11. External Memory Interface (EMIF) Peripheral Registers⁽¹⁾ (continued)

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|----------------------|-----------------|---|
| 104Ch | EIMCR | EMIF Interrupt Mask Clear Register |
| 1060h | NANDFCR | NAND Flash Control Register |
| 1064h | NANDFSR1 | NAND Flash Status Register 1 |
| 1065h | NANDFSR2 | NAND Flash Status Register 2 |
| 1068h | PGMODECTRL1 | Page Mode Control Register 1 |
| 1069h | PGMODECTRL2 | Page Mode Control Register 2 |
| 1070h | NCS2ECC1 | NAND Flash CS2 1-Bit ECC Register 1 |
| 1071h | NCS2ECC2 | NAND Flash CS2 1-Bit ECC Register 2 |
| 1074h | NCS3ECC1 | NAND Flash CS3 1-Bit ECC Register 1 |
| 1075h | NCS3ECC2 | NAND Flash CS3 1-Bit ECC Register 2 |
| 1078h | NCS4ECC1 | NAND Flash CS4 1-Bit ECC Register 1 |
| 1079h | NCS4ECC2 | NAND Flash CS4 1-Bit ECC Register 2 |
| 107Ch | NCS5ECC1 | NAND Flash CS5 1-Bit ECC Register 1 |
| 107Dh | NCS5ECC2 | NAND Flash CS5 1-Bit ECC Register 2 |
| 10BCh | NAND4BITECCLOAD | NAND Flash 4-Bit ECC Load Register |
| 10C0h | NAND4BITECC1 | NAND Flash 4-Bit ECC Register 1 |
| 10C1h | NAND4BITECC2 | NAND Flash 4-Bit ECC Register 2 |
| 10C4h | NAND4BITECC3 | NAND Flash 4-Bit ECC Register 3 |
| 10C5h | NAND4BITECC4 | NAND Flash 4-Bit ECC Register 4 |
| 10C8h | NAND4BITECC5 | NAND Flash 4-Bit ECC Register 5 |
| 10C9h | NAND4BITECC6 | NAND Flash 4-Bit ECC Register 6 |
| 10CCh | NAND4BITECC7 | NAND Flash 4-Bit ECC Register 7 |
| 10CDh | NAND4BITECC8 | NAND Flash 4-Bit ECC Register 8 |
| 10D0h | NANDERRADD1 | NAND Flash 4-Bit ECC Error Address Register 1 |
| 10D1h | NANDERRADD2 | NAND Flash 4-Bit ECC Error Address Register 2 |
| 10D4h | NANDERRADD3 | NAND Flash 4-Bit ECC Error Address Register 3 |
| 10D5h | NANDERRADD4 | NAND Flash 4-Bit ECC Error Address Register 4 |
| 10D8h | NANDERRVAL1 | NAND Flash 4-Bit ECC Error Value Register 1 |
| 10D9h | NANDERRVAL2 | NAND Flash 4-Bit ECC Error Value Register 2 |
| 10DCh | NANDERRVAL3 | NAND Flash 4-Bit ECC Error Value Register 3 |
| 10DDh | NANDERRVAL4 | NAND Flash 4-Bit ECC Error Value Register 4 |

5.9.4 EMIF Electrical Data/Timing $CV_{DD} = 1.05\text{ V}$, $DV_{DDEMIF} = 3.3/2.75/2.5/1.8\text{ V}$, External Loading = 10 pF

Table 5-12. Timing Requirements for EMIF SDRAM/mSDRAM Interface⁽¹⁾ (see [Figure 5-16](#) and [Figure 5-17](#))

| NO. | | | $CV_{DD} = 1.05\text{ V}$ $DV_{DDEMIF} = 3.3/2.75/2.5\text{ V}$ | | $CV_{DD} = 1.05\text{ V}$ $DV_{DDEMIF} = 1.8\text{ V}$ | | UNIT |
|-----|-------------------|--|--|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 19 | $t_{su}(DV-CLKH)$ | Input setup time, read data valid on EM_D[15:0] before EM_SDCLK rising | 3.4 | | 3.4 | | ns |
| 20 | $t_h(CLKH-DIV)$ | Input hold time, read data valid on EM_D[15:0] after EM_SDCLK rising | 1.2 | | 1.2 | | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

Table 5-13. Switching Characteristics Over Recommended Operating Conditions for EMIF SDRAM/mSDRAM Interface⁽¹⁾⁽²⁾ (see [Figure 5-16](#) and [Figure 5-17](#))

| NO. | PARAMETER | | $CV_{DD} = 1.05\text{ V}$ $DV_{DDEMIF} = 3.3/2.75/2.5\text{ V}$ | | | $CV_{DD} = 1.05\text{ V}$ $DV_{DDEMIF} = 1.8\text{ V}$ | | | UNIT |
|-----|------------------|--|--|-----|------|---|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| 1 | $t_c(CLK)$ | Cycle time, EMIF clock EM_SDCLK | 16.67 ⁽³⁾ | | | 20 ⁽⁴⁾ | | | ns |
| 2 | $t_w(CLK)$ | Pulse width, EMIF clock EM_SDCLK high or low | 8.34 | | | 10 | | | ns |
| 3 | $t_d(CLKH-CSV)$ | Delay time, EM_SDCLK rising to EMA_CS[1:0] valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 5 | $t_d(CLKH-DQMV)$ | Delay time, EM_SDCLK rising to EM_DQM[1:0] valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 7 | $t_d(CLKH-AV)$ | Delay time, EM_SDCLK rising to EM_A[20:0] and EM_BA[1:0] valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 9 | $t_d(CLKH-DV)$ | Delay time, EM_SDCLK rising to EM_D[15:0] valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 11 | $t_d(CLKH-RASV)$ | Delay time, EM_SDCLK rising to $\overline{EM_SDRAS}$ valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 13 | $t_d(CLKH-CASV)$ | Delay time, EM_SDCLK rising to $\overline{EM_SDCAS}$ valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 15 | $t_d(CLKH-WEV)$ | Delay time, EM_SDCLK rising to $\overline{EM_WE}$ valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |
| 21 | $t_d(CLKH-CKEV)$ | Delay time, EM_SDCLK rising to EM_SDCKE valid | 1.1 | | 13.2 | 1.1 | | 13.2 | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 60 or 100 MHz, E = 16.67 or 10 ns, respectively. For more detail on the EM_SDCLK speed see [Section 5.9.2](#), *EMIF Non-Mobile and Mobile Synchronous DRAM Memory Supported*.

(3) When $CV_{DD} = 1.05\text{ V}$, and $DV_{DDEMIF} = 3.3\text{ V}$, 2.75 V or 2.5 V, the max clock frequency on the EM_SDCLK pin is limited to 60 MHz (EM_SDCLK = 60 MHz). For more information, see *TMS320C5515/14/05/04 DSP External Memory Interface (EMIF) User's Guide* (literature number [SPRUGU6](#)).

(4) When $DV_{DDEMIF} = 1.8\text{ V}$, the max clock frequency on the EM_SDCLK pin is limited to 50 MHz (EM_SDCLK = 50 MHz). For more information, see *TMS320C5515/14/05/04 DSP External Memory Interface (EMIF) User's Guide* (literature number [SPRUGU6](#)).

Table 5-14. Timing Requirements for EMIF Asynchronous Memory⁽¹⁾⁽²⁾ (see [Figure 5-18](#), [Figure 5-20](#), and [Figure 5-21](#))

| NO. | | | CV _{DD} = 1.05 V DV _{DDEMIF} = 3.3/2.75/2.5/1.8 V | | | UNIT |
|--------|---|---|--|-----|-----|------|
| | | | MIN | NOM | MAX | |
| | | | READS and WRITES | | | |
| 2 | t _w (EM_WAIT) | Pulse duration, EM_WAITx assertion and deassertion | 2E | | | ns |
| READS | | | | | | |
| 12 | t _{su} (EMDV-EMOE _H) | Setup time, EM_D[15:0] valid before $\overline{\text{EM_OE}}$ high | 14.5 | | | ns |
| 13 | t _h (EMOE _H -EMDIV) | Hold time, EM_D[15:0] valid after $\overline{\text{EM_OE}}$ high | 0 | | | ns |
| 14 | t _{su} (EMOEL-EMWAIT) | Setup time, EM_WAITx asserted before end of Strobe Phase ⁽³⁾ | 4E + 13 | | | ns |
| WRITES | | | | | | |
| 28 | t _{su} (EMWEL-EMWAIT) | Setup time, EM_WAITx asserted before end of Strobe Phase ⁽³⁾ | 4E + 13 | | | ns |

(1) E = SYSCLK period in ns. For example, when SYSCLK is set to 100/120 MHz, E = 10/8.33 ns, respectively.

(2) Timing parameters are obtained with 10pF loading on the EMIF pins.

(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. [Figure 5-20](#) and [Figure 5-21](#) describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-15. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory^{(1)(2) (3)} (see Figure 5-19 and Figure 5-21)⁽⁴⁾

| NO. | PARAMETER | | CV _{DD} = 1.05 V DV _{DEMIF} = 3.3/2.75/2.5/1.8 V | | | UNIT |
|------------------|--------------------------------|--|---|------------------------|-----------------------------|------|
| | | | MIN | NOM | MAX | |
| READS and WRITES | | | | | | |
| 1 | t _d (TURNAROUND) | Turn around time | (TA)*E - 13 | (TA)*E | (TA)*E + 13 | ns |
| READS | | | | | | |
| 3 | t _c (EMRCYCLE) | EMIF read cycle time (EW = 0) | (RS+RST+RH)*E - 13 | (RS+RST+RH)*E | (RS+RST+RH)*E + 13 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+(EWC*16))*E - 13 | (RS+RST+RH+(EWC*16))*E | (RS+RST+RH+(EWC*16))*E +139 | ns |
| 4 | t _{su} (EMCEL-EMOEL) | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_OE}}$ low (SS = 0) | (RS)*E-13 | (RS)*E | (RS)*E+13 | ns |
| | | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_OE}}$ low (SS = 1) | -13 | 0 | +13 | ns |
| 5 | t _h (EMOEH-EMCEH) | Output hold time, $\overline{\text{EM_OE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 0) | (RH)*E - 13 | (RH)*E | (RH)*E + 13 | ns |
| | | Output hold time, $\overline{\text{EM_OE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 1) | -13 | 0 | +13 | ns |
| 6 | t _{su} (EMBAV-EMOEL) | Output setup time, EM_BA[1:0] valid to $\overline{\text{EM_OE}}$ low | (RS)*E-13 | (RS)*E | (RS)*E+13 | ns |
| 7 | t _h (EMOEH-EMBAIV) | Output hold time, $\overline{\text{EM_OE}}$ high to EM_BA[1:0] invalid | (RH)*E-13 | (RH)*E | (RH)*E+13 | ns |
| 8 | t _{su} (EMBAV-EMOEL) | Output setup time, EM_A[20:0] valid to $\overline{\text{EM_OE}}$ low | (RS)*E-13 | (RS)*E | (RS)*E+13 | ns |
| 9 | t _h (EMOEH-EMAIV) | Output hold time, $\overline{\text{EM_OE}}$ high to EM_A[20:0] invalid | (RH)*E-13 | (RH)*E | (RH)*E+13 | ns |
| 10 | t _w (EMOEL) | $\overline{\text{EM_OE}}$ active low width (EW = 0) | (RST)*E-13 | (RST)*E | (RST)*E+13 | ns |
| | | $\overline{\text{EM_OE}}$ active low width (EW = 1) | (RST+(EWC*16))*E-13 | (RST+(EWC*16))*E | (RST+(EWC*16))*E+13 | ns |
| 11 | t _d (EMWAITH-EMOEH) | Delay time from EM_WAITx deasserted to $\overline{\text{EM_OE}}$ high | 4E-13 | 4E | 4E+13 | ns |
| WRITES | | | | | | |
| 15 | t _c (EMWCYCLE) | EMIF write cycle time (EW = 0) | (WS+WST+WH)*E-13 | (WS+WST+WH)*E | (WS+WST+WH)*E+13 | ns |
| | | EMIF write cycle time (EW = 1) | (WS+WST+WH+(EWC*16))*E - 13 | (WS+WST+WH+(EWC*16))*E | (WS+WST+WH+(EWC*16))*E + 13 | ns |
| 16 | t _{su} (EMCSL-EMWEL) | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_WE}}$ low (SS = 0) | (WS)*E - 13 | (WS)*E | (WS)*E + 13 | ns |
| | | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_WE}}$ low (SS = 1) | -13 | 0 | +13 | ns |
| 17 | t _h (EMWEH-EMCSH) | Output hold time, $\overline{\text{EM_WE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 0) | (WH)*E-13 | (WH)*E | (WH)*E+13 | ns |
| | | Output hold time, $\overline{\text{EM_WE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 1) | -13 | 0 | +13 | ns |
| 18 | t _{su} (EMBAV-EMWEL) | Output setup time, EM_BA[1:0] valid to $\overline{\text{EM_WE}}$ low | (WS)*E-13 | (WS)*E | (WS)*E+13 | ns |
| 19 | t _h (EMWEH-EMBAIV) | Output hold time, $\overline{\text{EM_WE}}$ high to EM_BA[1:0] invalid | (WH)*E-13 | (WH)*E | (WH)*E+13 | ns |
| 20 | t _{su} (EMAV-EMWEL) | Output setup time, EM_A[20:0] valid to $\overline{\text{EM_WE}}$ low | (WS)*E-13 | (WS)*E | (WS)*E+13 | ns |
| 21 | t _h (EMWEH-EMAIV) | Output hold time, $\overline{\text{EM_WE}}$ high to EM_A[20:0] invalid | (WH)*E-13 | (WH)*E | (WH)*E+13 | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.

(3) E = SYSCLK period in ns. For example, when SYSCLK is set to 100/120 MHz, E = 10/8.33 ns, respectively.

(4) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 5-15. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory^{(1)(2) (3)} (see [Figure 5-19](#) and [Figure 5-21](#))⁽⁴⁾ (continued)

| NO. | PARAMETER | | $CV_{DD} = 1.05\text{ V}$ $DV_{DDEMIF} = 3.3/2.75/2.5/1.8\text{ V}$ | | | UNIT |
|-----|------------------------|--|--|------------------|---------------------|------|
| | | | MIN | NOM | MAX | |
| 22 | $t_{w(EMWEL)}$ | $\overline{EM_WE}$ active low width (EW = 0) | (WST)*E-13 | (WST)*E | (WST)*E+13 | ns |
| | | $\overline{EM_WE}$ active low width (EW = 1) | (WST+(EWC*16))*E-13 | (WST+(EWC*16))*E | (WST+(EWC*16))*E+13 | ns |
| 23 | $t_{d(EMWAITH-EMWEH)}$ | Delay time from EM_WAITx deasserted to $\overline{EM_WE}$ high | 3E-13 | 4E | 4E+13 | ns |
| 24 | $t_{su(EMDV-EMWEL)}$ | Output setup time, EM_D[15:0] valid to $\overline{EM_WE}$ low | (WS)*E-13 | (WS)*E | (WS)*E+13 | ns |
| 25 | $t_{h(EMWEH-EMDIV)}$ | Output hold time, $\overline{EM_WE}$ high to EM_D[15:0] invalid | (WH)*E-13 | (WH)*E | (WH)*E+13 | ns |

5.9.5 EMIF Electrical Data/Timing $CV_{DD} = 1.3\text{ V}$, $DV_{DDEMIF} = 3.3/2.75/2.5/1.8\text{ V}$, External Loading = 10 pF

Table 5-16. Timing Requirements for EMIF SDRAM/mSDRAM Interface⁽¹⁾ (see [Figure 5-16](#) and [Figure 5-17](#))

| NO. | | | $CV_{DD} = 1.3\text{ V}$ $DV_{DDEMIF} = 3.3/2.75/2.5\text{ V}$ | | $CV_{DD} = 1.3\text{ V}$ $DV_{DDEMIF} = 1.8\text{ V}$ | | UNIT |
|-----|-------------------|--|---|-----|--|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 19 | $t_{su}(DV-CLKH)$ | Input setup time, read data valid on EM_D[15:0] before EM_SDCLK rising | 3.4 | | 3.4 | | ns |
| 20 | $t_h(CLKH-DIV)$ | Input hold time, read data valid on EM_D[15:0] after EM_SDCLK rising | 1.2 | | 1.2 | | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

Table 5-17. Switching Characteristics Over Recommended Operating Conditions for EMIF SDRAM/mSDRAM Interface⁽¹⁾⁽²⁾ (see [Figure 5-16](#) and [Figure 5-17](#))

| NO. | PARAMETER | $CV_{DD} = 1.3\text{ V}$ $DV_{DDEMIF} = 3.3/2.75/2.5\text{ V}$ | | | $CV_{DD} = 1.3\text{ V}$ $DV_{DDEMIF} = 1.8\text{ V}$ | | | UNIT |
|-----|------------------|---|-----|-----|--|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| 1 | $t_{c(CLK)}$ | 10 ⁽³⁾ | | | 20 ⁽⁴⁾ | | | ns |
| 2 | $t_{w(CLK)}$ | 5 | | | 10 | | | ns |
| 3 | $t_d(CLKH-CSV)$ | Delay time, EM_SDCLK rising to EMA_CS[1:0] valid | | | 1.1 | | | ns |
| 5 | $t_d(CLKH-DQMV)$ | Delay time, EM_SDCLK rising to EM_DQM[1:0] valid | | | 1.1 | | | ns |
| 7 | $t_d(CLKH-AV)$ | Delay time, EM_SDCLK rising to EM_A[20:0] and EM_BA[1:0] valid | | | 1.1 | | | ns |
| 9 | $t_d(CLKH-DV)$ | Delay time, EM_SDCLK rising to EM_D[15:0] valid | | | 1.1 | | | ns |
| 11 | $t_d(CLKH-RASV)$ | Delay time, EM_SDCLK rising to $\overline{EM_SDRAS}$ valid | | | 1.1 | | | ns |
| 13 | $t_d(CLKH-CASV)$ | Delay time, EM_SDCLK rising to $\overline{EM_SDCAS}$ valid | | | 1.1 | | | ns |
| 15 | $t_d(CLKH-WEV)$ | Delay time, EM_SDCLK rising to $\overline{EM_WE}$ valid | | | 1.1 | | | ns |
| 21 | $t_d(CLKH-CKEV)$ | Delay time, EM_SDCLK rising to EM_SDCKE valid | | | 1.1 | | | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 60 or 100 MHz, E = 16.67 or 10 ns, respectively. For more detail on the EM_SDCLK speed see [Section 5.9.2](#), *EMIF Non-Mobile and Mobile Synchronous DRAM Memory Supported*.

(3) When $CV_{DD} = 1.3\text{ V}$, and $DV_{DDEMIF} = 3.3\text{ V}$, 2.75 V or 2.5 V, the max clock frequency on the EM_SDCLK pin is limited to 100 MHz (EM_SDCLK = 100 MHz). For more information, see *TMS320C5515/14/05/04 DSP External Memory Interface (EMIF) User's Guide* (literature number [SPRUGU6](#)).

(4) When $DV_{DDEMIF} = 1.8\text{ V}$, the max clock frequency on the EM_SDCLK pin is limited to 50 MHz (EM_SDCLK = 50 MHz). For more information, see *TMS320C5515/14/05/04 DSP External Memory Interface (EMIF) User's Guide* (literature number [SPRUGU6](#)).

Table 5-18. Timing Requirements for EMIF Asynchronous Memory⁽¹⁾⁽²⁾ (see [Figure 5-18](#), [Figure 5-20](#), and [Figure 5-21](#))

| NO. | | | CV _{DD} = 1.3 V DV _{DDEMIF} = 3.3/2.75/2.5/1.8 V | | | UNIT |
|------------------|---|---|---|-----|-----|------|
| | | | MIN | NOM | MAX | |
| READS and WRITES | | | | | | |
| 2 | t _w (EM_WAIT) | Pulse duration, EM_WAITx assertion and deassertion | 2E | | | ns |
| READS | | | | | | |
| 12 | t _{su} (EMDV-EMOE _H) | Setup time, EM_D[15:0] valid before $\overline{\text{EM_OE}}$ high | 11 | | | ns |
| 13 | t _h (EMOE _H -EMDIV) | Hold time, EM_D[15:0] valid after $\overline{\text{EM_OE}}$ high | 0 | | | ns |
| 14 | t _{su} (EMOEL-EMWAIT) | Setup Time, EM_WAITx asserted before end of Strobe Phase ⁽³⁾ | 4E + 7.5 | | | ns |
| WRITES | | | | | | |
| 28 | t _{su} (EMWEL-EMWAIT) | Setup Time, EM_WAITx asserted before end of Strobe Phase ⁽³⁾ | 4E + 7.5 | | | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

(2) E = SYSCLK period in ns. For example, when SYSCLK is set to 100/120 MHz, E = 10/8.33 ns, respectively.

(3) Setup before end of STROBE phase (if no extended wait states are inserted) by which EM_WAITx must be asserted to add extended wait states. [Figure 5-20](#) and [Figure 5-21](#) describe EMIF transactions that include extended wait states inserted during the STROBE phase. However, cycles inserted as part of this extended wait period should not be counted; the 4E requirement is to the start of where the HOLD phase would begin if there were no extended wait cycles.

Table 5-19. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory^{(1)(2) (3) (4)} (see [Figure 5-18](#), [Figure 5-20](#), and [Figure 5-21](#))

| NO. | PARAMETER | | CV _{DD} = 1.3 V DV _{DD} EMIF = 3.3/2.75/2.5/1.8 V | | | UNIT |
|------------------|-------------------------------------|--|--|------------------------|------------------------------|------|
| | | | MIN | NOM | MAX | |
| READS and WRITES | | | | | | |
| 1 | t _d (TURNAROUND) | Turn around time | (TA)*E - 7.5 | (TA)*E | (TA)*E + 7.5 | ns |
| READS | | | | | | |
| 3 | t _c (EMRCYCLE) | EMIF read cycle time (EW = 0) | (RS+RST+RH)*E - 7.5 | (RS+RST+RH)*E | (RS+RST+RH)*E + 7.5 | ns |
| | | EMIF read cycle time (EW = 1) | (RS+RST+RH+(EWC*16))*E - 7.5 | (RS+RST+RH+(EWC*16))*E | (RS+RST+RH+(EWC*16))*E + 7.5 | ns |
| 4 | t _{su} (EMCSL-EMOEL) | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_OE}}$ low (SS = 0) | (RS)*E - 7.5 | (RS)*E | (RS)*E + 7.5 | ns |
| | | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_OE}}$ low (SS = 1) | -7.5 | 0 | +7.5 | ns |
| 5 | t _h (EMOE-EMCSH) | Output hold time, $\overline{\text{EM_OE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 0) | (RH)*E - 7.5 | (RH)*E | (RH)*E + 7.5 | ns |
| | | Output hold time, $\overline{\text{EM_OE}}$ high to $\overline{\text{EM_CE}}[5:2]$ high (SS = 1) | -7.5 | 0 | +7.5 | ns |
| 6 | t _{su} (EMBAV-EMOEL) | Output setup time, EM_BA[1:0] valid to $\overline{\text{EM_OE}}$ low | (RS)*E - 7.5 | (RS)*E | (RS)*E + 7.5 | ns |
| 7 | t _h (EMOE-EMBAIV) | Output hold time, $\overline{\text{EM_OE}}$ high to EM_BA[1:0] invalid | (RH)*E - 7.5 | (RH)*E | (RH)*E + 7.5 | ns |
| 8 | t _{su} (EMAV-EMOEL) | Output setup time, EM_A[20:0] valid to $\overline{\text{EM_OE}}$ low | (RS)*E - 7.5 | (RS)*E | (RS)*E + 7.5 | ns |
| 9 | t _h (EMOE-EMAIV) | Output hold time, $\overline{\text{EM_OE}}$ high to EM_A[20:0] invalid | (RH)*E - 7.5 | (RH)*E | (RH)*E + 7.5 | ns |
| 10 | t _w (EMOEL) | $\overline{\text{EM_OE}}$ active low width (EW = 0) | (RST)*E - 7.5 | (RST)*E | (RST)*E + 7.5 | ns |
| | | $\overline{\text{EM_OE}}$ active low width (EW = 1) | (RST+(EWC*16))*E - 7.5 | (RST+(EWC*16))*E | (RST+(EWC*16))*E + 7.5 | ns |
| 11 | t _d (EMWAITH-EMOE-EMOEH) | Delay time from EM_WAITx deasserted to $\overline{\text{EM_OE}}$ high | 4E - 7.5 | 4E | 4E + 7.5 | ns |
| WRITES | | | | | | |
| 15 | t _c (EMWCYCLE) | EMIF write cycle time (EW = 0) | (WS+WST+WH)*E - 7.5 | (WS+WST+WH)*E | (WS+WST+WH)*E + 7.5 | ns |
| | | EMIF write cycle time (EW = 1) | (WS+WST+WH+(EWC*16))*E - 7.5 | (WS+WST+WH+(EWC*16))*E | (WS+WST+WH+(EWC*16))*E + 7.5 | ns |
| 16 | t _{su} (EMCSL-EMWEL) | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_WE}}$ low (SS = 0) | (WS)*E - 7.5 | (WS)*E | (WS)*E + 7.5 | ns |
| | | Output setup time, $\overline{\text{EM_CS}}[5:2]$ low to $\overline{\text{EM_WE}}$ low (SS = 1) | -7.5 | 0 | +7.5 | ns |
| 17 | t _h (EMWEH-EMCSH) | Output hold time, $\overline{\text{EM_WE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 0) | (WH)*E - 7.5 | (WH)*E | (WH)*E + 7.5 | ns |
| | | Output hold time, $\overline{\text{EM_WE}}$ high to $\overline{\text{EM_CS}}[5:2]$ high (SS = 1) | -7.5 | 0 | +7.5 | ns |
| 18 | t _{su} (EMBAV-EMWEL) | Output setup time, EM_BA[1:0] valid to $\overline{\text{EM_WE}}$ low | (WS)*E - 7.5 | (WS)*E | (WS)*E + 7.5 | ns |
| 19 | t _h (EMWEH-EMBAIV) | Output hold time, $\overline{\text{EM_WE}}$ high to EM_BA[1:0] invalid | (WH)*E - 7.5 | (WH)*E | (WH)*E + 7.5 | ns |
| 20 | t _{su} (EMAV-EMWEL) | Output setup time, EM_A[20:0] valid to $\overline{\text{EM_WE}}$ low | (WS)*E - 7.5 | (WS)*E | (WS)*E + 7.5 | ns |
| 21 | t _h (EMWEH-EMAIV) | Output hold time, $\overline{\text{EM_WE}}$ high to EM_A[20:0] invalid | (WH)*E - 7.5 | (WH)*E | (WH)*E + 7.5 | ns |

(1) Timing parameters are obtained with 10pF loading on the EMIF pins.

(2) TA = Turn around, RS = Read setup, RST = Read strobe, RH = Read hold, WS = Write setup, WST = Write strobe, WH = Write hold, MEWC = Maximum external wait cycles. These parameters are programmed via the Asynchronous Configuration and Asynchronous Wait Cycle Configuration Registers.

(3) E = SYSCLK period in ns. For example, when SYSCLK is set to 100/120 MHz, E = 10/8.33 ns, respectively.

(4) EWC = external wait cycles determined by EM_WAITx input signal. EWC supports the following range of values EWC[256-1]. Note that the maximum wait time before timeout is specified by bit field MEWC in the Asynchronous Wait Cycle Configuration Register.

Table 5-19. Switching Characteristics Over Recommended Operating Conditions for EMIF Asynchronous Memory^{(1)(2) (3) (4)} (see Figure 5-18, Figure 5-20, and Figure 5-21) (continued)

| NO. | PARAMETER | | CV _{DD} = 1.3 V DV _{DDEMIF} = 3.3/2.75/2.5/1.8 V | | | UNIT |
|-----|--------------------------------|--|---|------------------|------------------------|------|
| | | | MIN | NOM | MAX | |
| 22 | t _w (EMWEL) | EM_WE active low width (EW = 0) | (WST)*E - 7.5 | (WST)*E | (WST)*E + 7.5 | ns |
| | | EM_WE active low width (EW = 1) | (WST+(EWC*16))*E - 7.5 | (WST+(EWC*16))*E | (WST+(EWC*16))*E + 7.5 | ns |
| 23 | t _d (EMWAITH-EMWEH) | Delay time from EM_WAITx deasserted to EM_WE high | 3E - 7.5 | 4E | 4E + 7.5 | ns |
| 24 | t _{su} (EMDV-EMWEL) | Output setup time, EM_D[15:0] valid to EM_WE low | (WS)*E - 7.5 | (WS)*E | (WS)*E + 7.5 | ns |
| 25 | t _h (EMWEH-EMDIV) | Output hold time, EM_WE high to EM_D[15:0] invalid | (WH)*E - 7.5 | (WH)*E | (WH)*E + 7.5 | ns |

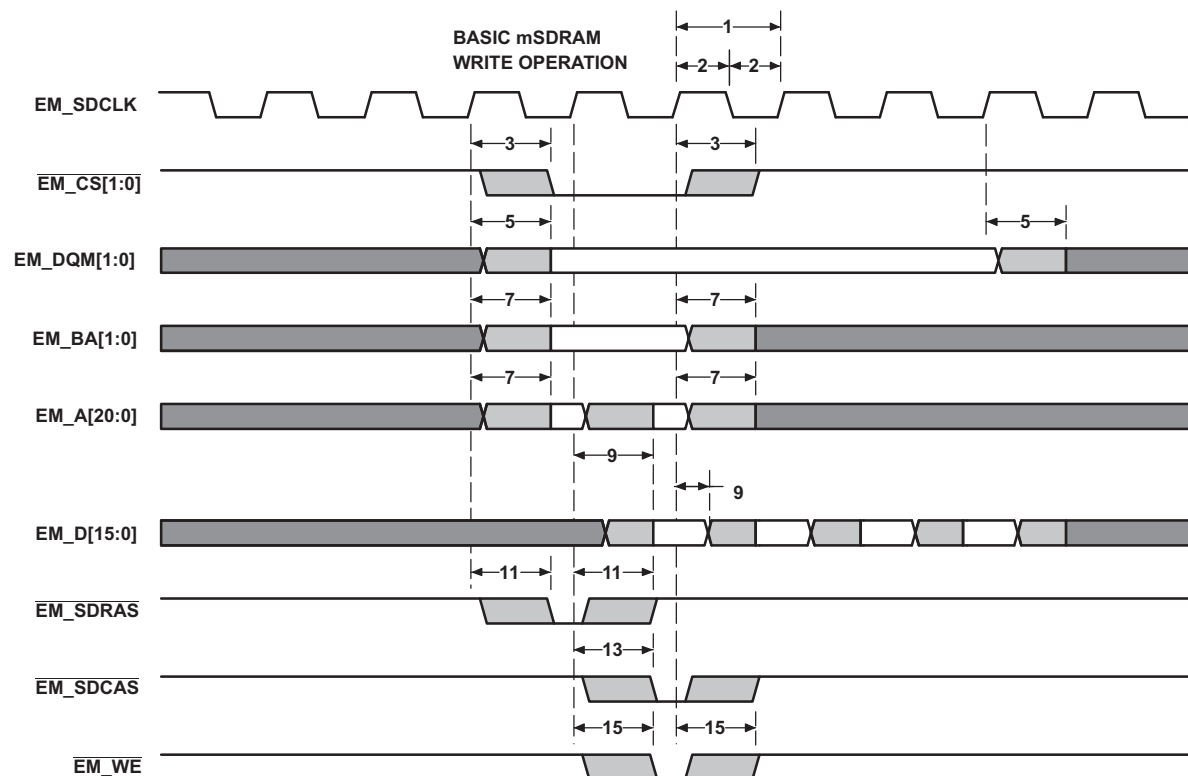


Figure 5-16. EMIF Basic SDRAM/mSDRAM Write Operation

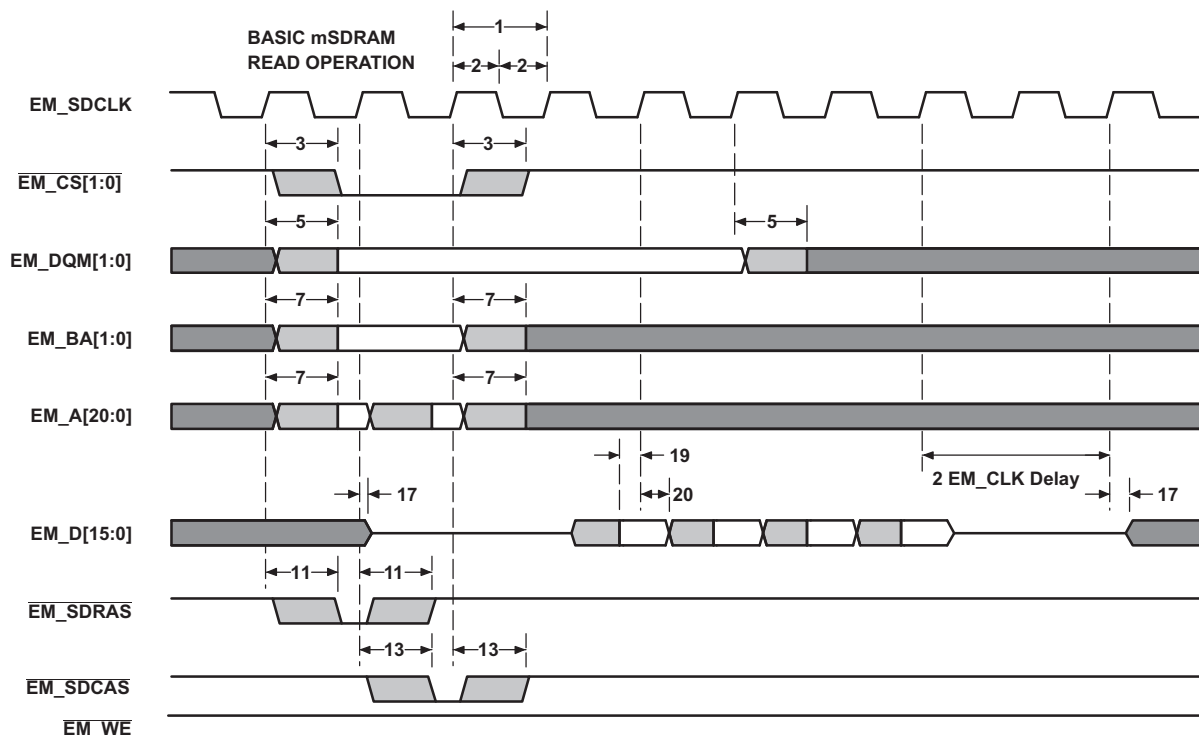


Figure 5-17. EMIF Basic SDRAM/mSDRAM Read Operation

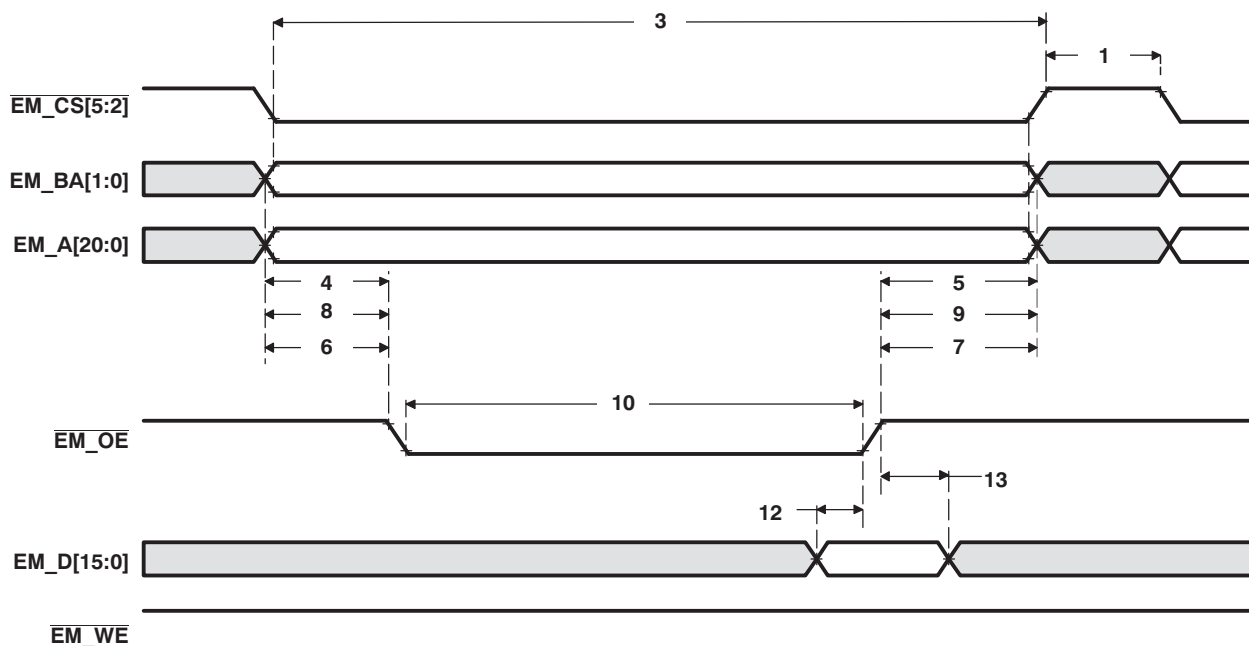


Figure 5-18. Asynchronous Memory Read Timing for EMIF

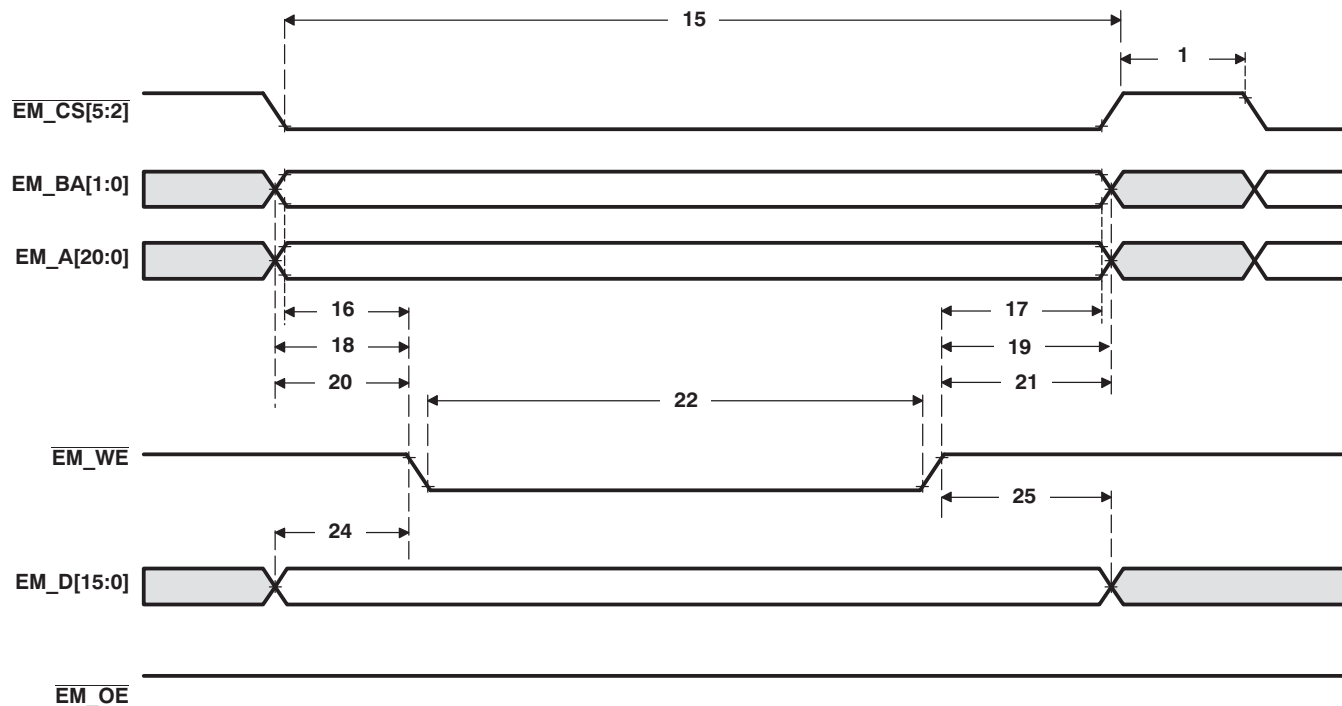


Figure 5-19. Asynchronous Memory Write Timing for EMIF

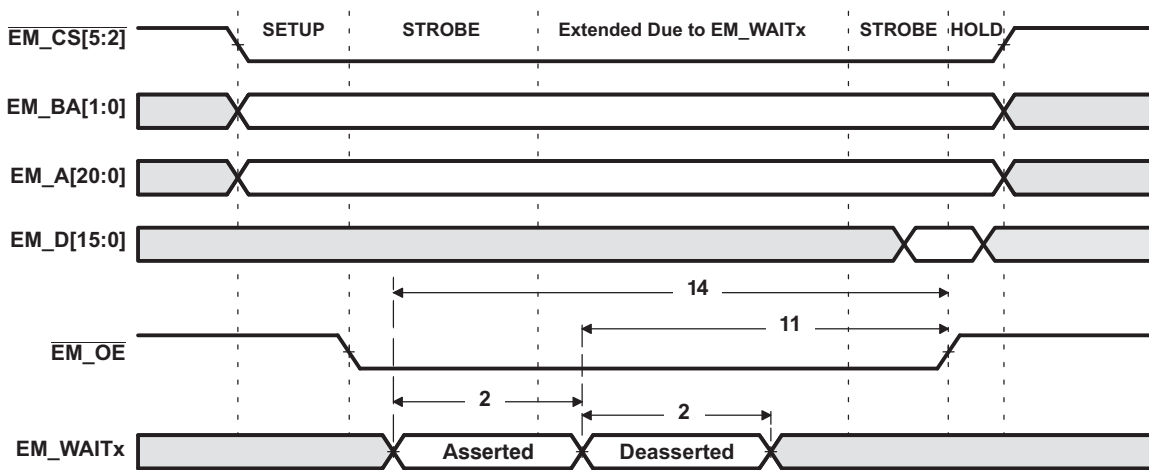


Figure 5-20. EM_WAITx Read Timing Requirements

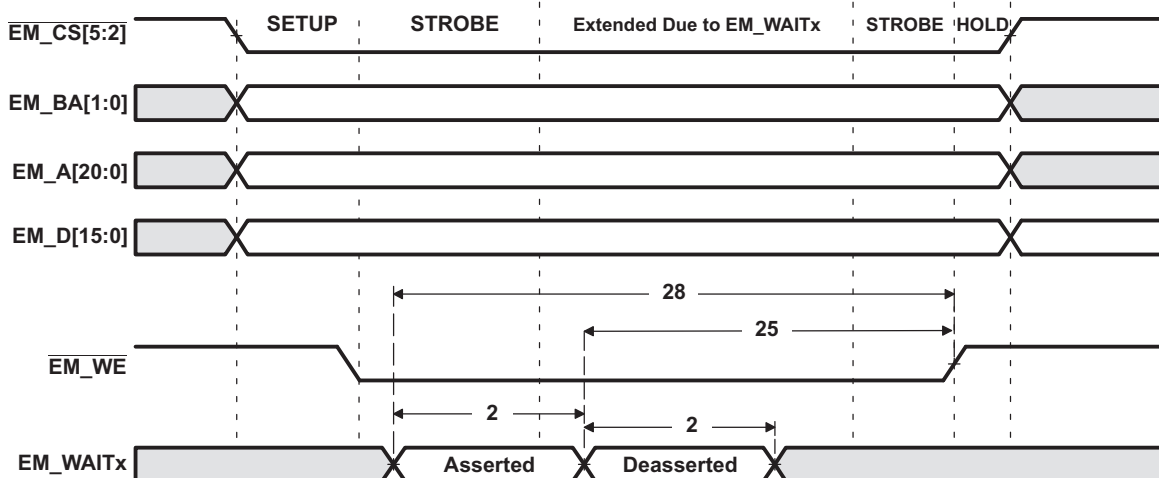


Figure 5-21. EM_WAITx Write Timing Requirements

5.10 Multimedia Card/Secure Digital (MMC/SD)

The device includes two MMC/SD controllers which are compliant with MMC V3.31, Secure Digital Part 1 Physical Layer Specification V2.0, and Secure Digital Input Output (SDIO) V3.3 specifications. The MMC/SD card controller supports these industry standards and assumes the reader is familiar with these standards.

Each MMC/SD Controller in the device has the following features:

- Multimedia Card/Secure Digital (MMC/SD) protocol support
- Programmable clock frequency
- 512 bit Read/Write FIFO to lower system overhead
- Slave DMA transfer capability

The MMC/SD card controller transfers data between the CPU and DMA controller on one side and MMC/SD card on the other side. The CPU and DMA controller can read/write the data in the card by accessing the registers in the MMC/SD controller.

The MMC/SD controller on this device, does not support the SPI mode of operation.

5.10.1 MMC/SD Peripheral Register Descriptions

[Table 5-20](#) and [Table 5-21](#) show the MMC/SD registers. The MMC/SD0 registers start at address 0x3A00 and the MMC/SD1 registers start at address 0x3B00.

Table 5-20. MMC/SD0 Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|----------------------|------------|---------------------------------------|
| 3A00h | MMCCTL | MMC Control Register |
| 3A04h | MMCCLK | MMC Memory Clock Control Register |
| 3A08h | MMCST0 | MMC Status Register 0 |
| 3A0Ch | MMCST1 | MMC Status Register 1 |
| 3A10h | MMCIM | MMC Interrupt Mask Register |
| 3A14h | MMCTOR | MMC Response Time-Out Register |
| 3A18h | MMCTOD | MMC Data Read Time-Out Register |
| 3A1Ch | MMCBLEN | MMC Block Length Register |
| 3A20h | MMCNBLK | MMC Number of Blocks Register |
| 3A24h | MMCNBLC | MMC Number of Blocks Counter Register |
| 3A28h | MMCDRR1 | MMC Data Receive 1 Register |
| 3A29h | MMCDRR2 | MMC Data Receive 2 Register |
| 3A2Ch | MMCDXR1 | MMC Data Transmit 1 Register |
| 3A2Dh | MMCDXR2 | MMC Data Transmit 2 Register |
| 3A30h | MMCCMD | MMC Command Register |
| 3A34h | MMCARGHL | MMC Argument Register |
| 3A38h | MMCRSP0 | MMC Response Register 0 |
| 3A39h | MMCRSP1 | MMC Response Register 1 |
| 3A3Ch | MMCRSP2 | MMC Response Register 2 |
| 3A3Dh | MMCRSP3 | MMC Response Register 3 |
| 3A40h | MMCRSP4 | MMC Response Register 4 |
| 3A41h | MMCRSP5 | MMC Response Register 5 |
| 3A44h | MMCRSP6 | MMC Response Register 6 |
| 3A45h | MMCRSP7 | MMC Response Register 7 |
| 3A48h | MMCDRSP | MMC Data Response Register |
| 3A50h | MMCCIDX | MMC Command Index Register |
| 3A64h – 3A70h | – | Reserved |
| 3A74h | MMCFIFOCTL | MMC FIFO Control Register |

Table 5-21. MMC/SD1 Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|------------|---------------------------------------|
| 3B00h | MMCCTL | MMC Control Register |
| 3B04h | MMCCLK | MMC Memory Clock Control Register |
| 3B08h | MMCST0 | MMC Status Register 0 |
| 3B0Ch | MMCST1 | MMC Status Register 1 |
| 3B10h | MMCIM | MMC Interrupt Mask Register |
| 3B14h | MMCTOR | MMC Response Time-Out Register |
| 3B18h | MMCTOD | MMC Data Read Time-Out Register |
| 3B1Ch | MMCBLEN | MMC Block Length Register |
| 3B20h | MMCNBLK | MMC Number of Blocks Register |
| 3B24h | MMCNBLC | MMC Number of Blocks Counter Register |
| 3B28h | MMCDRR1 | MMC Data Receive 1 Register |
| 3B29h | MMCDRR2 | MMC Data Receive 2 Register |
| 3B2Ch | MMCDXR1 | MMC Data Transmit 1 Register |
| 3B2Dh | MMCDXR2 | MMC Data Transmit 2 Register |
| 3B30h | MMCCMD | MMC Command Register |
| 3B34h | MMCARGHL | MMC Argument Register |
| 3B38h | MMCRSP0 | MMC Response Register 0 |
| 3B39h | MMCRSP1 | MMC Response Register 1 |
| 3B3Ch | MMCRSP2 | MMC Response Register 2 |
| 3B3Dh | MMCRSP3 | MMC Response Register 3 |
| 3B40h | MMCRSP4 | MMC Response Register 4 |
| 3B41h | MMCRSP5 | MMC Response Register 5 |
| 3B44h | MMCRSP6 | MMC Response Register 6 |
| 3B45h | MMCRSP7 | MMC Response Register 7 |
| 3B48h | MMCDRSP | MMC Data Response Register |
| 3B50h | MMCCIDX | MMC Command Index Register |
| 3B74h | MMCFIFOCTL | MMC FIFO Control Register |

5.10.2 MMC/SD Electrical Data/Timing

Table 5-22. Timing Requirements for MMC/SD (see Figure 5-22 and Figure 5-25)

| NO . | | CV _{DD} = 1.3 V | | CV _{DD} = 1.05 V | | UNIT |
|---------|--|--------------------------|-----|---------------------------|-----|------|
| | | FAST MODE | | STD MODE | | |
| | | MIN | MAX | MIN | MAX | |
| 1 | t _{su} (CMDV-CLKH) Setup time, MMCx_CMD data input valid before MMCx_CLK high | 3 | | 3 | | ns |
| 2 | t _h (CLKH-CMDV) Hold time, MMCx_CMD data input valid after MMCx_CLK high | 3 | | 3 | | ns |
| 3 | t _{su} (DATV-CLKH) Setup time, MMC_Dx data input valid before MMCx_CLK high | 3 | | 3 | | ns |
| 4 | t _h (CLKH-DATV) Hold time, MMC_Dx data input valid after MMCx_CLK high | 3 | | 3 | | ns |

Table 5-23. Switching Characteristics Over Recommended Operating Conditions for MMC Output⁽¹⁾ (see Figure 5-22 and Figure 5-25)

| NO | PARAMETER | | CV _{DD} = 1.3 V | | CV _{DD} = 1.05 V | | UNIT |
|----|-------------------------------|---|--------------------------|-------------------|---------------------------|-------------------|------|
| | | | FAST MODE | | STD MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 7 | f _(CLK) | Operating frequency, MMCx_CLK | 0 | 50 ⁽²⁾ | 0 | 25 ⁽²⁾ | MHz |
| 8 | f _(CLK_ID) | Identification mode frequency, MMCx_CLK | 0 | 400 | 0 | 400 | kHz |
| 9 | t _w (CLKL) | Pulse width, MMCx_CLK low | 7 | | 10 | | ns |
| 10 | t _w (CLKH) | Pulse width, MMCx_CLK high | 7 | | 10 | | ns |
| 11 | t _r (CLK) | Rise time, MMCx_CLK | | 3 | | 3 | ns |
| 12 | t _f (CLK) | Fall time, MMCx_CLK | | 3 | | 3 | ns |
| 13 | t _d (MDCLKL-CMDIV) | Delay time, MMCx_CLK low to MMC_CMD data output invalid | -4 | | -4.1 | | ns |
| 14 | t _d (MDCLKL-CMDV) | Delay time, MMCx_CLK low to MMC_CMD data output valid | | 4 | | 5.1 | ns |
| 15 | t _d (MDCLKL-DATIV) | Delay time, MMCx_CLK low to MMC_Dx data output invalid | -4 | | -4.1 | | ns |
| 16 | t _d (MDCLKL-DATV) | Delay time, MMCx_CLK low to MMC_Dx data output valid | | 4 | | 5.1 | ns |

(1) For MMC/SD, the parametric values are measured at DV_{DDIO} = 3.3 V and 2.75 V.

(2) Use this value or SYS_CLK/2 whichever is smaller.

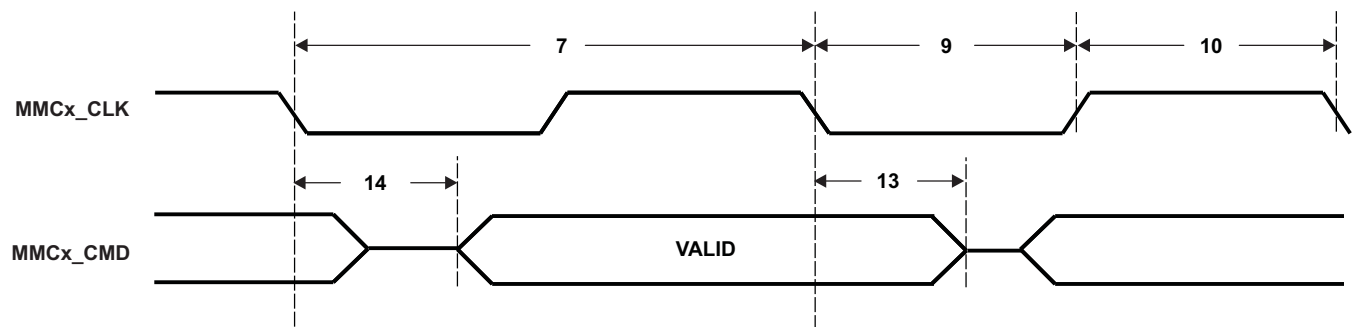


Figure 5-22. MMC/SD Host Command Write Timing

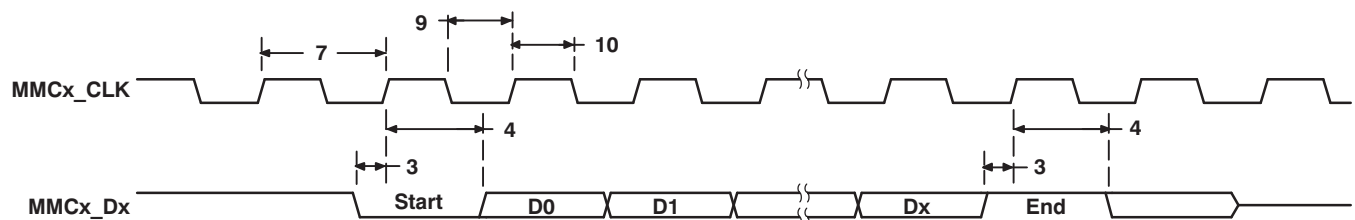


Figure 5-23. MMC/SD Card Response Timing

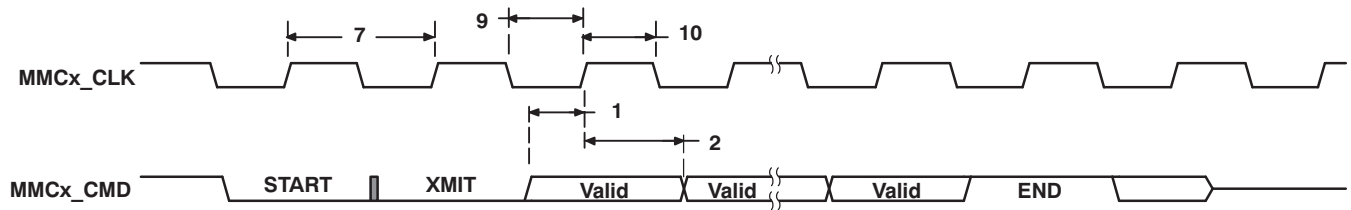


Figure 5-24. MMC/SD Host Write Timing

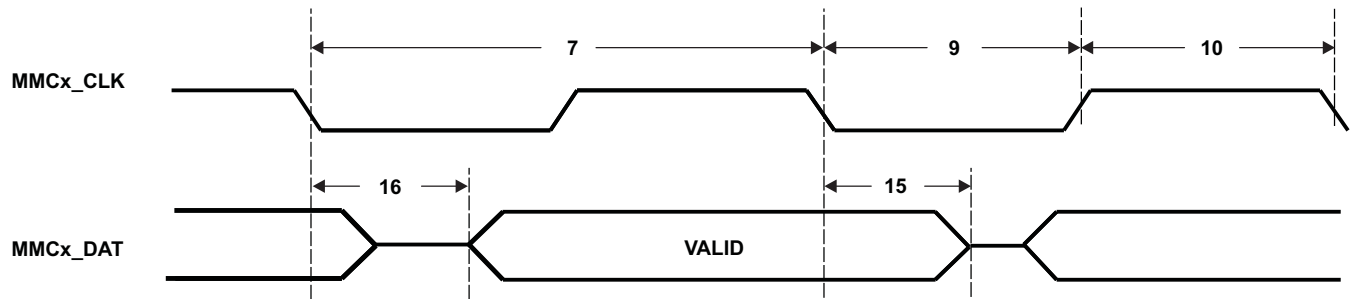


Figure 5-25. MMC/SD Data Write Timing

5.11 Real-Time Clock (RTC)

The device includes a Real-Time Clock (RTC) with its own separated power supply and isolation circuits. The separate supply and isolation circuits allow the RTC to run with the least possible power consumption, called RTC only mode. The RTC only mode requires CV_{DDRTC} , LDO1, and DV_{DDRTC} power domains to be powered, but other power domains can be shut off. See [Section 5.11.1, RTC Only Mode](#) for details. All RTC registers are preserved (except for RTC Control and RTC Update Registers) and the counter continues to operate when the device is powered off. The RTC also has the capability to wakeup the device from idle states via alarms, periodic interrupts, or an external WAKEUP input. Additionally, the RTC is able to output an alarm or periodic interrupt on the WAKEUP pin to cause external power management to re-enable power to the DSP Core and I/O. **Note:** The RTC Core (CV_{DDRTC}) must be powered by an external power source even though RTC is not used. None of the on-chip LDOs can power CV_{DDRTC} .

The device RTC provides the following features:

- 100-year calendar up to year 2099.
- Counts seconds, minutes, hours, day of the week, date, month, and year with leap year compensation
- Millisecond time correction
- Binary-coded-decimal (BCD) representation of time, calendar, and alarm
- 24-hour clock mode
- Second, minute, hour, day, or week alarm interrupt
- Periodic interrupt: every millisecond, second, minute, hour, or day
- Alarm interrupt: precise time of day
- Single interrupt to the DSP CPU
- 32.768-kHz crystal oscillator with frequency calibration

Control of the RTC is maintained through a set of I/O memory mapped registers (see [Table 5-25](#)). Note that any write to these registers will be synchronized to the RTC 32.768-KHz clock; thus, the CPU must run at least 3X faster than the RTC. Writes to these registers will not be evident until the next two 32.768-KHz clock cycles later. Furthermore, if the RTC Oscillator is disabled, no RTC register can be written to.

The RTC has its own power-on-reset (POR) circuit which resets the registers in the RTC core domain when power is first applied to the CV_{DDRTC} power pin. The RTC flops are not reset by the device's \overline{RESET} pin nor the digital core's POR (powergood signal).

The scratch registers in the RTC can be used to take advantage of this unique reset domain to keep track of when the DSP boots and whether the RTC time registers have already been initialized to the current clock time or whether the software needs to go into a routine to prompt the user to set the time/date.

5.11.1 RTC Only Mode

The maximum power saving can be achieved by using the RTC only mode. There are hardware and software requirements to use the RTC only mode.

Hardware Requirements:

- The $\overline{DSP_LDO_EN}$ pin must be tied to GND or pulled down to GND.
- The RTC Core (CV_{DDRTC}), RTC I/O (DV_{DDRTC}), and LDO inputs (LDO1) must always be powered.
- VDDA_ANA is recommended to be powered from the ANA_LDOO pin. If VDDA_ANA is powered externally, then it must always be powered.
- All other power domains can be totally shut down during the RTC only mode.
- A high pulse for a minimum of one RTC clock period (30.5 μ s) to the WAKEUP pin is required to wake up the device from the RTC only mode.

Power Down Sequence:

1. CPU must set the LDO_PD bit or the BG_PD bit in the RTCPMGT register (See [Figure 5-26](#)). Once the LDO_PD bit or the BG_PD bit is set to 1, the DSP_LDOO will be internally shut off and it will cause the internal POR holds the internal POWERGOOD signal low, which creates isolation for RTC.
2. All of the device power domains can be shut down except RTC Core (CVDDRTC), RTC I/O (DVDDRTC), and LDO inputs (LDOI).

Wake-Up Sequence:

1. When waking up the device, all power domains must be turned back on before or upon applying a pulse to WAKEUP.
2. A pulse ($\geq 30.5 \mu\text{s}$) must be applied to the WAKEUP pin (active high). When the WAKEUP pin is asserted, the voltage on the DSP_LDOO pin will start ramping up at the positive level of WAKEUP and it is monitored by the internal POR. Until the voltage reaches to the threshold level, the internal POR will hold the internal POWERGOOD signal low, which provides isolation to RTC during transition period. Once the voltage reaches to the threshold level, the internal POR asserts the internal POWERGOOD signal (logic level high) and it resets reset of the system and disables RTC isolation and enables CPU to communicate with RTC.

Figure 5-26. RTC Power Management Register (RTCPMGT) [1930h]

| | | | | | | |
|----------|---|---------|--------|-------|--------------------|---|
| 15 | | | | | | 8 |
| Reserved | | | | | | |
| R-0 | | | | | | |
| 7 | 5 | 4 | 3 | 2 | 1 0 | |
| Reserved | | WU_DOUT | WU_DIR | BG_PD | LDO_PD RTCCLKOUTEN | |
| R-0 | | R/W-1 | R/W-0 | R/W-0 | R/W-0 R/W-0 | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5-24. RTCPMGT Register Bit Descriptions

| BIT | NAME | DESCRIPTION |
|------|----------|--|
| 15:5 | RESERVED | Reserved. Read-only, writes have no effect. |
| 4 | WU_DOUT | Wakeup output, active low/open-drain. 0 = WAKEUP pin driven low. 1 = WAKEUP pin is in high-impedance (Hi-Z). |
| 3 | WU_DIR | Wakeup pin direction control. 0 = WAKEUP pin configured as an input. 1 = WAKEUP pin configured as an output. Note: When the WAKEUP pin is configured as an input, it is active high. When the WAKEUP pin is configured as an output, is an open-drain that is active low and should be externally pulled-up via a 10-k Ω resistor to DV _{DDRTC} . WU_DIR must be configured as an input to allow the WAKEUP pin to wake the device up from idle modes. |
| 2 | BG_PD | Bandgap, on-chip LDOs, and the analog POR power down bit. This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO), the Analog POR, and Bandgap reference. BG_PD and LDO_PD are only intended to be used when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and not used then the BG_PD and LDO_PD power down mechanisms should not be used since POR gets powered down and the POWERGOOD signal is not generated properly. After this bit is asserted, the on-chip LDOs, Analog POR, and the Bandgap reference can be re-enabled by the WAKEUP pin (high) or the RTC alarm interrupt. The Bandgap circuit will take about 100 msec to charge the external 0.1 μF capacitor via the internal 326-k Ω resistor. 0 = On-chip LDOs, Analog POR, and Bandgap reference are enabled. 1 = On-chip LDOs, Analog POR, and Bandgap reference are disabled (shutdown). |

Table 5-24. RTCPMGT Register Bit Descriptions (continued)

| BIT | NAME | DESCRIPTION |
|-----|-------------|---|
| 1 | LDO_PD | <p>On-chip LDOs and Analog POR power down bit.</p> <p>This bit shuts down the on-chip LDOs (ANA_LDO, DSP_LDO, and USB_LDO) and the Analog POR. BG_PD and LDO_PD are only intended to be used when the internal LDOs supply power to the chip. If the internal LDOs are bypassed and not used then the BG_PD and LDO_PD power down mechanisms should not be used since POR gets powered down and the POWERGOOD signal is not generated properly.</p> <p>After this bit is asserted, the on-chip LDOs and Analog POR can be re-enabled by the WAKEUP pin (high) or the RTC alarm interrupt. This bit keeps the Bandgap reference turned on to allow a faster wake-up time with the expense power consumption of the Bandgap reference.</p> <p>0 = On-chip LDOs and Analog POR are enabled. 1 = On-chip LDOs and Analog POR are disabled (shutdown).</p> |
| 0 | RTCCLKOUTEN | <p>Clockout output enable bit.</p> <p>0 = Clock output disabled. 1 = Clock output enabled.</p> |

5.11.2 RTC Peripheral Register Descriptions

Table 5-25 shows the RTC registers.

Table 5-25. Real-Time Clock (RTC) Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|----------------------|-----------|--------------------------------|
| 1900h | RTCINTEN | RTC Interrupt Enable Register |
| 1901h | RTCUPDATE | RTC Update Register |
| 1904h | RTCMIL | Milliseconds Register |
| 1905h | RTCMILA | Milliseconds Alarm Register |
| 1908h | RTCSEC | Seconds Register |
| 1909h | RTCSECA | Seconds Alarm Register |
| 190Ch | RTCMIN | Minutes Register |
| 190Dh | RTCMINA | Minutes Alarm Register |
| 1910h | RTCHOUR | Hours Register |
| 1911h | RTCHOURA | Hours Alarm Register |
| 1914h | RTCDAY | Days Register |
| 1915h | RTCDAYA | Days Alarm Register |
| 1918h | RTCMONTH | Months Register |
| 1919h | RTCMONTHA | Months Alarm Register |
| 191Ch | RTCYEAR | Years Register |
| 191Dh | RTCYEARA | Years Alarm Register |
| 1920h | RTCINTFL | RTC Interrupt Flag Register |
| 1921h | RTCNOPWR | RTC Lost Power Status Register |
| 1924h | RTCINTREG | RTC Interrupt Register |
| 1928h | RTCDRIFT | RTC Compensation Register |
| 192Ch | RTCOSC | RTC Oscillator Register |
| 1930h | RTCPMGT | RTC Power Management Register |
| 1960h | RTCSCR1 | RTC LSW Scratch Register 1 |
| 1961h | RTCSCR2 | RTC MSW Scratch Register 2 |
| 1964h | RTCSCR3 | RTC LSW Scratch Register 3 |
| 1965h | RTCSCR4 | RTC MSW Scratch Register 4 |

5.11.2.1 RTC Electrical Data/Timing

For more detailed information on RTC electrical timings, specifically WAKEUP, see the [Section 5.7.3](#), *Reset Electrical Data/Timing*.

5.12 Inter-Integrated Circuit (I2C)

The inter-integrated circuit (I2C) module provides an interface between the device and other devices compliant with Philips Semiconductors Inter-IC bus (I²C-bus™) specification version 2.1. External components attached to this 2-wire serial bus can transmit/receive 2 to 8-bit data to/from the DSP through the I2C module. The I2C port *does not* support CBUS compatible devices.

The I2C port supports the following features:

- Compatible with Philips I2C Specification Revision 2.1 (January 2000)
- Data Transfer Rate from 10 kbps to 400 kbps (Philips Fast-Mode Rate)
- Noise Filter to Remove Noise 50 ns or Less
- Seven- and Ten-Bit Device Addressing Modes
- Master (Transmit/Receive) and Slave (Transmit/Receive) Functionality
- One Read DMA Event and One Write DMA Event, which can be used by the DMA Controller
- One Interrupt that can be used by the CPU
- Slew-Rate Limited Open-Drain Output Buffers

The I2C module clock must be in the range from 6.7 MHz to 13.3 MHz. This is necessary for proper operation of the I2C module. With the I2C module clock in this range, the noise filters on the SDA and SCL pins suppress noise that has a duration of 50 ns or shorter. The I2C module clock is derived from the DSP clock divided by a programmable prescaler.

5.12.1 I2C Peripheral Register Descriptions

Table 5-26 shows the Inter-Integrated Circuit (I2C) registers.

Table 5-26. Inter-Integrated Circuit (I2C) Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|----------------------|---------|--|
| 1A00h | ICOAR | I2C Own Address Register |
| 1A04h | ICIMR | I2C Interrupt Mask Register |
| 1A08h | ICSTR | I2C Interrupt Status Register |
| 1A0Ch | ICCLKL | I2C Clock Low-Time Divider Register |
| 1A10h | ICCLKH | I2C Clock High-Time Divider Register |
| 1A14h | ICCNT | I2C Data Count Register |
| 1A18h | ICDRR | I2C Data Receive Register |
| 1A1Ch | ICSAR | I2C Slave Address Register |
| 1A20h | ICDXR | I2C Data Transmit Register |
| 1A24h | ICMDR | I2C Mode Register |
| 1A28h | ICIVR | I2C Interrupt Vector Register |
| 1A2Ch | ICEMDR | I2C Extended Mode Register |
| 1A30h | ICPSC | I2C Prescaler Register |
| 1A34h | ICPID1 | I2C Peripheral Identification Register 1 |
| 1A38h | ICPID2 | I2C Peripheral Identification Register 2 |

5.12.2 I²C Electrical Data/Timing

Table 5-27. Timing Requirements for I²C Timings⁽¹⁾ (see Figure 5-27)

| NO. | | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | | | UNIT |
|-----|-------------------------------|---|---|-----|---------------------------------------|--------------------|------|
| | | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | t _c (SCL) | Cycle time, SCL | 10 | | 2.5 | | μs |
| 2 | t _{su} (SCLH-SDAL) | Setup time, SCL high before SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μs |
| 3 | t _h (SCLL-SDAL) | Hold time, SCL low after SDA low (for a START and a repeated START condition) | 4 | | 0.6 | | μs |
| 4 | t _w (SCLL) | Pulse duration, SCL low | 4.7 | | 1.3 | | μs |
| 5 | t _w (SCLH) | Pulse duration, SCL high | 4 | | 0.6 | | μs |
| 6 | t _{su} (SDAV-SCLH) | Setup time, SDA valid before SCL high | 250 | | 100 ⁽²⁾ | | ns |
| 7 | t _h (SDA-SCLL) | Hold time, SDA valid after SCL low | 0 ⁽³⁾ | | 0 ⁽³⁾ | 0.9 ⁽⁴⁾ | μs |
| 8 | t _w (SDAH) | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μs |
| 9 | t _r (SDA) | Rise time, SDA ⁽⁵⁾ | 1000 | | 20 + 0.1C _b ⁽⁶⁾ | 300 | ns |
| 10 | t _r (SCL) | Rise time, SCL ⁽⁵⁾ | 1000 | | 20 + 0.1C _b ⁽⁶⁾ | 300 | ns |
| 11 | t _f (SDA) | Fall time, SDA ⁽⁵⁾ | 300 | | 20 + 0.1C _b ⁽⁶⁾ | 300 | ns |
| 12 | t _f (SCL) | Fall time, SCL ⁽⁵⁾ | 300 | | 20 + 0.1C _b ⁽⁶⁾ | 300 | ns |
| 13 | t _{su} (SCLH-SDAH) | Setup time, SCL high before SDA high (for STOP condition) | 4 | | 0.6 | | μs |
| 14 | t _w (SP) | Pulse duration, spike (must be suppressed) | | | 0 | 50 | ns |
| 15 | C _b ⁽⁶⁾ | Capacitive load for each bus line | 400 | | | 400 | pF |

- (1) The I²C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down. Also these pins are not 3.6 V-tolerant (their V_{IH} cannot go above DV_{DDIO} + 0.3 V).
- (2) A Fast-mode I²C-bus™ device can be used in a Standard-mode I²C-bus system, but the requirement t_{su}(SDA-SCLH) ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r max + t_{su}(SDA-SCLH) = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-Bus Specification) before the SCL line is released.
- (3) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- (4) The maximum t_h(SDA-SCLL) has only to be met if the device does not stretch the low period [t_w(SCLL)] of the SCL signal.
- (5) The rise/fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. However, the rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I²C rise and fall time values specified.
- (6) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.

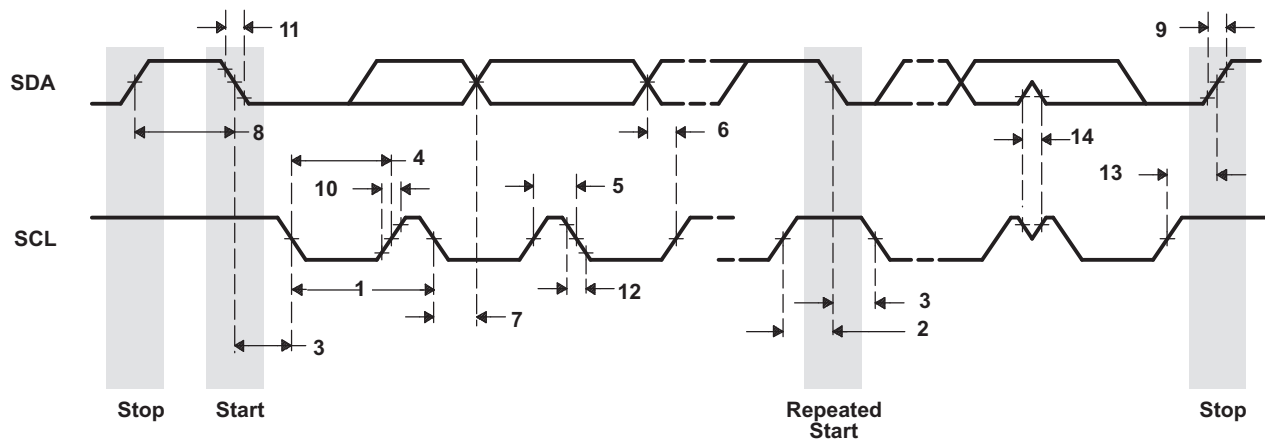


Figure 5-27. I²C Receive Timings

Table 5-28. Switching Characteristics for I2C Timings⁽¹⁾ (see Figure 5-28)

| NO. | PARAMETER | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | | | UNIT |
|-----|----------------------------|---|---|-----|---------------------------------------|-----|------|
| | | | STANDARD MODE | | FAST MODE | | |
| | | | MIN | MAX | MIN | MAX | |
| 16 | t _c (SCL) | Cycle time, SCL | 10 | | 2.5 | | μs |
| 17 | t _d (SCLH-SDAL) | Delay time, SCL high to SDA low (for a repeated START condition) | 4.7 | | 0.6 | | μs |
| 18 | t _d (SDAL-SCLL) | Delay time, SDA low to SCL low (for a START and a repeated START condition) | 4 | | 0.6 | | μs |
| 19 | t _w (SCLL) | Pulse duration, SCL low | 4.7 | | 1.3 | | μs |
| 20 | t _w (SCLH) | Pulse duration, SCL high | 4 | | 0.6 | | μs |
| 21 | t _d (SDAV-SCLH) | Delay time, SDA valid to SCL high | 250 | | 100 | | ns |
| 22 | t _v (SCLL-SDAV) | Valid time, SDA valid after SCL low | 0 | | 0 | 0.9 | μs |
| 23 | t _w (SDAH) | Pulse duration, SDA high between STOP and START conditions | 4.7 | | 1.3 | | μs |
| 24 | t _r (SDA) | Rise time, SDA ⁽²⁾ | 1000 | | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| 25 | t _r (SCL) | Rise time, SCL ⁽²⁾ | 1000 | | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| 26 | t _f (SDA) | Fall time, SDA ⁽²⁾ | 300 | | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| 27 | t _f (SCL) | Fall time, SCL ⁽²⁾ | 300 | | 20 + 0.1C _b ⁽¹⁾ | 300 | ns |
| 28 | t _d (SCLH-SDAH) | Delay time, SCL high to SDA high (for STOP condition) | 4 | | 0.6 | | μs |
| 29 | C _p | Capacitance for each I2C pin | 10 | | 10 | | pF |

- (1) C_b = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times are allowed.
(2) The rise/fall times are measured at 30% and 70% of DV_{DDIO}. The fall time is only slightly influenced by the external bus load (C_b) and external pullup resistor. However, the rise time (t_r) is mainly determined by the bus load capacitance and the value of the pullup resistor. The pullup resistor must be selected to meet the I2C rise and fall time values specified.

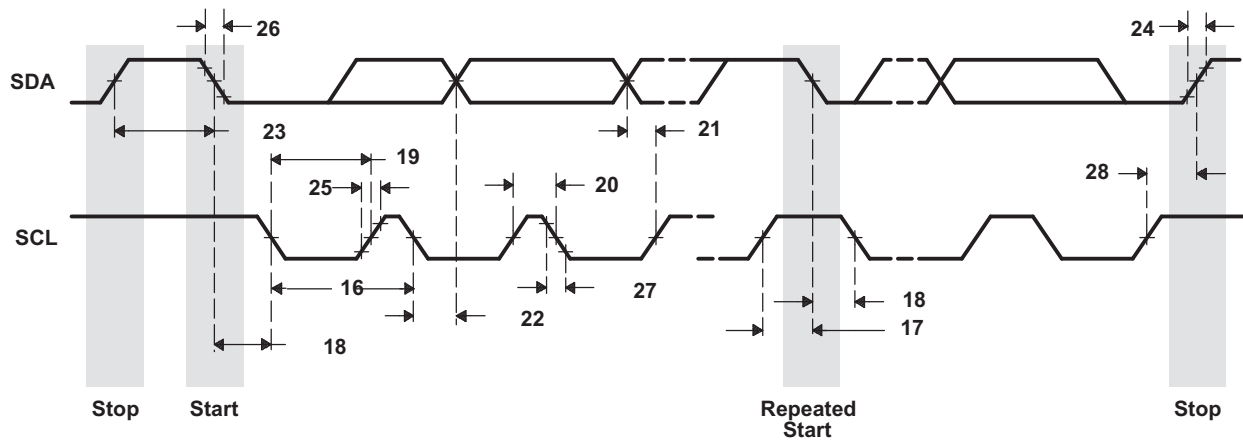


Figure 5-28. I2C Transmit Timings

5.13 Universal Asynchronous Receiver/Transmitter (UART)

The UART performs serial-to-parallel conversions on data received from an external peripheral device and parallel-to-serial conversions on data transmitted to an external peripheral device via a serial bus.

The device has one UART peripheral with the following features:

- Programmable baud rates (frequency pre-scale values from 1 to 65535)
- Fully programmable serial interface characteristics:
 - 5, 6, 7, or 8-bit characters
 - Even, odd, or no PARITY bit generation and detection
 - 1, 1.5, or 2 STOP bit generation
- 16-byte depth transmitter and receiver FIFOs:
 - The UART can be operated with or without the FIFOs
 - 1, 4, 8, or 14 byte selectable receiver FIFO trigger level for autoflow control and DMA
- DMA signaling capability for both received and transmitted data
- CPU interrupt capability for both received and transmitted data
- False START bit detection
- Line break generation and detection
- Internal diagnostic capabilities:
 - Loopback controls for communications link fault isolation
 - Break, parity, overrun, and framing error simulation
- Programmable autoflow control using CTS and RTS signals

5.13.1 UART Peripheral Register Descriptions

[Table 5-29](#) shows the UART registers.

Table 5-29. UART Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|-------------|---|
| 1B00h | RBR | Receiver Buffer Register (read only) |
| 1B00h | THR | Transmitter Holding Register (write only) |
| 1B02h | IER | Interrupt Enable Register |
| 1B04h | IIR | Interrupt Identification Register (read only) |
| 1B04h | FCR | FIFO Control Register (write only) |
| 1B06h | LCR | Line Control Register |
| 1B08h | MCR | Modem Control Register |
| 1B0Ah | LSR | Line Status Register |
| 1B0Ch | MSR | Modem Status Register |
| 1B0Eh | SCR | Scratch Register |
| 1B10h | DLL | Divisor LSB Latch |
| 1B12h | DLH | Divisor MSB Latch |
| 1B18h | PWREMU_MGMT | Power and Emulation Management Register |

5.13.2 UART Electrical Data/Timing [Receive/Transmit]

Table 5-30. Timing Requirements for UART Receive⁽¹⁾⁽²⁾ (see Figure 5-29)

| NO. | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | UNIT |
|-----|------------------------|--|---------------------------|-------|--------------------------|-------|------|
| | | | MIN | MAX | MIN | MAX | |
| 4 | t _w (URXDB) | Pulse duration, receive data bit (UART_RXD) [15/30/100 pF] | U - 3.5 | U + 3 | U - 3.5 | U + 3 | ns |
| 5 | t _w (URXSB) | Pulse duration, receive start bit [15/30/100 pF] | U - 3.5 | U + 3 | U - 3.5 | U + 3 | ns |

(1) U = UART baud time = 1/programmed baud rate.

(2) These parametric values are measured at DV_{DDIO} = 3.3 V, 2.75 V, and 2.5 V

Table 5-31. Switching Characteristics Over Recommended Operating Conditions for UART Transmit^{(1) (2)} (see Figure 5-29)

| NO. | PARAMETER | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3V | | UNIT |
|-----|------------------------|---|---------------------------|-------|-------------------------|-------|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | f _(baud) | Maximum programmable bit rate | | 3.75 | | 6.25 | MHz |
| 2 | t _w (UTXDB) | Pulse duration, transmit data bit (UART_TXD) [15/30/100 pF] | U - 3.5 | U + 4 | U - 3.5 | U + 4 | ns |
| 3 | t _w (UTXSB) | Pulse duration, transmit start bit [15/30/100 pF] | U - 3.5 | U + 4 | U - 3.5 | U + 4 | ns |

(1) U = UART baud time = 1/programmed baud rate.

(2) These parametric values are measured at DV_{DDIO} = 3.3 V, 2.75 V, and 2.5 V

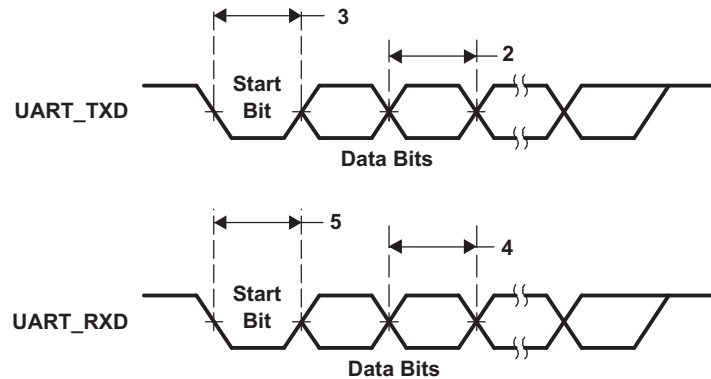


Figure 5-29. UART Transmit/Receive Timing

5.14 Inter-IC Sound (I2S)

The device I2S peripherals allow serial transfer of full-duplex streaming data, usually audio data, between the device and an external I2S peripheral device such as an audio codec.

The device supports 4 independent dual-channel I2S peripherals, each with the following features:

- Full-duplex (transmit and receive) dual-channel communication
- Double buffered data registers that allow for continuous data streaming
- I2S/Left-justified and DSP data format with a data delay of 1 or 2 bits
- Data word-lengths of 8, 10, 12, 14, 16, 18, 20, 24, or 32 bits
- Ability to sign-extend received data samples for easy use in signal processing algorithms
- Programmable polarity for both frame synchronization and bit clocks
- Stereo (in I2S/Left-justified or DSP data formats) or mono (in DSP data format) mode
- Detection of over-run, under-run, and frame-sync error conditions

5.14.1 I2S Peripheral Register Descriptions

Table 5-32 through Table 5-35 show the I2S0 through I2S3 registers.

Table 5-32. I2S0 Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|-------------|-------------------------------------|
| 2800h | I2S0SCTRL | I2S0 Serializer Control Register |
| 2804h | I2S0SRATE | I2S0 Sample Rate Generator Register |
| 2808h | I2S0TXLT0 | I2S0 Transmit Left Data 0 Register |
| 2809h | I2S0TXLT1 | I2S0 Transmit Left Data 1 Register |
| 280Ch | I2S0TXRT0 | I2S0 Transmit Right Data 0 Register |
| 280Dh | I2S0TXRT1 | I2S0 Transmit Right Data 1 Register |
| 2810h | I2S0INTFL | I2S0 Interrupt Flag Register |
| 2814h | I2S0INTMASK | I2S0 Interrupt Mask Register |
| 2828h | I2S0RXLT0 | I2S0 Receive Left Data 0 Register |
| 2829h | I2S0RXLT1 | I2S0 Receive Left Data 1 Register |
| 282Ch | I2S0RXRT0 | I2S0 Receive Right Data 0 Register |
| 282Dh | I2S0RXRT1 | I2S0 Receive Right Data 1 Register |

Table 5-33. I2S1 Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|-------------|-------------------------------------|
| 2900h | I2S1SCTRL | I2S1 Serializer Control Register |
| 2904h | I2S1SRATE | I2S1 Sample Rate Generator Register |
| 2908h | I2S1TXLT0 | I2S1 Transmit Left Data 0 Register |
| 2909h | I2S1TXLT1 | I2S1 Transmit Left Data 1 Register |
| 290Ch | I2S1TXRT0 | I2S1 Transmit Right Data 0 Register |
| 290Dh | I2S1TXRT1 | I2S1 Transmit Right Data 1 Register |
| 2910h | I2S1INTFL | I2S1 Interrupt Flag Register |
| 2914h | I2S1INTMASK | I2S1 Interrupt Mask Register |
| 2928h | I2S1RXLT0 | I2S1 Receive Left Data 0 Register |
| 2929h | I2S1RXLT1 | I2S1 Receive Left Data 1 Register |
| 292Ch | I2S1RXRT0 | I2S1 Receive Right Data 0 Register |
| 292Dh | I2S1RXRT1 | I2S1 Receive Right Data 1 Register |

Table 5-34. I2S2 Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|-------------|-------------------------------------|
| 2A00h | I2S2SCTRL | I2S2 Serializer Control Register |
| 2A04h | I2S2SRATE | I2S2 Sample Rate Generator Register |
| 2A08h | I2S2TXLT0 | I2S2 Transmit Left Data 0 Register |
| 2A09h | I2S2TXLT1 | I2S2 Transmit Left Data 1 Register |
| 2A0Ch | I2S2TXRT0 | I2S2 Transmit Right Data 0 Register |
| 2A0Dh | I2S2TXRT1 | I2S2 Transmit Right Data 1 Register |
| 2A10h | I2S2INTFL | I2S2 Interrupt Flag Register |
| 2A14h | I2S2INTMASK | I2S2 Interrupt Mask Register |
| 2A28h | I2S2RXLT0 | I2S2 Receive Left Data 0 Register |
| 2A29h | I2S2RXLT1 | I2S2 Receive Left Data 1 Register |
| 2A2Ch | I2S2RXRT0 | I2S2 Receive Right Data 0 Register |
| 2A2Dh | I2S2RXRT1 | I2S2 Receive Right Data 1 Register |

Table 5-35. I2S3 Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|-------------------|-------------|-------------------------------------|
| 2B00h | I2S3SCTRL | I2S3 Serializer Control Register |
| 2B04h | I2S3SRATE | I2S3 Sample Rate Generator Register |
| 2B08h | I2S3TXLT0 | I2S3 Transmit Left Data 0 Register |
| 2B09h | I2S3TXLT1 | I2S3 Transmit Left Data 1 Register |
| 2B0Ch | I2S3TXRT0 | I2S3 Transmit Right Data 0 Register |
| 2B0Dh | I2S3TXRT1 | I2S3 Transmit Right Data 1 Register |
| 2B10h | I2S3INTFL | I2S3 Interrupt Flag Register |
| 2B14h | I2S3INTMASK | I2S3 Interrupt Mask Register |
| 2B28h | I2S3RXLT0 | I2S3 Receive Left Data 0 Register |
| 2B29h | I2S3RXLT1 | I2S3 Receive Left Data 1 Register |
| 2B2Ch | I2S3RXRT0 | I2S3 Receive Right Data 0 Register |
| 2B2Dh | I2S3RXRT1 | I2S3 Receive Right Data 1 Register |

5.14.2 I2S Electrical Data/Timing

Table 5-36. Timing Requirements for I2S [I/O = 3.3 V, 2.75 V, and 2.5 V]⁽¹⁾ (see [Figure 5-30](#))

| NO. | | | MASTER | | | | SLAVE | | | | UNIT |
|-----|----------------------------|---|----------------------------|-----|----------------------------|-----|--|-----|--|-----|------|
| | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | t _c (CLK) | Cycle time, I2S_CLK | 40 or 2P ⁽¹⁾⁽²⁾ | | 40 or 2P ⁽¹⁾⁽²⁾ | | 40 or 2P ⁽¹⁾⁽²⁾ | | 40 or 2P ⁽¹⁾⁽²⁾ | | ns |
| 2 | t _w (CLKH) | Pulse duration, I2S_CLK high | 20 | | 20 | | 20 | | 20 | | ns |
| 3 | t _w (CLKL) | Pulse duration, I2S_CLK low | 20 | | 20 | | 20 | | 20 | | ns |
| 7 | t _{su} (RXV-CLKH) | Setup time, I2S_RX valid before I2S_CLK high (CLKPOL = 0) | 5 | | 5 | | 5 | | 5 | | ns |
| | t _{su} (RXV-CLKL) | Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1) | 5 | | 5 | | 5 | | 5 | | ns |
| 8 | t _h (CLKH-RXV) | Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0) | 3 | | 3 | | 3 | | 3 | | ns |
| | t _h (CLKL-RXV) | Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1) | 3 | | 3 | | 3 | | 3 | | ns |
| 9 | t _{su} (FSV-CLKH) | Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0) | — | | — | | 15 | | 15 | | ns |
| | t _{su} (FSV-CLKL) | Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1) | — | | — | | 15 | | 15 | | ns |
| 10 | t _h (CLKH-FSV) | Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0) | — | | — | | t _w (CLKH) + 0.6 ⁽³⁾ | | t _w (CLKH) + 0.6 ⁽³⁾ | | ns |
| | t _h (CLKL-FSV) | Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1) | — | | — | | t _w (CLKL) + 0.6 ⁽³⁾ | | t _w (CLKL) + 0.6 ⁽³⁾ | | ns |

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) Use whichever value is greater.

(3) In Slave Mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 5-37. Timing Requirements for I2S [I/O = 1.8 V]⁽¹⁾ (see Figure 5-30)

| NO. | | | MASTER | | | | SLAVE | | | | UNIT |
|-----|----------------------------|---|--|-----|--|-----|--|-----|--|-----|------|
| | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | t _c (CLK) | Cycle time, I2S_CLK | 50 or 2P ⁽¹⁾ ₍₂₎ | | 40 or 2P ⁽¹⁾ ₍₂₎ | | 50 or 2P ⁽¹⁾ (2) | | 40 or 2P ⁽¹⁾ (2) | | ns |
| 2 | t _w (CLKH) | Pulse duration, I2S_CLK high | 25 | | 20 | | 25 | | 20 | | ns |
| 3 | t _w (CLKL) | Pulse duration, I2S_CLK low | 25 | | 20 | | 25 | | 20 | | ns |
| 7 | t _{su} (RXV-CLKH) | Setup time, I2S_RX valid before I2S_CLK high (CLKPOL = 0) | 5 | | 5 | | 5 | | 5 | | ns |
| | t _{su} (RXV-CLKL) | Setup time, I2S_RX valid before I2S_CLK low (CLKPOL = 1) | 5 | | 5 | | 5 | | 5 | | ns |
| 8 | t _h (CLKH-RXV) | Hold time, I2S_RX valid after I2S_CLK high (CLKPOL = 0) | 3 | | 3 | | 3 | | 3 | | ns |
| | t _h (CLKL-RXV) | Hold time, I2S_RX valid after I2S_CLK low (CLKPOL = 1) | 3 | | 3 | | 3 | | 3 | | ns |
| 9 | t _{su} (FSV-CLKH) | Setup time, I2S_FS valid before I2S_CLK high (CLKPOL = 0) | — | | — | | 15 | | 15 | | ns |
| | t _{su} (FSV-CLKL) | Setup time, I2S_FS valid before I2S_CLK low (CLKPOL = 1) | — | | — | | 15 | | 15 | | ns |
| 10 | t _h (CLKH-FSV) | Hold time, I2S_FS valid after I2S_CLK high (CLKPOL = 0) | — | | — | | t _w (CLKH) + 0.6 ⁽³⁾ | | t _w (CLKH) + 0.6 ⁽³⁾ | | ns |
| | t _h (CLKL-FSV) | Hold time, I2S_FS valid after I2S_CLK low (CLKPOL = 1) | — | | — | | t _w (CLKL) + 0.6 ⁽³⁾ | | t _w (CLKL) + 0.6 ⁽³⁾ | | ns |

(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) Use whichever value is greater.

(3) In Slave Mode, I2S_FS is required to be latched on both edges of I2S input clock (I2S_CLK).

Table 5-38. Switching Characteristics Over Recommended Operating Conditions for I2S Output
[I/O = 3.3 V, 2.75 V, or 2.5 V] (see [Figure 5-30](#))

| NO. | PARAMETER | | MASTER | | | | SLAVE | | | | UNIT |
|-----|------------------------------|--|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|------|
| | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | t _c (CLK) | Cycle time, I2S_CLK | 40 or 2P ⁽¹⁾ (2) | | 40 or 2P ⁽¹⁾ (2) | | 40 or 2P ⁽¹⁾ (2) | | 40 or 2P ⁽¹⁾ (2) | | ns |
| 2 | t _w (CLKH) | Pulse duration, I2S_CLK high (CLKPOL = 0) | 20 | | 20 | | 20 | | 20 | | ns |
| | t _w (CLKL) | Pulse duration, I2S_CLK low (CLKPOL = 1) | 20 | | 20 | | 20 | | 20 | | ns |
| 3 | t _w (CLKL) | Pulse duration, I2S_CLK low (CLKPOL = 0) | 20 | | 20 | | 20 | | 20 | | ns |
| | t _w (CLKH) | Pulse duration, I2S_CLK high (CLKPOL = 1) | 20 | | 20 | | 20 | | 20 | | ns |
| 4 | t _{dmax} (CLKL-DXV) | Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0) | 0 | 15 | 0 | 14 | 0 | 15 | 0 | 15 | ns |
| | t _{dmax} (CLKH-DXV) | Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1) | 0 | 15 | 0 | 14 | 0 | 15 | 0 | 15 | ns |
| 5 | t _{dmax} (CLKL-FSV) | Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0) | -1.1 | 14 | -1.1 | 14 | – | – | – | – | ns |
| | t _{dmax} (CLKH-FSV) | Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1) | -1.1 | 14 | -1.1 | 14 | – | – | – | – | ns |

- (1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

Table 5-39. Switching Characteristics Over Recommended Operating Conditions for I2S Output
[I/O = 1.8 V] (see [Figure 5-30](#))

| NO. | PARAMETER | | MASTER | | | | SLAVE | | | | UNIT |
|-----|------------------------------|--|--------------------------------|-----|--------------------------------|-----|--------------------------------|-----|--------------------------------|------|------|
| | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| 1 | t _c (CLK) | Cycle time, I2S_CLK | 50 or 2P ^{(1) (2)} | | 40 or 2P ^{(1) (2)} | | 50 or 2P ^{(1) (2)} | | 40 or 2P ^{(1) (2)} | | ns |
| 2 | t _w (CLKH) | Pulse duration, I2S_CLK high (CLKPOL = 0) | 25 | | 20 | | 25 | | 20 | | ns |
| | t _w (CLKL) | Pulse duration, I2S_CLK low (CLKPOL = 1) | 25 | | 20 | | 25 | | 20 | | ns |
| 3 | t _w (CLKL) | Pulse duration, I2S_CLK low (CLKPOL = 0) | 25 | | 20 | | 25 | | 20 | | ns |
| | t _w (CLKH) | Pulse duration, I2S_CLK high (CLKPOL = 1) | 25 | | 20 | | 25 | | 20 | | ns |
| 4 | t _{dmax} (CLKL-DXV) | Output Delay time, I2S_CLK low to I2S_DX valid (CLKPOL = 0) | 0 | 19 | 0 | 14 | 0 | 19 | 0 | 16.5 | ns |
| | t _{dmax} (CLKH-DXV) | Output Delay time, I2S_CLK high to I2S_DX valid (CLKPOL = 1) | 0 | 19 | 0 | 14 | 0 | 19 | 0 | 16.5 | ns |
| 5 | t _{dmax} (CLKL-FSV) | Delay time, I2S_CLK low to I2S_FS valid (CLKPOL = 0) | -1.1 | 14 | -1.1 | 14 | – | | – | | ns |
| | t _{dmax} (CLKH-FSV) | Delay time, I2S_CLK high to I2S_FS valid (CLKPOL = 1) | -1.1 | 14 | -1.1 | 14 | – | | – | | ns |

- (1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.
(2) Use whichever value is greater.

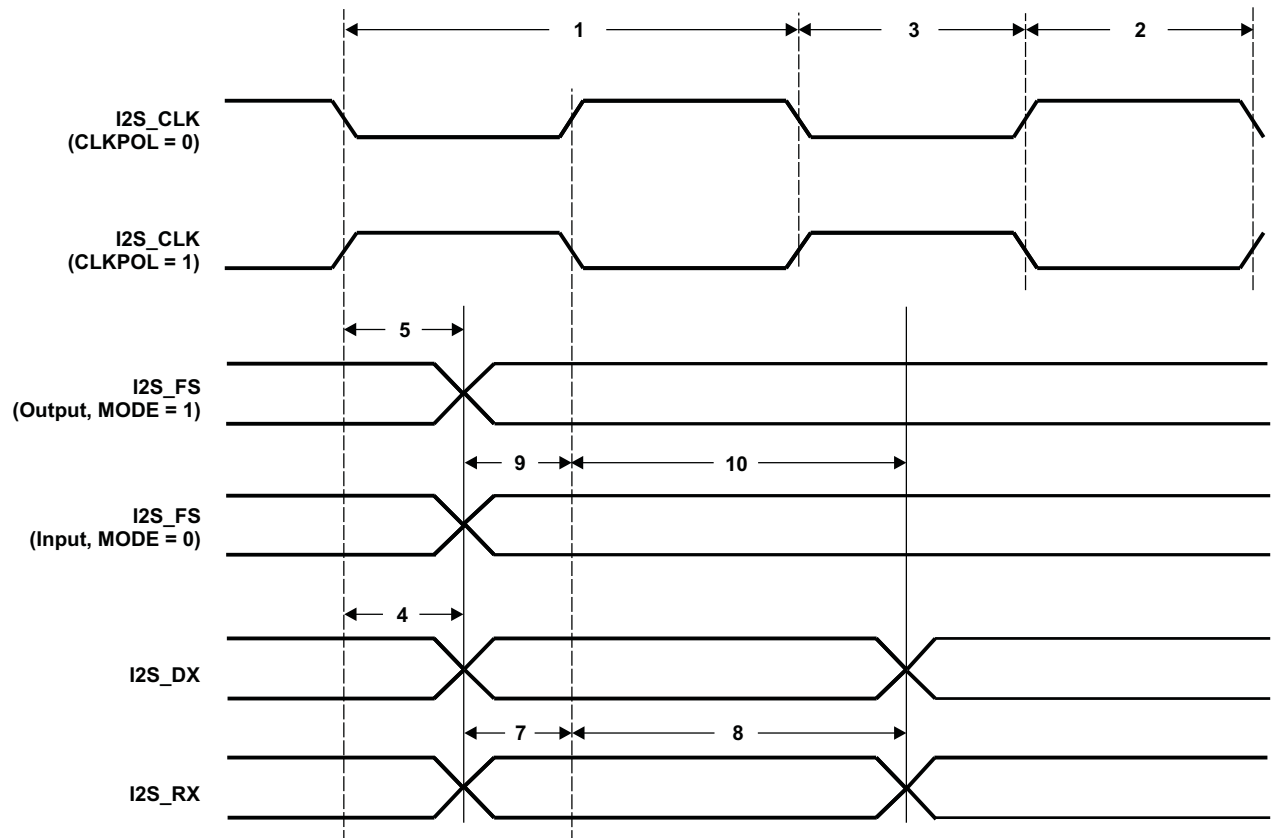


Figure 5-30. I2S Input and Output Timings

5.15 Liquid Crystal Display Controller (LCDC)

The device includes a LCD Interface Display Driver (LIDD) controller.

The LIDD Controller supports the asynchronous LCD interface and has the following features:

- Provides full-timing programmability of control signals and output data

Note: Raster mode is *not* supported on this device.

The LCD controller is responsible for generating the correct external timing. The DMA engine provides a constant flow of data from the frame buffers to the external LCD panel via the LIDD controller. In addition, CPU access is provided to read and write registers.

5.15.1 LCDC Peripheral Register Descriptions

Table 5-40 shows the LCDC peripheral registers.

Table 5-40. LCD Controller Registers

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|-------------------|---|
| 2E00h | LCDREVMIN | LCD Minor Revision Register |
| 2E01h | LCDREVMAJ | LCD Major Revision Register |
| 2E04h | LCDCR | LCD Control Register |
| 2E08h | LCDSR | LCD Status Register |
| 2E0Ch | LCDLIDDCR | LCD LIDD Control Register |
| 2E10h | LCDLIDDCS0CONFIG0 | LCD LIDD CS0 Configuration Register 0 |
| 2E11h | LCDLIDDCS0CONFIG1 | LCD LIDD CS0 Configuration Register 1 |
| 2E14h | LCDLIDDCS0ADDR | LCD LIDD CS0 Address Read/Write Register |
| 2E18h | LCDLIDDCS0DATA | LCD LIDD CS0 Data Read/Write Register |
| 2E1Ch | LCDLIDDCS1CONFIG0 | LCD LIDD CS1 Configuration Register 0 |
| 2E1Dh | LCDLIDDCS1CONFIG1 | LCD LIDD CS1 Configuration Register 1 |
| 2E20h | LCDLIDDCS1ADDR | LCD LIDD CS1 Address Read/Write Register |
| 2E24h | LCDLIDDCS1DATA | LCD LIDD CS1 Data Read/Write Register |
| 2E28h – 2E3Ah | — | Reserved |
| 2E40h | LCDDMACR | LCD DMA Control Register |
| 2E44h | LCDDMAFB0BAR0 | LCD DMA Frame Buffer 0 Base Address Register 0 |
| 2E45h | LCDDMAFB0BAR1 | LCD DMA Frame Buffer 0 Base Address Register 1 |
| 2E48h | LCDDMAFB0CAR0 | LCD DMA Frame Buffer 0 Ceiling Address Register 0 |
| 2E49h | LCDDMAFB0CAR1 | LCD DMA Frame Buffer 0 Ceiling Address Register 1 |
| 2E4Ch | LCDDMAFB1BAR0 | LCD DMA Frame Buffer 1 Base Address Register 0 |
| 2E4Dh | LCDDMAFB1BAR1 | LCD DMA Frame Buffer 1 Base Address Register 1 |
| 2E50h | LCDDMAFB1CAR0 | LCD DMA Frame Buffer 1 Ceiling Address Register 0 |
| 2E51h | LCDDMAFB1CAR1 | LCD DMA Frame Buffer 1 Ceiling Address Register 1 |

5.15.2 LCDC Electrical Data/Timing

Table 5-41. Timing Requirements for LCD LIDD Mode⁽¹⁾ (see Figure 5-31 through Figure 5-38)

| NO. | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | UNIT |
|-----|-----------------------------|--|---------------------------|-----|--------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 16 | t _{su} (LCD_D-CLK) | Setup time, LCD_D[15:0] valid before LCD_CLK rising edge | 27 | | 42 | | ns |
| 17 | t _h (CLK-LCD_D) | Hold time, LCD_D[15:0] valid after LCD_CLK rising edge | 0 | | 0 | | ns |

(1) Over operating free-air temperature range (unless otherwise noted)

Table 5-42. Switching Characteristics Over Recommended Operating Conditions for LCD LIDD Mode (see Figure 5-31 through Figure 5-38)

| NO. | PARAMETER | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | UNIT |
|-----|-----------------------------|---|---------------------------|-----|--------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 4 | t _d (LCD_D_V) | Delay time, LCD_CLK rising edge to LCD_D[15:0] valid (write) | | 5 | | 7 | ns |
| 5 | t _d (LCD_D_I) | Delay time, LCD_CLK rising edge to LCD_D[15:0] invalid (write) | -6 | | -6 | | ns |
| 6 | t _d (LCD_E_A) | Delay time, LCD_CLK rising edge to LCD_CSx_Ex low | | 5 | | 7 | ns |
| 7 | t _d (LCD_E_I) | Delay time, LCD_CLK rising edge to LCD_CSx_Ex high | -6 | | -6 | | ns |
| 8 | t _d (LCD_A_A) | Delay time, LCD_CLK rising edge to LCD_RS low | | 5 | | 7 | ns |
| 9 | t _d (LCD_A_I) | Delay time, LCD_CLK rising edge to LCD_RS high | -6 | | -6 | | ns |
| 10 | t _d (LCD_W_A) | Delay time, LCD_CLK rising edge to LCD_RW_WRB low | | 5 | | 7 | ns |
| 11 | t _d (LCD_W_I) | Delay time, LCD_CLK rising edge to LCD_RW_WRB high | -6 | | -6 | | ns |
| 12 | t _d (LCD_STRB_A) | Delay time, LCD_CLK rising edge to LCD_EN_RDB high | | 5 | | 7 | ns |
| 13 | t _d (LCD_STRB_I) | Delay time, LCD_CLK rising edge to LCD_EN_RDB low | -6 | | -6 | | ns |
| 14 | t _d (LCD_D_Z) | Delay time, LCD_CLK rising edge to LCD_D[15:0] in 3-state | | 5 | | 7 | ns |
| 15 | t _d (Z_LCD_D) | Delay time, LCD_CLK rising edge to LCD_D[15:0] valid from 3-state | -6 | | -6 | | ns |

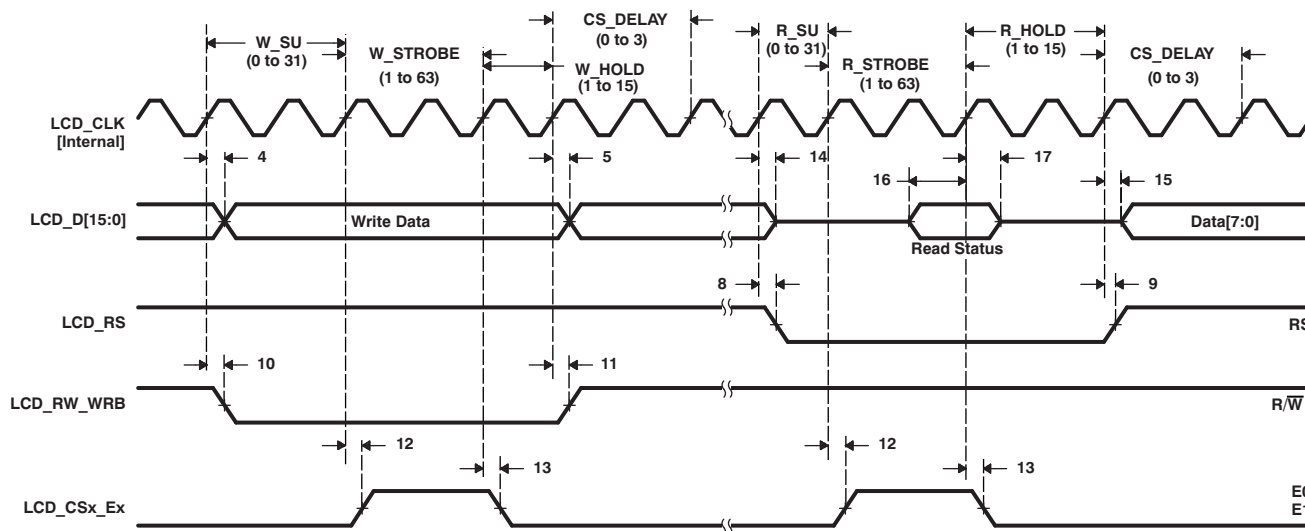


Figure 5-31. Character Display HD44780 Write

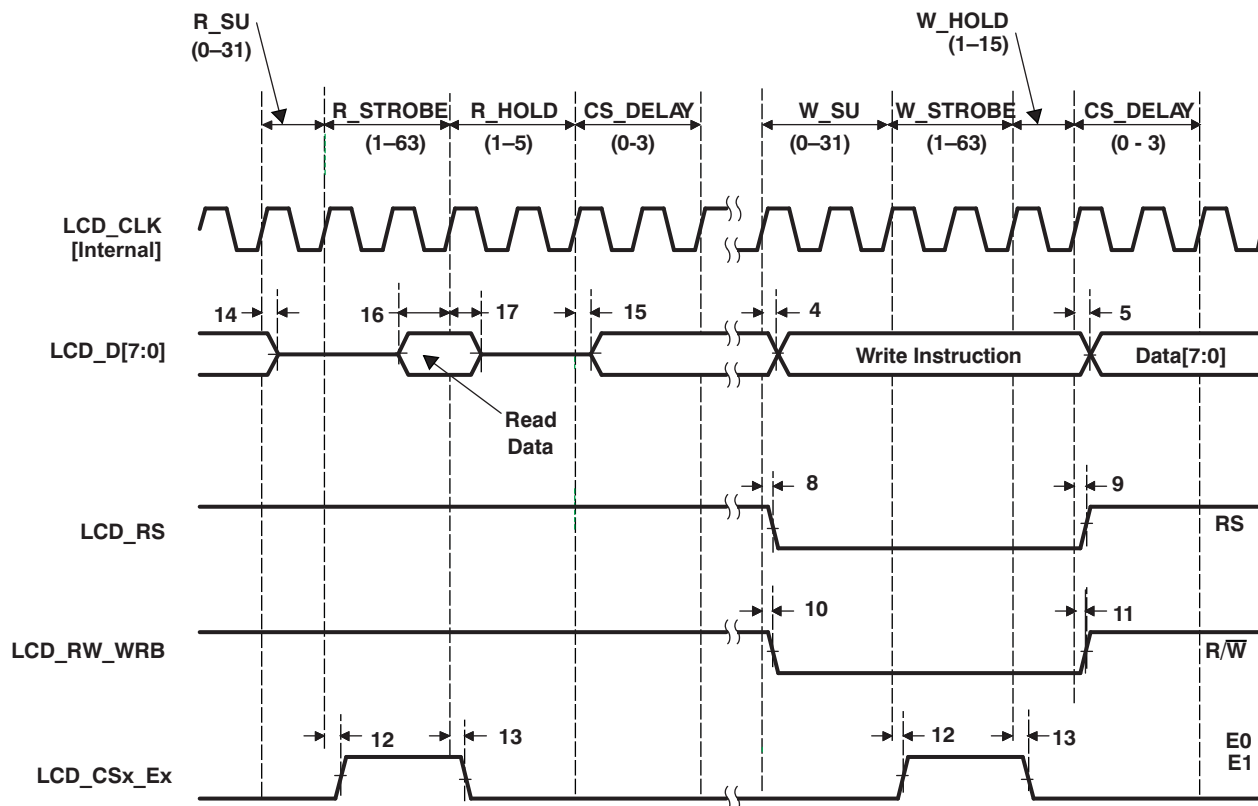


Figure 5-32. Character Display HD44780 Read

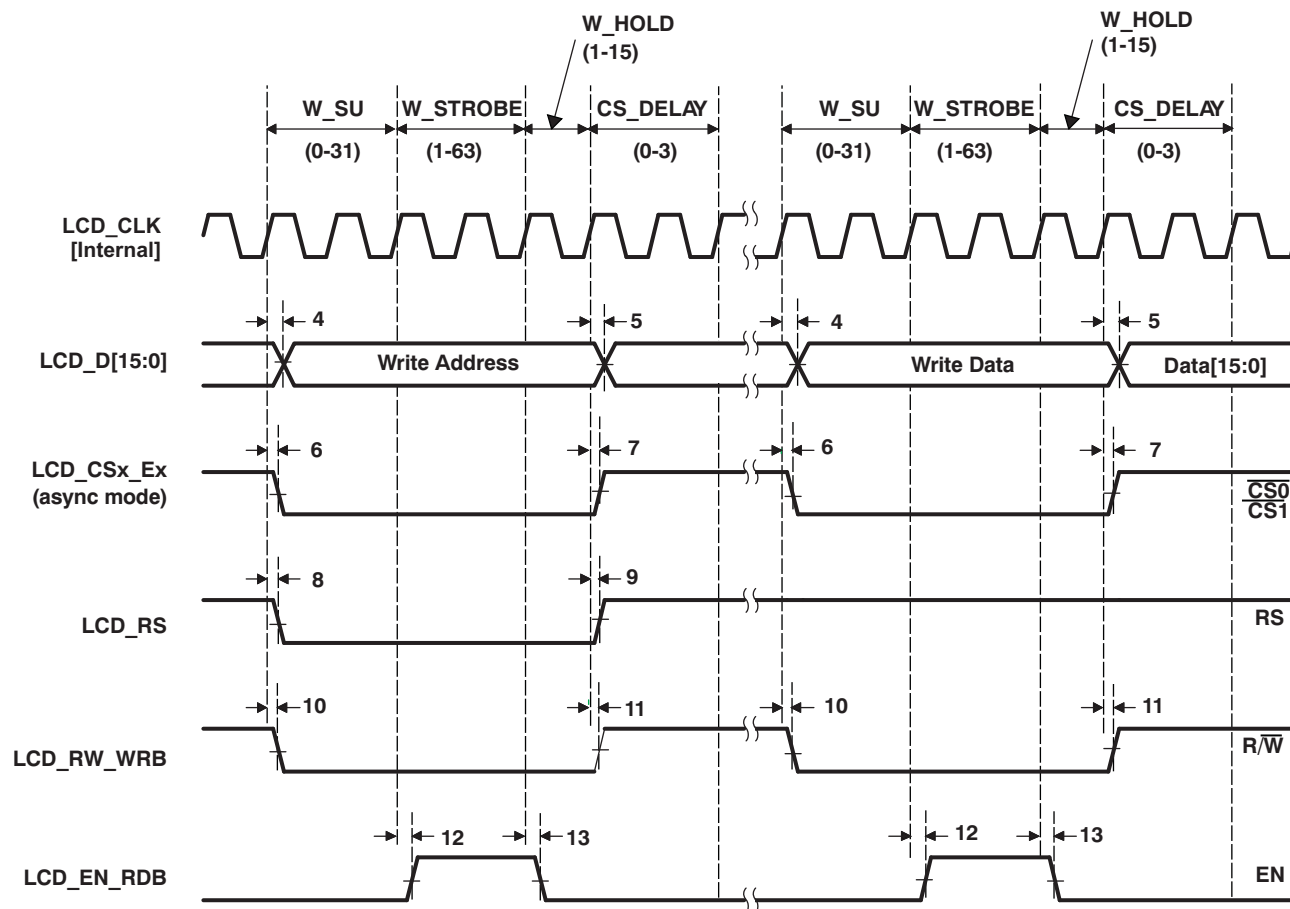


Figure 5-33. Micro-Interface Graphic Display 6800 Write

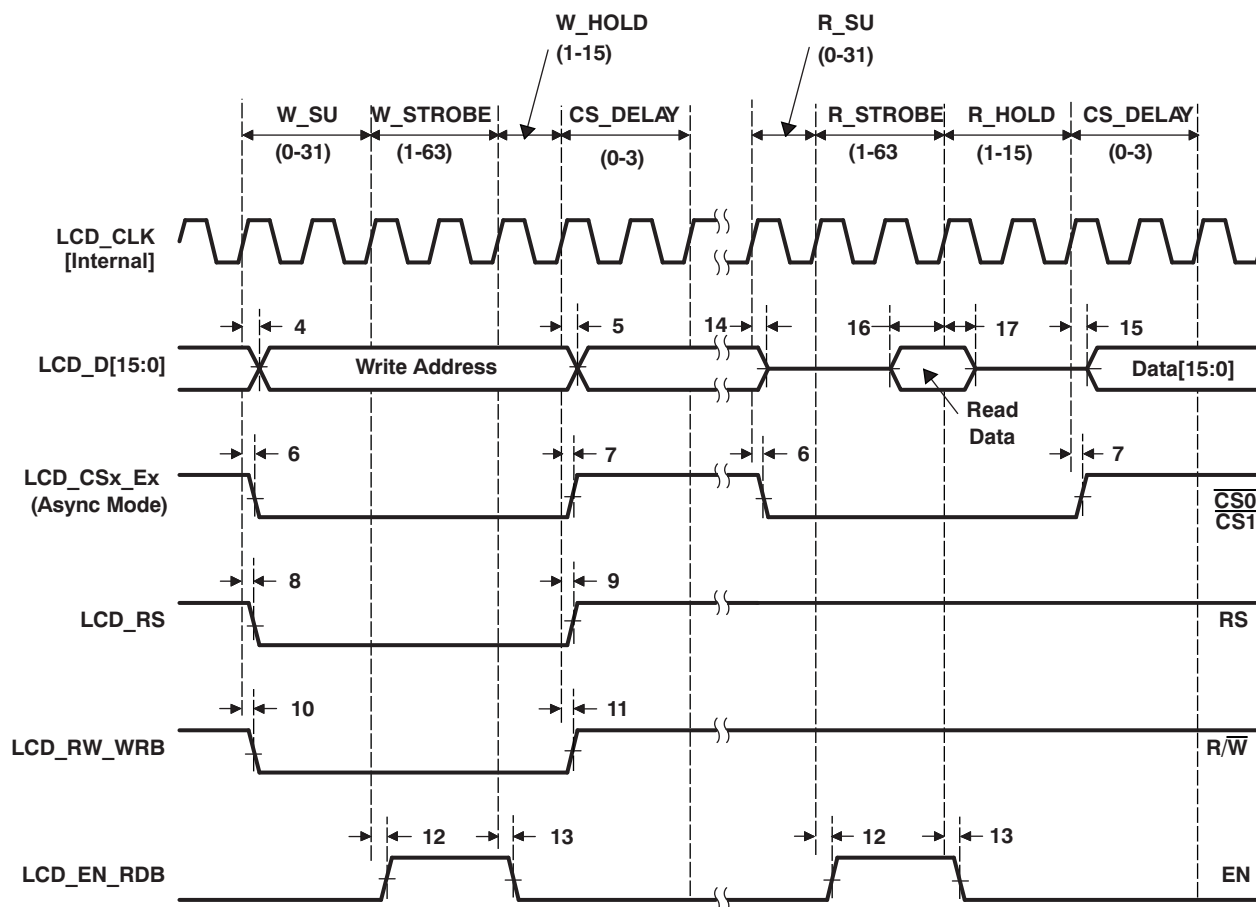


Figure 5-34. Micro-Interface Graphic Display 6800 Read

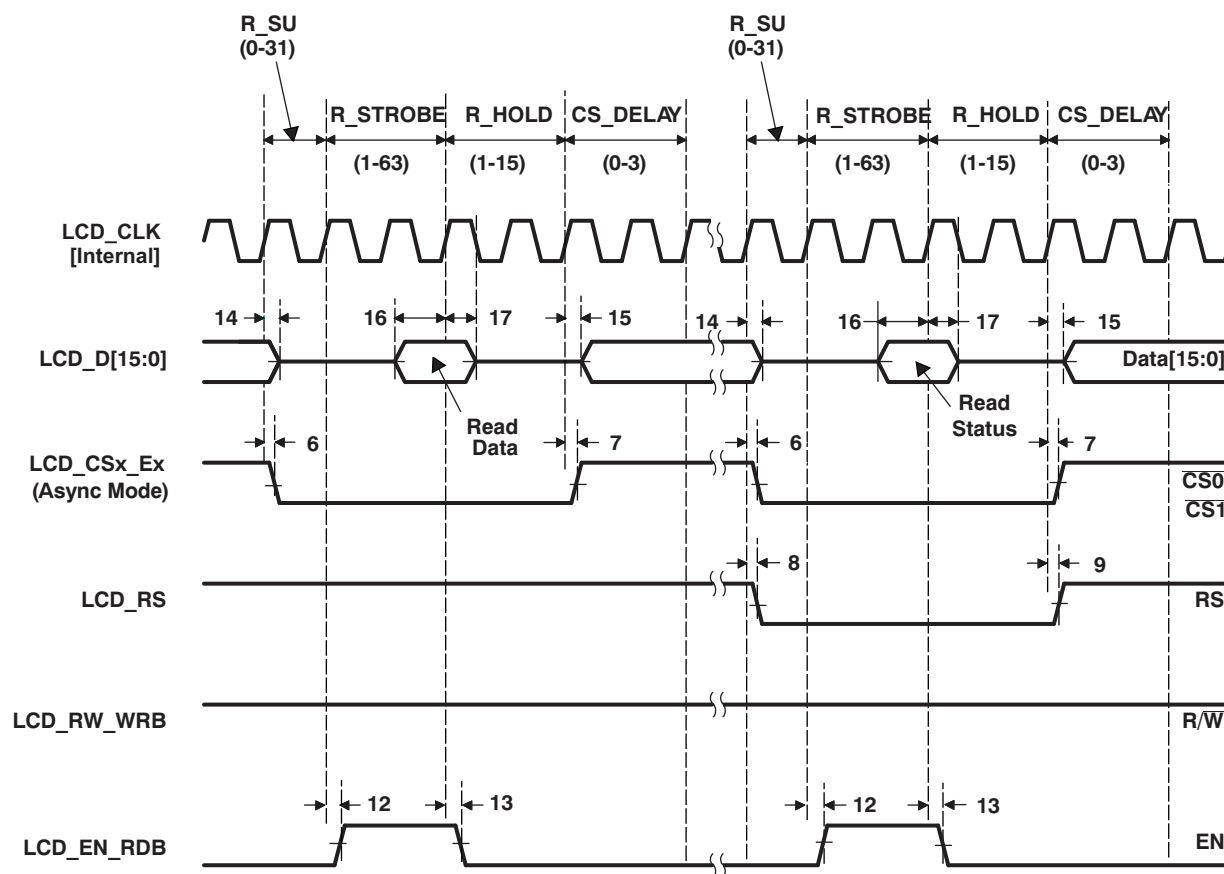


Figure 5-35. Micro-Interface Graphic Display 6800 Status

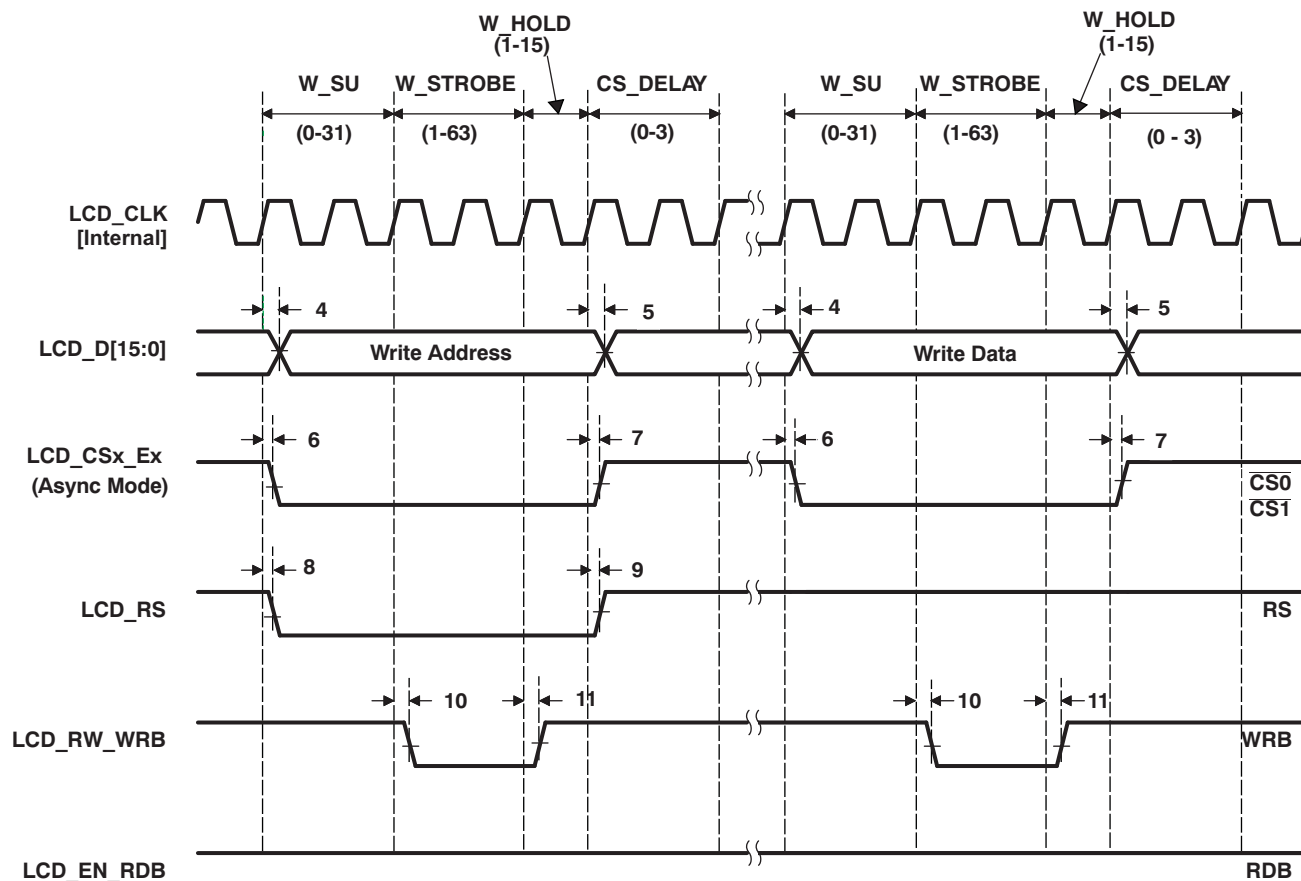


Figure 5-36. Micro-Interface Graphic Display 8080 Write

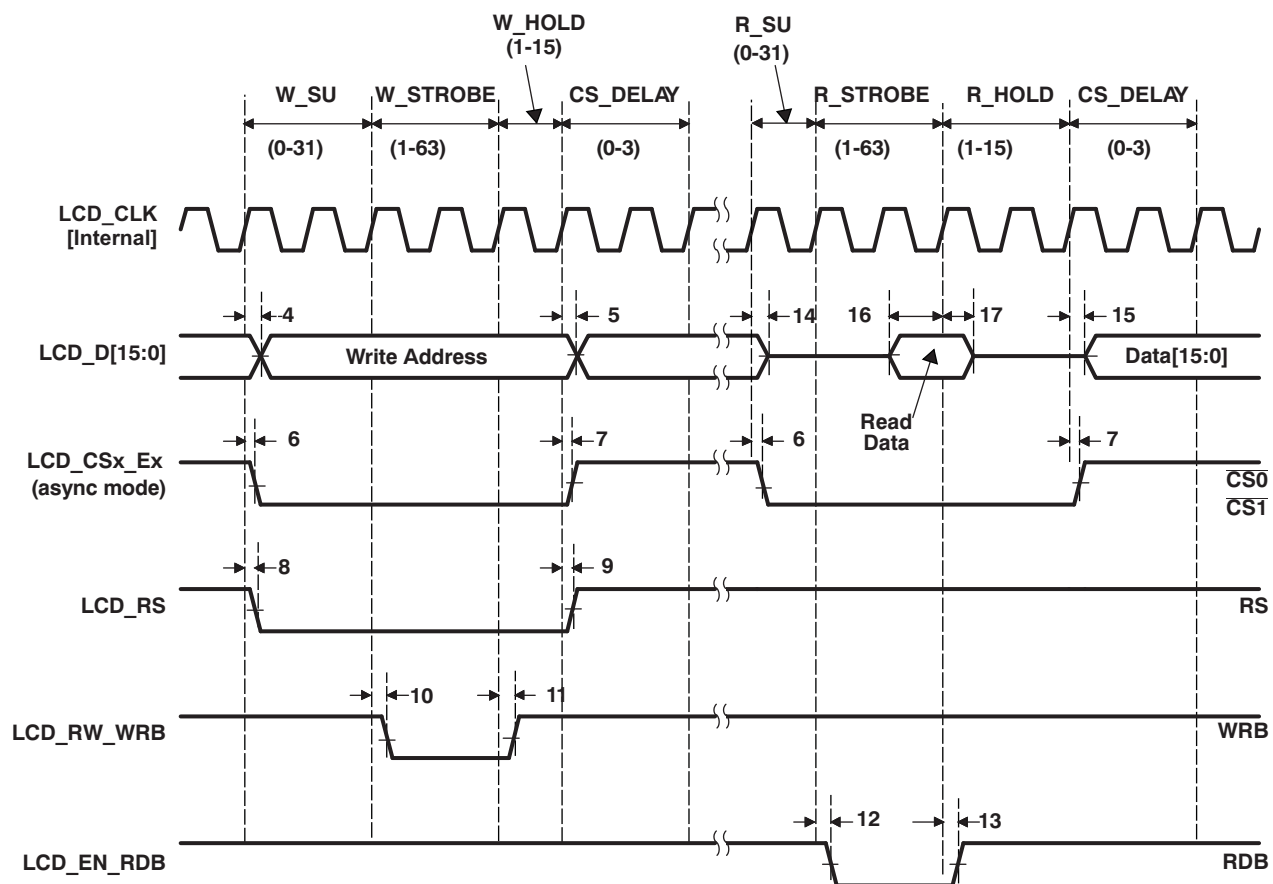


Figure 5-37. Micro-Interface Graphic Display 8080 Read

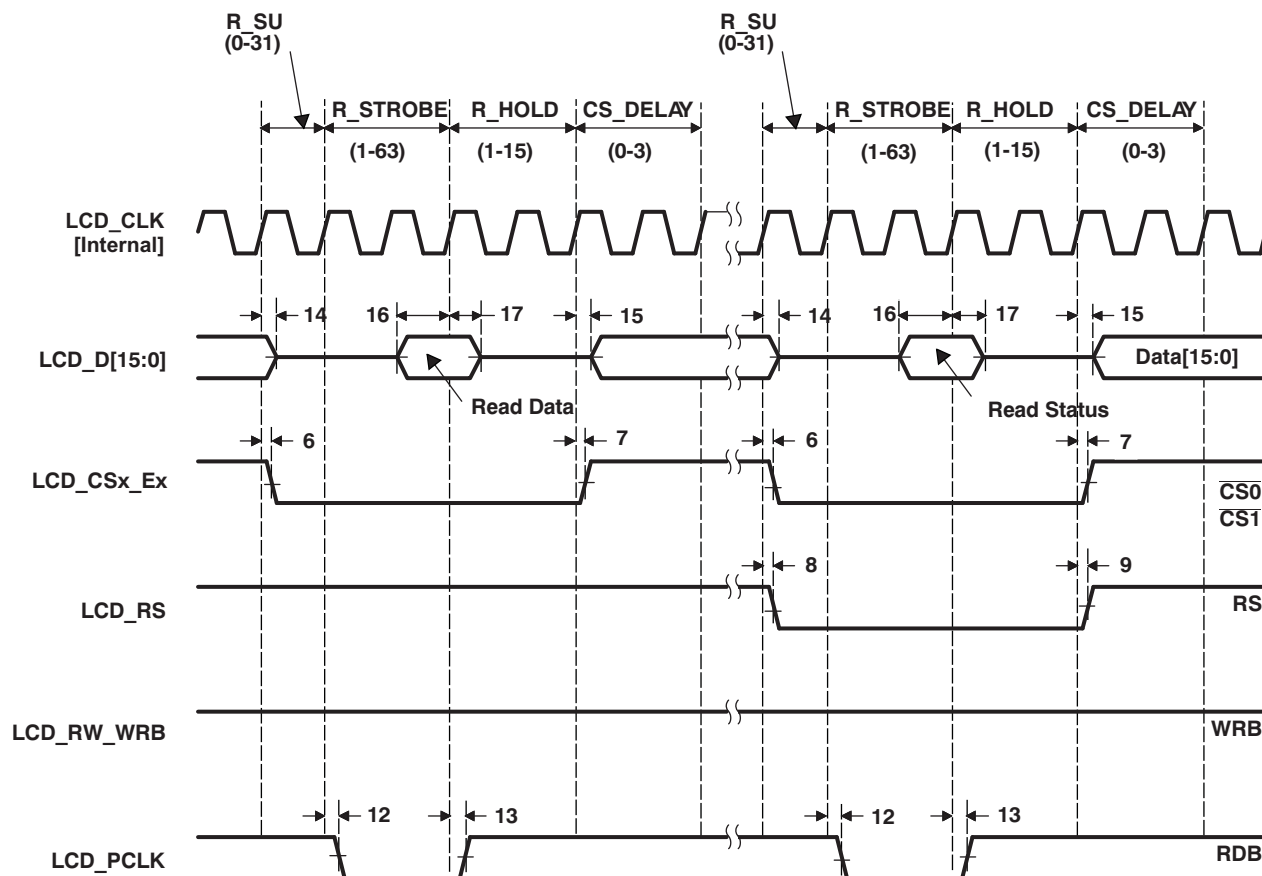


Figure 5-38. Micro-Interface Graphic Display 8080 Status

5.16 10-Bit SAR ADC

The device includes a 10-bit SAR ADC using a switched capacitor architecture which converts an analog input signal to a digital value at a maximum rate of 62.5-k samples per second (ksps) for use by the DSP. This SAR module supports six channels that are connected to four general purpose analog pins (GPAIN [3:0]) which can be used as general purpose outputs.

The device SAR supports the following features:

- Up to 62.5 ksps (2-MHz clock with 32 cycles per conversion)
- Single conversion and continuous back-to-back conversion modes
- Interrupt driven or polling conversion or DMA event generation
- Internal configurable bandgap reference voltages of 1 V or 0.8 V; or external V_{ref} of V_{DDA_ANA}
- One 3.6-V Tolerant analog input (GPAIN0) with internal voltage division for conversion of battery voltage
- Software controlled power down
- Individually configurable general-purpose digital outputs

5.16.1 SAR ADC Peripheral Register Descriptions

Table 5-43 shows the SAR ADC peripheral registers.

Table 5-43. SAR Analog Control Registers

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|------------|--|
| 7012h | SARCTRL | SAR A/D Control Register |
| 7014h | SARDATA | SAR A/D Data Register |
| 7016h | SARCLKCTRL | SAR A/D Clock Control Register |
| 7018h | SARPINCTRL | SAR A/D Reference and Pin Control Register |
| 701Ah | SARGPOCTRL | SAR A/D GPO Control Register |

5.16.2 SAR ADC Electrical Data/Timing

Table 5-44. Switching Characteristics Over Recommended Operating Conditions for ADC Characteristics

| NO. | PARAMETER | | $CV_{DD} = 1.3\text{ V}$ $CV_{DD} = 1.05\text{ V}$ | | | UNIT |
|-----|---------------|---|---|-----------|-----------------|------|
| | | | MIN | TYP | MAX | |
| 1 | $t_{C(SCLC)}$ | Cycle time, ADC internal conversion clock | | | 2 | MHz |
| 3 | $t_{d(CONV)}$ | Delay time, ADC conversion time | | | $32t_{C(SCLC)}$ | ns |
| 4 | S_{DNL} | Static differential non-linearity error (DNL measured for 9 bits) | | ± 0.6 | | LSB |
| 5 | S_{INL} | Static integral non-linearity error | | ± 1 | | LSB |
| 6 | Z_{set} | Zero-scale offset error (INL measured for 9 bits) | | | 2 | LSB |
| 7 | F_{set} | Full-scale offset error | | | 2 | LSB |
| 8 | | Analog input impedance | 1 | | | MΩ |
| 9 | | Signal-to-noise ratio | | 54 | | dB |

5.17 Serial Port Interface (SPI)

The device serial port interface (SPI) is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 32 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI supports multi-chip operation of up to four SPI slave devices. The SPI can operate as a master device only, slave mode is not supported. **Note:** The SPI is not supported by the device DMA controller, so DMA cannot be used in transferring data between the SPI and the on-chip RAM.

The SPI is normally used for communication between the DSP and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EEPROMs, and analog-to-digital converters.

The SPI has the following features:

- Programmable divider for serial data clock generation
- Four pin interface (SPI_CLK, SPI_CS_n, SPI_RX, and SPI_TX)
- Programmable data length (1 to 32 bits)
- 4 external chip select signals
- Programmable transfer or frame size (1 to 4096 characters)
- Optional interrupt generation on character completion
- Programmable SPI_CS_n to SPI_TX delay from 0 to 3 SPI_CLK cycles
- Programmable signal polarities
- Programmable active clock edge
- Internal loopback mode for testing

5.17.1 SPI Peripheral Register Descriptions

Table 5-45 shows the SPI registers.

Table 5-45. SPI Module Registers

| CPU WORD ADDRESS | ACRONYM | REGISTER NAME |
|------------------------|----------|---------------------------------|
| 3000h | SPICDR | Clock Divider Register |
| 3001h | SPICCR | Clock Control Register |
| 3002h | SPIDCR1 | Device Configuration Register 1 |
| 3003h | SPIDCR2 | Device Configuration Register 2 |
| 3004h | SPICMD1 | Command Register 1 |
| 3005h | SPICMD2 | Command Register 2 |
| 3006h | SPISTAT1 | Status Register 1 |
| 3007h | SPISTAT2 | Status Register 2 |
| 3008h | SPIDAT1 | Data Register 1 |
| 3009h | SPIDAT2 | Data Register 2 |

5.17.2 SPI Electrical Data/Timing

Table 5-46. Timing Requirements for SPI Inputs (see Figure 5-39 through Figure 5-42)

| NO. | | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | UNIT |
|-----|----------------------------|--|------------------------------|-----|----------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 4 | t _{C(SCLK)} | Cycle time, SPI_CLK | 66.4 or 4P ⁽¹⁾⁽²⁾ | | 40 or 4P ⁽¹⁾⁽²⁾ | | ns |
| 5 | t _{w(SCLKH)} | Pulse duration, SPI_CLK high | 30 | | 19 | | ns |
| 6 | t _{w(SCLKL)} | Pulse duration, SPI_CLK low | 30 | | 19 | | ns |
| 7 | t _{su(SRXV-SCLK)} | Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 0 | 16.1 | | 13.9 | | ns |
| | | Setup time, SPI_RX valid before SPI_CLK low, SPI Mode 1 | 16.1 | | 13.9 | | ns |
| | | Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 2 | 16.1 | | 13.9 | | ns |
| | | Setup time, SPI_RX valid before SPI_CLK high, SPI Mode 3 | 16.1 | | 13.9 | | ns |
| 8 | t _{h(SCLK-SRXV)} | Hold time, SPI_RX valid after SPI_CLK high, SPI Mode 0 | 0 | | 0 | | ns |
| | | Hold time, SPI_RX valid after SPI_CLK low, SPI Mode 1 | 0 | | 0 | | ns |
| | | Hold time, SPI_RX valid after SPI_CLK low, SPI Mode 2 | 0 | | 0 | | ns |
| | | Hold time, SPI_RX valid after SPI_CLK high, SPI Mode 3 | 0 | | 0 | | ns |

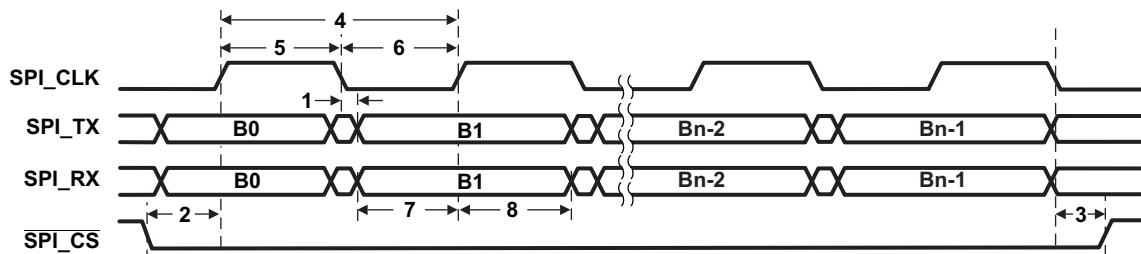
(1) P = SYSCLK period in ns. For example, when the CPU core is clocked at 100 MHz, use P = 10 ns.

(2) Use whichever value is greater.

Table 5-47. Switching Characteristics Over Recommended Operating Conditions for SPI Outputs (see Figure 5-39 through Figure 5-42)

| NO. | PARAMETER | | CV _{DD} = 1.05 V | | CV _{DD} = 1.3 V | | UNIT |
|-----|------------------------------|--|---------------------------------------|-----|---------------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | t _{d(SCLK-STXV)} | Delay time, SPI_CLK low to SPI_TX valid, SPI Mode 0 | -4.2 | 8.9 | -4.9 | 5.3 | ns |
| | | Delay time, SPI_CLK high to SPI_TX valid, SPI Mode 1 | -4.2 | 8.9 | -4.9 | 5.3 | ns |
| | | Delay time, SPI_CLK high to SPI_TX valid, SPI Mode 2 | -4.2 | 8.9 | -4.9 | 5.3 | ns |
| | | Delay time, SPI_CLK low to SPI_TX valid, SPI Mode 3 | -4.2 | 8.9 | -4.9 | 5.3 | ns |
| 2 | t _{d(SPICS-SCLK)} | Delay time, $\overline{\text{SPI_CS}}$ active to SPI_CLK active | t _C - 8 + D ⁽¹⁾ | | t _C - 8 + D ⁽¹⁾ | | ns |
| 3 | t _{oh(SCLK-SPICSI)} | Output hold time, $\overline{\text{SPI_CS}}$ inactive to SPI_CLK inactive | 0.5t _C - 2.2 | | 0.5t _C - 2.2 | | ns |

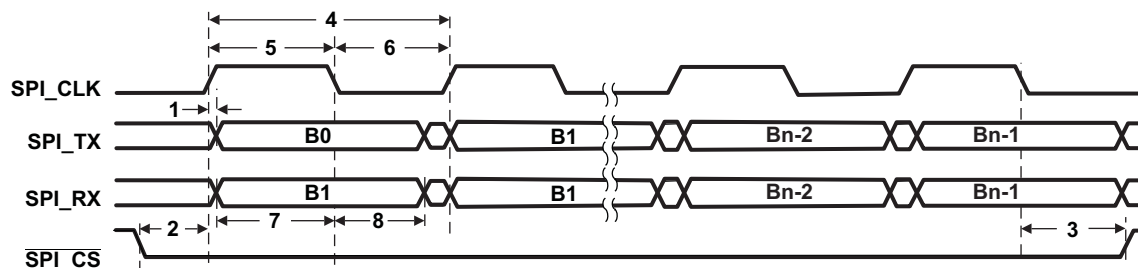
(1) D is the programmable data delay in ns. Data delay can be programmed to 0, 1, 2, or 3 SPICLK clock cycles.



A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.

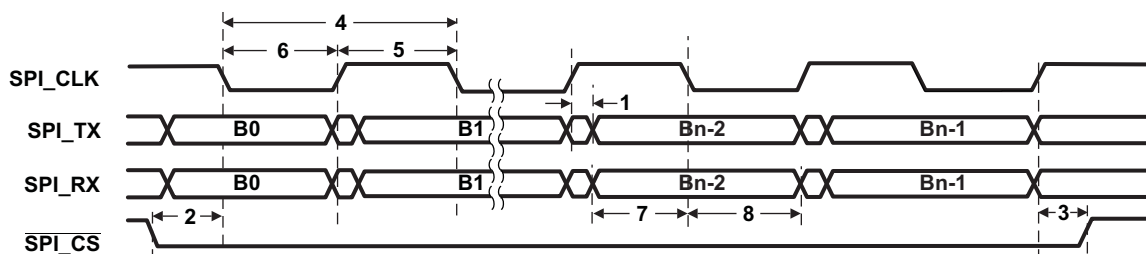
B. Polarity of SPI_CS_n is configurable, active-low polarity is shown.

Figure 5-39. SPI Mode 0 Transfer (CKP_n = 0, CKPH_n = 0)



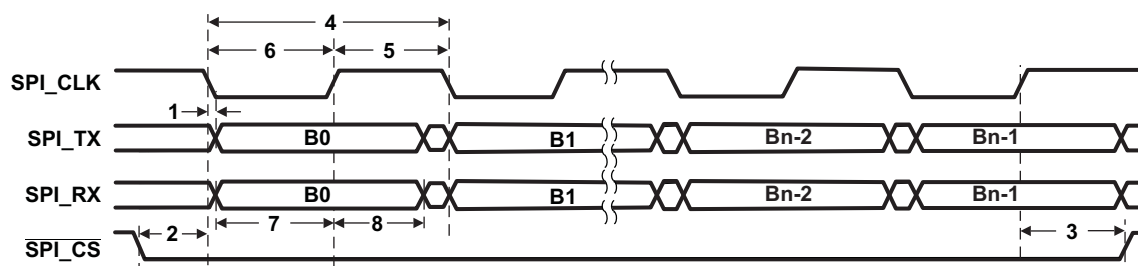
- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-40. SPI Mode 1 Transfer (CKPn = 0, CKPHn = 1)



- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-41. SPI Mode 2 Transfer (CKPn = 1, CKPHn = 0)



- A. Character length is programmable between 1 and 32 bits; 8-bit character length shown.
- B. Polarity of SPI_CSn is configurable, active-low polarity is shown.

Figure 5-42. SPI Mode 3 Transfer (CKPn = 1, CKPHn = 1)

5.18 Universal Serial Bus (USB) 2.0 Controller

The device USB2.0 peripheral supports the following features:

- USB2.0 peripheral at speeds high-speed (480 Mb/s) and full-speed (12 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous asynchronous mode)
- 4 Transmit (TX) and 4 Receive (RX) Endpoints in addition to Control Endpoint 0
- FIFO RAM
 - 4K endpoint
 - Programmable size
- Integrated USB2.0 High Speed PHY
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

The USB2.0 peripheral on this device, does *not* support:

- Host Mode (Peripheral/Device Modes supported *only*)
- On-Chip Charge Pump
- On-the-Go (OTG) Mode

5.18.1 USB2.0 Peripheral Register Descriptions

Table 5-48 lists of the USB2.0 peripheral registers.

Table 5-48. Universal Serial Bus (USB) Registers⁽¹⁾

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|-------------|--|
| 8000h | REVID1 | Revision Identification Register 1 |
| 8001h | REVID2 | Revision Identification Register 2 |
| 8004h | CTRLR | Control Register |
| 8008h | STATR | Status Register |
| 800Ch | EMUR | Emulation Register |
| 8010h | MODER1 | Mode Register 1 |
| 8011h | MODER2 | Mode Register 2 |
| 8014h | AUTOREQ | Auto Request Register |
| 8018h | SRPFIXTIME1 | SRP Fix Time Register 1 |
| 8019h | SRPFIXTIME2 | SRP Fix Time Register 2 |
| 801Ch | TEARDOWN1 | Teardown Register 1 |
| 801Dh | TEARDOWN2 | Teardown Register 2 |
| 8020h | INTSRCR1 | USB Interrupt Source Register 1 |
| 8021h | INTSRCR2 | USB Interrupt Source Register 2 |
| 8024h | INTSETR1 | USB Interrupt Source Set Register 1 |
| 8025h | INTSETR2 | USB Interrupt Source Set Register 2 |
| 8028h | INTCLRR1 | USB Interrupt Source Clear Register 1 |
| 8029h | INTCLRR2 | USB Interrupt Source Clear Register 2 |
| 802Ch | INTMSKR1 | USB Interrupt Mask Register 1 |
| 802Dh | INTMSKR2 | USB Interrupt Mask Register 2 |
| 8030h | INTMSKSETR1 | USB Interrupt Mask Set Register 1 |
| 8031h | INTMSKSETR2 | USB Interrupt Mask Set Register 2 |
| 8034h | INTMSKCLRR1 | USB Interrupt Mask Clear Register 1 |
| 8035h | INTMSKCLRR2 | USB Interrupt Mask Clear Register 2 |
| 8038h | INTMASKEDR1 | USB Interrupt Source Masked Register 1 |
| 8039h | INTMASKEDR2 | USB Interrupt Source Masked Register 2 |
| 803Ch | EOIR | USB End of Interrupt Register |
| 8040h | INTVECTR1 | USB Interrupt Vector Register 1 |
| 8041h | INTVECTR2 | USB Interrupt Vector Register 2 |
| 8050h | GREP1SZR1 | Generic RNDIS EP1Size Register 1 |
| 8051h | GREP1SZR2 | Generic RNDIS EP1Size Register 2 |
| 8054h | GREP2SZR1 | Generic RNDIS EP2 Size Register 1 |
| 8055h | GREP2SZR2 | Generic RNDIS EP2 Size Register 2 |
| 8058h | GREP3SZR1 | Generic RNDIS EP3 Size Register 1 |
| 8059h | GREP3SZR2 | Generic RNDIS EP3 Size Register 2 |
| 805Ch | GREP4SZR1 | Generic RNDIS EP4 Size Register 1 |
| 805Dh | GREP4SZR2 | Generic RNDIS EP4 Size Register 2 |

- (1) Before reading or writing to the USB registers, be sure to set the BYTEMODE bits to "00b" in the USB system control register to enable word accesses to the USB registers .

Table 5-48. Universal Serial Bus (USB) Registers⁽¹⁾ (continued)

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---------------------------------------|--|---|
| Common USB Registers | | |
| 8401h | FADDR_POWER | Function Address Register, Power Management Register |
| 8402h | INTRTX | Interrupt Register for Endpoint 0 plus Transmit Endpoints 1 to 4 |
| 8405h | INTRRX | Interrupt Register for Receive Endpoints 1 to 4 |
| 8406h | INTRTXE | Interrupt enable register for INTRTX |
| 8409h | INTRRXE | Interrupt Enable Register for INTRRX |
| 840Ah | INTRUSB_INTRUSBE | Interrupt Register for Common USB Interrupts, Interrupt Enable Register |
| 840Dh | FRAME | Frame Number Register |
| 840Eh | INDEX_TESTMODE | Index Register for Selecting the Endpoint Status and Control Registers, Register to Enable the USB 2.0 Test Modes |
| USB Indexed Registers | | |
| 8411h | TXMAXP_IND | Maximum Packet Size for Peripheral/Host Transmit Endpoint. (Index register set to select Endpoints 1-4) |
| 8412h | PERI_CSR0_IND | Control Status Register for Endpoint 0 in Peripheral Mode. (Index register set to select Endpoint 0) |
| | PERI_TXCSR_IND | Control Status Register for Peripheral Transmit Endpoint. (Index register set to select Endpoints 1-4) |
| 8415h | RXMAXP_IND | Maximum Packet Size for Peripheral/Host Receive Endpoint. (Index register set to select Endpoints 1-4) |
| 8416h | PERI_RXCSR_IND | Control Status Register for Peripheral Receive Endpoint. (Index register set to select Endpoints 1-4) |
| 8419h | COUNT0_IND | Number of Received Bytes in Endpoint 0 FIFO. (Index register set to select Endpoint 0) |
| | RXCOUNT_IND | Number of Bytes in Host Receive Endpoint FIFO. (Index register set to select Endpoints 1- 4) |
| 841Ah | - | Reserved |
| 841Dh | - | Reserved |
| 841Eh | CONFIGDATA_INDC (Upper byte of 841Eh) | Returns details of core configuration. (index register set to select Endpoint 0) |
| USB FIFO Registers | | |
| 8421h | FIFO0R1 | Transmit and Receive FIFO Register 1 for Endpoint 0 |
| 8422h | FIFO0R2 | Transmit and Receive FIFO Register 2 for Endpoint 0 |
| 8425h | FIFO1R1 | Transmit and Receive FIFO Register 1 for Endpoint 1 |
| 8426h | FIFO1R2 | Transmit and Receive FIFO Register 2 for Endpoint 1 |
| 8429h | FIFO2R1 | Transmit and Receive FIFO Register 1 for Endpoint 2 |
| 842Ah | FIFO2R2 | Transmit and Receive FIFO Register 2 for Endpoint 2 |
| 842Dh | FIFO3R1 | Transmit and Receive FIFO Register 1 for Endpoint 3 |
| 842Eh | FIFO3R2 | Transmit and Receive FIFO Register 2 for Endpoint 3 |
| 8431h | FIFO4R1 | Transmit and Receive FIFO Register 1 for Endpoint 4 |
| 8432h | FIFO4R2 | Transmit and Receive FIFO Register 2 for Endpoint 4 |
| Dynamic FIFO Control Registers | | |
| 8461h | - | Reserved |
| 8462h | TXFIFOSZ_RXFIFOSZ | Transmit Endpoint FIFO Size, Receive Endpoint FIFO Size (Index register set to select Endpoints 1-4) |
| 8465h | TXFIFOADDR | Transmit Endpoint FIFO Address (Index register set to select Endpoints 1-4) |
| 8466h | RXFIFOADDR | Receive Endpoint FIFO Address (Index register set to select Endpoints 1-4) |
| 846Dh | - | Reserved |

Table 5-48. Universal Serial Bus (USB) Registers⁽¹⁾ (continued)

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---|-------------------------------------|--|
| Control and Status Register for Endpoint 0 | | |
| 8501h | - | Reserved |
| 8502h | PERI_CSR0 | Control Status Register for Peripheral Endpoint 0 |
| 8505h | - | Reserved |
| 8506h | - | Reserved |
| 8509h | COUNT0 | Number of Received Bytes in Endpoint 0 FIFO |
| 850Ah | - | Reserved |
| 850Dh | - | Reserved |
| 850Eh | CONFIGDATA (Upper byte of 850Eh) | Returns details of core configuration. |
| Control and Status Register for Endpoint 1 | | |
| 8511h | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 8512h | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8515h | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 8516h | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| 8519h | RXCOUNT | Number of Bytes in the Receiving Endpoint's FIFO |
| 851Ah | - | Reserved |
| 851Dh | - | Reserved |
| 851Eh | - | Reserved |
| Control and Status Register for Endpoint 2 | | |
| 8521h | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 8522h | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8525h | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 8526h | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| 8529h | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 852Ah | - | Reserved |
| 852Dh | - | Reserved |
| 852Eh | - | Reserved |
| Control and Status Register for Endpoint 3 | | |
| 8531h | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 8532h | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8535h | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 8536h | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| 8539h | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 853Ah | - | Reserved |
| 853Dh | - | Reserved |
| 853Eh | - | Reserved |
| Control and Status Register for Endpoint 4 | | |
| 8541h | TXMAXP | Maximum Packet Size for Peripheral/Host Transmit Endpoint |
| 8542h | PERI_TXCSR | Control Status Register for Peripheral Transmit Endpoint (peripheral mode) |
| 8545h | RXMAXP | Maximum Packet Size for Peripheral/Host Receive Endpoint |
| 8546h | PERI_RXCSR | Control Status Register for Peripheral Receive Endpoint (peripheral mode) |
| 8549h | RXCOUNT | Number of Bytes in Host Receive endpoint FIFO |
| 854Ah | - | Reserved |
| 854Dh | - | Reserved |
| 854Eh | - | Reserved |

Table 5-48. Universal Serial Bus (USB) Registers⁽¹⁾ (continued)

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|----------------------------------|-----------------|--|
| CPPI DMA (CMDA) Registers | | |
| 9000h | - | Reserved |
| 9001h | - | Reserved |
| 9004h | TDFDQ | CDMA Teardown Free Descriptor Queue Control Register |
| 9008h | DMAEMU | CDMA Emulation Control Register |
| 9800h | TXGCR1[0] | Transmit Channel 0 Global Configuration Register 1 |
| 9801h | TXGCR2[0] | Transmit Channel 0 Global Configuration Register 2 |
| 9808h | RXGCR1[0] | Receive Channel 0 Global Configuration Register 1 |
| 9809h | RXGCR2[0] | Receive Channel 0 Global Configuration Register 2 |
| 980Ch | RXHPCR1A[0] | Receive Channel 0 Host Packet Configuration Register 1 A |
| 980Dh | RXHPCR2A[0] | Receive Channel 0 Host Packet Configuration Register 2 A |
| 9810h | RXHPCR1B[0] | Receive Channel 0 Host Packet Configuration Register 1 B |
| 9811h | RXHPCR2B[0] | Receive Channel 0 Host Packet Configuration Register 2 B |
| 9820h | TXGCR1[1] | Transmit Channel 1 Global Configuration Register 1 |
| 9821h | TXGCR2[1] | Transmit Channel 1 Global Configuration Register 2 |
| 9828h | RXGCR1[1] | Receive Channel 1 Global Configuration Register 1 |
| 9829h | RXGCR2[1] | Receive Channel 1 Global Configuration Register 2 |
| 982Ch | RXHPCR1A[1] | Receive Channel 1 Host Packet Configuration Register 1 A |
| 982Dh | RXHPCR2A[1] | Receive Channel 1 Host Packet Configuration Register 2 A |
| 9830h | RXHPCR1B[1] | Receive Channel 1 Host Packet Configuration Register 1 B |
| 9831h | RXHPCR2B[1] | Receive Channel 1 Host Packet Configuration Register 2 B |
| 9840h | TXGCR1[2] | Transmit Channel 2 Global Configuration Register 1 |
| 9841h | TXGCR2[2] | Transmit Channel 2 Global Configuration Register 2 |
| 9848h | RXGCR1[2] | Receive Channel 2 Global Configuration Register 1 |
| 9849h | RXGCR2[2] | Receive Channel 2 Global Configuration Register 2 |
| 984Ch | RXHPCR1A[2] | Receive Channel 2 Host Packet Configuration Register 1 A |
| 984Dh | RXHPCR2A[2] | Receive Channel 2 Host Packet Configuration Register 2 A |
| 9850h | RXHPCR1B[2] | Receive Channel 2 Host Packet Configuration Register 1 B |
| 9851h | RXHPCR2B[2] | Receive Channel 2 Host Packet Configuration Register 2 B |
| 9860h | TXGCR1[3] | Transmit Channel 3 Global Configuration Register 1 |
| 9861h | TXGCR2[3] | Transmit Channel 3 Global Configuration Register 2 |
| 9868h | RXGCR1[3] | Receive Channel 3 Global Configuration Register 1 |
| 9869h | RXGCR2[3] | Receive Channel 3 Global Configuration Register 2 |
| 986Ch | RXHPCR1A[3] | Receive Channel 3 Host Packet Configuration Register 1 A |
| 986Dh | RXHPCR2A[3] | Receive Channel 3 Host Packet Configuration Register 2 A |
| 9870h | RXHPCR1B[3] | Receive Channel 3 Host Packet Configuration Register 1 B |
| 9871h | RXHPCR2B[3] | Receive Channel 3 Host Packet Configuration Register 2 B |
| A000h | DMA_SCHED_CTRL1 | CDMA Scheduler Control Register 1 |
| A001h | DMA_SCHED_CTRL2 | CDMA Scheduler Control Register 1 |
| A800h + 4 × N | ENTRYLSW[N] | CDMA Scheduler Table Word N Registers LSW (N = 0 to 63) |
| A801h + 4 × N | ENTRYMSW[N] | CDMA Scheduler Table Word N Registers MSW (N = 0 to 63) |

Table 5-48. Universal Serial Bus (USB) Registers⁽¹⁾ (continued)

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|---------------------------------------|---------------|---|
| Queue Manager (QMGR) Registers | | |
| C000h | - | Reserved |
| C001h | - | Reserved |
| C008h | DIVERSION1 | Queue Manager Queue Diversion Register 1 |
| C009h | DIVERSION2 | Queue Manager Queue Diversion Register 2 |
| C020h | FDBSC0 | Queue Manager Free Descriptor/Buffer Starvation Count Register 0 |
| C021h | FDBSC1 | Queue Manager Free Descriptor/Buffer Starvation Count Register 1 |
| C024h | FDBSC2 | Queue Manager Free Descriptor/Buffer Starvation Count Register 2 |
| C025h | FDBSC3 | Queue Manager Free Descriptor/Buffer Starvation Count Register 3 |
| C028h | FDBSC4 | Queue Manager Free Descriptor/Buffer Starvation Count Register 4 |
| C029h | FDBSC5 | Queue Manager Free Descriptor/Buffer Starvation Count Register 5 |
| C02Ch | FDBSC6 | Queue Manager Free Descriptor/Buffer Starvation Count Register 6 |
| C02Dh | FDBSC7 | Queue Manager Free Descriptor/Buffer Starvation Count Register 7 |
| C080h | LRAM0BASE1 | Queue Manager Linking RAM Region 0 Base Address Register 1 |
| C081h | LRAM0BASE2 | Queue Manager Linking RAM Region 0 Base Address Register 2 |
| C084h | LRAM0SIZE | Queue Manager Linking RAM Region 0 Size Register |
| C085h | - | Reserved |
| C088h | LRAM1BASE1 | Queue Manager Linking RAM Region 1 Base Address Register 1 |
| C089h | LRAM1BASE2 | Queue Manager Linking RAM Region 1 Base Address Register 2 |
| C090h | PEND0 | Queue Manager Queue Pending 0 |
| C091h | PEND1 | Queue Manager Queue Pending 1 |
| C094h | PEND2 | Queue Manager Queue Pending 2 |
| C095h | PEND3 | Queue Manager Queue Pending 3 |
| C098h | PEND4 | Queue Manager Queue Pending 4 |
| C099h | PEND5 | Queue Manager Queue Pending 5 |
| D000h + 16 × R | QMEMRBASE1[R] | Queue Manager Memory Region R Base Address Register 1 (R = 0 to 15) |
| D001h + 16 × R | QMEMRBASE2[R] | Queue Manager Memory Region R Base Address Register 2 (R = 0 to 15) |
| D004h + 16 × R | QMEMRCTRL1[R] | Queue Manager Memory Region R Control Register (R = 0 to 15) |
| D005h + 16 × R | QMEMRCTRL2[R] | Queue Manager Memory Region R Control Register (R = 0 to 15) |
| E000h + 16 × N | CTRL1A | Queue Manager Queue N Control Register 1A (N = 0 to 63) |
| E001h + 16 × N | CTRL2A | Queue Manager Queue N Control Register 2A (N = 0 to 63) |
| E004h + 16 × N | CTRL1B | Queue Manager Queue N Control Register 1B (N = 0 to 63) |
| E005h + 16 × N | CTRL2B | Queue Manager Queue N Control Register 2B (N = 0 to 63) |
| E008h + 16 × N | CTRL1C | Queue Manager Queue N Control Register 1C (N = 0 to 63) |
| E009h + 16 × N | CTRL2C | Queue Manager Queue N Control Register 2C (N = 0 to 63) |
| E00Ch + 16 × N | CTRL1D | Queue Manager Queue N Control Register 1D (N = 0 to 63) |
| E00Dh + 16 × N | CTRL2D | Queue Manager Queue N Control Register 2D (N = 0 to 63) |
| E800h + 16 × N | QSTAT1A | Queue Manager Queue N Status Register 1A (N = 0 to 63) |
| E801h + 16 × N | QSTAT2A | Queue Manager Queue N Status Register 2A (N = 0 to 63) |
| E804h + 16 × N | QSTAT1B | Queue Manager Queue N Status Register 1B (N = 0 to 63) |
| E805h + 16 × N | QSTAT2B | Queue Manager Queue N Status Register 2B (N = 0 to 63) |
| E808h + 16 × N | QSTAT1C | Queue Manager Queue N Status Register 1C (N = 0 to 63) |
| E809h + 16 × N | QSTAT1C | Queue Manager Queue N Status Register 2C (N = 0 to 63) |

5.18.2 USB 2.0 Electrical Data/Timing

Table 5-49. Switching Characteristics Over Recommended Operating Conditions for USB 2.0 (see Figure 5-43)

| NO. | PARAMETER | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | | | UNIT |
|-----|----------------------|---|---|------|---------------------------------------|------|------|
| | | | FULL SPEED 12 Mbps | | HIGH SPEED 480 Mbps ⁽¹⁾ | | |
| | | | MIN | MAX | MIN | MAX | |
| 1 | t _{r(D)} | Rise time, USB_DP and USB_DM signals ⁽²⁾ | 4 | 20 | 0.5 | | ns |
| 2 | t _{f(D)} | Fall time, USB_DP and USB_DM signals ⁽²⁾ | 4 | 20 | 0.5 | | ns |
| 3 | t _{r/fM} | Rise/Fall time, matching ⁽³⁾ | 90 | 111 | – | – | % |
| 4 | V _{CRS} | Output signal cross-over voltage ⁽²⁾ | 1.3 | 2 | – | – | V |
| 7 | t _{w(EOPT)} | Pulse duration, EOP transmitter ⁽⁴⁾ | 160 | 175 | – | – | ns |
| 8 | t _{w(EOPR)} | Pulse duration, EOP receiver ⁽⁴⁾ | 82 | | – | | ns |
| 9 | t _(DRATE) | Data Rate | | 12 | | 480 | Mb/s |
| 10 | Z _{DRV} | Driver Output Resistance | 40.5 | 49.5 | 40.5 | 49.5 | Ω |
| 11 | Z _{INP} | Receiver Input Impedance | 100k | | - | - | Ω |

(1) For more detailed information, see the Universal Serial Bus Specification, Revision 2.0, Chapter 7.

(2) Full Speed and High Speed $C_L = 50\text{ pF}$

(3) $t_{RFM} = (t_r/t_f) \times 100$. [Excluding the first transaction from the Idle state.]

(4) Must accept as valid EOP

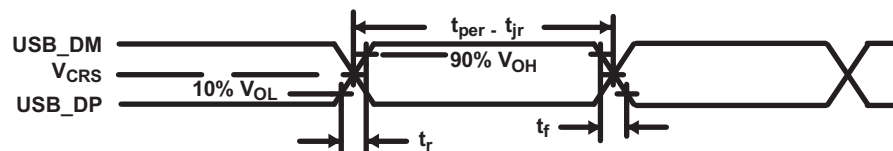


Figure 5-43. USB2.0 Integrated Transceiver Interface Timing

5.19 General-Purpose Timers

The device has three 32-bit software programmable Timers. Each timer can be used as a general-purpose (GP) timer. Timer2 can be configured as either a GP or a Watchdog (WD) or both. General-purpose timers are typically used to provide interrupts to the CPU to schedule periodic tasks or a delayed task. A watchdog timer is used to reset the CPU in case it gets into an infinite loop. The GP timers are 32-bit timers with a 13-bit prescaler that can divide the CPU clock and uses this scaled value as a reference clock. These timers can be used to generate periodic interrupts. The Watchdog Timer is a 16-bit counter with a 16-bit prescaler used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

The device Timers support the following:

- 32-bit Programmable Countdown Timer
- 13-bit Prescaler Divider
- Timer Modes:
 - 32-bit General-Purpose Timer
 - 32-bit Watchdog Timer (Timer2 only)
- Auto Reload Option
- Generates Single Interrupt to CPU (The interrupt is individually latched to determine which timer triggered the interrupt.)
- Generates Active Low Pulse to the Hardware Reset (Watchdog *only*)
- Interrupt can be used for DMA Event

5.19.1 Timers Peripheral Register Descriptions

Table 5-50 through Table 5-53 show the Timer and Watchdog registers.

Table 5-50. Watchdog Timer Registers (Timer2 *only*)

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|---------|------------------------------------|
| 1880h | WDKCKLK | Watchdog Kick Lock Register |
| 1882h | WDKICK | Watchdog Kick Register |
| 1884h | WDSVLR | Watchdog Start Value Lock Register |
| 1886h | WDSVR | Watchdog Start Value Register |
| 1888h | WDENLOK | Watchdog Enable Lock Register |
| 188Ah | WDEN | Watchdog Enable Register |
| 188Ch | WDPSLR | Watchdog Prescale Lock Register |
| 188Eh | WDPS | Watchdog Prescale Register |

Table 5-51. General-Purpose Timer 0 Registers

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|---------|----------------------------|
| 1810h | TCR | Timer 0 Control Register |
| 1812h | TIMPRD1 | Timer 0 Period Register 1 |
| 1813h | TIMPRD2 | Timer 0 Period Register 2 |
| 1814h | TIMCNT1 | Timer 0 Counter Register 1 |
| 1815h | TIMCNT2 | Timer 0 Counter Register 2 |

Table 5-52. General-Purpose Timer 1 Registers

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|---------|----------------------------|
| 1850h | TCR | Timer 1 Control Register |
| 1852h | TIMPRD1 | Timer 1 Period Register 1 |
| 1853h | TIMPRD2 | Timer 1 Period Register 2 |
| 1854h | TIMCNT1 | Timer 1 Counter Register 1 |
| 1855h | TIMCNT2 | Timer 1 Counter Register 2 |

Table 5-53. General-Purpose Timer 2 Registers

| CPU WORD ADDRESS | ACRONYM | REGISTER DESCRIPTION |
|------------------|---------|----------------------------|
| 1890h | TCR | Timer 2 Control Register |
| 1892h | TIMPRD1 | Timer 2 Period Register 1 |
| 1893h | TIMPRD2 | Timer 2 Period Register 2 |
| 1894h | TIMCNT1 | Timer 2 Counter Register 1 |
| 1895h | TIMCNT2 | Timer 2 Counter Register 2 |

5.20 General-Purpose Input/Output

The GPIO peripheral provides general-purpose pins that can be configured as either inputs or outputs. When configured as an output, you can write to an internal register to control the state driven on the output pin. When configured as an input, you can detect the state of the input by reading the state of the internal register. The GPIO can also be used to send interrupts to the CPU.

The GPIO peripheral supports the following:

- Up to 26 GPIOs plus 1 general-purpose output (XF) and 4 Special-Purpose Outputs for Use With SAR
- The 26 GPIO pins have internal pulldowns (IPDs) which can be individually disabled
- The 26 GPIOs can be configured to generate edge detected interrupts to the CPU on either the rising or falling edge

The device GPIO pin functions are multiplexed with various other signals. For more detailed information on what signals are multiplexed with the GPIO and how to configure them, see [Section 2.5, Terminal Functions](#) and [Section 3, Device Configuration](#) of this document.

5.20.1 General-Purpose Input/Output Peripheral Register Descriptions

The external parallel port interface includes a 16-bit general purpose I/O that can be individually programmed as input or output with interrupt capability. Control of the general purpose I/O is maintained through a set of I/O memory-mapped registers shown in [Table 5-54](#).

Table 5-54. GPIO Registers

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME |
|----------------------|------------|---|
| 1C06h | IODIR1 | GPIO Direction Register 1 |
| 1C07h | IODIR2 | GPIO Direction Register 2 |
| 1C08h | IOINDATA1 | GPIO Data In Register 1 |
| 1C09h | IOINDATA2 | GPIO Data In Register 2 |
| 1C0Ah | IODATAOUT1 | GPIO Data Out Register 1 |
| 1C0Bh | IODATAOUT2 | GPIO Data Out Register 2 |
| 1C0Ch | IOINTEDG1 | GPIO Interrupt Edge Trigger Enable Register 1 |
| 1C0Dh | IOINTEDG2 | GPIO Interrupt Edge Trigger Enable Register 2 |
| 1C0Eh | IOINTEN1 | GPIO Interrupt Enable Register 1 |
| 1C0Fh | IOINTEN2 | GPIO Interrupt Enable Register 2 |
| 1C10h | IOINTFLG1 | GPIO Interrupt Flag Register 1 |
| 1C11h | IOINTFLG2 | GPIO Interrupt Flag Register 2 |

5.20.2 GPIO Peripheral Input/Output Electrical Data/Timing

Table 5-55. Timing Requirements for GPIO Inputs⁽¹⁾ (see Figure 5-44)

| NO. | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|---|---|-----|------|
| | | MIN | MAX | |
| 1 | t _{w(ACTIVE)} Pulse duration, GPIO input/external interrupt pulse active | 2C ⁽¹⁾⁽²⁾ | | ns |
| 2 | t _{w(INACTIVE)} Pulse duration, GPIO input/external interrupt pulse inactive | C ⁽¹⁾⁽²⁾ | | ns |

(1) The pulse width given is sufficient to get latched into the GPIO_IFR register and to generate an interrupt. However, if a user wants to have the device recognize the GPIO changes through software polling of the GPIO Data In (GPIO_DIN) register, the GPIO duration must be extended to allow the device enough time to access the GPIO register through the internal bus.

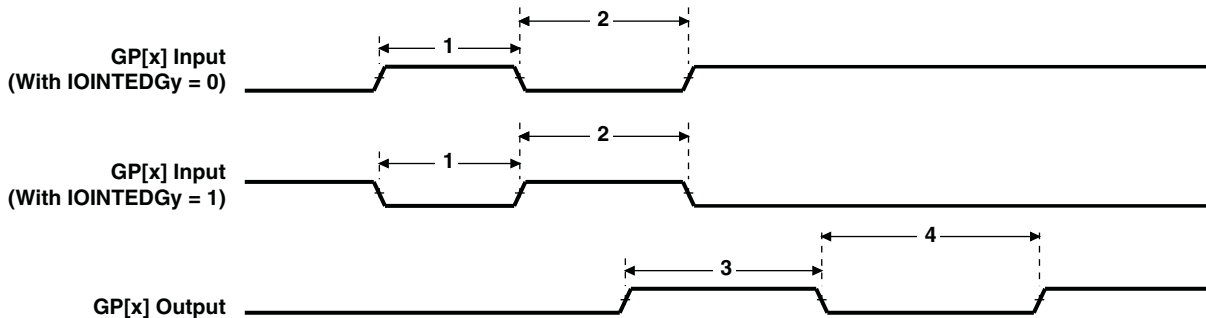
(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.

Table 5-56. Switching Characteristics Over Recommended Operating Conditions for GPIO Outputs (see Figure 5-44)

| NO. | PARAMETER | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|--|---|-----|------|
| | | MIN | MAX | |
| 3 | t _{w(GPOH)} Pulse duration, GP[x] output high | 3C ⁽¹⁾⁽²⁾ | | ns |
| 4 | t _{w(GPOL)} Pulse duration, GP[x] output low | 3C ⁽¹⁾⁽²⁾ | | ns |

(1) This parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.

(2) C = SYSCLK period in ns. For example, when running parts at 100 MHz, use C = 10 ns.


Figure 5-44. GPIO Port Timing

5.20.3 GPIO Peripheral Input Latency Electrical Data/Timing

Table 5-57. Timing Requirements for GPIO Input Latency⁽¹⁾

| NO. | | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|--|---------------------------|---|-----|------|
| | | | MIN | MAX | |
| 1 | t _{L(GPI)} Latency, GP[x] input | Polling GPIO_DIN register | 5 | | cyc |
| | | Polling GPIO_IFR register | 7 | | cyc |
| | | Interrupt Detection | 8 | | cyc |

- (1) The pulse width given is sufficient to generate a CPU interrupt. However, if a user wants to have the device recognize the GP[x] input changes through software polling of the GPIO register, the GP[x] input duration must be extended to allow device enough time to access the GPIO register through the internal bus.

5.21 IEEE 1149.1 JTAG

The JTAG interface is used for Boundary-Scan testing and emulation of the device.

$\overline{\text{TRST}}$ should only to be deasserted when it is necessary to use a JTAG controller to debug the device or exercise the device's boundary scan functionality.

The device includes an internal pulldown (IPD) on the $\overline{\text{TRST}}$ pin to ensure that $\overline{\text{TRST}}$ will always be asserted upon power up and the device's internal emulation logic will always be properly initialized. It is also recommended that an external pulldown be added to ensure proper device operation when an emulation or boundary scan JTAG controller is not connected to the JTAG pins. JTAG controllers from Texas Instruments actively drive $\overline{\text{TRST}}$ high. However, some third-party JTAG controllers may not drive $\overline{\text{TRST}}$ high but expect the use of a pullup resistor on $\overline{\text{TRST}}$. When using this type of JTAG controller, assert $\overline{\text{TRST}}$ to initialize the device after powerup and externally drive $\overline{\text{TRST}}$ high before attempting any emulation or boundary scan operations. The device will not operate properly if $\overline{\text{TRST}}$ is not asserted low during powerup.

5.21.1 JTAG ID (JTAGID) Register Descriptions

Table 5-58. JTAG ID Register

| HEX ADDRESS RANGE | ACRONYM | REGISTER NAME | COMMENTS |
|-------------------|---------|------------------------------|---|
| N/A | JTAGID | JTAG Identification Register | Read-only. Provides 32-bit JTAG ID of the device. |

The JTAG ID register is a read-only register that identifies to the customer the JTAG/Device ID. The register hex value for the device is: 0x01B8F E02F. For the actual register bit names and their associated bit field descriptions, see [Figure 5-45](#) and [Table 5-59](#).

| 31-28 | 27-12 | 11-1 | 0 |
|-----------------|-----------------------|-----------------------|-----|
| VARIANT (4-Bit) | PART NUMBER (16-Bit) | MANUFACTURER (11-Bit) | LSB |
| R-0001 | R-1011 1000 1111 1110 | R-0000 0010 111 | R-1 |

LEGEND: R = Read, W = Write, n = value at reset

Figure 5-45. JTAG ID Register Description - C5515 Register Value - 0x01B8F E02F

Table 5-59. JTAG ID Register Selection Bit Descriptions

| BIT | NAME | DESCRIPTION |
|-------|--------------|--|
| 31:28 | VARIANT | Variant (4-Bit) value: 0001. |
| 27:12 | PART NUMBER | Part Number (16-Bit) value: 1011 1000 1111 1110. |
| 11:1 | MANUFACTURER | Manufacturer (11-Bit) value: 0000 0010 111. |
| 0 | LSB | LSB. This bit is read as a "1". |

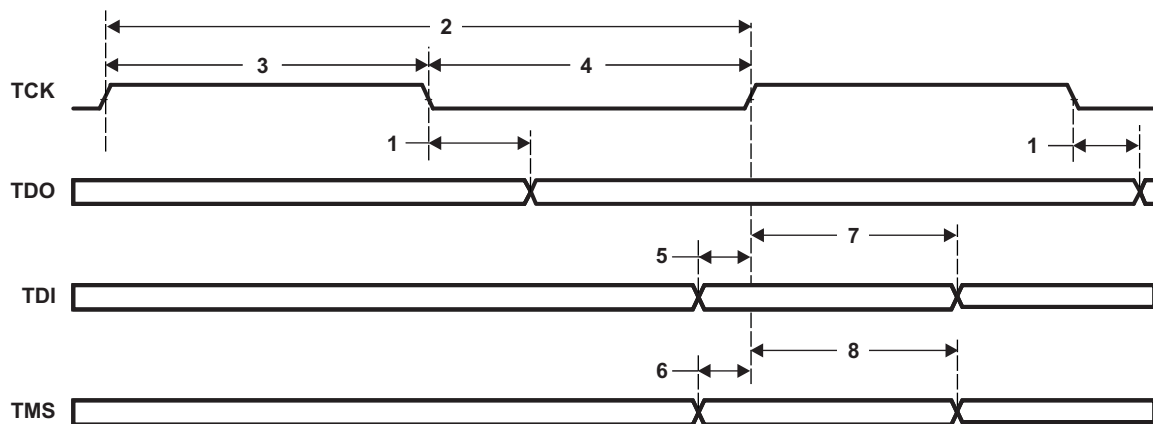
5.21.2 JTAG Test_port Electrical Data/Timing

Table 5-60. Timing Requirements for JTAG Test Port (see Figure 5-46)

| NO. | | | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|-----------------------------|---------------------------------------|---|-----|------|
| | | | MIN | MAX | |
| 2 | t _c (TCK) | Cycle time, TCK | 60 | | ns |
| 3 | t _w (TCKH) | Pulse duration, TCK high | 24 | | ns |
| 4 | t _w (TCKL) | Pulse duration, TCK low | 24 | | ns |
| 5 | t _{su} (TDIV-TCKH) | Setup time, TDI valid before TCK high | 10 | | ns |
| 6 | t _{su} (TMSV-TCKH) | Setup time, TMS valid before TCK high | 6 | | ns |
| 7 | t _h (TCKH-TDIV) | Hold time, TDI valid after TCK high | 5 | | ns |
| 8 | t _h (TCKH-TDIV) | Hold time, TMS valid after TCK high | 4 | | ns |

Table 5-61. Switching Characteristics Over Recommended Operating Conditions for JTAG Test Port (see Figure 5-46)

| NO. | PARAMETER | CV _{DD} = 1.05 V CV _{DD} = 1.3 V | | UNIT |
|-----|----------------------------|---|------|------|
| | | MIN | MAX | |
| 1 | t _d (TCKL-TDOV) | | 30.5 | ns |

**Figure 5-46. JTAG Test-Port Timing**

6 Device and Documentation Support

6.1 Device Support

6.1.1 Development Support

TI offers an extensive line of development tools for the TMS320C55x DSP platform, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of TMS320C55x fixed-point DSP-based applications:

Software Development Tools:

Code Composer Studio™ Integrated Development Environment (IDE): Version 3.3 or later

C/C++/Assembly Code Generation, and Debug plus additional development tools

Scalable, Real-Time Foundation Software (DSP/BIOS™ Version 5.33 or later), which provides the basic run-time target software needed to support any DSP application.

Hardware Development Tools:

Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TMS320C55x DSP platform, visit the Texas Instruments web site on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

6.1.2 Device and Development-Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all DSP devices and support tools. Each DSP commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., TMS320C5515AZCHA12). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications.

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification.

TMS Fully-qualified production device.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

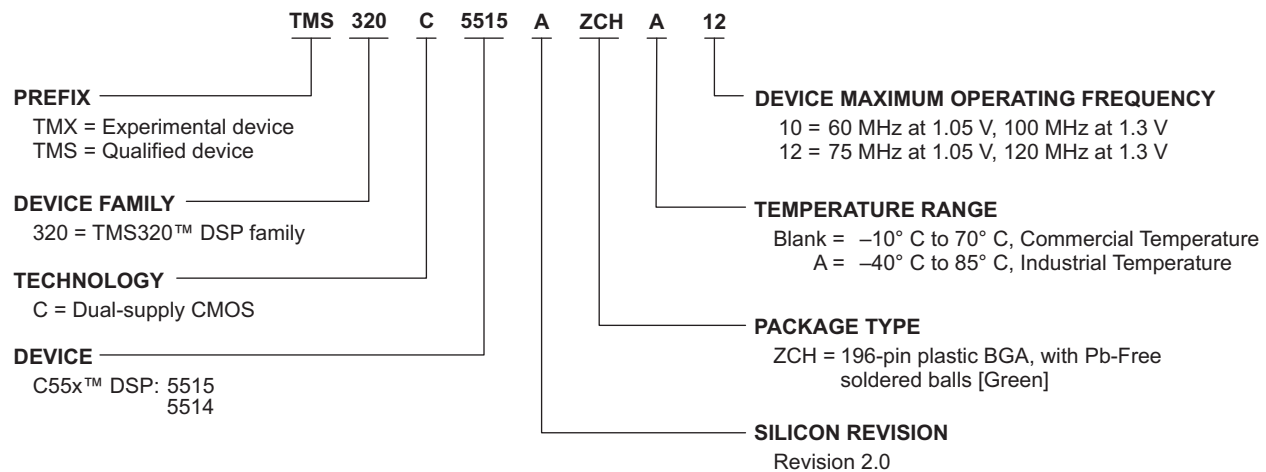
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, ZCH), and the temperature range (for example, "Blank" is the commercial temperature range).

Figure 6-1 provides a legend for reading the complete device name for any DSP platform member.



A. For actual device part numbers (P/Ns) and ordering information, see the TI website (<http://www.ti.com>)

Figure 6-1. Device Nomenclature

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7 Mechanical Packaging and Orderable Information

The following table shows the thermal resistance characteristics for the PBGA–ZCH mechanical package.

7.1 Thermal Data for ZCH

Table 7-1. Thermal Resistance Characteristics (PBGA Package) [ZCH]

| NO. | | | | °C/W ⁽¹⁾ | AIR FLOW (m/s) ⁽²⁾ |
|-----|-------------------|-------------------------|------|---------------------|----------------------------------|
| 1 | R _{ΘJC} | Junction-to-case | 1S0P | 6.74 | N/A |
| 2 | R _{ΘJB} | Junction-to-board | 1S0P | 14.5 | N/A |
| | | | 2S2P | 13.8 | |
| 3 | R _{ΘJA} | Junction-to-free air | 1S0P | 57.0 | 0.00 |
| | | | 2S2P | 33.4 | |
| 4 | R _{ΘJMA} | Junction-to-moving air | | | 0.50 |
| 5 | | | | | 1.00 |
| 6 | | | | | 2.00 |
| 7 | | | | | 3.00 |
| 8 | Psi _{JT} | Junction-to-package top | | 0.09 | 0.00 |
| 9 | | | | | 0.50 |
| 10 | | | | | 1.00 |
| 11 | | | | | 2.00 |
| 12 | Psi _{JB} | Junction-to-board | | | 3.00 |
| 13 | | | | 13.7 | 0.00 |
| 14 | | | | | 0.50 |
| 15 | | | | | 1.00 |
| 16 | | | | | 2.00 |
| 17 | | | | | 3.00 |

(1) These measurements were conducted in a JEDEC defined 2S2P system and will change based on environment as well as application. For more information, see these EIA/JEDEC standards – EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)* and JESD51-7, *High Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages*.

(2) m/s = meters per second

7.2 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device. This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TMS320C5515AZCH10 | ACTIVE | NFBGA | ZCH | 196 | 184 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -10 to 70 | 15AZCH10 | Samples |
| TMS320C5515AZCH12 | ACTIVE | NFBGA | ZCH | 196 | 184 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -10 to 70 | 15AZCH12 | Samples |
| TMS320C5515AZCHA10 | ACTIVE | NFBGA | ZCH | 196 | 184 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | 15AZCHA10 | Samples |
| TMS320C5515AZCHA12 | ACTIVE | NFBGA | ZCH | 196 | 184 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | 15AZCHA12 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

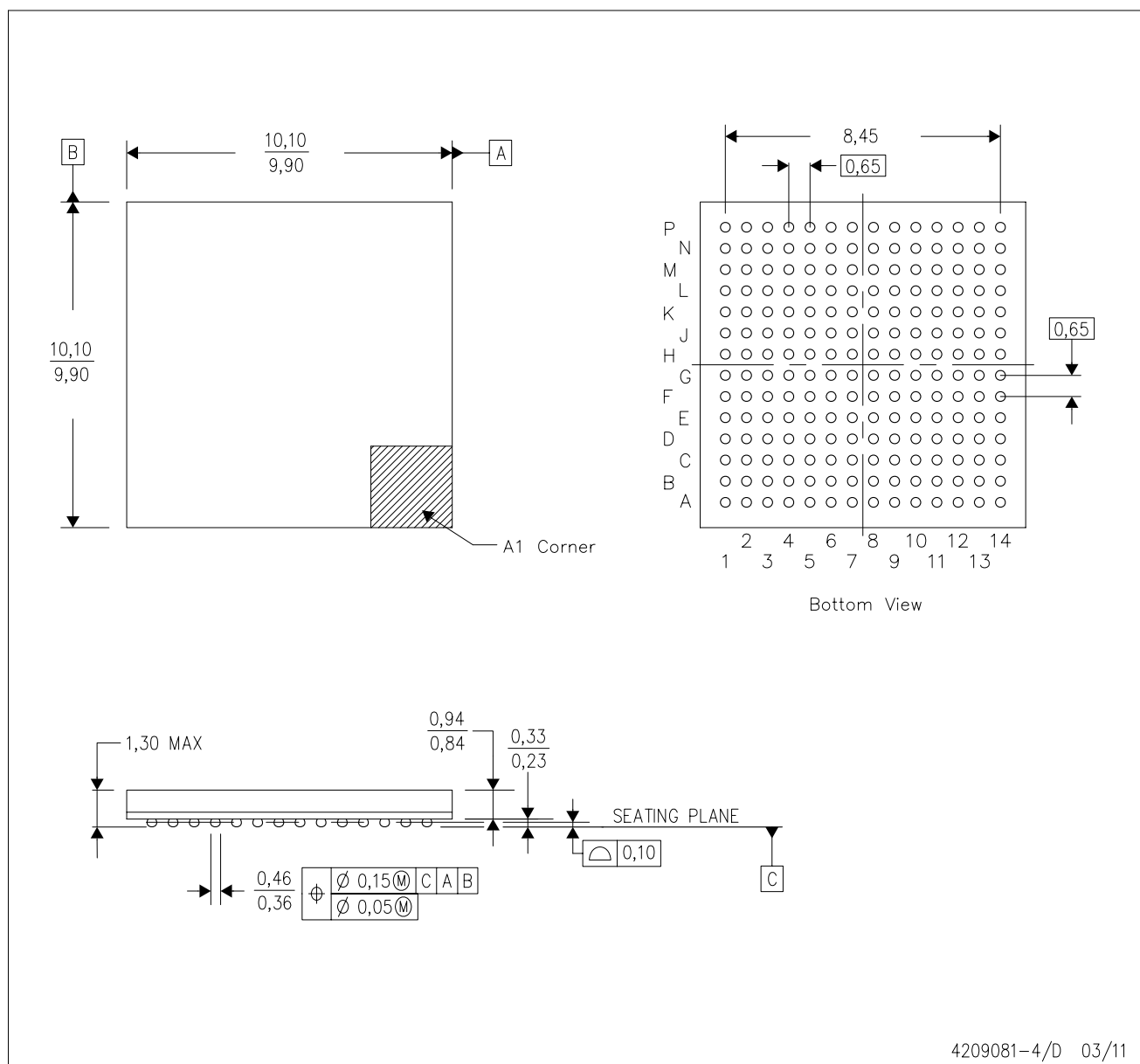
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ZCH (S-PBGA-N196)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. nFBGA configuration
 - D. This is a Pb-free solder ball design.

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