TPS6526x 4.5V to 18V Input Voltage, 3A/2A/2A Output Current Triple Synchronous Step-Down Converter

1 Features

- Operating Input Supply Voltage Range (4.5 V to 18 V)
- Feedback Reference Voltage 0.6V±1%
- Maximum Continuous Output Current 3A/2A/2A
- Adjustable Clock Frequency from 250kHz to 2MHz
- Dedicated Enable and Soft Start Pins for Each Buck
- Automatic Power-up/Power-down Sequence
- Pulse Skipping Mode (PSM) at Light Load (TPS65261 only)
- Output Voltage Power Good Indicator
- Input Voltage Power Failure Indicator
- Thermal Overloading Protection

2 Applications

- DTV
- Set Top Boxes
- Home Gateway and Access Point Networks
- Wireless Routers
- Surveillance
- POS Machine

3 Description

The TPS65261, TPS65261-1 is a monolithic triple synchronous step-down (buck) converter with 3A/2A/2A output currents. A wide 4.5V to 18V input supply voltage range encompasses the most intermediate bus voltages operating off 5V, 9V, 12V or 15V power bus. The converter, with constant frequency peak current mode, is designed to simplify its application while giving designers options to optimize the system according to targeted applications. The switching frequency of the converters can be adjusted from 250kHz to 2MHz with an external resistor. The 180° out-of-phase operation between Buck1 and Buck2, 3 (Buck2 and 3 run in phase) minimizes the input filter requirements.

The TPS65261, TPS65261-1 features an automatic power sequence with connecting MODE pin to V7V and configuring EN1/2/3 pins. The device also features an open drain RESET signal to monitor power down.

At light load, the TPS65261 automatically operates in pulse skipping mode (PSM) and the TPS65261-1 operates in force continuous current mode (FCC). PSM mode provides high efficiency by reducing switching losses at light loads and FCC mode reduces noise susceptibility and RF interference.

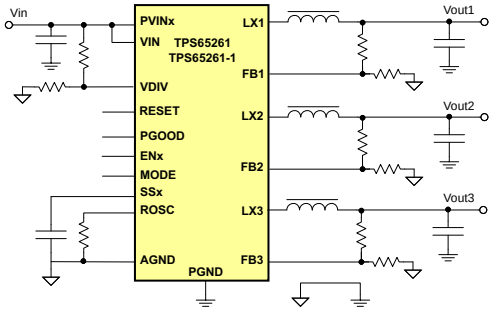
The device features overvoltage protection, overcurrent and short-circuit protection and over-temperature protection. A power good pin asserts when any output voltages are out of regulation.

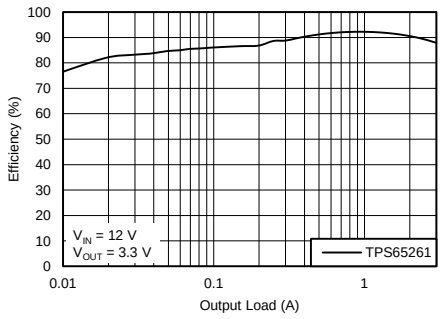
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65261, TPS65261-1	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Typical Application





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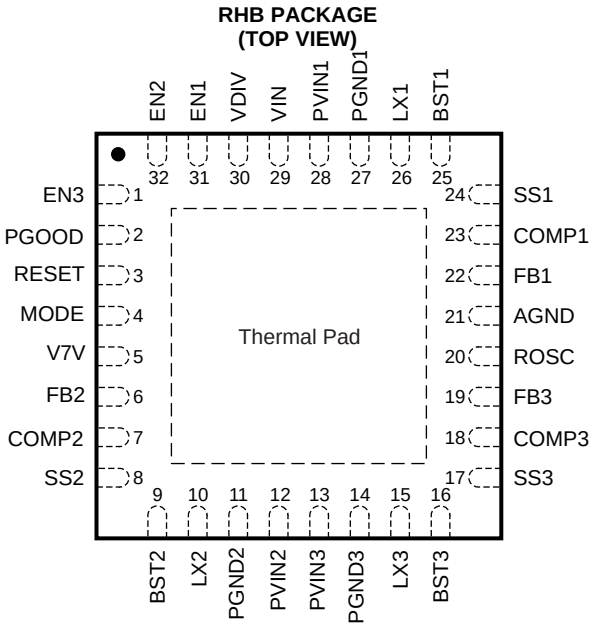
5 Revision History

Changes from Revision A (December 2013) to Revision B **Page**

- Changed all text, tables and graphics to match the new data sheet template. ... 1
- Changed Figure 70 ... 35

6 Pin Configuration and Functions



(There is no electric signal down bonded to thermal pad inside IC.
Exposed thermal pad must be soldered to PCB for optimal thermal performance.)

Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	EN3	Enable for buck3. Float to enable. Can use this pin to adjust the input under-voltage lockout of buck3 with a resistor divider.
2	PGOOD	An open drain output, asserts low if output voltage of any buck beyond regulation range due to thermal shutdown, over-current, under-voltage or ENx shut down.
3	RESET	Open drain power failure output signal.
4	MODE	When high, an automatic power-up/power-down sequence is provided according to states of EN1, EN2 and EN3 pins.
5	V7V	Internal LDO for gate driver and internal controller. Connect a 1µF capacitor from the pin to power ground
6	FB2	Feedback Kelvin sensing pin for buck2 output voltage. Connect this pin to buck2 resistor divider.
7	COMP2	Error amplifier output and Loop compensation pin for buck2. Connect a series resistor and capacitor to compensate the control loop of buck2 with peak current PWM mode.
8	SS2	Soft-start and tracking input for buck2. An internal 5µA pull-up current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
9	BST2	Boot strapped supply to the high side floating gate driver in buck2. Connect a capacitor (recommend 47nF) from BST2 pin to LX2 pin.
10	LX2	Switching node connection to the inductor and bootstrap capacitor for buck2. The voltage swing at this pin is from a diode voltage below the ground up to PVIN2 voltage.
11	PGND2	Power ground connection of buck2. Connect PGND2 pin as close as practical to the (–) terminal of VIN2 input ceramic capacitor.
12	PVIN2	Input power supply for buck2. Connect PVIN2 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10µF).
13	PVIN3	Input power supply for buck3. Connect PVIN3 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10µF).
14	PGND3	Power ground connection of buck3. Connect PGND3 pin as close as practical to the (–) terminal of VIN3 input ceramic capacitor.
15	LX3	Switching node connection to the inductor and bootstrap capacitor for buck3. The voltage swing at this pin is from a diode voltage below the ground up to PVIN3 voltage.

Pin Functions (continued)

PIN		DESCRIPTION
NO.	NAME	
16	BST3	Boot strapped supply to the high side floating gate driver in buck3. Connect a capacitor (recommend 47nF) from BST3 pin to LX3 pin.
17	SS3	Soft-start and tracking input for buck3. An internal 5µA pull-up current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
18	COMP3	Error amplifier output and Loop compensation pin for buck3. Connect a series resistor and capacitor to compensate the control loop of buck3 with peak current PWM mode.
19	FB3	Feedback Kelvin sensing pin for buck3 output voltage. Connect this pin to buck3 resistor divider.
20	ROSC	Oscillator frequency programmable pin. Connect an external resistor to set the switching frequency.
21	AGND	Analog ground common to buck controllers and other analog circuits. It must be routed separately from high current power grounds to the (–) terminal of bypass capacitor of input voltage VIN.
22	FB1	Feedback Kelvin sensing pin for buck1 output voltage. Connect this pin to buck1 resistor divider.
23	COMP1	Error amplifier output and Loop compensation pin for buck1. Connect a series resistor and capacitor to compensate the control loop of buck1 with peak current PWM mode.
24	SS1	Soft-start and tracking input for buck1. An internal 5µA pull-up current source is connected to this pin. The soft-start time can be programmed by connecting a capacitor between this pin and ground.
25	BST1	Boot strapped supply to the high side floating gate driver in buck1. Connect a capacitor (recommend 47nF) from BST1 pin to LX1 pin.
26	LX1	Switching node connection to the inductor and bootstrap capacitor for buck1. The voltage swing at this pin is from a diode voltage below the ground up to PVIN1 voltage.
27	PGND1	Power ground connection of Buck1. Connect PGND1 pin as close as practical to the (–) terminal of VIN1 input ceramic capacitor.
28	PVIN1	Input power supply for buck1. Connect PVIN1 pin as close as practical to the (+) terminal of an input ceramic capacitor (suggest 10µF).
29	VIN	Buck controller power supply.
30	VDIV	Input voltage threshold for power failure detection of input voltage.
31	EN1	Enable for buck1. Float to enable. Can use this pin to adjust the input under-voltage lockout of buck1 with a resistor divider.
32	EN2	Enable for buck2. Float to enable. Can use this pin to adjust the input under-voltage lockout of buck2 with a resistor divider.
	PAD	There is no electric signal down bonded to thermal pad inside IC. Exposed thermal pad must be soldered to PCB for optimal thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
PVIN1, PVIN2, PVIN3,VIN	–0.3	20	V
LX1, LX2, LX3 (Maximum withstand voltage transient < 20 ns)	–1.0	20	V
BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	–0.3	7	V
EN1, EN2, EN3, PGOOD, V7V, MODE, RESET, VDIV	–0.3	7	V
FB1, FB2, FB3, COMP1 , COMP2, COMP3, SS1, SS2, SS3, ROSC	–0.3	3.6	V
AGND, PGND1, PGND2, PGND3	–0.3	0.3	V
Operating junction temperature, T_J	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	-2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	-500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	PVIN1, PVIN2, PVIN3,VIN	4.5		18	V
	LX1, LX2, LX3 (Maximum withstand voltage transient < 20 ns)	-0.8		18	V
	BST1, BST2, BST3 referenced to LX1, LX2, LX3 pins respectively	-0.1		6.8	V
	EN1, EN2, EN3, PGOOD, V7V, MODE, RESET, VDIV	-0.1		6.3	V
	FB1, FB2, FB3, COMP1 , COMP2, COMP3, SS1, SS2, SS3, ROSC	-0.1		3	V
T_A	Operating junction temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS65261 RHB (32 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	6.1	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range		4.5		18	V
UVLO	VIN under-voltage lockout	VIN rising	4	4.25	4.5	V
		VIN falling	3.5	3.75	4	
		Hysteresis		500		mV
IDD_{SDN}	Shutdown supply current	EN1=EN2=EN3=MODE=0V		9.2		µA
IDD_{Q_NSW}	Input quiescent current without buck1/2/3 switching	EN1=EN2=EN3=5V, FB1=FB2=FB3=0.8V		605		µA
IDD_{Q_NSW1}		EN1=5V, EN2=EN3=0V, FB1=0.8V		330		µA
IDD_{Q_NSW2}		EN2=5V, EN1=EN3=0V, FB2=0.8V		330		µA
IDD_{Q_NSW3}		EN3=5V, EN1=EN2=0V, FB3=0.8V		330		µA
V_{7V}	V7V LDO output voltage	V_{7V} load current=0A	6	6.3	6.6	V
I_{OCP_V7V}	V7V LDO current limit			175		mA
FEEDBACK VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{COMP} = 1.2 V, T_J = 25°C	0.596	0.6	0.605	V
		V_{COMP} = 1.2 V, T_J = -40°C to 125°C	0.594	0.6	0.606	V
$V_{LINEREG\_BUCK}$	Line regulation-DC	I_{OUT1} = 1.5A, I_{OUT2} = 1A, I_{OUT3} = 1A 5V < PVINx < 18V		0.002		%/V
$V_{LOADREG\_BUCK}$	Load regulation-DC	I_{OUTx} = (10–100%) × I_{OUTx_max}		0.02		%/A
Buck1, Buck2, Buck3						
V_{ENXH}	EN1/2/3 high level input voltage			1.2	1.26	V
V_{ENXL}	EN1/2/3 low level input voltage		1.1	1.15		V
I_{ENX1}	EN1/2/3 pull-up current	ENx = 1V		3.6		µA
I_{ENX2}	EN1/2/3 pull-up current	ENx = 1.5V		6.6		µA
I_{ENhys}	Hysteresis current			3		µA
I_{SSX}	Soft start charging current		4.3	5	6	µA
T_{ON_MIN}	Minimum on time			80	100	ns
G_{m_EA}	Error amplifier trans-conductance	–2 µA < I_{COMPX} < 2 µA		300		µS
$G_{m\_PS1/2/3}$	COMP1/2/3 voltage to inductor current Gm	I_{LX} = 0.5 A		7.4		A/V
I_{LIMIT1}	Buck1 peak inductor current limit		4.33	5.1	6.02	A
$I_{LIMITSOURCE1}$	Buck1 low side source current limit			4.3		A
$I_{LIMITSINK1}$	Buck1 low side sink current limit			1.3		A
$I_{LIMIT2/3}$	Buck2/3 peak inductor current limit		2.6	3.1	3.73	A
$I_{LIMITSOURCE2/3}$	Buck2/3 low side source current limit			2.7		A
$I_{LIMITSINK2/3}$	Buck2/3 low side sink current limit			1		A
T_{Hiccup_wait}	Over current wait time			256		cycles
T_{Hiccup_re}	Hiccup time before re-start			8192		cycles
Rdson_HS1	Buck1 High-side switch resistance	VIN = 12V		100		mΩ
Rdson_LS1	Buck1 low-side switch resistance	VIN = 12V		65		mΩ
Rdson_HS2	Buck2 High-side switch resistance	VIN = 12V		140		mΩ
Rdson_LS2	Buck2 low-side switch resistance	VIN = 12V		95		mΩ
Rdson_HS3	Buck3 High-side switch resistance	VIN = 12V		140		mΩ
Rdson_LS3	Buck3 low-side switch resistance	VIN = 12V		95		mΩ

Electrical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 600 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD, MODE, POWER SEQUENCE						
V_{th_PG}	Feedback voltage threshold	FBx under-voltage Falling		92.5		$\%V_{REF}$
		FBx under-voltage Rising		95		$\%V_{REF}$
		FBx over-voltage Rising		107.5		$\%V_{REF}$
		FBx over-voltage Falling		105		$\%V_{REF}$
$T_{DEGLITCH(PG)\_F}$	PGOOD falling edge deglitch time			128		cycles
$T_{RDEGLITCH(PG)\_R}$	PGOOD rising edge deglitch time			512		cycles
I_{PG}	PGOOD pin leakage				0.05	µA
V_{LOW_PG}	PGOOD pin low voltage	I_{SINK} = 1 mA			0.4	V
V_{MODEH}	MODE high level input voltage			1.2	1.26	V
V_{MODEL}	MODE low level input voltage		1.1	1.15		V
I_{MODE1}	MODE pull-up current	MODE = 1V		3.6		µA
I_{MODE2}	MODE pull-up current	MODE = 1.5V		6.6		µA
$T_{psdelay}$	Delay time between bucks at automatic power sequencing mode	MODE = 1.5V		1024		cycles
POWER FAILURE DETECTOR						
$VDIV_{th}$	VDIV threshold		1.18	1.23	1.26	V
I_{VDIV}	VDIV pull-up current	VDIV = 1V		1		µA
		VDIV = 1.5V		2		µA
$I_{VDIVhys}$	VDIV hysteresis current			1		µA
$T_{deglitch\_R}$	RESET deglitch on the rising edge			534		cycles
$T_{deglitch\_F}$	RESET deglitch on the falling edge		12	14	16	cycles
OSCILLATOR						
F_{SW}	Switching frequency	ROSC = 73.2 kΩ	560	600	640	kHz
F_{SW_range}			250		2000	kHz
THERMAL PROTECTION						
T_{TRIP_OTP}	Thermal protection trip point	Temperature rising		160		°C
T_{HYST_OTP}		Hysteresis		20		°C

7.6 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, V_{OUT1} = 1.2 V, V_{OUT2} = 3.3 V, V_{OUT3} = 1.8 V, f_{SW} = 600 kHz (unless otherwise noted)

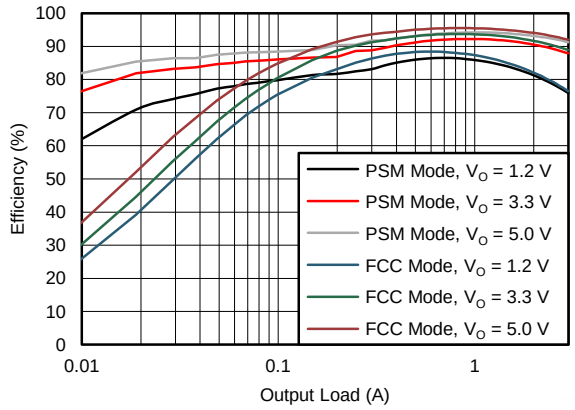


Figure 1. BUCK 1 Efficiency

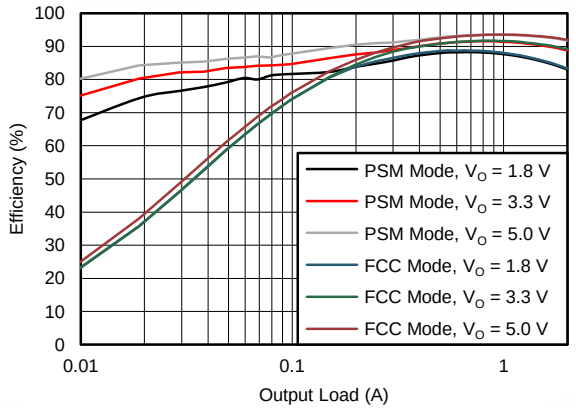


Figure 2. BUCK 2 Efficiency

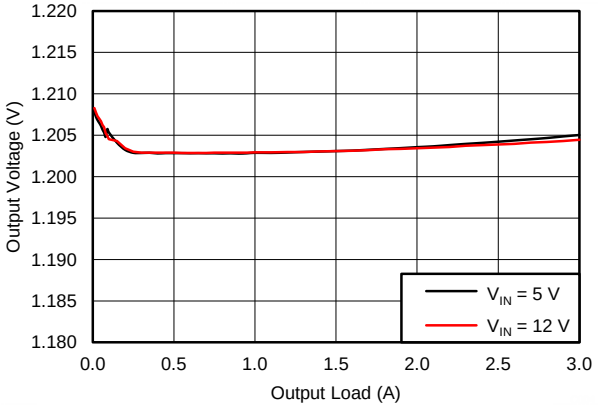


Figure 3. BUCK1, PSM Mode, Load Regulation

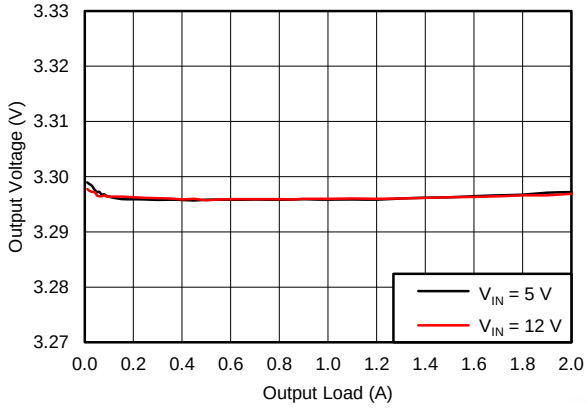


Figure 4. BUCK2, PSM Mode, Load Regulation

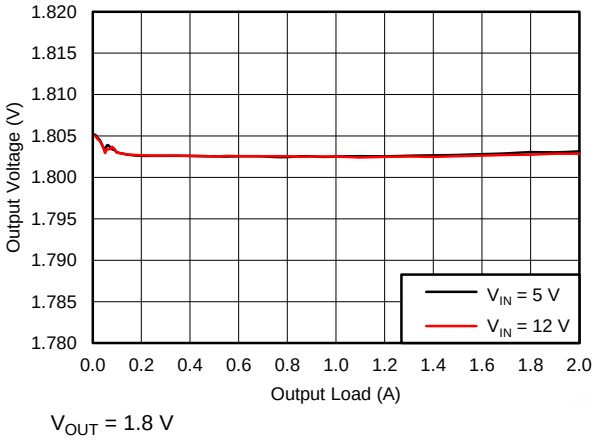


Figure 5. BUCK3, PSM Mode, Load Regulation

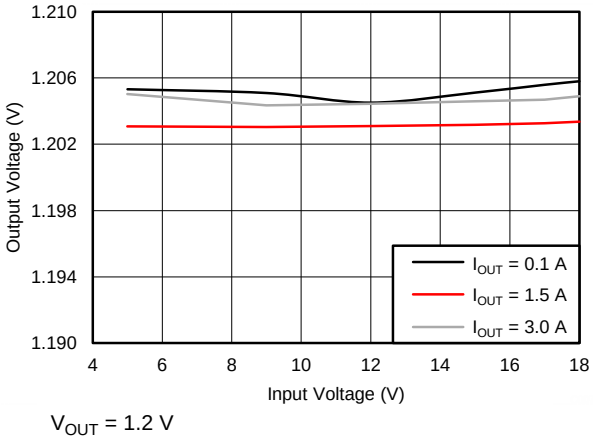
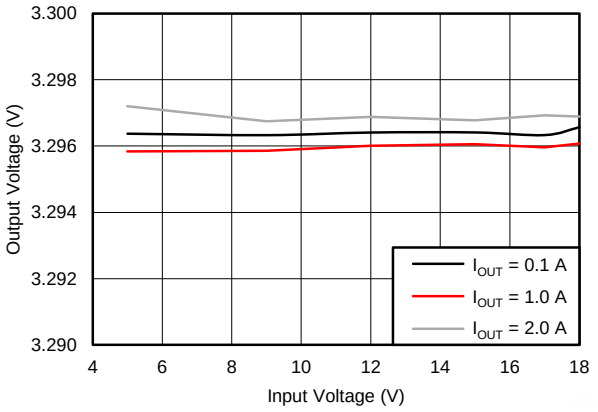


Figure 6. BUCK1, PSM Mode, Line Regulation

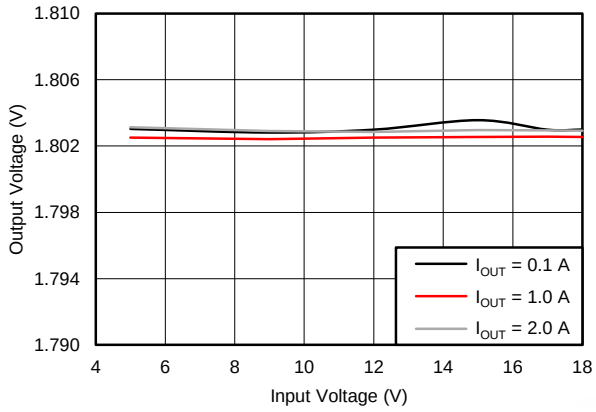
Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT1} = 1.2 V, V_{OUT2} = 3.3 V, V_{OUT3} = 1.8 V, f_{SW} = 600 kHz (unless otherwise noted)



V_{OUT} = 3.3 V

Figure 7. BUCK2, PSM MODE, LINE REGULATION



V_{OUT} = 1.8 V

Figure 8. BUCK3, PSM Mode, Line Regulation

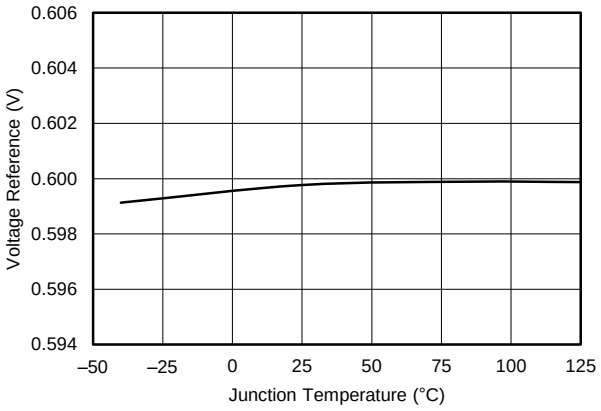
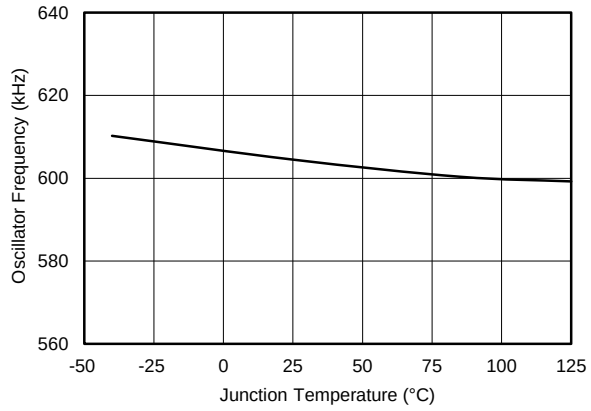
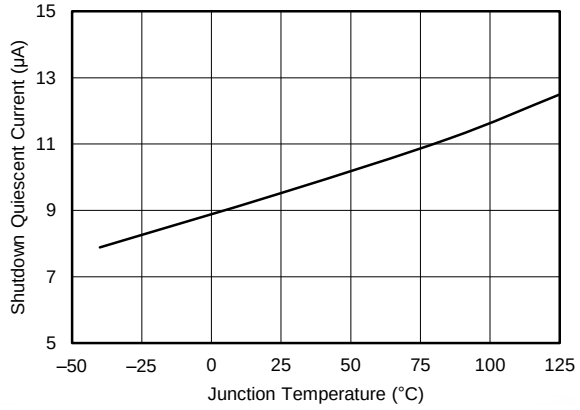


Figure 9. Voltage Reference vs Temperature



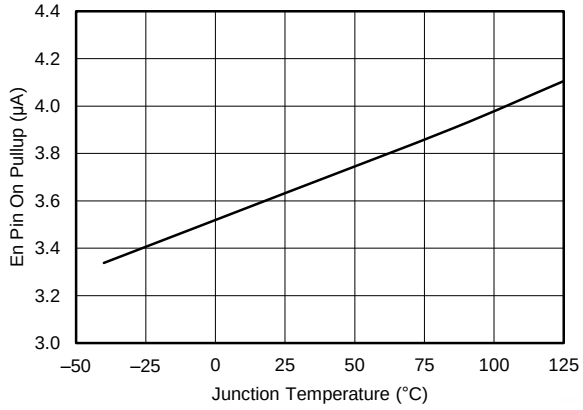
ROSC = 73.2 kΩ

Figure 10. Oscillator Frequency vs Temperature



V_{IN} = 12 V

Figure 11. Shutdown Quiescent vs Temperature



V_{IN} = 12 V EN = 1 V

Figure 12. EN Pin Pull-Up Current vs Temperature, EN=1.0V

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT1} = 1.2 V, V_{OUT2} = 3.3 V, V_{OUT3} = 1.8 V, f_{SW} = 600 kHz (unless otherwise noted)

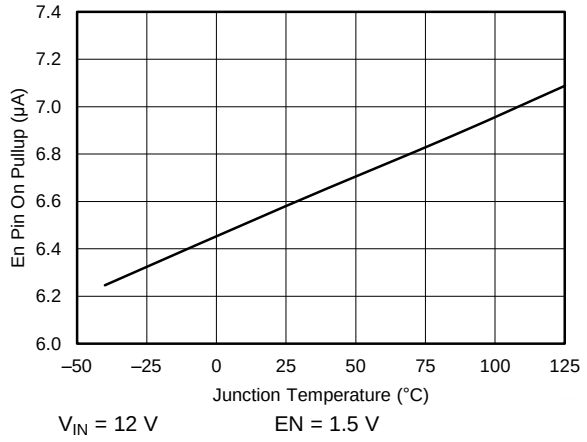


Figure 13. EN Pin Pull-Up Current vs Temperature, EN=1.5V

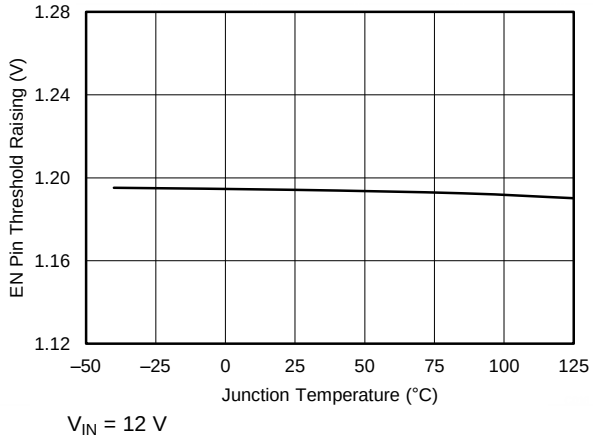


Figure 14. EN Pin Threshold Raising vs Temperature

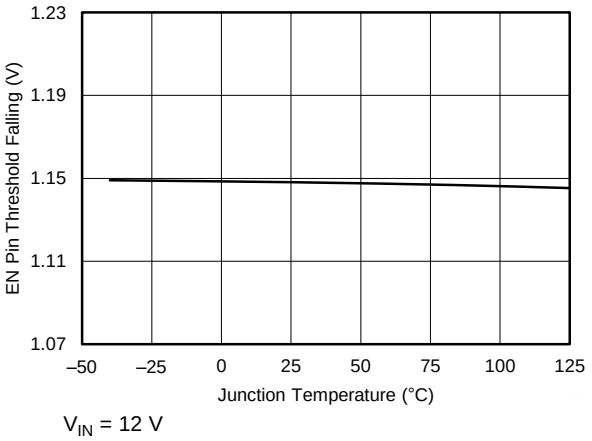


Figure 15. EN Pin Threshold Falling vs Temperature

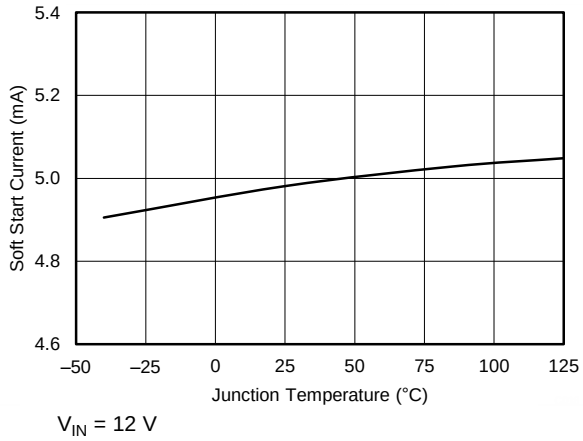


Figure 16. SS Pin Charge Current vs Temperature

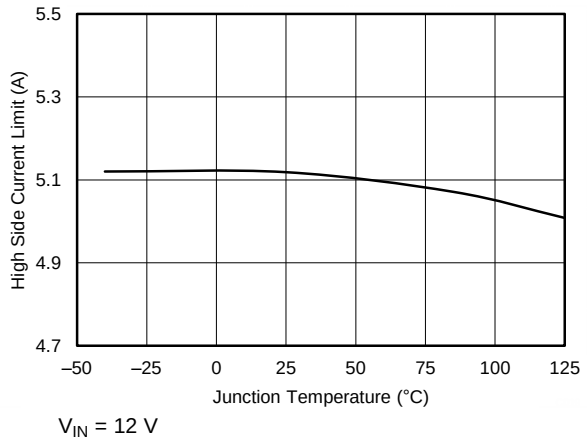


Figure 17. Buck1 High-Side Current Limit vs Temperature

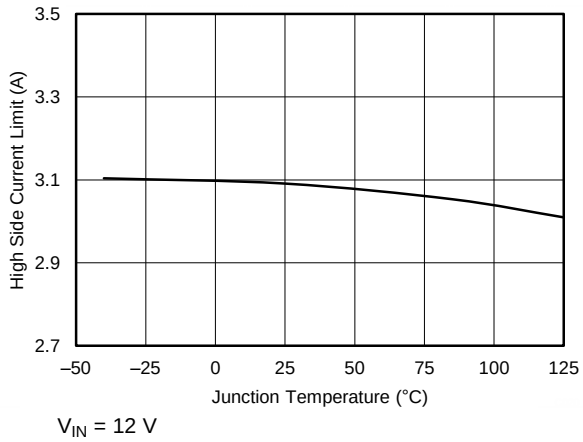


Figure 18. Buck2 High-Side Current Limit vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12 V, V_{OUT1} = 1.2 V, V_{OUT2} = 3.3 V, V_{OUT3} = 1.8 V, f_{SW} = 600 kHz (unless otherwise noted)

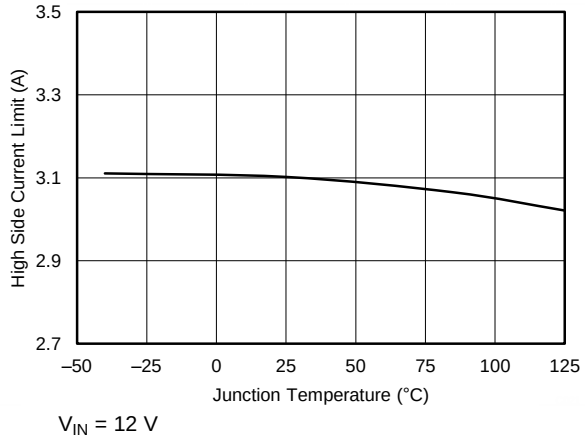


Figure 19. Buck3 High-Side Current Limit vs Temperature

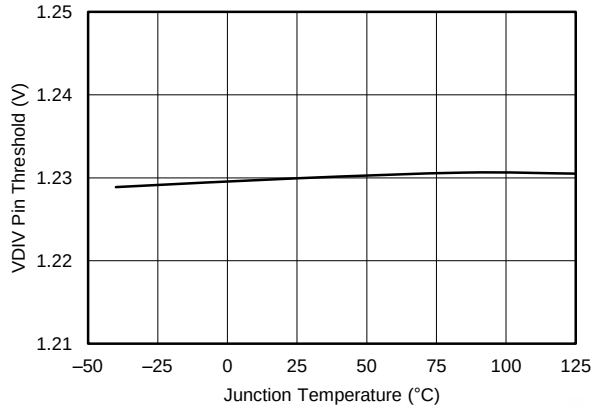


Figure 20. VDIV Pin Threshold vs Temperature

8 Detailed Description

8.1 Overview

The TPS65261, TPS65261-1 is a monolithic triple synchronous step-down (buck) converter with 3A/2A/2A output currents. A wide 4.5V to 18V input supply voltage range encompasses the most intermediate bus voltages operating off 5V, 9V, 12V or 15V power bus. The feedback voltage reference for each buck is 0.6V. Each buck is independent with dedicated enable, soft-start and loop compensation pins.

The TPS65261, TPS65261-1 implements a constant frequency, peak current mode control that simplifies external loop compensation. The wide switching frequency of 250kHz to 2MHz allows optimizing system efficiency, filtering size and bandwidth. The switching frequency can be adjusted with an external resistor connected between ROSC pin and ground. The switching clock of buck1 is 180° out-of-phase operation from the clocks of buck2 and buck3 channels to reduce input current ripple, input capacitor size and power supply induced noise.

The TPS65261, TPS65261-1 has been designed for safe monotonic startup into pre-biased loads. The default start up is when VIN is typically 4.5V. The ENx pin also can be used to adjust the input voltage under voltage lockout (UVLO) with an external resistor divider. In addition, the ENx pin has an internal 3.6uA current source, so the EN pin can be floating to automatically power up the converters.

The TPS65261, TPS65261-1 reduces the external component count by integrating a bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and LX pin. A UVLO circuit monitors the bootstrap capacitor voltage VBST-VLX in each buck. When $V_{BST-VLX}$ voltage drops to the threshold, LX pin is pulled low to recharge the bootstrap capacitor. The TPS65261, TPS65261-1 can operate at 100% duty cycle as long as the bootstrap capacitor voltage is higher than the BOOT-LX UVLO threshold which is typically 2.1V.

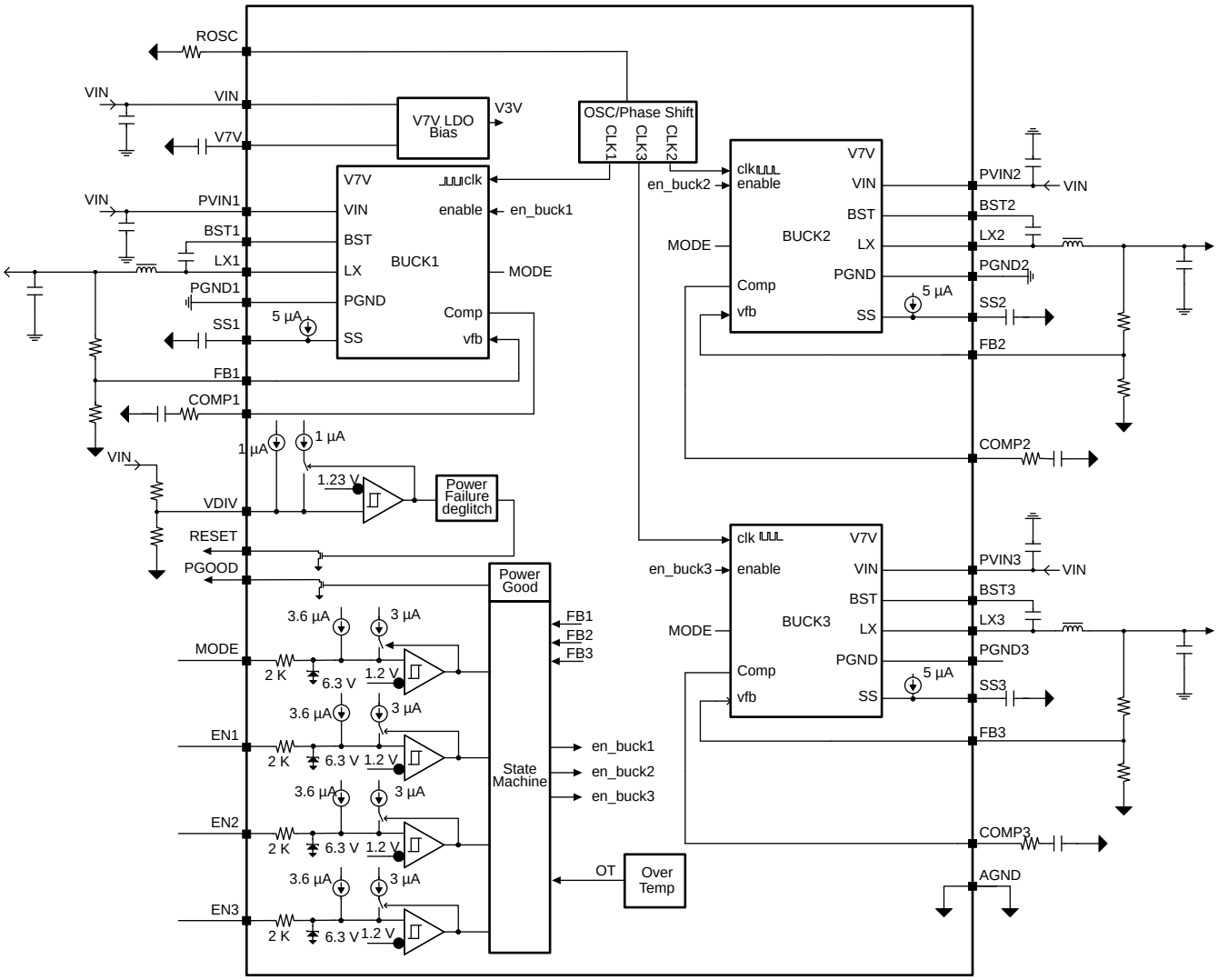
The TPS65261, TPS65261-1 features a PGOOD pin to supervise each output voltage of the buck converters. The TPS65261, TPS65261-1 has power good comparators with hysteresis, which monitor the output voltages through feedback voltages. When all bucks are in regulation range and power sequence is done, PGOOD is asserted to high.

The SS (soft start/tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor or resistor divider is connected to the pin for soft start or voltage tracking.

At light loading, TPS65261 will automatically operate in pulse skipping mode (PSM) to save power.

The TPS65261, TPS65261-1 is protected from overload and over temperature fault conditions. The converter minimizes excessive output overvoltage transients by taking advantage of the power good comparator. When the output is overvoltage, the high-side MOSFET is turned off until the internal feedback voltage is lower than 105% of the 0.6V reference voltage. The TPS65261, TPS65261-1 implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protection to avoid inductor current runaway. If the over current condition has lasted for more than the OC wait time (256 clock cycles), the converter will shut down and re-start after the hiccup time (8192 clock cycles). The TPS65261, TPS65261-1 shuts down if the junction temperature is higher than the thermal shutdown trip point. When the junction temperature drops 20°C typically below the thermal shutdown trip point, the TPS65261, TPS65261-1 will be restarted under control of the soft start circuit automatically.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjusting the Output Voltage

The output voltage of each buck is set with a resistor divider from the output of buck to the FB pin. It is recommended to use 1% tolerance or better resistors.

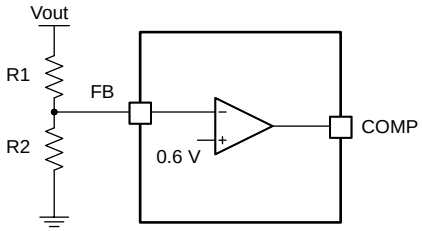


Figure 21. Voltage Divider Circuit

$$R_2 = R_1 \times \frac{0.6}{V_{out} - 0.6} \quad (1)$$

Feature Description (continued)

To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more sensitive to noise. The recommended resistor values are shown in Table 1.

Table 1. Output Resistor Divider Selection

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)
1	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	31.6	10
3.3	45.3	10
3.3	22.6	4.99
5	73.2	10
5	36.5	4.99

8.3.2 Power Failure Detector

The power failure detector monitors the voltage on VDIV, and sets open-drain output RESET low when VDIV is below 1.23V. There is deglitch on the rising edge, 534 frequency cycles. Figure 22 shows the power failure detector timing diagram.

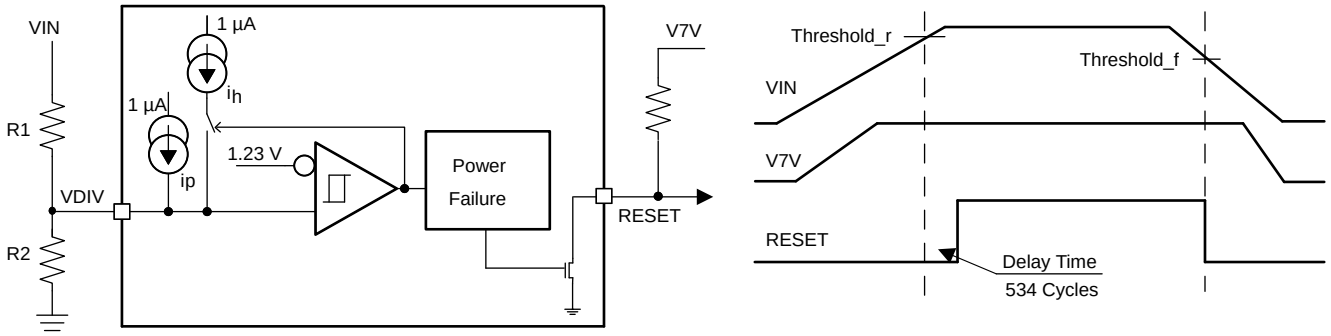


Figure 22. Power Failure Detector Timing Diagram

The thresholds can be calculated using Equation 2 and Equation 3.

$$Threshold_{\_r} = Vref\left(1+\frac{R1}{R2}\right) - I_p \times R1 \quad (2)$$

$$Threshold_{\_f} = Vref\left(1+\frac{R1}{R2}\right) - (I_P + I_h)\times R1 \quad (3)$$

The divider resisters can be calculated using Equation 4 and Equation 5.

$$R1 = \frac{Threshold_{\_r} - Threshold_{\_f}}{I_h} \quad (4)$$

$$R2 = \frac{Vref}{\frac{Threshold_{\_r} - Vref}{Threshold_{\_r} - Threshold_{\_f}} \times I_h + I_p} \quad (5)$$

Where I_h = 1µA, I_p = 1µA.

8.3.3 Enable and Adjusting Under-Voltage Lockout

The EN1/2/3 pin provides electrical on/off control of the device. Once the EN1/2/3 pin voltage exceeds the threshold voltage, the device starts operation. If each ENx pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin to enable the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 500mV. If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVINx in split rail applications, then the ENx pin can be configured as shown in Figure 23, Figure 24 and Figure 25. When using the external UVLO function, it is recommended to set the hysteresis to be greater than 500mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 6 and Equation 7.

$$R_1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1-\frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (6)$$

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLILNG} + R_1(I_h + I_p)} \quad (7)$$

Where I_h = 3µA, I_P = 3.6uA, $V_{ENSRISING}$ = 1.2V, $V_{ENFALLING}$ = 1.15V.

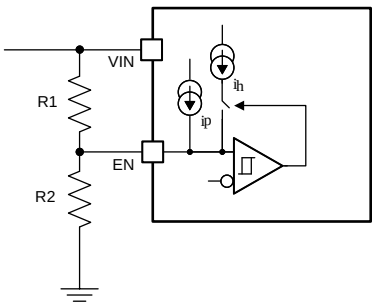


Figure 23. Adjustable VIN Under-voltage Lockout

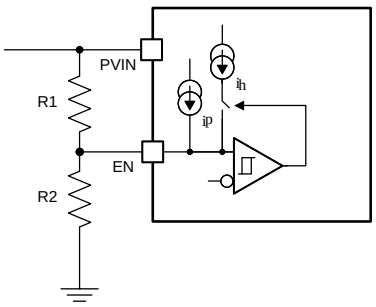


Figure 24. Adjustable PVIN Under-voltage Lockout, VIN>4.5V

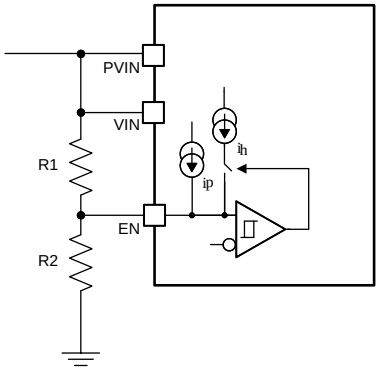


Figure 25. Adjustable VIN and PVIN Under-voltage Lockout

8.3.4 Soft-Start Time

The voltage on the respective SS pin controls the start-up of the buck output. When the voltage on the SS pin is less than the internal 0.6V reference, the TPS65261, TPS65261-1 regulates the internal feedback voltage to the voltage on the SS pin instead of 0.6V. The SS pin can be used to program an external soft-start function or to allow output of the buck to track another supply during start-up. The device has an internal pull-up current source of 5µA (typical) that charges an external soft-start capacitor to provide a linear ramping voltage at the SS pin. The TPS65261, TPS65261-1 regulates the internal feedback voltage to the voltage on the SS pin, allowing VOUT to rise smoothly from 0V to its regulated voltage without inrush current. The soft-start time can be calculated approximately by Equation 8.

$$Tss(ms) = \frac{Css(nF) \times Vref(V)}{Iss(\mu A)} \quad (8)$$

Many of the common power supply sequencing methods can be implemented using the SSx and ENx pins. Figure 26 shows the method implementing ratio-metric sequencing by connecting the SSx pins of three buck channels together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time, the pull-up current source must be tripled in Equation 8.

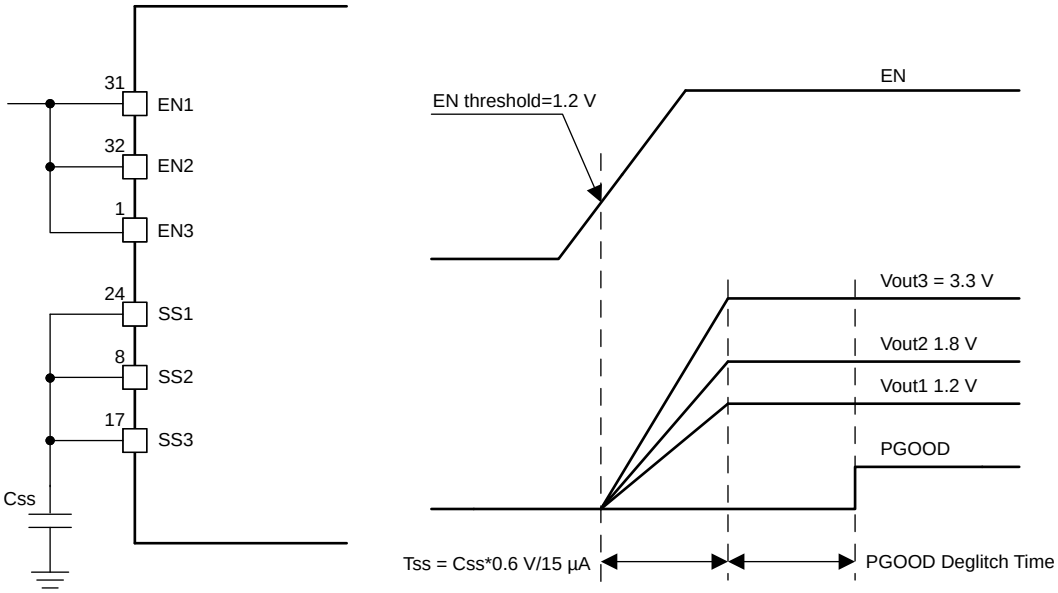


Figure 26. Ratio Metric Power Up Using SSx Pins

Simultaneous power supply sequencing can be implemented by connecting capacitor to SSx pin, shown in Figure 27. The capacitors can be calculated using Equation 8 and Equation 9.

$$\frac{Css1}{Vout1} = \frac{Css2}{Vout2} = \frac{Css3}{Vout3} \quad (9)$$

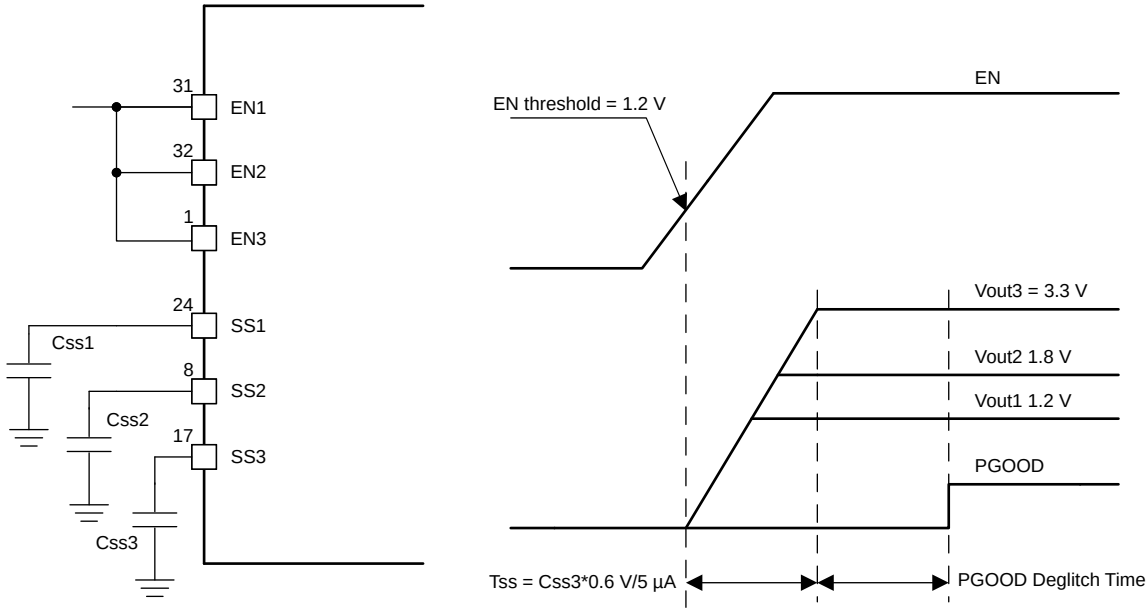


Figure 27. Simultaneous Startup Sequence Using SSx Pins

8.3.5 Power Up Sequencing

TPS65261, TPS65261-1 features a comprehensive sequencing circuit for the 3 bucks. If the MODE pin ties high to V7V, three buck start up and shutdown is in sequence according to different buck enable pin setup. If the MODE pin ties low to ground, three buck on/off is separately controlled by three enable pins.

8.3.5.1 External Power Sequencing

The TPS65261, TPS65261-1 has a dedicated enable pin and soft-start pin for each converter. The converter enable pins are biased by a current source that allows for easy sequencing with the addition of an external capacitor. Disabling the converter with an active pull-down transistor on the ENs pin allows for a predictable power-down timing operation. Figure 28 shows the timing diagram of a typical buck power-up sequence by connecting a capacitor at ENx pin.

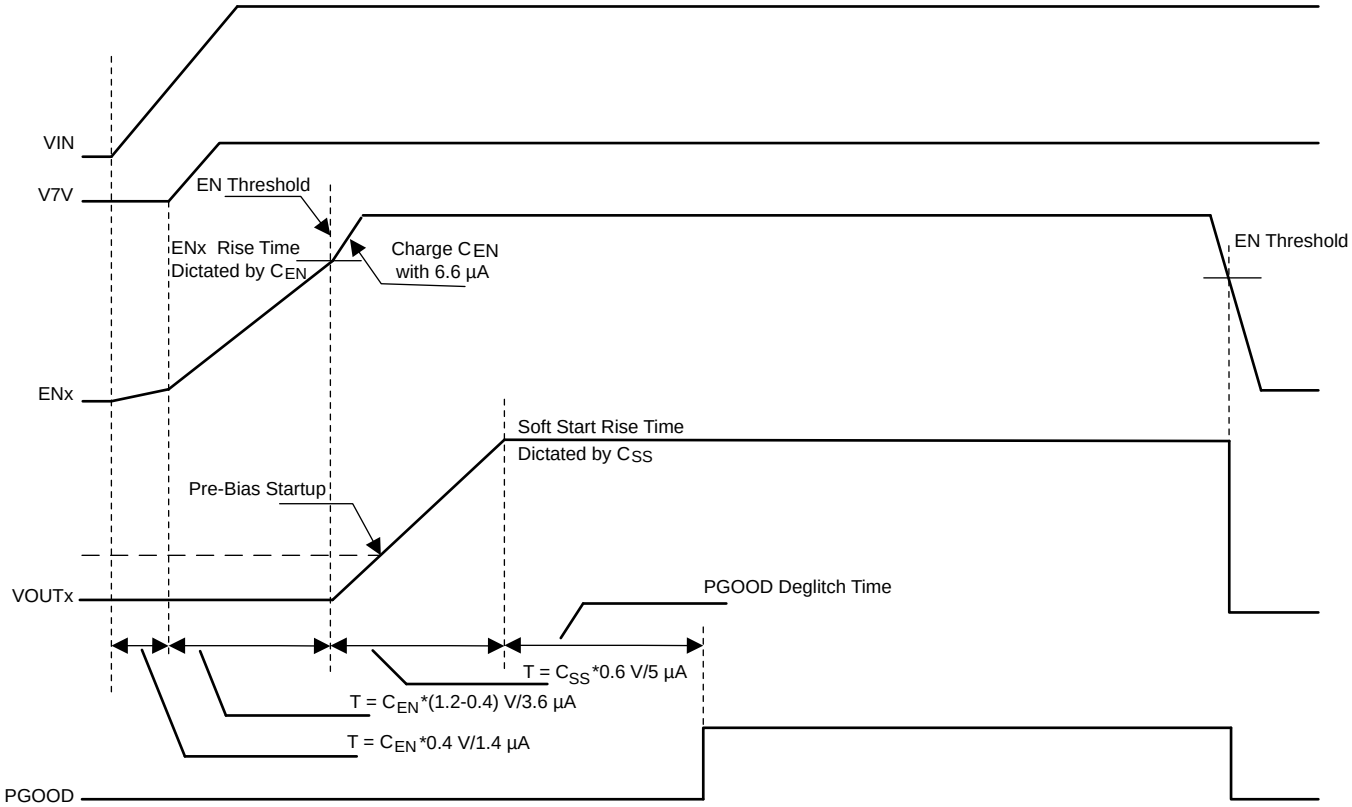


Figure 28. Startup Power Sequence

8.3.5.2 Automatic Power Sequencing

The TPS65261, TPS65261-1 starts with a pre-defined power-up and power-down sequence when the MODE pin ties high to V7V. As shown in Table 2, the sequence is dictated by the different combinations of EN1 and EN2 status. EN3 is used to start/stop the converters. Buck2 and buck3 are identical converters and can be swapped in the system operation to allow for additional sequencing stages. Figure 29 shows the power sequencing when EN1 and EN2 are pulled up high.

Table 2. Power Sequencing

	MODE	EN1	EN2	EN3	Start Sequencing	Shutdown Sequencing
Automatic Power Sequencing	High	High	High	Used to start/stop bucks in sequence	Buck1→Buck2→Buck3	Buck3→Buck2→Buck1
	High	Low	High		Buck2→Buck1→Buck3	Buck3→Buck1→Buck2
	High	High	Low		Buck2→Buck3→Buck1	Buck1→Buck3→Buck2
	High	Low	Low	Reserved	Reserved	Reserved
Externally controlled sequencing	Low	Used to start/stop buck1	Used to start/stop buck2	Used to start/stop buck3	x	x

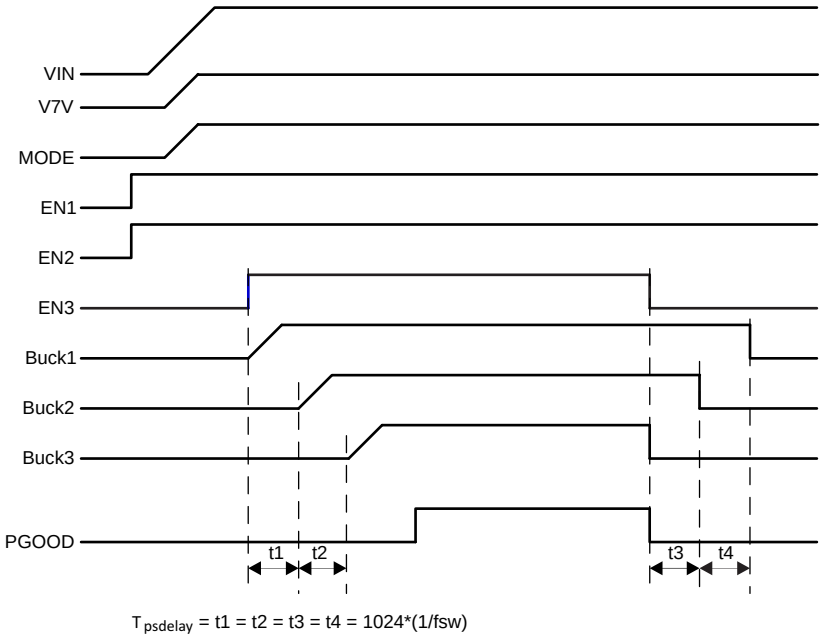


Figure 29. Automatic Power Sequencing

8.3.6 V7V Low Dropout Regulator and Bootstrap

Power for the high-side and low-side MOSFET drivers and most other internal circuitry is derived from the V7V pin. The internal built-in low dropout linear regulator (LDO) supplies 6.3V (typical) from VIN to V7V. A 1µF ceramic capacitor should be connected from V7V pin to power ground.

If the input voltage, VIN, decreases to UVLO threshold voltage, the UVLO comparator detects the V7V pin voltage and forces the converter off.

Each high-side MOSFET driver is biased from the floating bootstrap capacitor, CB, shown in Figure 30, which is normally recharged during each cycle through an internal low-side MOSFET or the body diode of a low-side MOSFET when the high-side MOSFET turns off. The boot capacitor is charged when the BST pin voltage is less than VIN and BST-LX voltage is below regulation. The recommended value of this ceramic capacitor is 47nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage. Each low-side MOSFET driver is powered from the V7V pin directly.

To improve drop out, the device is designed to operate at 100% duty cycle as long as the BST to LX pin voltage is greater than the BST-LX UVLO threshold, which is typically 2.1V. When the voltage between BST and LX drops below the BST-LX UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on allowing the boot capacitor to be recharged.

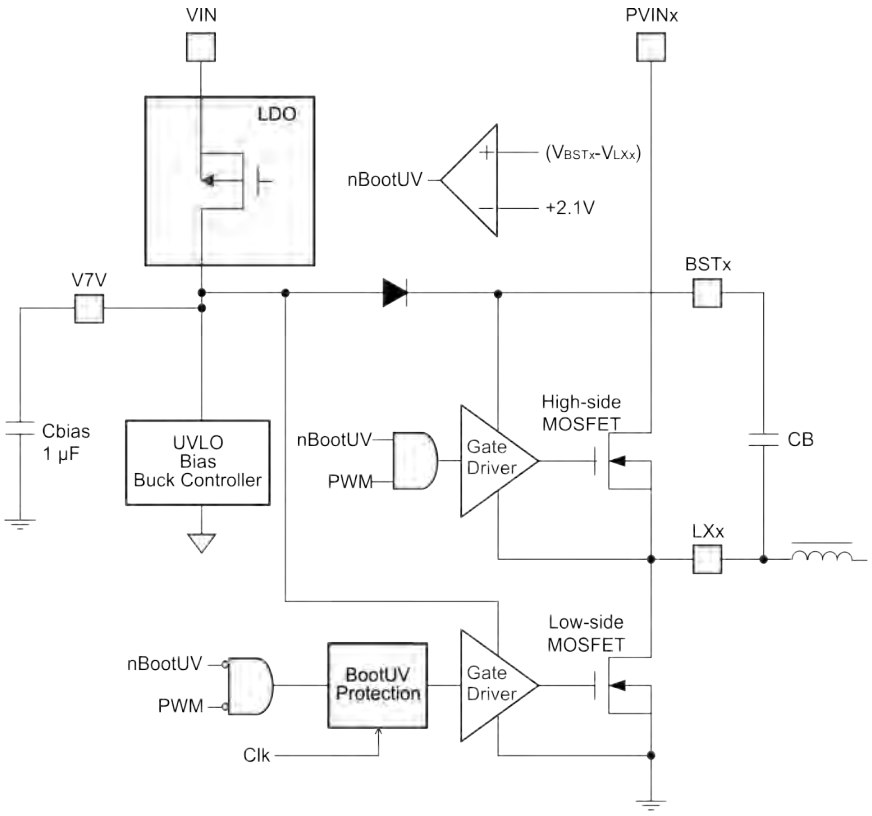


Figure 30. V7V Linear Dropout Regulator and Bootstrap Voltage Diagram

8.3.7 Out-of-Phase Operation

In order to reduce input ripple current, the switch clock of buck1 is 180° out-of-phase from the clock of buck2 and buck3. This enables the system, having less input current ripple, to reduce the input capacitors' size, cost and EMI.

8.3.8 Output Overvoltage Protection (OVP)

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. When the output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state voltage. In some applications with small output capacitance, the load can respond faster than the error amplifier. This leads to the possibility of an output overshoot. Each buck compares the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVP threshold, the high-side MOSFET turns on at the next clock cycle.

8.3.9 Slope Compensation

In order to prevent the sub-harmonic oscillations when the device operates at duty cycles greater than 50%, the device adds built-in slope compensation, which is a compensating ramp to the switch current signal.

8.3.10 Overcurrent Protection

The device is protected from over current conditions with cycle-by-cycle current limiting on both the high-side MOSFET and the low-side MOSFET.

8.3.10.1 High-side MOSFET Over Current Protection

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. During each cycle, the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.

8.3.10.2 Low-side MOSFET Over Current Protection

While the low-side MOSFET is turned on, its conduction current is monitored by the internal circuitry. During normal operation, the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario both MOSFETs are off until the start of the next cycle.

Furthermore, if an output overload condition (as measured by the COMP pin voltage) has lasted for more than the hiccup wait time which is programmed for 256 switching cycles shown in Figure 31, the device will shut down itself and restart after the hiccup time of 8192 cycles. The hiccup mode helps reduce the device power dissipation under severe overcurrent condition.

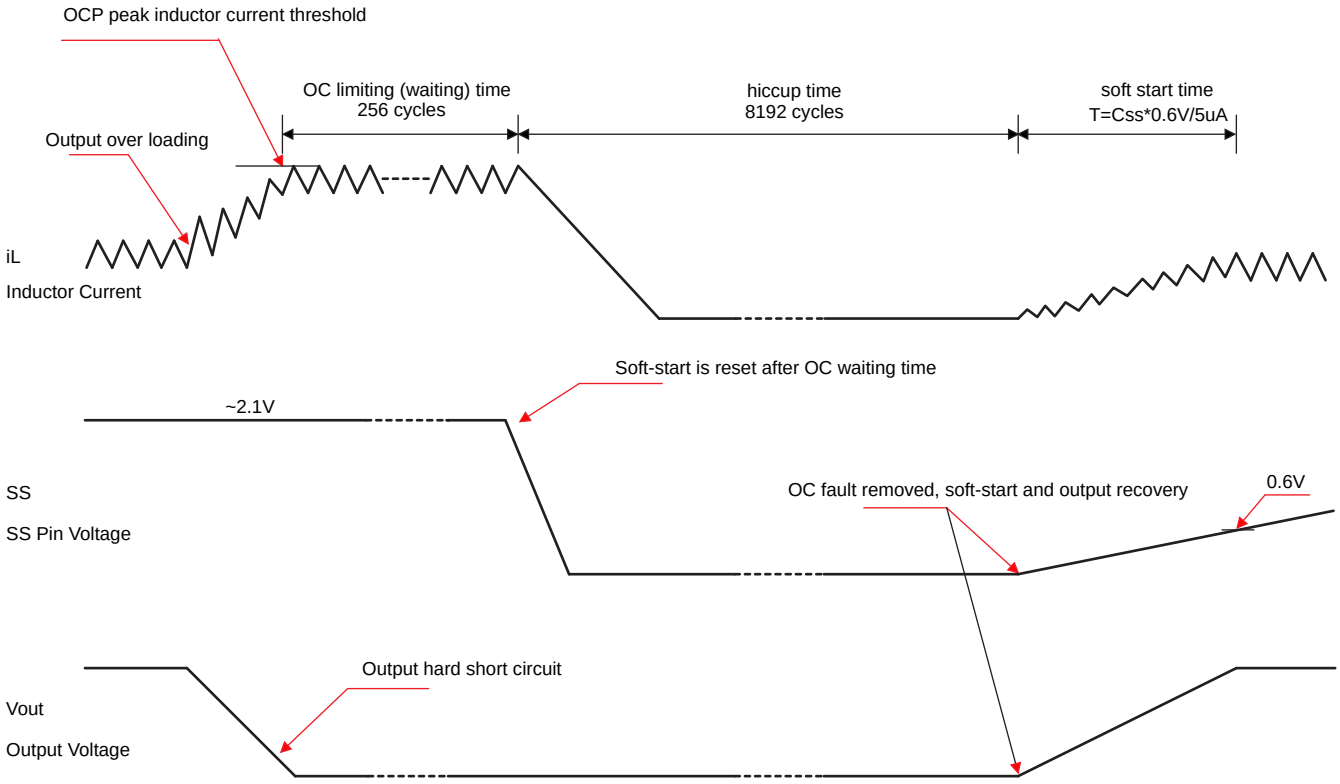


Figure 31. Over Current Protection

8.3.11 Power Good

The PGOOD pin is an open drain output. Once feedback voltage of each buck is between 95% (rising) and 105% (falling) of the internal voltage reference, the PGOOD pin pull-down is de-asserted and the pin floats. It is recommended to use a pull-up resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PGOOD is in a defined state once the VIN input voltage is greater than 1V, but with reduced current sinking capability. The PGOOD achieves full current sinking capability once the VIN input voltage is above UVLO threshold, which is 4.25V.

The PGOOD pin is pulled low when any feedback voltage of a buck is lower than 92.5% (falling) or greater than 107.5% (rising) of the nominal internal reference voltage. Also, the PGOOD is pulled low if the input voltage is under-voltage locked up, thermal shutdown is asserted, the EN pin is pulled low or the converter is in a soft-start period.

8.3.12 Adjustable Switching Frequency

The ROSC pin can be used to set the switching frequency by connecting a resistor to GND. The switching frequency of the device is adjustable from 250KHz to 2MHz.

To determine the ROSC resistance for a given switching frequency, use Equation 10 or the curve in Figure 32. To reduce the solution size, set the switching frequency as high as possible, but tradeoffs of the supply efficiency and minimum controllable on time should be considered.

$$f_{osc}(\text{kHz}) = 39557 \times R(\text{k}\Omega)^{-0.975} \quad (10)$$

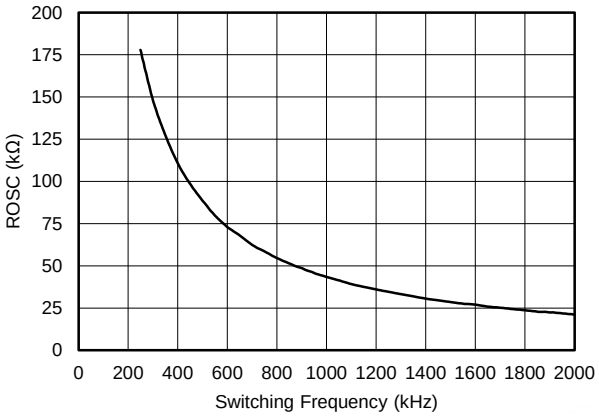


Figure 32. ROSC versus Switching Frequency

8.3.13 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power up sequence when the junction temperature drops below 140°C typically.

8.4 Device Functional Modes

8.4.1 Pulse Skipping MODE (PSM)

The TPS65261 can enter high efficiency pulse skipping mode (PSM) operation at light load current.

When a controller is enabled for PSM operation, the peak inductor current is sensed and compared with 230mA current typically. Since the integrated current comparator catches the peak inductor current only, the average load current entering PSM varies with applications and external output filters. In PSM, the sensed peak inductor current is clamped at 230mA.

When a controller operates in PSM, the inductor current is not allowed to reverse. The reverse current comparator turns off the low-side MOSFET when the inductor current reaches zero, preventing it from reversing and going negative.

Due to the delay in the circuit and current comparator tdly (typical 50ns at V_{IN} = 12V), the real peak inductor current threshold to turn off high-side power MOSFET, could shift higher depending on inductor inductance and input/output voltages. The threshold of peak inductor current to turn off high-side power MOSFET can be calculated by Equation 11.

$$IL_{PEAK} = 230\ \text{mA} + \frac{Vin - Vout}{L} \times tdly \quad (11)$$

Device Functional Modes (continued)

Once the charge accumulated on the Vout capacitor is more than loading need, COMP pin voltage drops to low voltage driven by the error amplifier. There is an internal comparator at the COMP pin. If COMP voltage is lower than 0.35V, the power stage stops switching to save power.

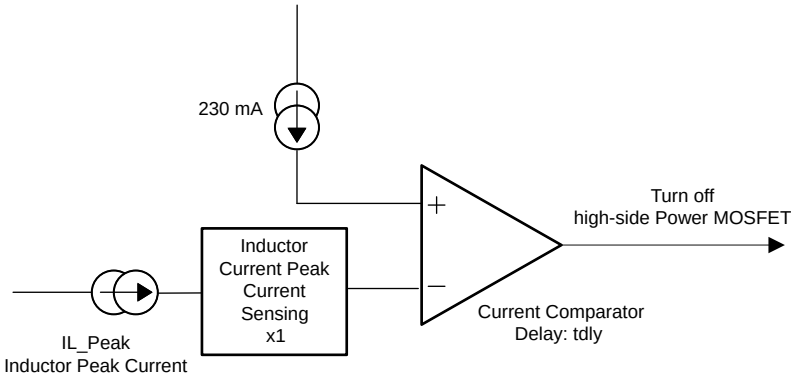


Figure 33. PSM Current Comparator

9 Application and Implementation

9.1 Application Information

The devices are triple synchronous step down dc/dc converters. They are typically used to convert a higher dc voltage to lower dc voltages with continuous available output current of 3A/2A/2A. The following design procedure can be used to select component values for the TPS65261 and TPS65261-1. This section presents a simplified discussion of the design process.

9.2 Typical Application

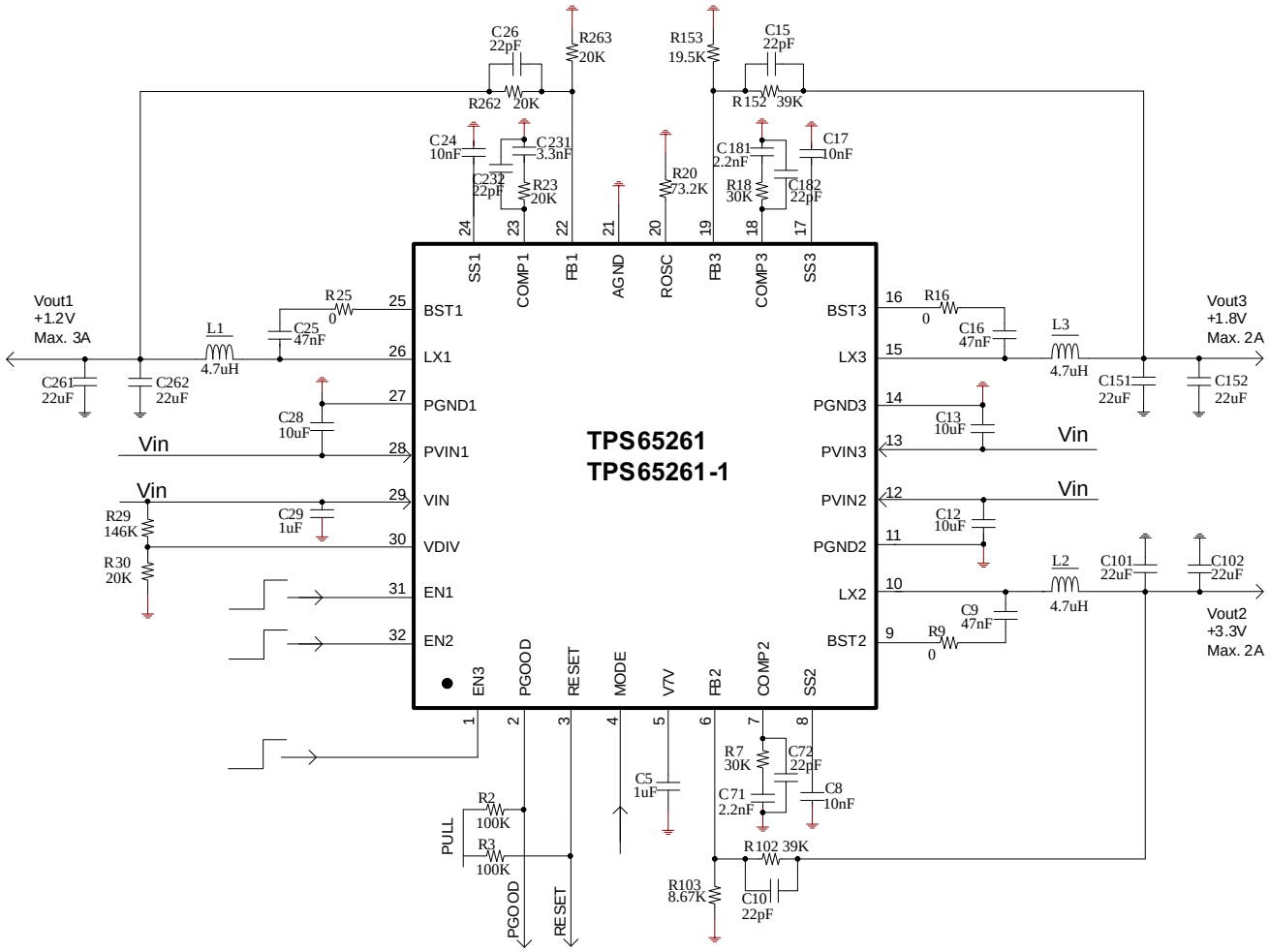


Figure 34. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

This example details the design of triple synchronous step-down converter. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Vout1	1.2 V
Iout1	3 A
Vout2	3.3 V
Iout2	2 A
Vout3	1.8 V
Iout3	2 A
Transient Response 1A Load Step	±5%
Input Voltage	12 V normal, 4.5 V to 18 V
Output Voltage Ripple	±1%
Switching Frequency	600 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Inductor Selection

To calculate the value of the output inductor, use Equation 12. LIR is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, LIR is normally from 0.1 to 0.3 for the majority of applications.

$$L = \frac{V_{inmax} - V_{out}}{I_o \times LIR} \times \frac{V_{out}}{V_{in\ max} \times f_{sw}} \quad (12)$$

For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 14 and Equation 15.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} \times \frac{V_{out}}{V_{inmax} \times f_{sw}} \quad (13)$$

$$I_{Lrms} = \sqrt{I_O^2 + \frac{\left(\frac{V_{out} \times (V_{inmax} - V_{out})}{V_{inmax} \times L \times f_{sw}}\right)^2}{12}} \quad (14)$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \quad (15)$$

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.2 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Equation 16 shows the minimum output capacitance necessary to accomplish this.

$$C_o = \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta V_{out}} \tag{16}$$

Where ΔI_{out} is the change in output current, f_{sw} is the regulators switching frequency and ΔV_{out} is the allowable change in the output voltage.

Equation 17 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, $V_{oripple}$ is the maximum allowable output voltage ripple, and $I_{oripple}$ is the inductor ripple current.

$$C_o > \frac{1}{8 \times f_{sw}} \times \frac{1}{\frac{V_{oripple}}{I_{oripple}}} \tag{17}$$

Equation 18 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification.

$$R_{esr} < \frac{V_{oripple}}{I_{oripple}} \tag{18}$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in, which increases this minimum value. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 19 can be used to calculate the RMS ripple current the output capacitor needs to support.

$$I_{corms} = \frac{V_{out} \times (V_{inmax} - V_{out})}{\sqrt{12} \times V_{inmax} \times L \times f_{sw}} \tag{19}$$

9.2.2.3 Input Capacitor Selection

The TPS65261, TPS65261-1 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance on the PVIN input voltage pins. In some applications, additional bulk capacitance may also be required for the PVIN input. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of The TPS65261, TPS65261-1. The input ripple current can be calculated using Equation 20.

$$I_{inrms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{inmin}} \times \frac{(V_{inmin} - V_{out})}{V_{inmin}}} \tag{20}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 21.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \quad (21)$$

9.2.2.4 Loop Compensation

The TPS65261, TPS65261-1 incorporates a peak current mode control scheme. The error amplifier is a trans-conductance amplifier with a gain of 300 µS. A typical type II compensation circuit adequately delivers a phase margin between 60° and 90°. C_b adds a high frequency pole to attenuate high frequency noise when needed. To calculate the external compensation components, follow these steps.

1. Select switching frequency f_{sw} that is appropriate for application depending on L and C sizes, output ripple, and EMI. Switching frequency between 500kHz to 1MHz gives best trade-off between performance and cost. To optimize efficiency, lower switching frequency is desired.
2. Set up cross over frequency, fc, which is typically between 1/5 and 1/20 of f_{sw}.
3. R_C can be determined by

$$R_C = \frac{2\pi \times f c \times Vo \times Co}{G_{m\_EA} \times Vref \times G_{m\_PS}} \quad (22)$$

   Where G_{m_EA} is the error amplifier gain (300µS), G_{m_PS} is the power stage voltage to current conversion gain (7.4A/V).

4. Calculate C_C by placing a compensation zero at or before the dominant pole $\left(f p = \frac{1}{C_o \times R_L \times 2\pi} \right)$.

$$C_C = \frac{R_L \times Co}{R_C} \quad (23)$$

5. Optional C_b can be used to cancel the zero from the ESR associated with C_O.

$$C_b = \frac{R_{ESR} \times Co}{R_C} \quad (24)$$

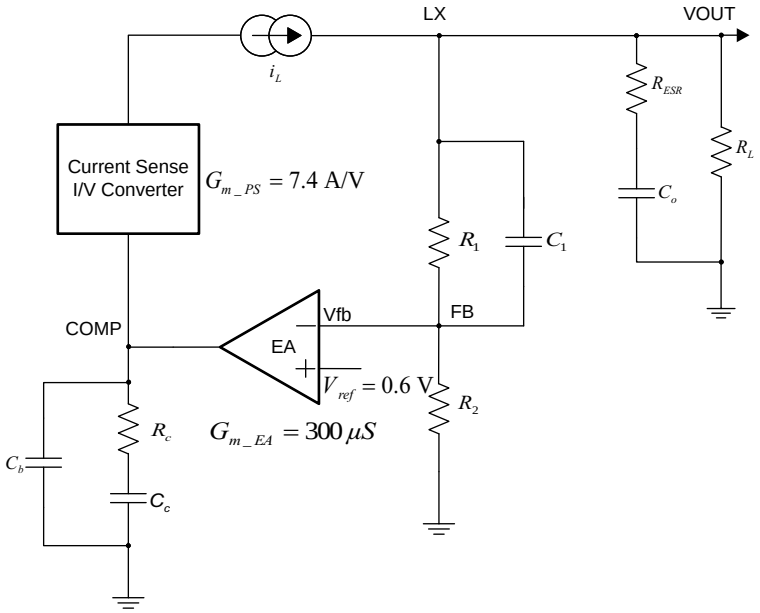


Figure 35. DC/DC Loop Compensation

9.2.3 Application Curves

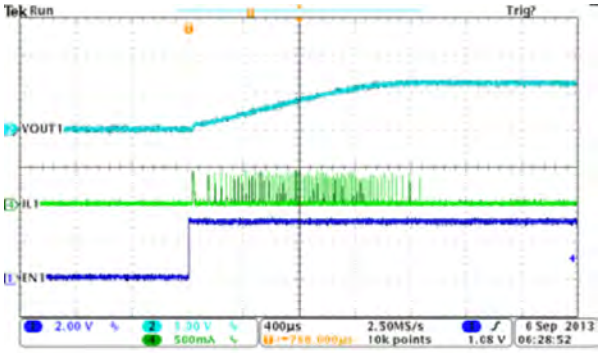


Figure 36. BUCK1, Soft-Start with No Load

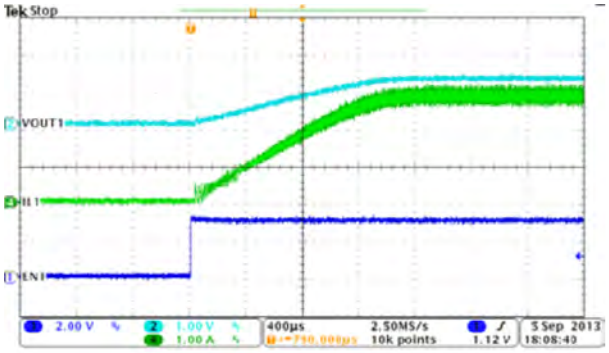


Figure 37. BUCK1, Soft-Start with Full Load

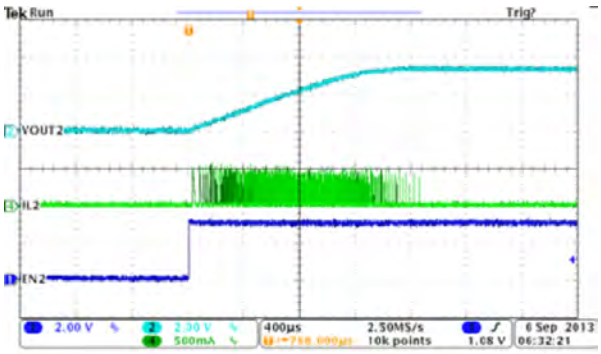


Figure 38. BUCK2, Soft-Start with No Load

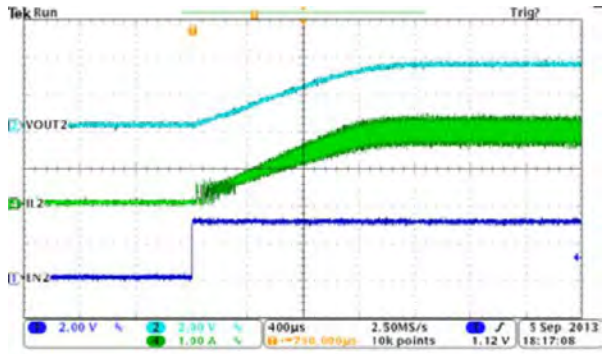


Figure 39. BUCK2, Soft-Start with Full Load

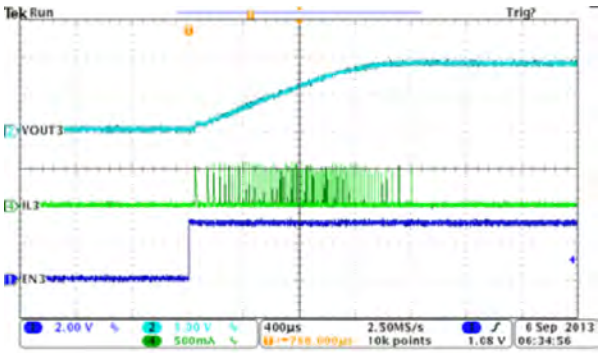


Figure 40. BUCK3, Soft-Start with No Load

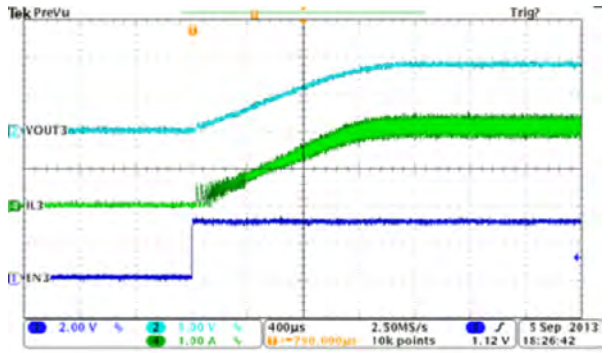


Figure 41. BUCK3, Soft-Start with Full Load

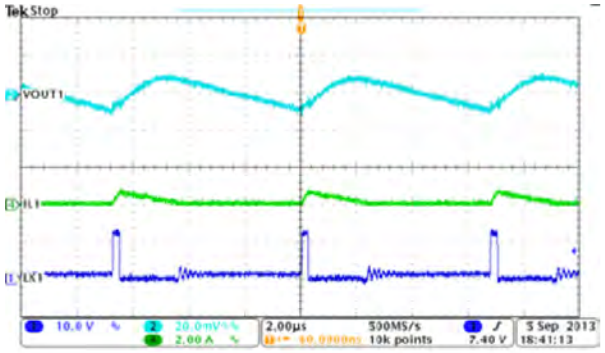


Figure 42. BUCK1, PSM Mode, Steady State Operation at Light Load

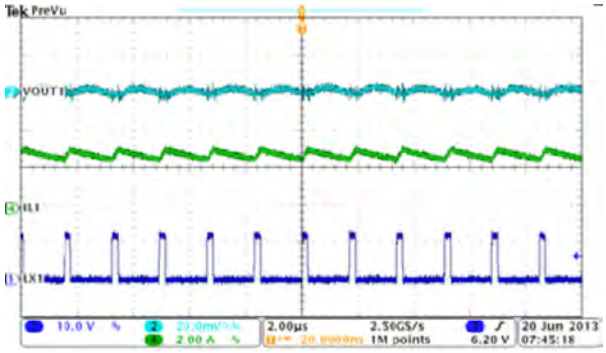


Figure 43. BUCK1, Steady State Operation with Full Load

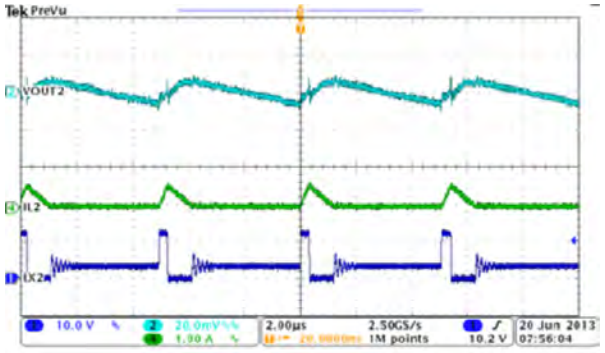


Figure 44. BUCK2, PSM Mode, Steady State Operation at Light Load

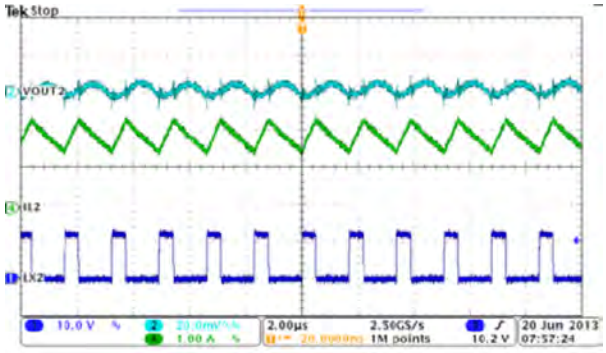


Figure 45. BUCK2, Steady State Operation with Full Load

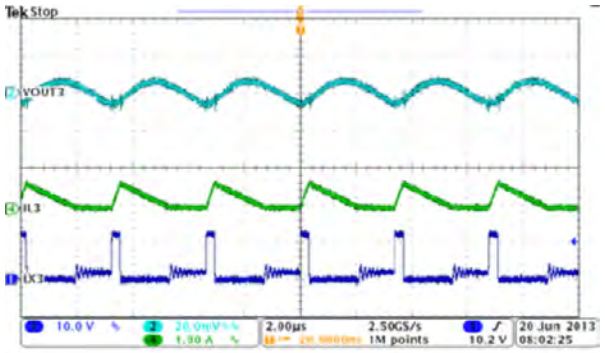


Figure 46. BUCK3, PSM Mode, Steady State Operation with Light Load

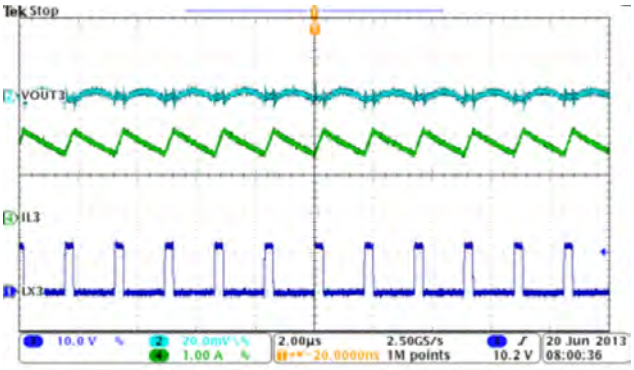


Figure 47. BUCK3, Steady State Operation with Full Load

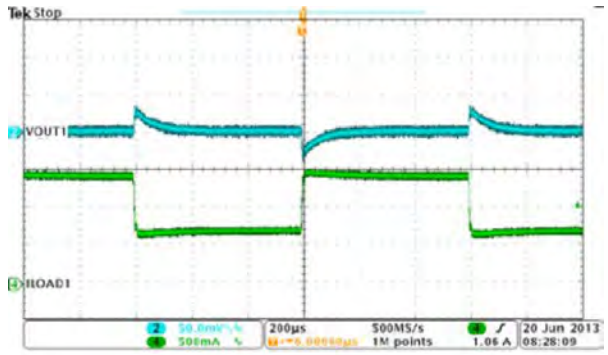


Figure 48. BUCK1, Load Transient, 0.75A to 1.5A SR=0.25A/µs

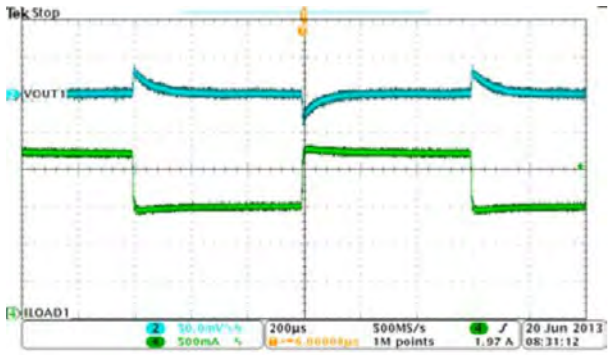


Figure 49. BUCK1, Load Transient, 1.5A to 2.25A SR=0.25A/µs

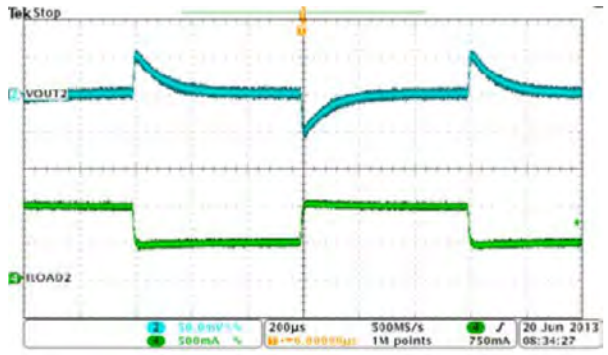


Figure 50. BUCK2, Load Transient, 0.5A to 1.0A SR=0.25A/µs

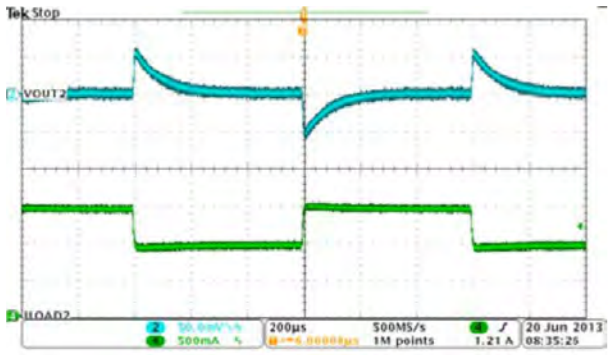


Figure 51. BUCK2, Load Transient, 1.0A to 1.5A SR=0.25A/µs

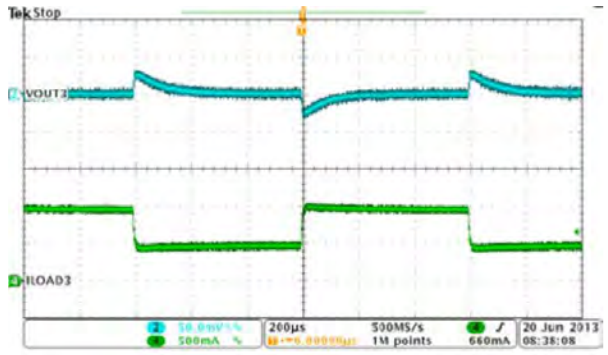


Figure 52. BUCK3, Load Transient, 0.5A to 1.0A SR=0.25A/µs

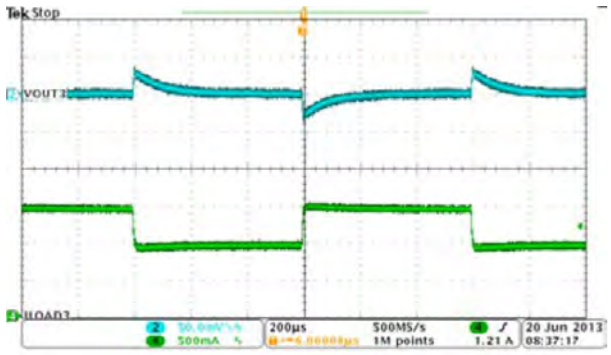


Figure 53. BUCK3, Load Transient, 1.0A to 1.5A SR=0.25A/µs

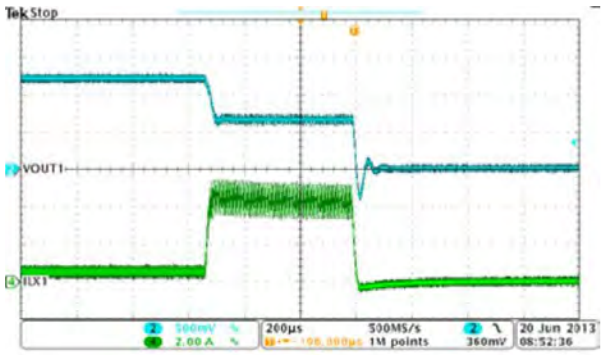


Figure 54. BUCK1, Over Current Protection

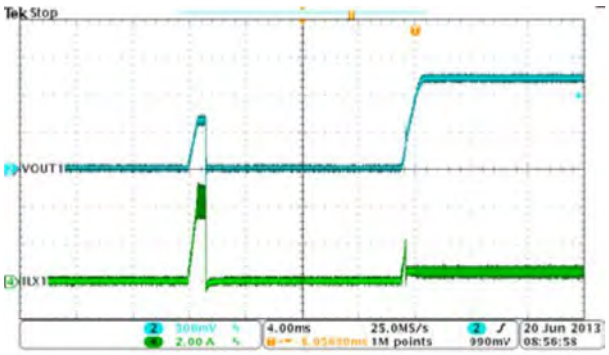


Figure 55. BUCK1, Hiccup and Recovery

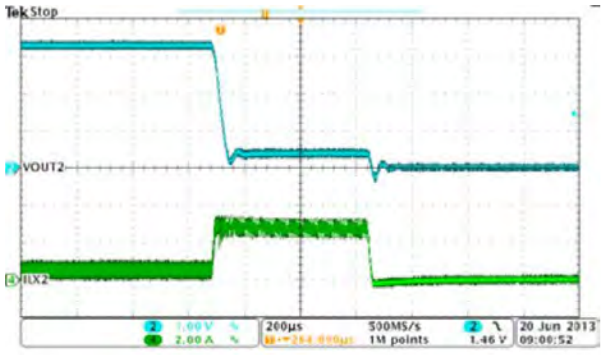


Figure 56. BUCK2, Over Current Protection

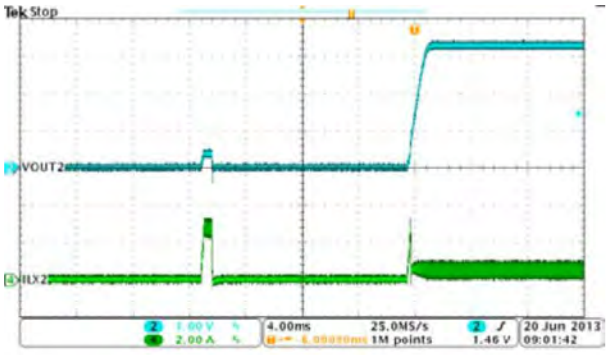


Figure 57. BUCK2, Hiccup and Recovery

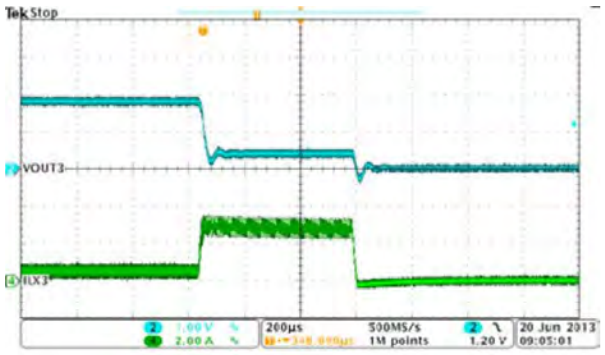


Figure 58. BUCK3, Over Current Protection

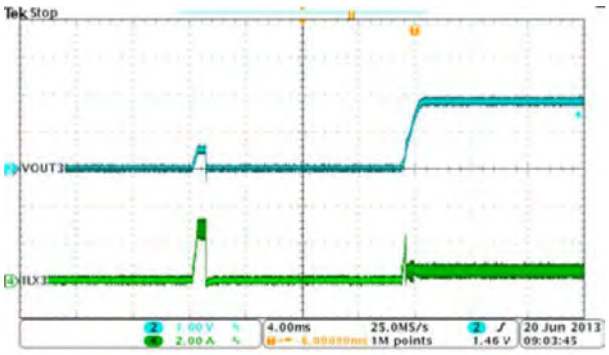


Figure 59. BUCK3, Hiccup and Recovery

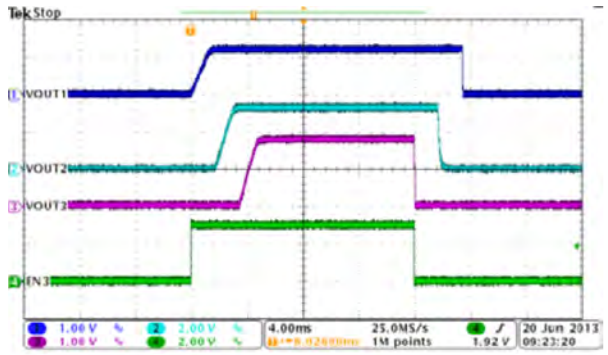


Figure 60. Automatic Power Sequencing, MODE=EN1=EN2=HIGH

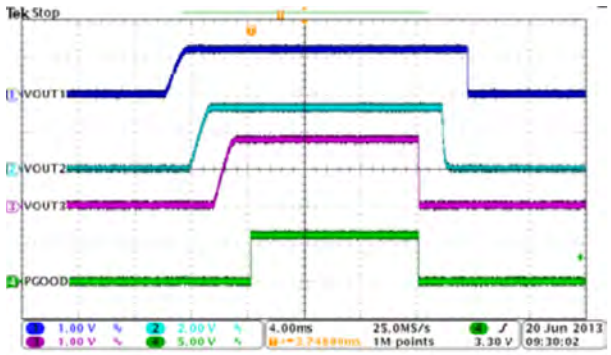


Figure 61. Automatic Power Sequencing, MODE=EN1=EN2=HIGH

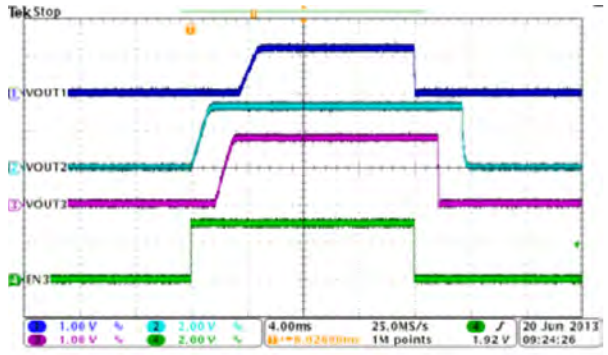


Figure 62. Automatic Power Sequencing, MODE=EN1= HIGH, EN2=LOW

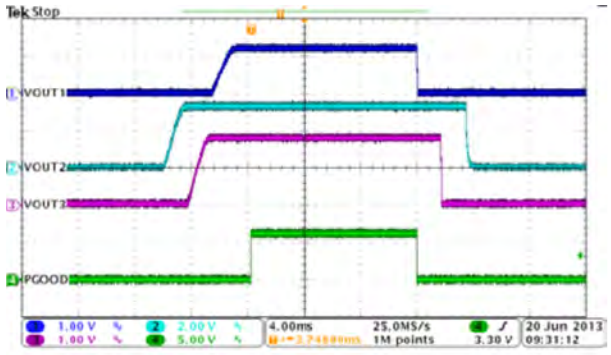


Figure 63. Automatic Power Sequencing, MODE=EN1=HIGH, EN2=LOW

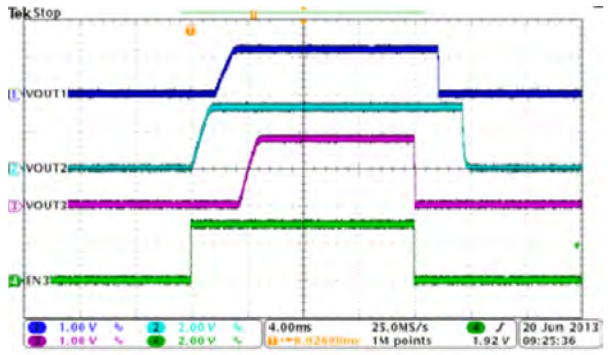


Figure 64. Automatic Power Sequencing, MODE=EN2=HIGH, EN1=LOW

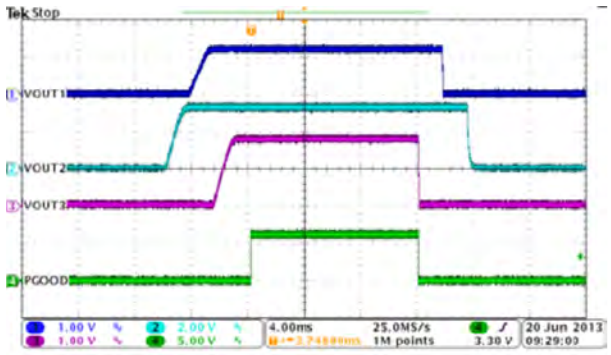


Figure 65. Automatic Power Sequencing, MODE=EN2=HIGH, EN1=LOW

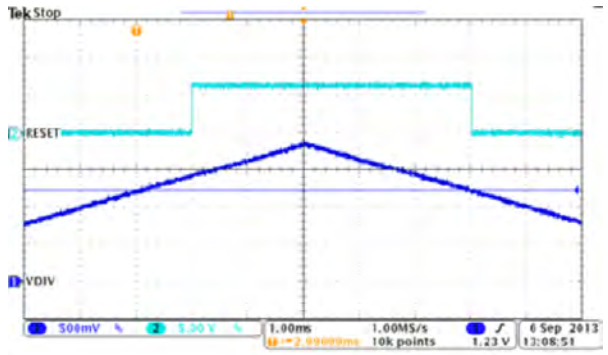


Figure 66. Trigger Voltage 1.23V, Reset vs VDIV

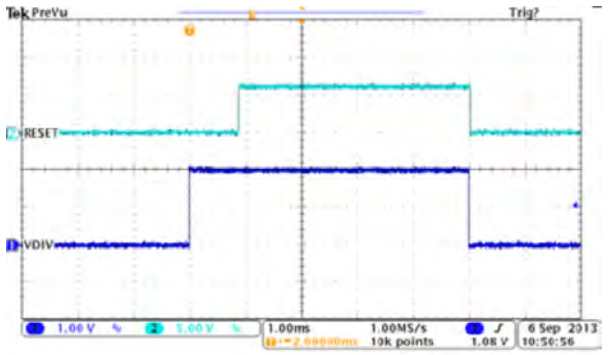
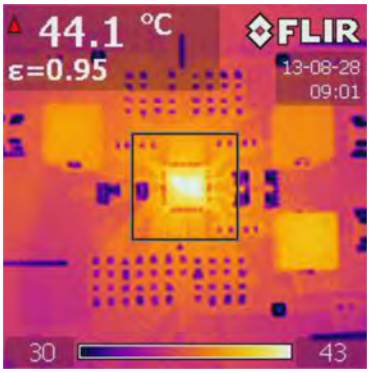
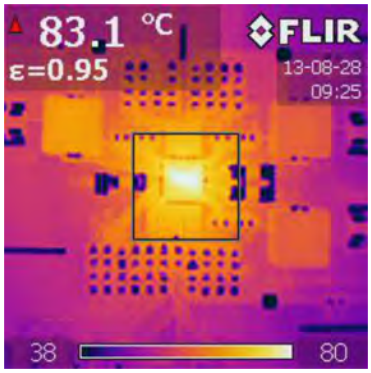


Figure 67. Deglitch Time, Reset vs VDIV



V_{IN} = 12 V V_{OUT1} = 1.2 V/1.5 A V_{OUT2} = 3.3 V/1 A
V_{OUT3} = 1.8 V/1 A
EVM Condition 4 Layers, 64mm x 69mm, T_A = 27.2°C

Figure 68. Thermal Signature of TPS65261EVM



V_{IN} = 12 V V_{OUT1} = 1.2 V/3 A V_{OUT2} = 3.3 V/2 A
V_{OUT3} = 1.8 V/2 A
EVM Condition 4 Layers, 64mm x 69mm, T_A = 27.2°C

Figure 69. Thermal Signature of TPS65261EVM

10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 18 V. This input power supply should be well regulated. If the input supply is located more than a few inches from the TPS65261 or TPS65261-1 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

The TPS65261, TPS65261-1 can be laid out on 2-layer PCB, illustrated in Figure 70.

Layout is a critical portion of good power supply design. See Figure 70 for a PCB layout example. The top contains the main power traces for PVIN, VOUT, and LX. Also on the top layer are connections for the remaining pins of the TPS65261, TPS65261-1 and a large top side area filled with ground. The top layer ground area should be connected to the bottom layer ground using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65261, TPS65261-1 device to provide a thermal path from the exposed thermal pad land to ground. The bottom layer acts as ground plane connecting analog ground and power ground.

For operation at full rated load, the top side ground area together with the bottom side ground plane must provide adequate heat dissipating area. There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path.

The FB and COMP pins are sensitive to noise so the resistors and capacitors should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown.

11.2 Layout Example

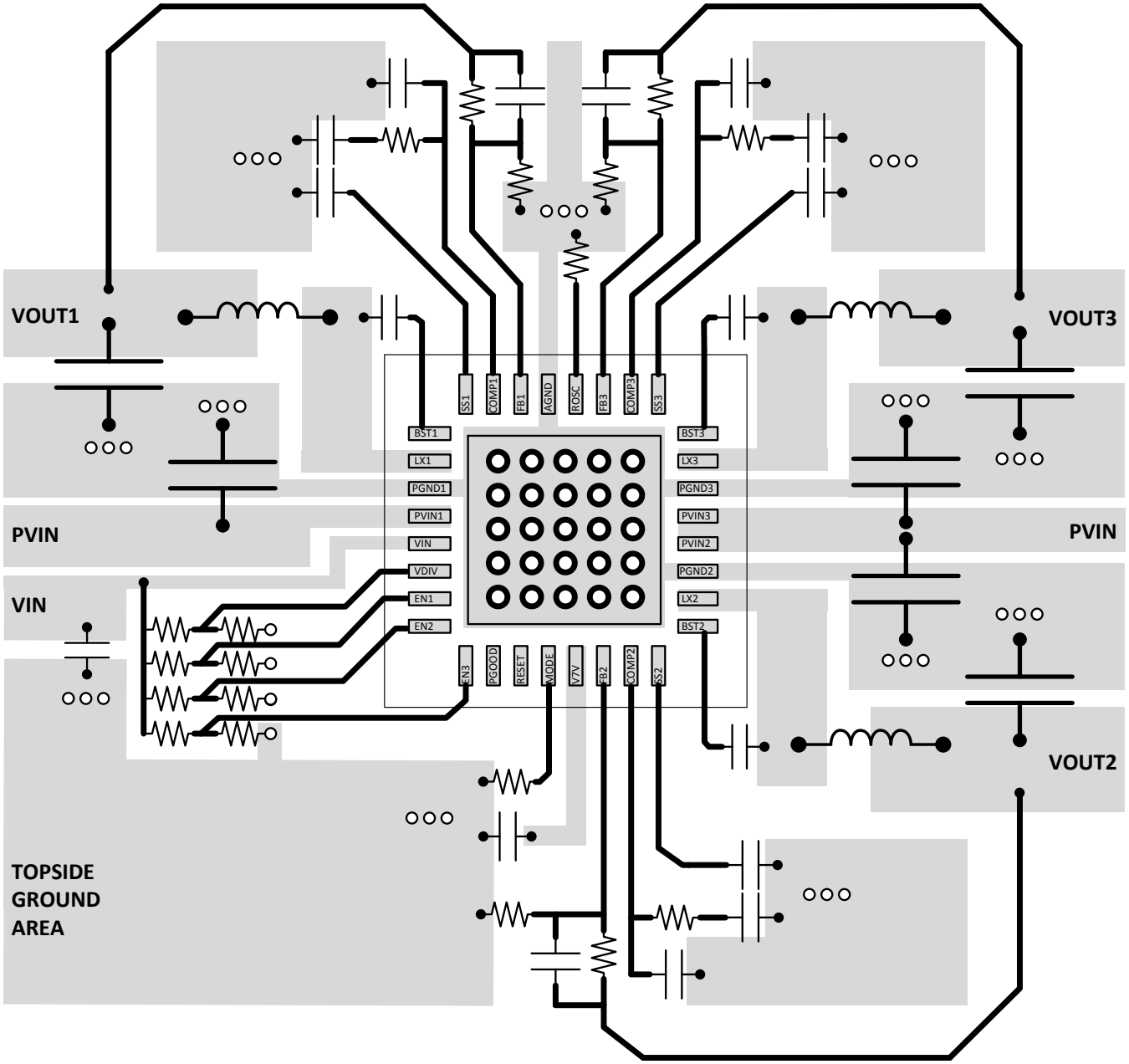


Figure 70. PCB Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
TPS65262	4.5V to 18V, triple buck with dual adjustable LDOs	Triple buck 3A/1A/1A output current, dual LDOs 100mA/200mA output current, automatic power sequencing
TPS65263	4.5V to 18V, triple buck with I2C interface	Triple buck 3A/2A/2A output current, I2C controlled dynamic voltage scaling (DVS)
TPS65651-1/2/3	4.5V to 18V, triple buck with different PGOOD deglitch time	Triple buck 3A/2A/2A output current, support 1s, 32ms, 256ms PGOOD deglitch time, adjustable current limit setting by external resistor
TPS65287	4.5V to 18V, triple buck with power switch and push button control	Triple buck 3A/2A/2A output current, up to 2.1-A USB power with over current setting by external resistor, push button control for intelligent system power-on/power-off operation
TPS65288	4.5V to 18V, triple buck with dual power switches	Triple buck 3A/2A/2A output current, 2 USB power switches current limiting at typical 1.2A (0.8/1.0/1.4/1.6/1.8/2.0/2.2A available with manufacture trim options)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65261	Click here	Click here	Click here	Click here	Click here
TPS65261-1	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65261-1RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65261-1	Samples
TPS65261-1RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65261-1	Samples
TPS65261RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65261	Samples
TPS65261RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65261	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

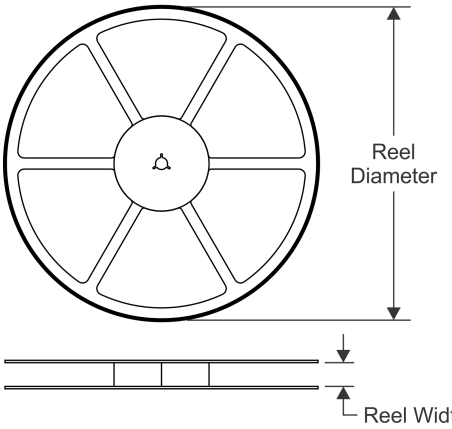
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

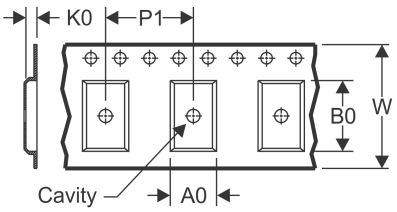
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

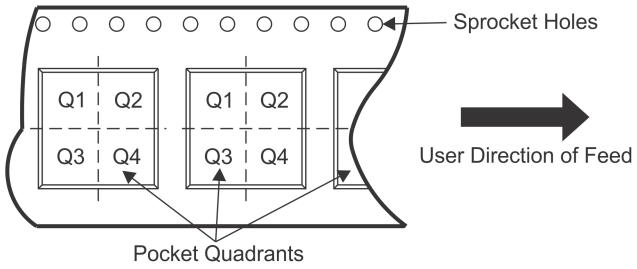


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

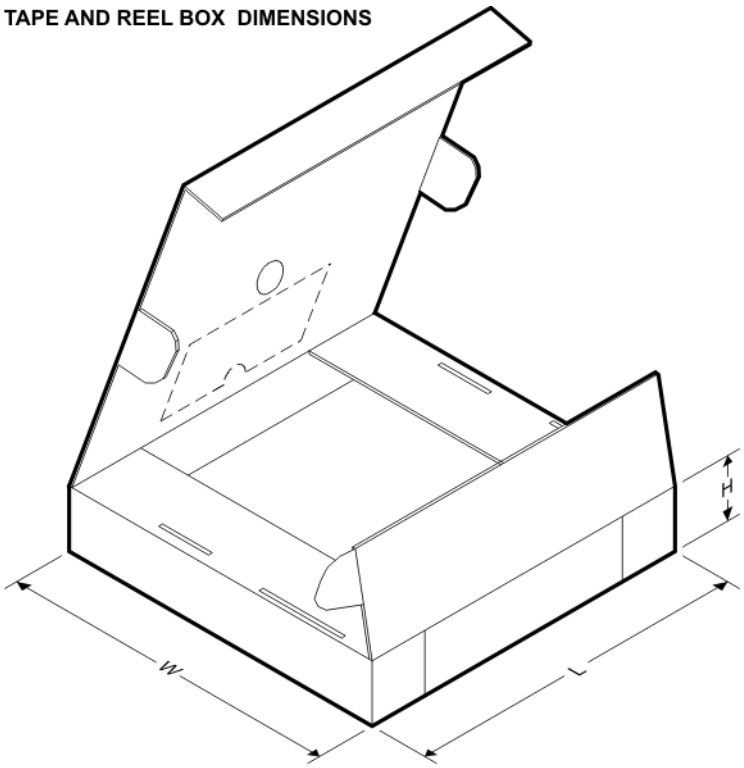
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65261-1RHBR	VQFN	RHB	32	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS65261-1RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65261-1RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65261-1RHBT	VQFN	RHB	32	250	180.0	12.5	5.25	5.25	1.1	8.0	12.0	Q2
TPS65261RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65261RHBT	VQFN	RHB	32	250	180.0	12.5	5.25	5.25	1.1	8.0	12.0	Q2
TPS65261RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

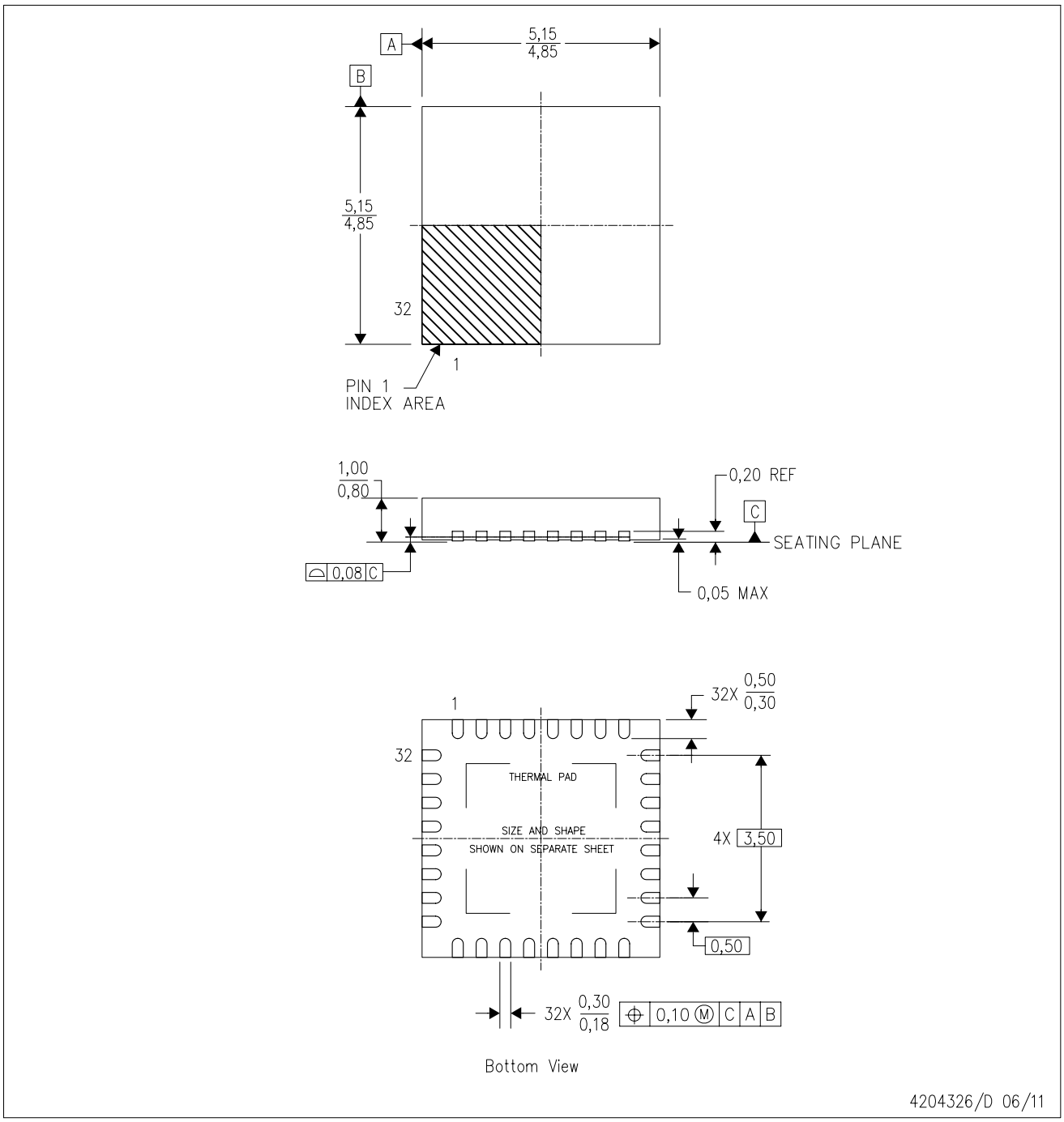
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65261-1RHBR	VQFN	RHB	32	3000	338.0	355.0	50.0
TPS65261-1RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS65261-1RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TPS65261-1RHBT	VQFN	RHB	32	250	205.0	200.0	33.0
TPS65261RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS65261RHBT	VQFN	RHB	32	250	338.0	355.0	50.0
TPS65261RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

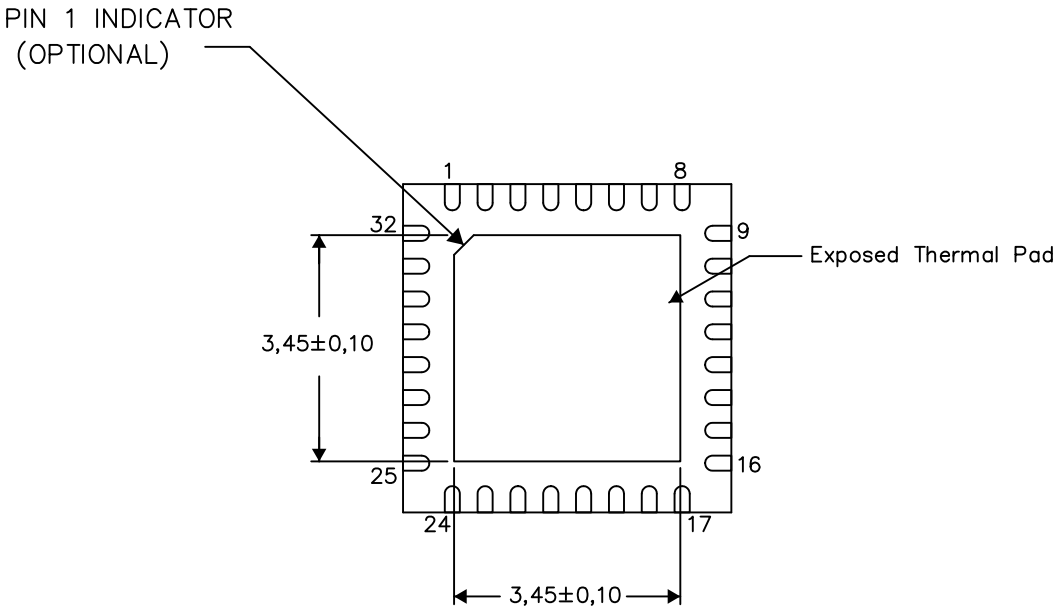
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



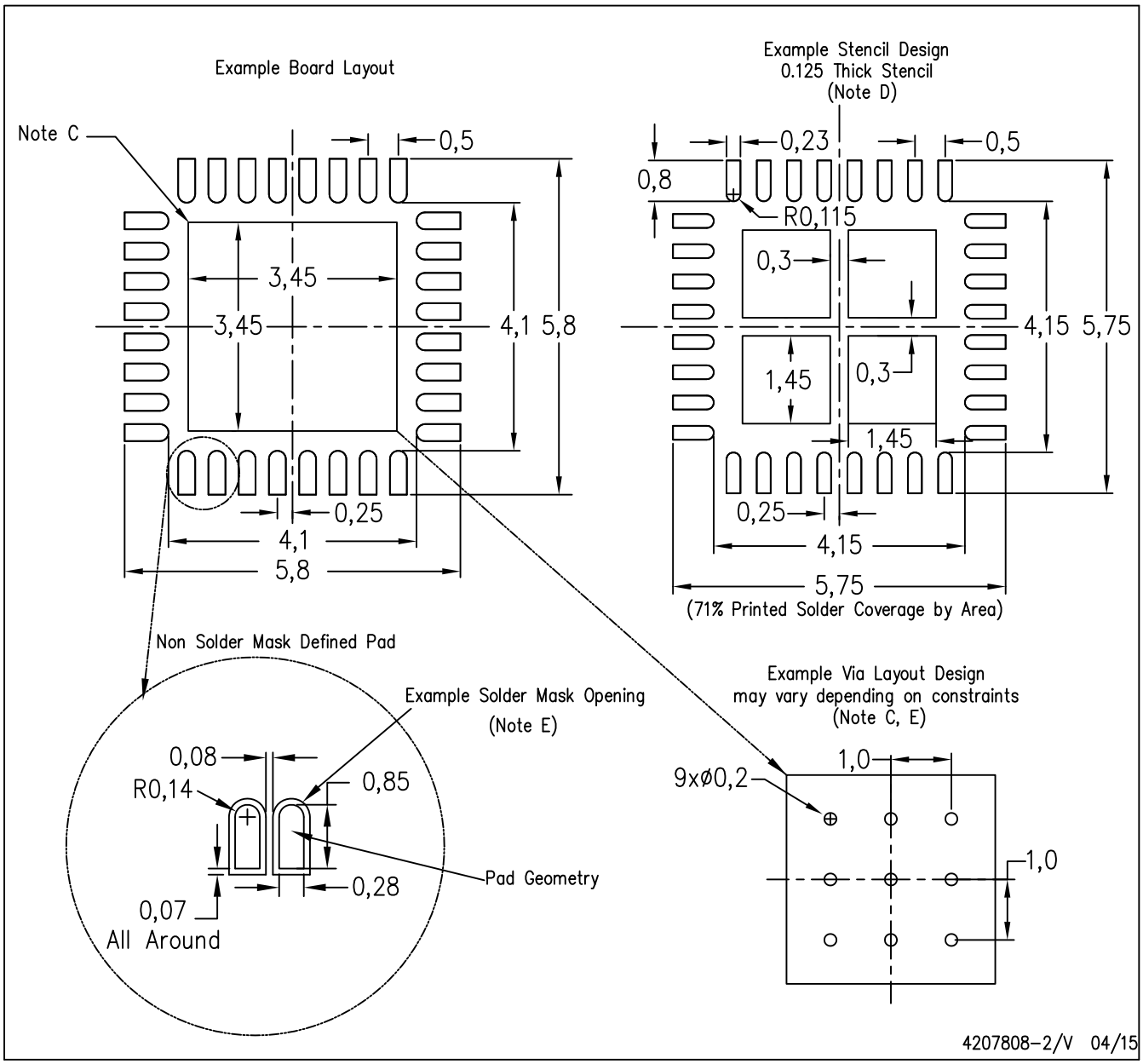
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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