LMC6022 Low Power CMOS Dual Operational Amplifier

Check for Samples: LMC6022

FEATURES

- **Specified for 100 kΩ and 5 kΩ Loads**
- **High Voltage Gain: 120 dB**
- **Low Offset Voltage Drift: 2.5 μV/°C**
- **Ultra Low Input Bias Current: 40 fA**
- **Input Common-Mode Range Includes V^-**
- **Operating Range from +5V to +15V Supply**
- **Low Distortion: 0.01% at 1 kHz**
- **Slew Rate: 0.11 V/μs**
- **Micropower Operation: 0.5 mW**

APPLICATIONS

- **High-Impedance Buffer or Preamplifier**
- **Current-to-Voltage Converter**
- **Long-Term Integrator**
- **Sample-and-Hold Circuit**
- **Peak Detector**
- **Medical Instrumentation**
- **Industrial Controls**

DESCRIPTION

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^-, low input bias current, and voltage gain (into 100k and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Connection Diagram

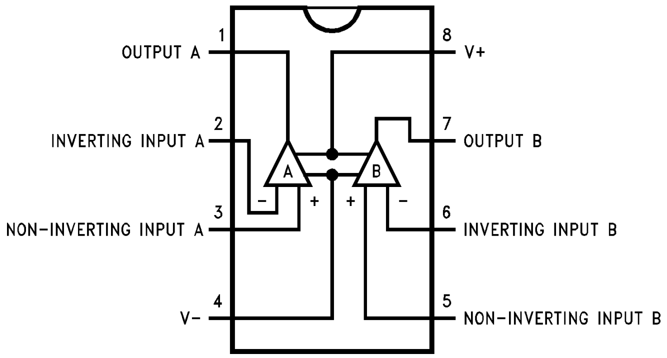

Figure 1. 8-Pin SOIC Top View

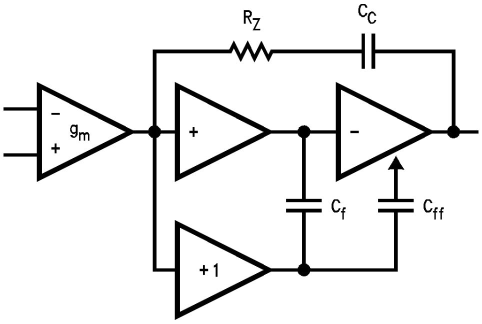

Figure 2. LMC6022 Circuit Topology (Each Amplifier)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance(2)	1000V
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	See(3)
Current at Input Pin	±5 mA
Output Short Circuit to V^-	See(4)
Output Short Circuit to V^+	See(5)

(1) Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(3) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

OPERATING RATINGS

Temperature Range		$-40°C \le T_J \le +85°C$
Supply Voltage Range		4.75V to 15.5V
Power Dissipation		See(1)
Thermal Resistance (θ_{JA})(2)	8-Pin SOIC	165°C/W

(1) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(2) All numbers apply for packages soldered directly into a PC board.

DC ELECTRICAL CHARACTERISTICS

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical(1)	LMC6022I Limit(2)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		μV/°C
I_B	Input Bias Current		0.04	**200**	pA max
I_{OS}	Input Offset Current		0.01	**100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or correlation.

DC ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical [1]	LMC6022I Limit [2]	Units
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **73**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **V^+ − 2.5**	V min
A_V	Large Signal Voltage Gain	$R_L = 100$ kΩ [3] Sinking Sourcing	1000	200 **100**	V/mV min
			500	90 **40**	V/mV min
		$R_L = 5$ kΩ [3] Sourcing Sinking	1000	100 **75**	V/mV min
			250	50 **20**	V/mV min
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100$ kΩ to 2.5V	4.987	4.40 **4.43**	V min
			0.004	0.06 **0.09**	V max
		$V^+ = 5V$ $R_L = 5$ kΩ to 2.5V	4.940	4.20 **4.00**	V min
			0.040	0.25 **0.35**	V max
		$V^+ = 15V$ $R_L = 100$ kΩ to 7.5V	14.970	14.00 **13.90**	V min
			0.007	0.06 **0.09**	V max
		$V^+ = 15V$ $R_L = 5$ kΩ to 7.5V	14.840	13.70 **13.50**	V min
			0.110	0.32 **0.40**	V max

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[3] $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

DC ELECTRICAL CHARACTERISTICS (continued)

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical(1)	LMC6022I Limit(2)	Units
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V Sinking, V_O = 5V(4)	22	13 **9**	mA min
			21	13 **9**	mA min
		V^+ = 15V Sourcing, V_O = 0V Sinking, V_O = 13V (5)	40	23 **15**	mA min
			39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers V_O = 1.5V	86	140 **165**	μA max

(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

AC ELECTRICAL CHARACTERISTICS

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless other otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical(1)	LMC6022I Limit(2)	Units
SR	Slew Rate	See(3)	0.11	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		0.35		MHz
φ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	See(4)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		**nV/$\sqrt{Hz}$**
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		**pA/$\sqrt{Hz}$**

(1) Typical values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or correlation.
(3) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred. V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage

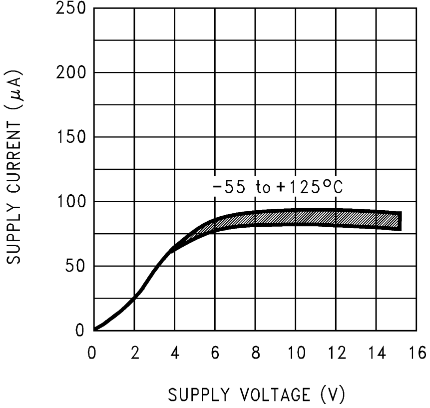


Figure 3.

Input Bias Current vs. Temperature

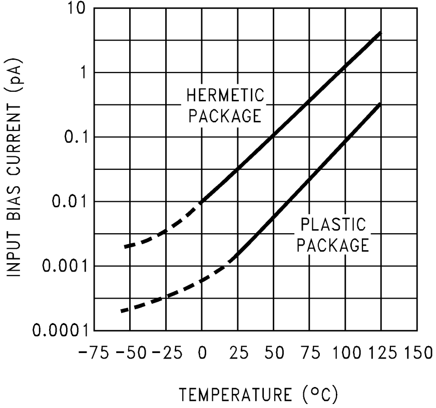


Figure 4.

Input Common-ModeVoltage Range vs.Temperature

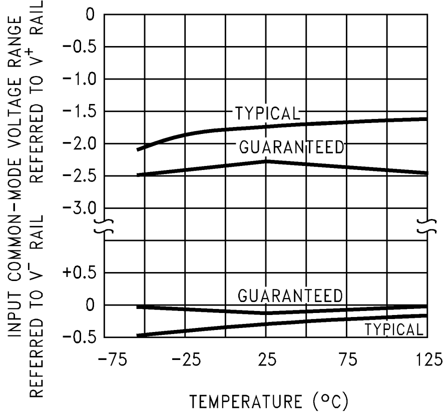


Figure 5.

Output Characteristics Current Sinking

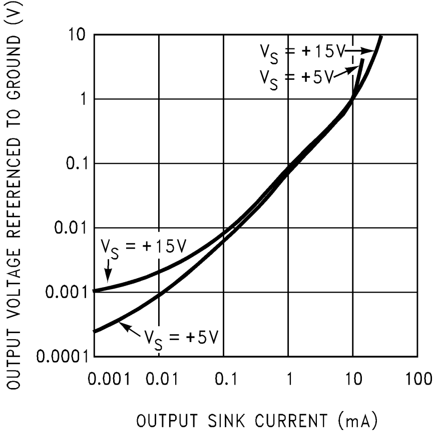


Figure 6.

Output Characteristics Current Sourcing

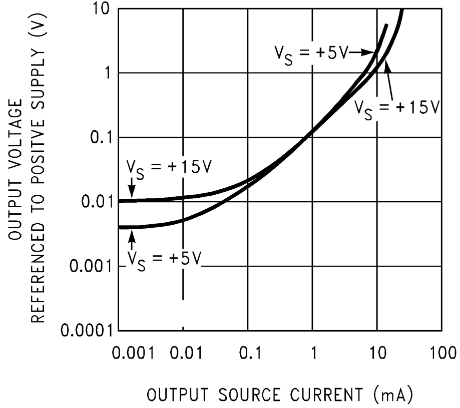


Figure 7.

Input Voltage Noise vs. Frequency

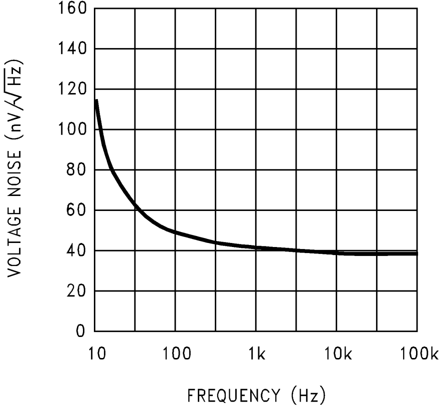


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Crosstalk Rejection vs. Frequency

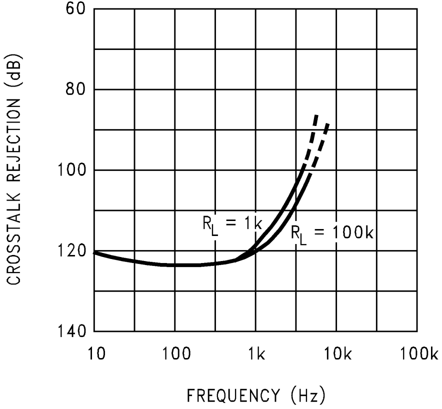


Figure 9.

CMRR vs. Frequency

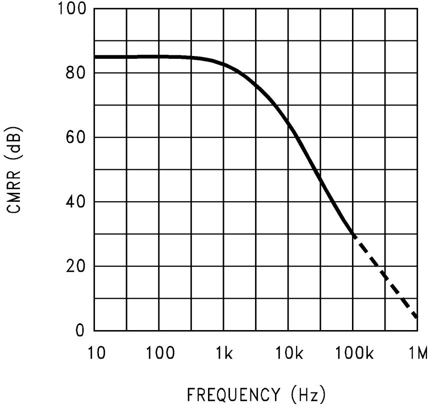


Figure 10.

CMRR vs. Temperature

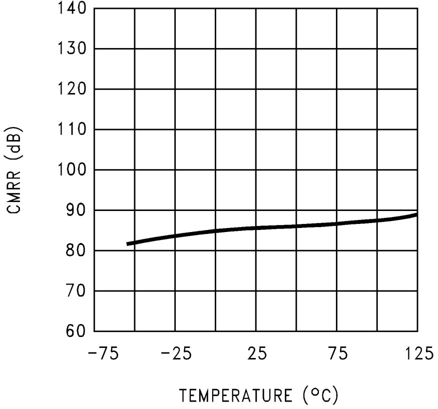


Figure 11.

Power Supply Rejection Ratio vs. Frequency

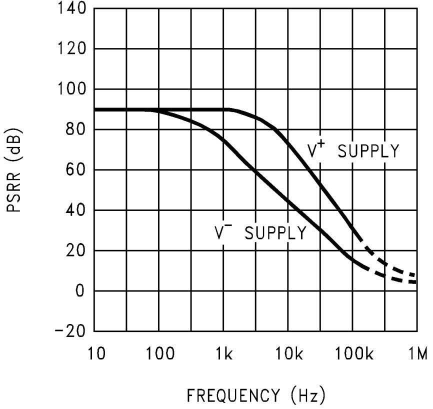


Figure 12.

Open-Loop Voltage Gain vs. Temperature

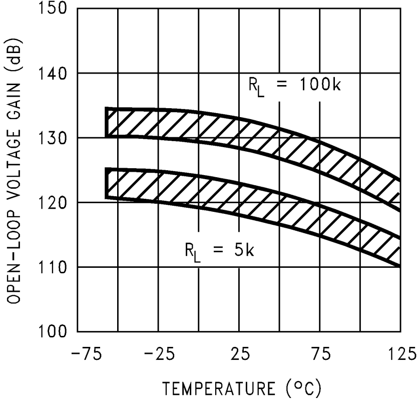


Figure 13.

Open-Loop Frequency Response

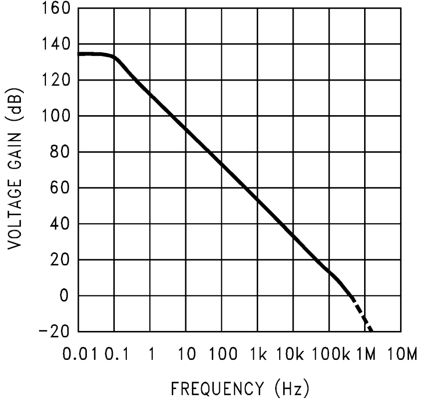


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_S = \pm7.5V$, $T_A = 25°C$ unless otherwise specified

Gain and Phase Responses vs. Load Capacitance

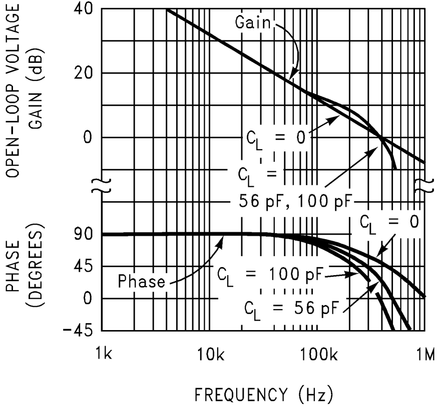


Figure 15.

Gain and Phase Responses vs. Temperature

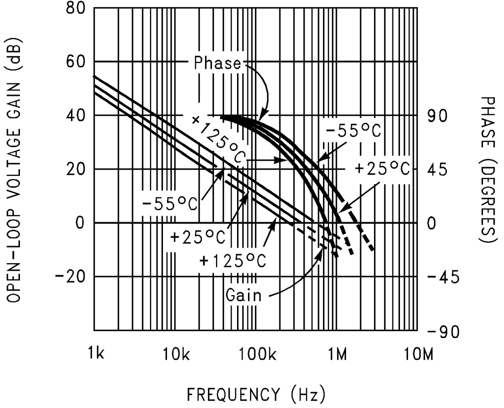


Figure 16.

Gain Error (V_{OS} vs. V_{OUT})

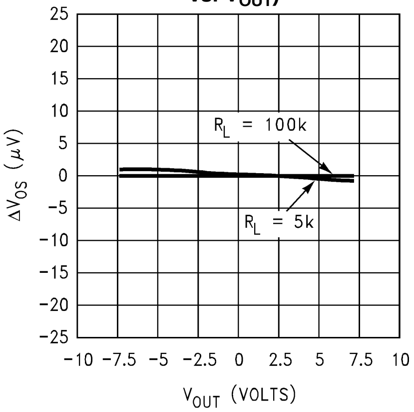


Figure 17.

Non-Inverting Slew Rate vs. Temperature

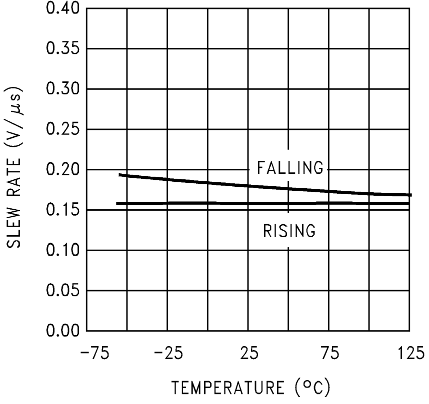


Figure 18.

Inverting Slew Rate vs. Temperature

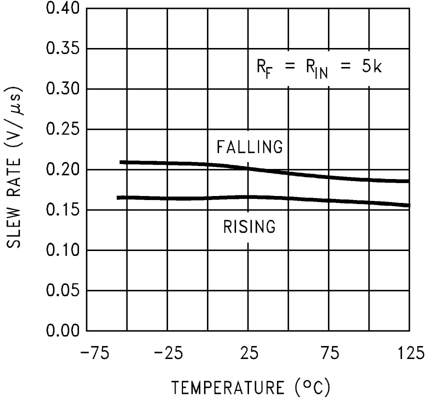


Figure 19.

Large-Signal Pulse Non-Inverting Response ($A_V = +1$)

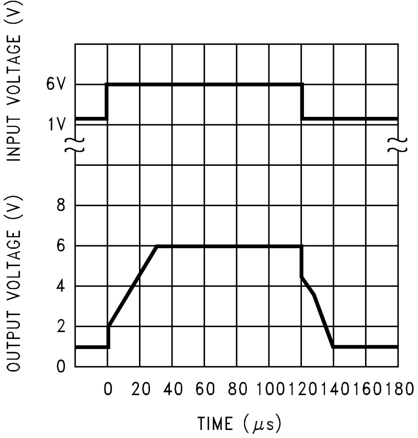


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Non-Inverting Small Signal Pulse Response (A_V = +1)

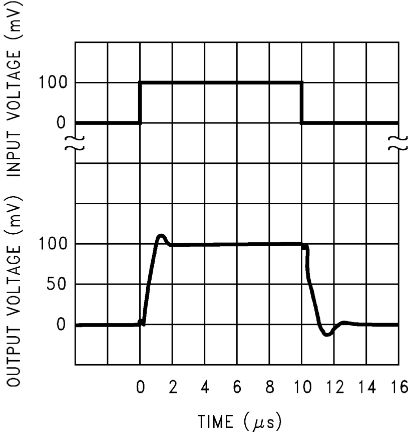


Figure 21.

Inverting Large-Signal Pulse Response

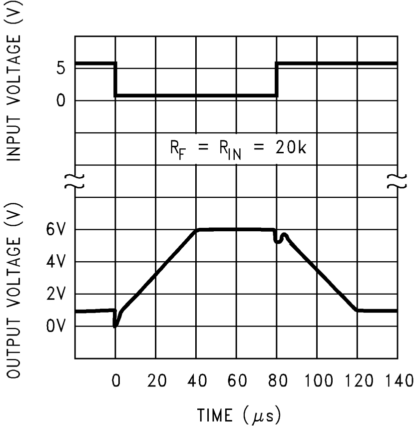


Figure 22.

Inverting Small-Signal Pulse Response

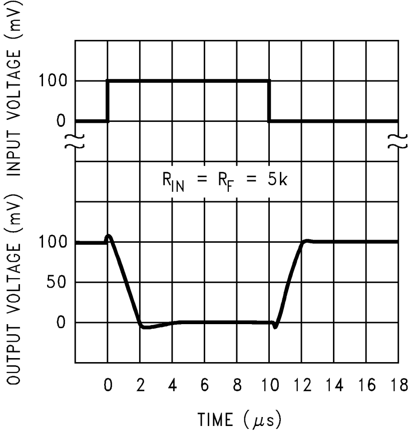
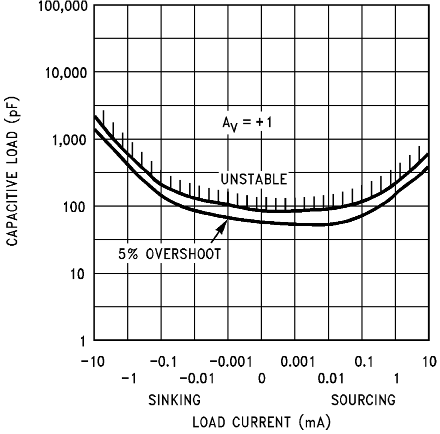


Figure 23.

Stability vs. Capacitive Load



Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Figure 24.

Stability vs. Capacitive Load

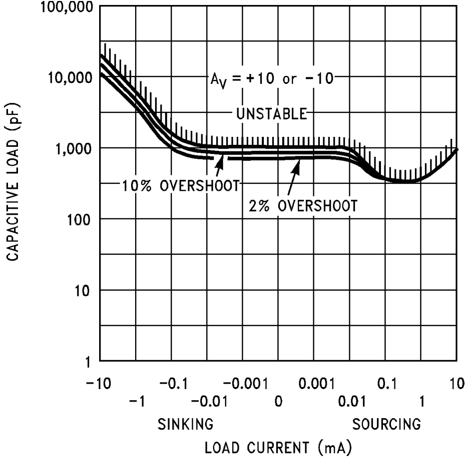


Figure 25.

APPLICATION HINTS

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6022 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

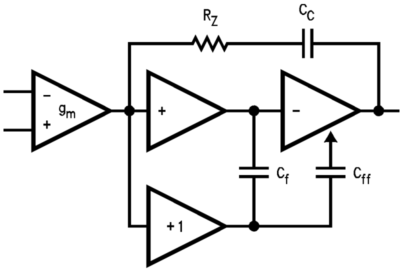


Figure 26. LMC6022 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6022 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the TYPICAL PERFORMANCE CHARACTERISTICS.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

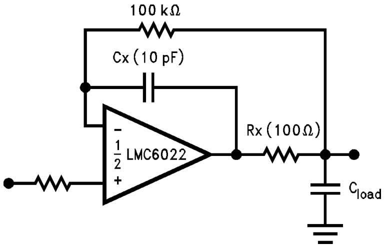


Figure 27. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 28). Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

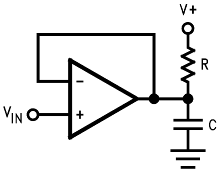


Figure 28. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6022, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6022's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 29. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6022's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 30a, Figure 30b, Figure 30c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 30d.

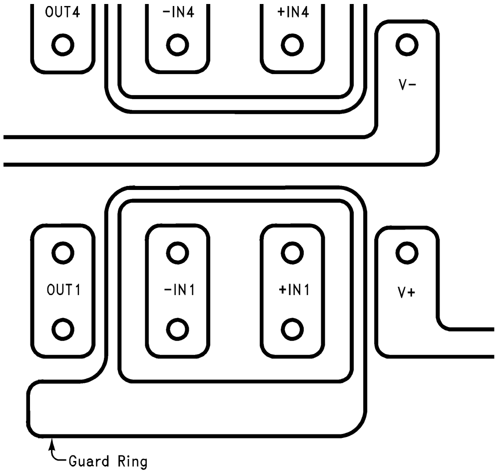
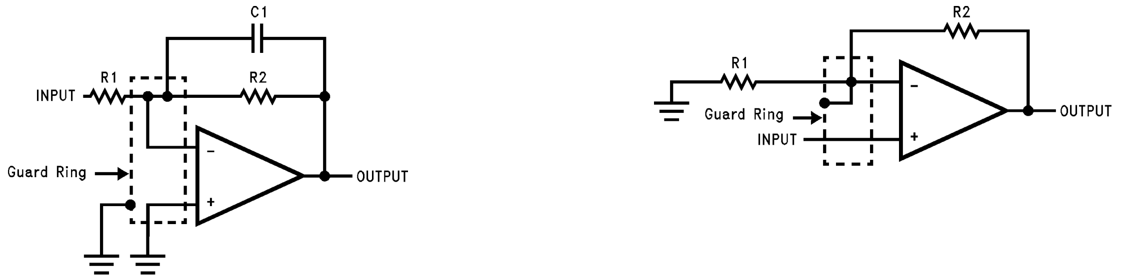
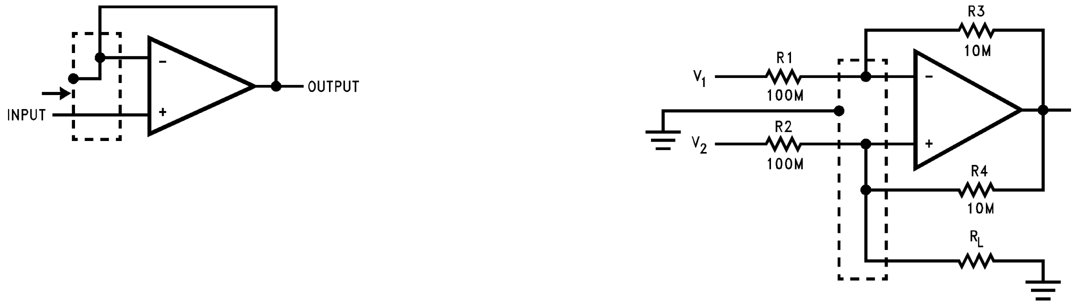


Figure 29. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)



(a) Inverting Amplifier Guard Ring Connections

(b) Non-Inverting Amplifier Guard Ring Connections

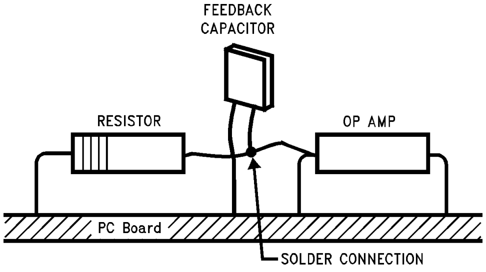


(c) Follower Guard Ring Connections

(d) Howland Current Pump Guard Ring Connections

Figure 30. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 31.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 31. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 32 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^{-} = \frac{dV_{OUT}}{dt} \times C2. \quad (1)$$

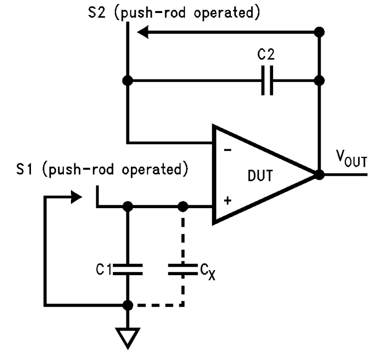


Figure 32. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

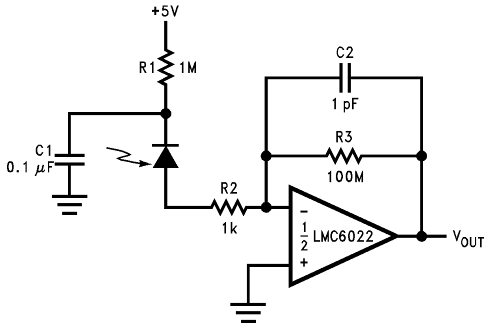
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x) \tag{2}$$

where C_x is the stray capacitance at the + input.

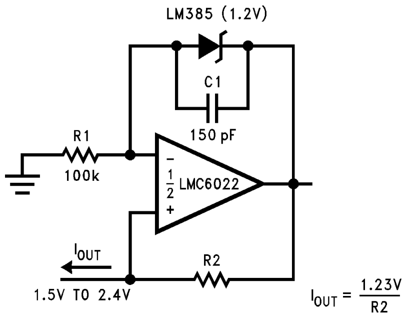
Typical Single-Supply Applications

($V+ = 5.0\ V_{DC}$)



Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Figure 33. Photodiode Current-to-Voltage Converter



(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Figure 34. Micropower Current Source

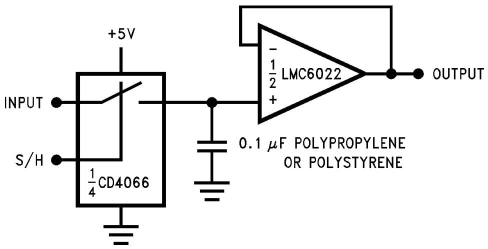
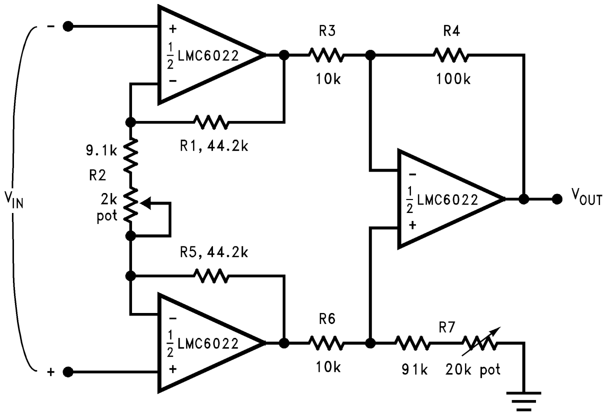


Figure 35. Low-Leakage Sample-and-Hold

($V+ = 5.0\ V_{DC}$)



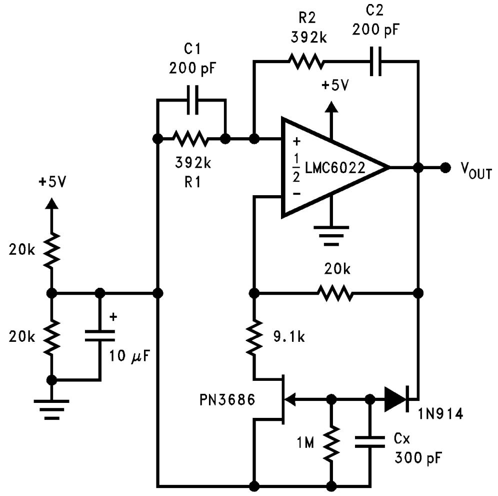
If R1 = R5, R3 = R6, and R4 = R7;

Then $\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$

$\therefore A_V \approx 100$ for circuit shown

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Figure 36. Instrumentation Amplifier



Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

Figure 37. Sine-Wave Oscillator

(V+ = 5.0 V_{DC})

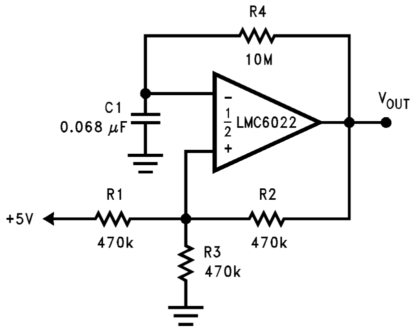


Figure 38. 1 Hz Square-Wave Oscillator

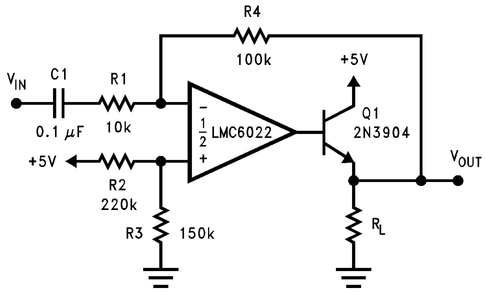
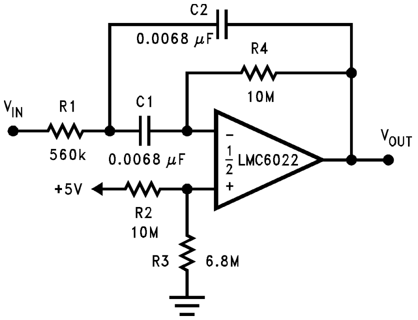
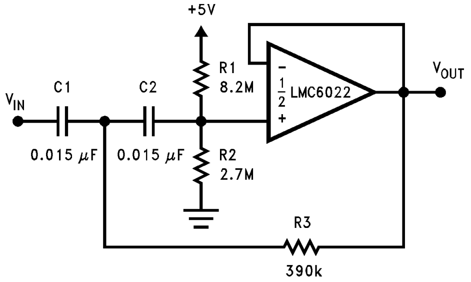


Figure 39. Power Amplifier



f_O = 10 Hz
Q = 2.1
Gain = −8.8

Figure 40. 10 Hz Bandpass Filter



f_C = 10 Hz
d = 0.895
Gain = 1

Figure 41. 10 Hz High-Pass Filter (2 dB Dip)

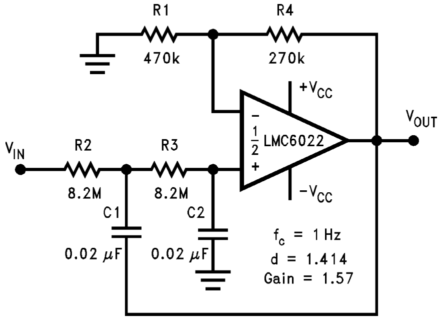
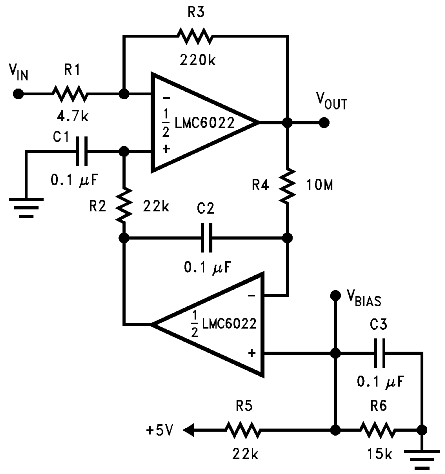


Figure 42. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)

($V+ = 5.0\ V_{DC}$)



Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

Figure 43. High Gain Amplifier with Offset Voltage Reduction

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6022IM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 22IM	Samples
LMC6022IMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMC60 22IM	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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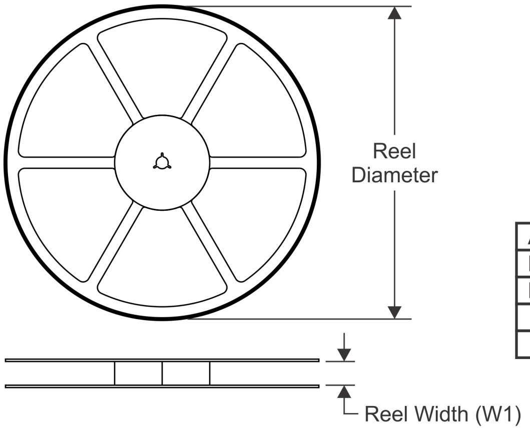
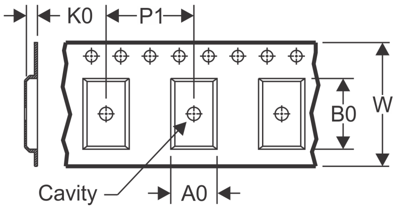
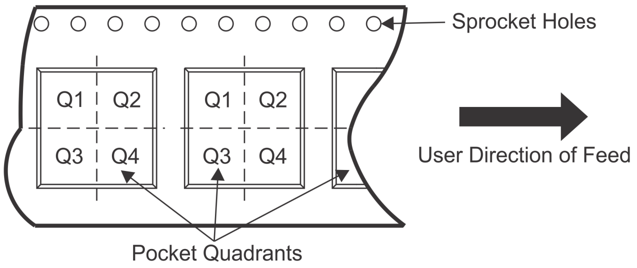


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

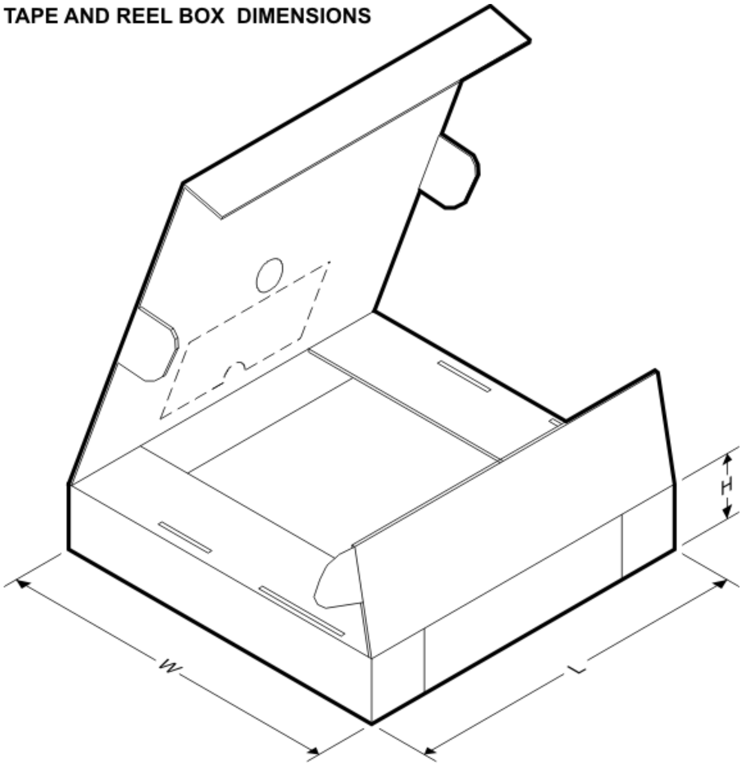
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6022IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

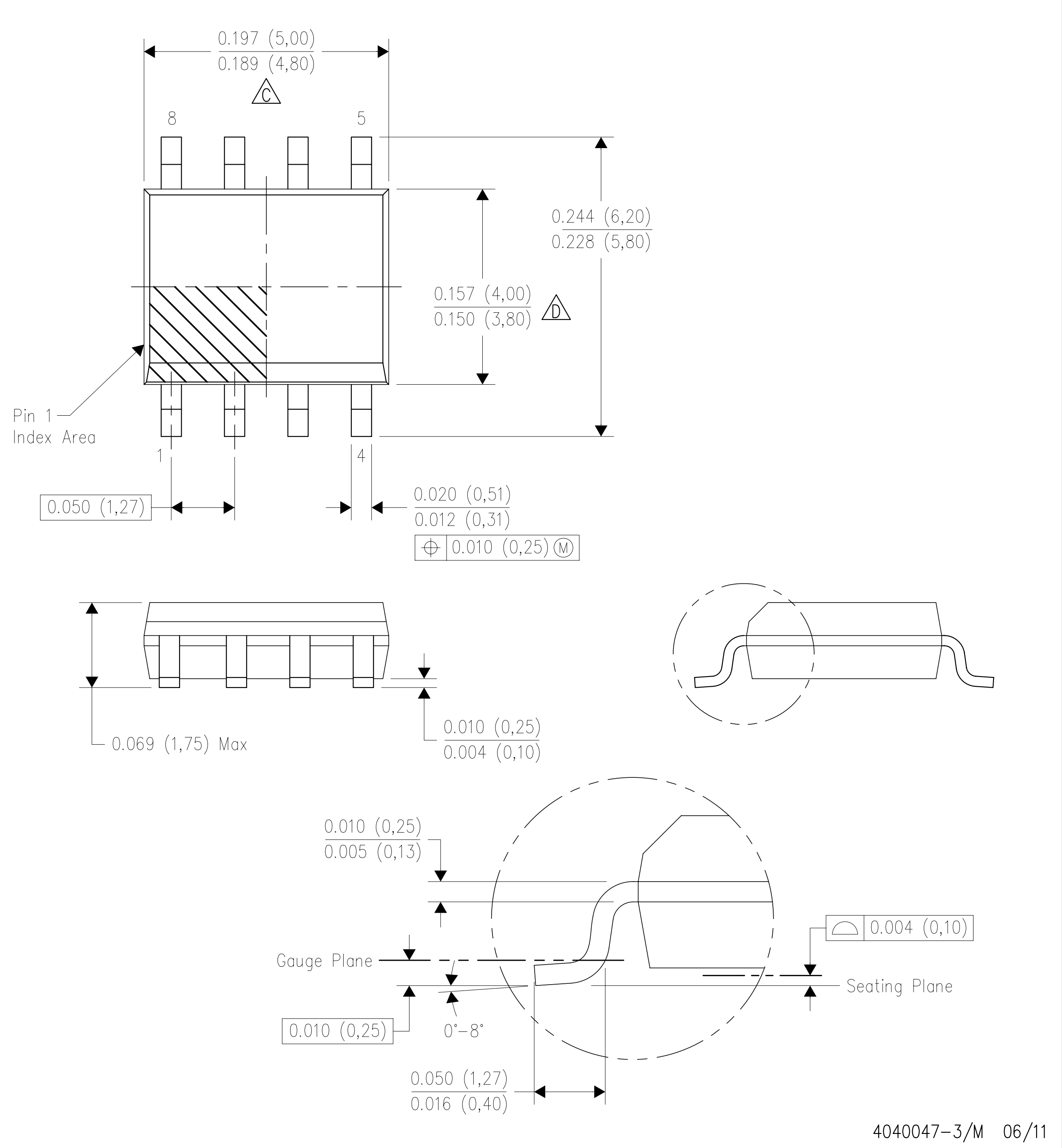
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6022IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

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