10-Bit, 35MSPS A/D Converter

PRODUCT DESCRIPTION

The MS9280 is a single-chip, single power supply, 10bit, 35MSPS analog-to-digital converter. It is integrated with the sample-and-hold amplifier and reference power supply internally. The MS9280 uses multistage differential pipeline architecture to guarantee no missing codes over the full operating temperature range at 35MSPS data rate.

The input of the MS9280 is suitable for image, video and communication system. User can select single-ended input or differential inputs according to actual need. User can also select input range and eliminate offset.

The sample-and-hold amplifier in the MS9280 is suitable for both multiplexed system and successive channels that switch full-scale voltage. The input frequency of sampling single channel can exceed the Nyquist rate. With internal clamp circuit, ac-coupled input can be shifted to a fixed level, and the dynamic performance is excellent.

The MS9280 is integrated with programmable reference internally. An external reference with high precision can be chosen to satisfy the system accuracy requirements according to the need of system.

A single clock input controls the internal conversion cycle. The digital output is in binary data information. The out-of-range (OTR) represents that the input signal exceeds the minimum or maximum quantization range.

The MS9280 operates in a single power supply ranging from 2.7V to 5.5V and suits for high-speed and low power dissipation applications. The industrial temperature of the MS9280 is from -40°C to +125°C.

SSOP28

FEATURES

- 10bit, 35MSPS Pipeline ADC
- Low Power Dissipation: 90mV (3V Power Supply)
- Wide Operating Voltage Range: 2.7V ~ 5.5V
- High Linearity: DNL: 0.2 LSB
- Low Power Dissipation Control Mode
- Three-state Outputs
- Quantized Range Detection
- Built-in Clamp Function
- High-precision Programmable Reference
- IF Sub-sampling up to 135MHz

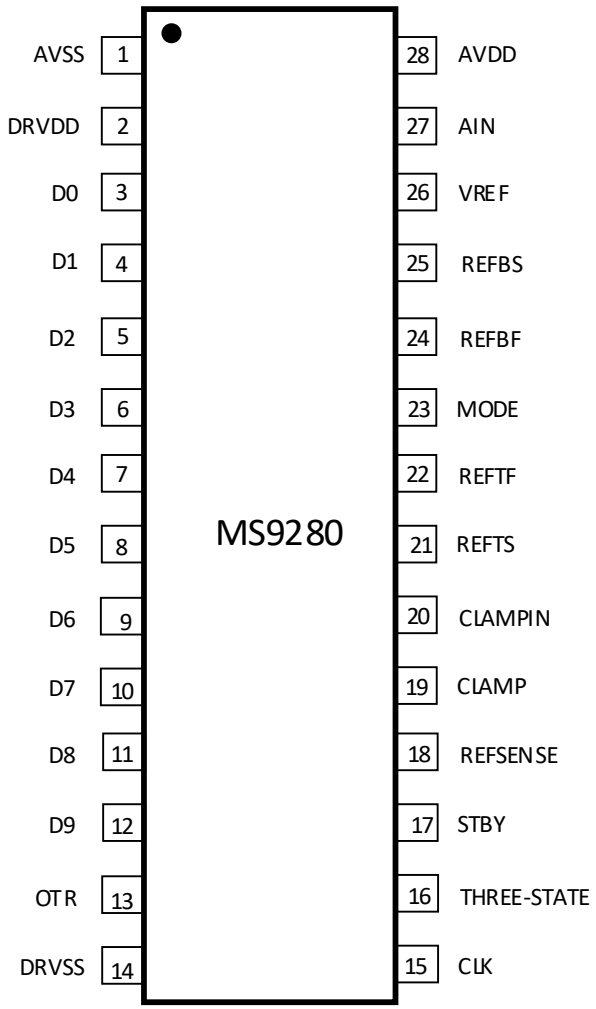
APPLICATIONS

- Image and Video
- Communication System

PRODUCT SPECIFICATIONS

Part Number	Package	Marking
MS9280	SSOP28	MS9280

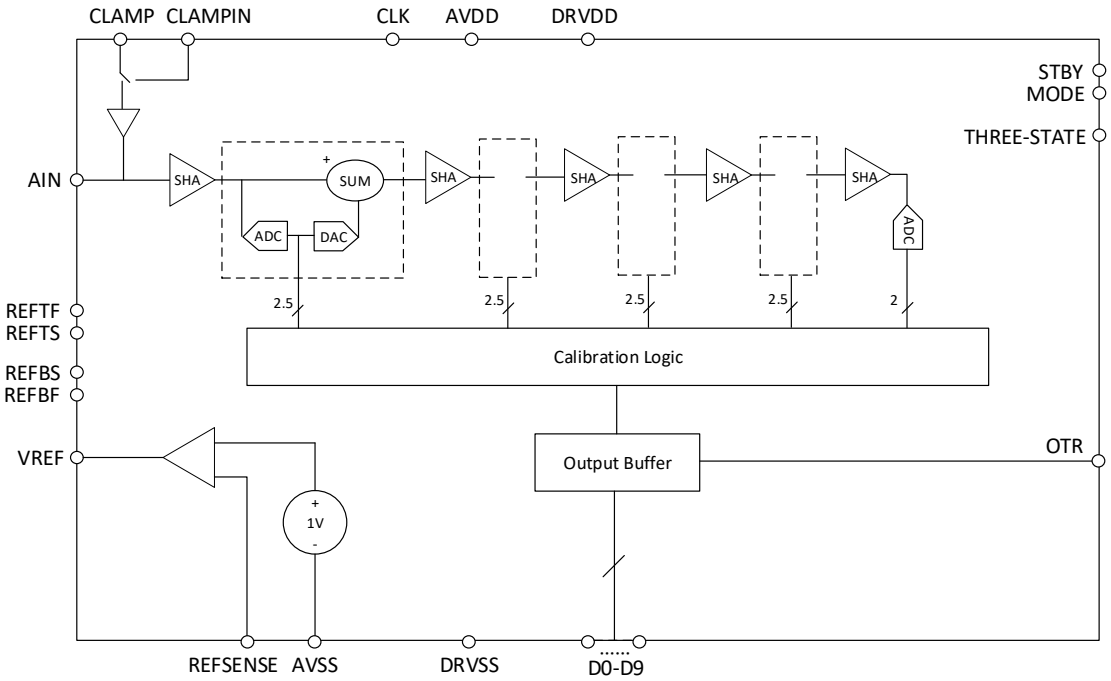
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Description
1	AVSS	Analog Ground
2	DRVDD	Digital Power Supply
3-12	D0-D9	Digital Bit. D0 is the LSB, and D9 is the MSB
13	OTR	Out-of-Range Detection
14	DRVSS	Digital Ground
15	CLK	Clock Input
16	THREE_STATE	Three-state Control. High: High Impedance State; Low: Normal Operation
17	STBY	Standby Mode. High: Standby Mode; Low: Normal Operation
18	REFSENSE	Reference Selection
19	CLAMP	Clamp Control. High: Clamp Mode; Low: No Clamp Mode
20	CLAMPIN	Clamp Voltage Setting
21	REFTS	Top Reference
22	REFTF	Top Reference Decoupling
23	MODE	Mode Selection
24	REFBF	Bottom Reference Decoupling
25	REFBS	Bottom Reference
26	VREF	Internal Reference Voltage
27	AIN	Analog Input
28	AVDD	Analog Power Supply

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	With Respect to	Symbol	Range	Unit
Analog Power Supply	AVSS	AVDD	-0.3 ~ +6.5	V
Analog Power Supply	DRVDD	AVDD	-6.5 ~ +6.5	V
Digital Power Supply	DRVSS	DRVDD	-0.3 ~ +6.5	V
Analog Ground	DRVSS	AVSS	-0.3 ~ +0.3	V
Mode Selection Pin Voltage	AVSS	MODE	-0.3 ~ AVDD + 0.3	V
Clock Input Pin Voltage	AVSS	CLK	-0.3 ~ AVDD + 0.3	V
Digital Output Voltage	DRVSS		-0.3 ~ DRVDD + 0.3	V
Analog Input Voltage	AVSS	AIN	-0.3 ~ AVDD + 0.3	V
Internal Reference Voltage	AVSS	VREF	-0.3 ~ AVDD + 0.3	V
Reference Selection Pin Voltage	AVSS	REFSENSE	-0.3 ~ AVDD + 0.3	V
Top Reference Voltage Decoupling, Bottom Reference Voltage Decoupling	AVSS	REFTF, REFBF	-0.3 ~ AVDD + 0.3	V
Top Reference Voltage, Bottom Reference Voltage	AVSS	REFTS, REFBS	-0.3 ~ AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature			-65 ~ +150	°C
Lead Temperature (10s)			+300	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, AVDD=+3V, DRVDD=+3V, Fs=35MHz (50% duty cycle), MODE=AVDD, 2V input range: from 0.5V to 2.5V, external reference.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution			10		Bits
Conversion Rate				35	MHz
Differential Nonlinearity	DNL	±0.2		±1.0	LSB
Integral Nonlinearity	INL	±0.3		±1.5	LSB
Offset Error	EZS	±0.2		±1.8	%FSR
Gain Error	EFS	±1.2		±3.9	%FSR
Top Reference Voltage	REFTS	1		AVDD	V
Bottom Reference Voltage	REFBS	GND		AVDD-1	V
Differential Reference Voltage			2		V
VREF (1V)			1		V
Reference Tolerance			10	25	mV
VREF (2V)			2		V
Load Regulation (1V)			0.5	2	mV
Input Voltage Range	AIN	REFBS		REFTS	V
Input Capacitance	CIN		1		pF
Aperture Delay	tAD		4		ns
Aperture Jitter	tAJ		2		ps
Input Bandwidth	BW		300		MHz
DC Leakage Current			43		μA
Analog Voltage	AVDD	2.7	3	5.5	V
Digital Drive Voltage	DRVDD	2.7	3	5.5	V
Power Supply Current	IAVDD		31.7	36.7	mA
Power Dissipation	PD		95	110	mW
Sleep Mode			4		mW
Gain Error Power Supply Rejection Ratio			1		%FS
Signal-to-Noise Ratio	SNR	47.8		49	dB
Signal-to-Noise and Distortion Ratio	SINAD	46.5		49	dB

Parameter	Symbol	Min	Typ	Max	Unit
Effective Bits		7.7		7.8	dB
Total Harmonic Distortion	THD		-62	-49.5	dB
Spurious Free Dynamic Range	SFDR	66		51.4	dB
Differential Phase	DP		0.2		Degree
Differential Gain	DG		0.08		%
High-Level Input Voltage	V_{IH}	2.4			V
Low-Level Input Voltage	V_{IL}			0.3	V
Output High Impedance	I_{OZ}	-10		+10	μA
Data Valid Delay	t_{OD}		25		ns
Data Enable Delay	t_{DEN}		25		ns
Data High-impedance Delay	t_{DHZ}		13		ns
Digital High-Level Output Voltage (Io=50μA)	V_{OH}	2.95			V
Digital High-Level Output Voltage (Io=500μA)		2.8			V
Digital Low-Level Output Voltage (Io=1.6mA)	V_{OL}			0.4	V
Digital Low-Level Output Voltage (Io=50μA)				0.05	V
Digital High-Level Output Voltage (Io=50μA)	V_{OH}	4.5			V
Digital High-Level Output Voltage (Io=500μA)		4.4			V
Digital Low-Level Output Voltage (Io=1.6mA)	V_{OL}			0.4	V
Digital Low-Level Output Voltage (Io=50μA)				0.1	V
Clock High-Level Pulse Width	t_{CH}	10			ns
Clock Low-level Pulse Width	t_{CL}	10			ns
Pipeline Latency			3		Cycles
Clamp Error Voltage	E_{OC}		50	80	mV
Clamp Pulse Width	t_{CPW}		2		μs

APPLICATIONS INFORMATION

Operating Principle

The MS9280 implements a pipelined multistage architecture to achieve low power dissipation and high-speed data conversion. It divides the whole conversion accuracy into single-order converters with low accuracy. The results of each order conversion achieve high-precision data conversion through internal digital calibration circuit under the timing control.

Operating Mode

The MS9280 is suitable for various kinds of image, video, communication and instrumentation applications, compatible with series AD876-8 series. Appropriate operating modes can be chosen to optimize characteristics according to factual system. To realize its flexibility, the internal programmable switches realize the different operating modes. The three internal modules: voltage reference, voltage buffer and analog input can be chosen in different switching modes. See Table 1 and mode description legends for the specific implementation form and operating modes.

Table 1. Mode Selection

<table>
<tr><th>Mode</th><th>Input Connection</th><th>Input Span</th><th>Mode Pin</th><th>REFSENSE Pin</th><th>REF</th><th>REFTS</th><th>REFBS</th></tr>
<tr><td rowspan="2">Top/Bottom</td><td>AIN</td><td>1V</td><td>AVDD</td><td colspan="3">Short REFSENSE、REFTS and VREF</td><td>AGND</td></tr>
<tr><td>AIN</td><td>2V</td><td>AVDD</td><td>AGND</td><td colspan="2">Short REFTS and VREF</td><td>AGND</td></tr>
<tr><td rowspan="2">Center</td><td>AIN</td><td>1V</td><td>AVDD/2</td><td colspan="2">Short VREF and REFSENSE</td><td>AVDD/2</td><td>AVDD/2</td></tr>
<tr><td>AIN</td><td>2V</td><td>AVDD/2</td><td>AGND</td><td>Not Connection</td><td>AVDD/2</td><td>AVDD/2</td></tr>
<tr><td rowspan="2">Differential</td><td rowspan="2">AIN is input 1, REFTS and REFBS are shorted for input 2</td><td>1V</td><td>AVDD/2</td><td colspan="2">Short VREF and REFSENSE</td><td>AVDD/2</td><td>AVDD/2</td></tr>
<tr><td>2V</td><td>AVDD/2</td><td>AGND</td><td>Not Connection</td><td>AVDD/2</td><td>AVDD/2</td></tr>
<tr><td rowspan="2">External Reference</td><td rowspan="2">AIN</td><td rowspan="2">2V Max</td><td>AVDD</td><td rowspan="2">AVDD</td><td rowspan="2">Not Connection</td><td colspan="2">Span=REFTS-REFBS</td></tr>
<tr><td>AGND</td><td>Short to VREFTF</td><td>Short to VREFBF</td></tr>
<tr><td>AD876-8</td><td>AIN</td><td>2V</td><td>Floating or AVSS</td><td>AVDD</td><td>Not Connection</td><td>Short to VREFTF</td><td>Short to VREFBF</td></tr>
</table>

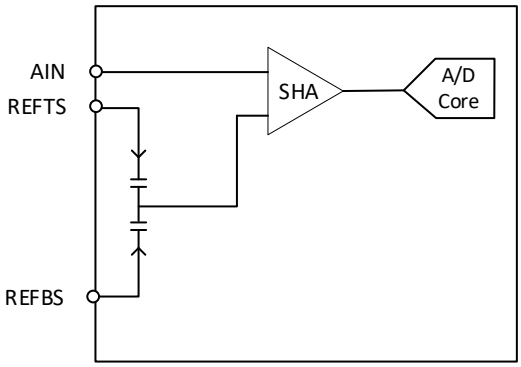


Figure 1. The MS9280 Equivalent Functional Input Circuit

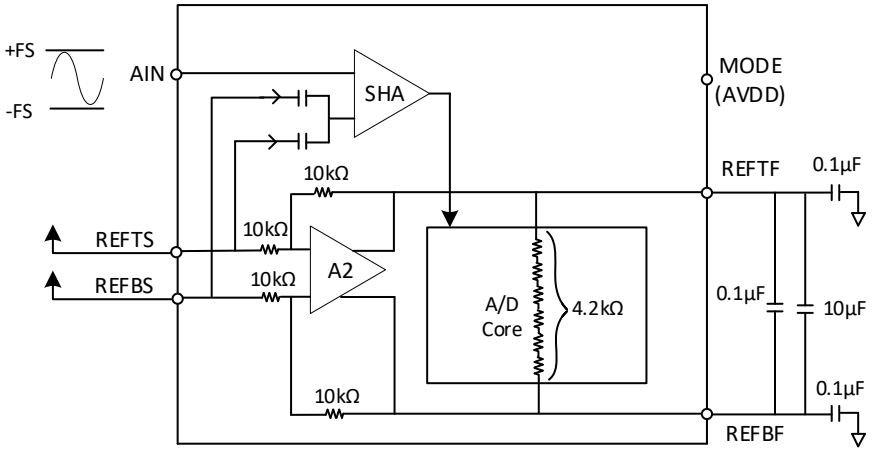


Figure 2a. Top/Bottom Mode

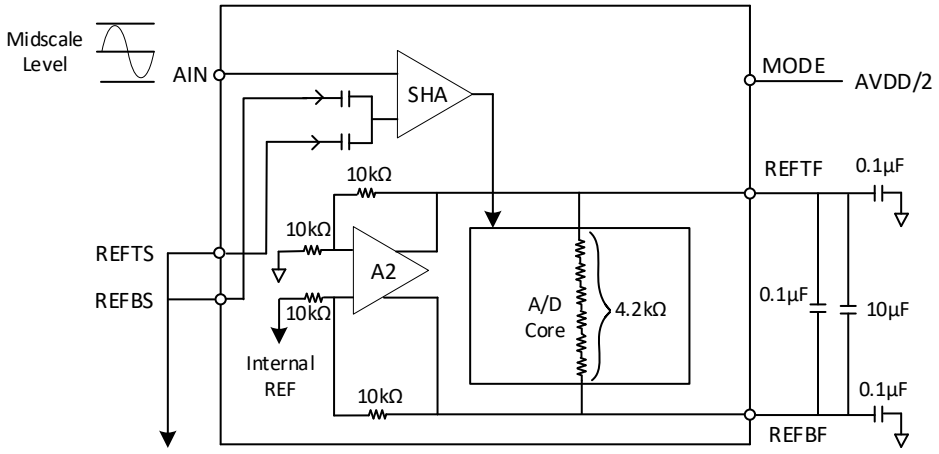


Figure 2b. Center Voltage Mode

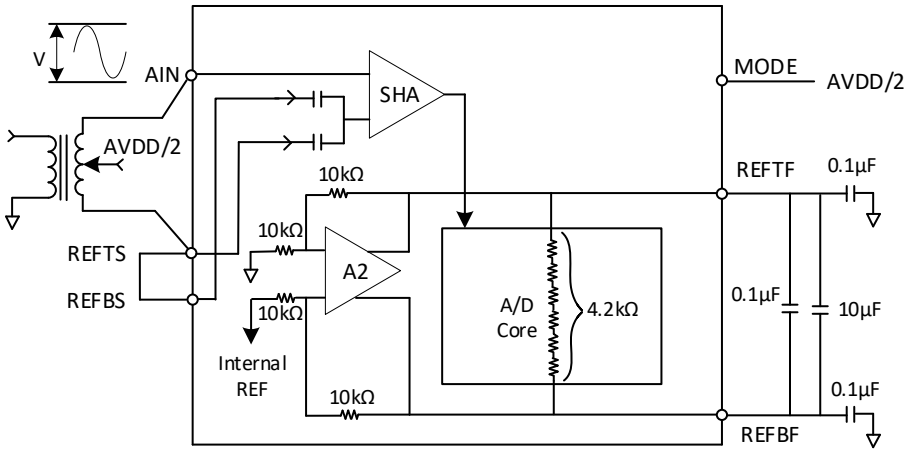


Figure 2c. Differential Mode

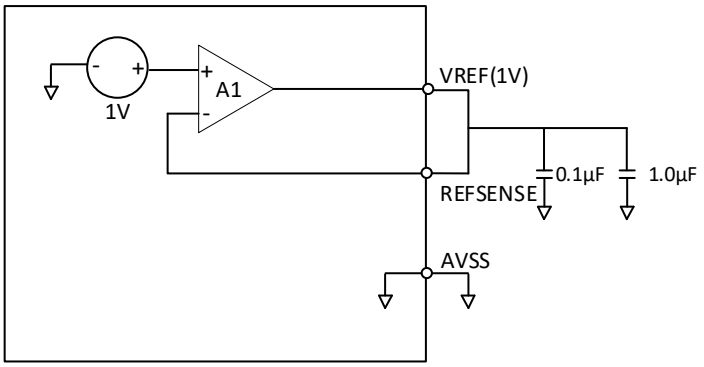


Figure 2d. 1V Reference Mode

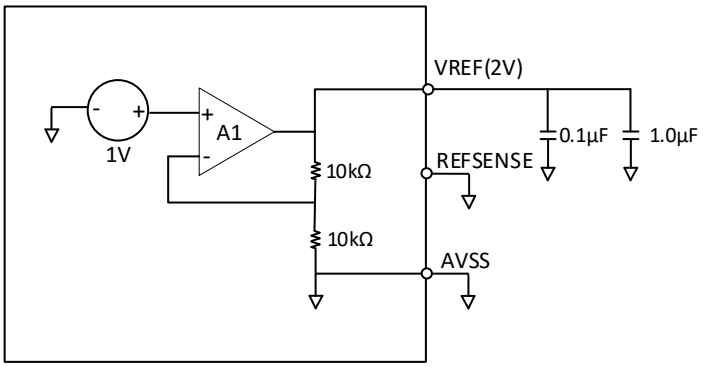


Figure 2e. 2V Reference Mode

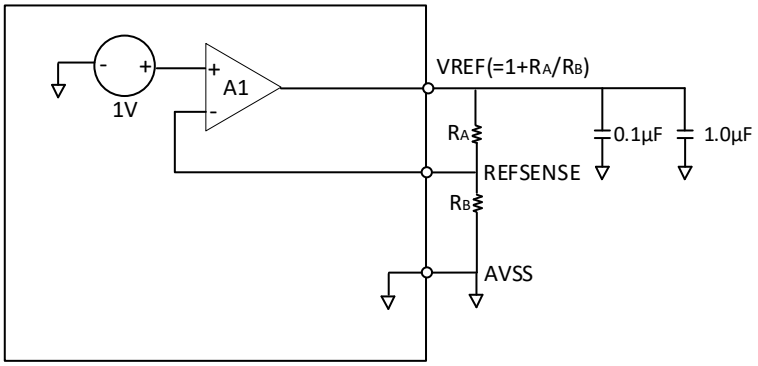


Figure 2f. Variable Reference Mode (between 1V and 2V)

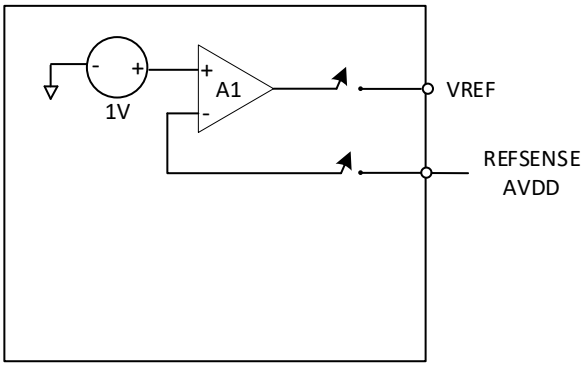


Figure 2g. Internal Reference Disable Mode

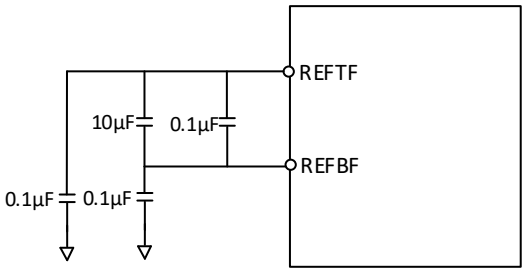


Figure 3. Reference Decoupling Network

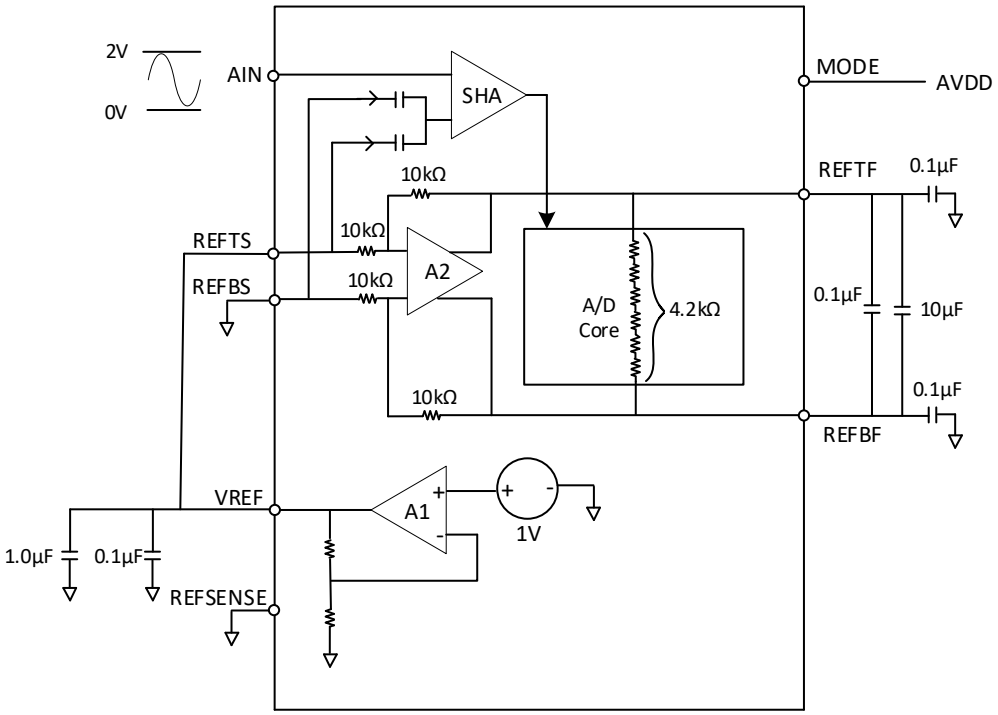


Figure 4. Internal Reference, 2V Input Range (Top/Bottom Mode)

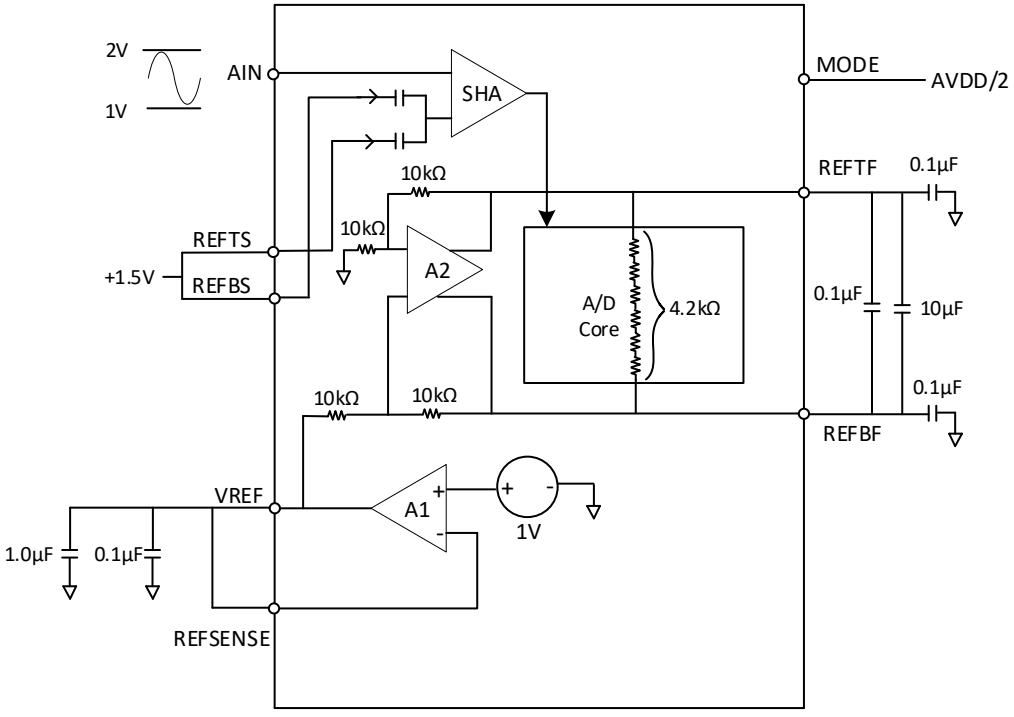


Figure 5. Internal Reference, 1V Input Range (Center Voltage Mode)

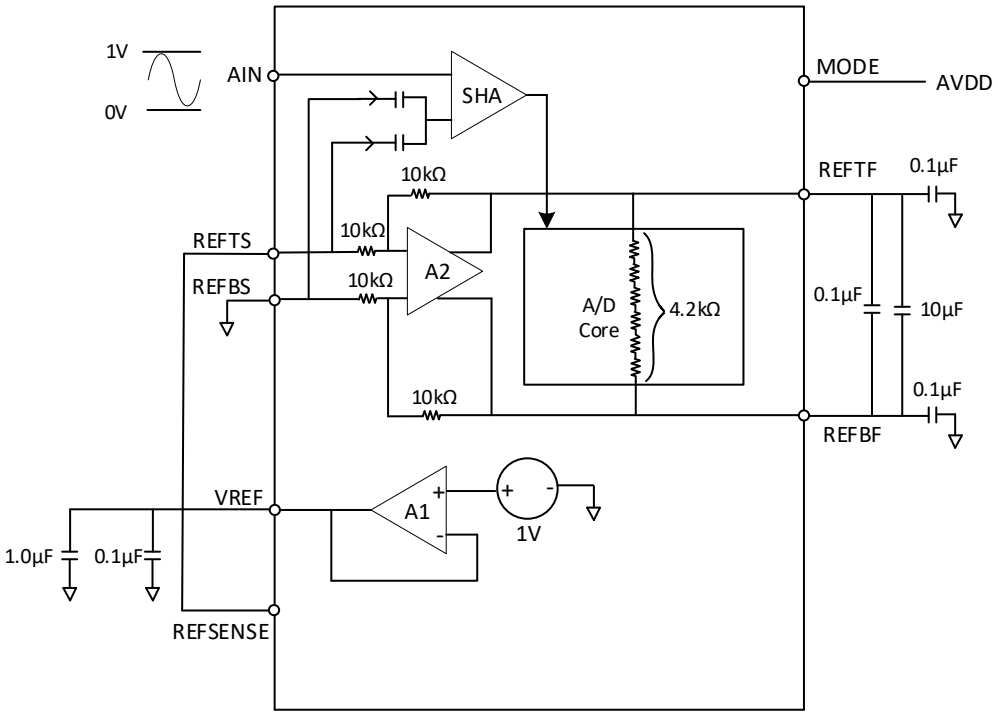


Figure 6. Internal Reference, 1V Input Range (Top/Bottom Mode)

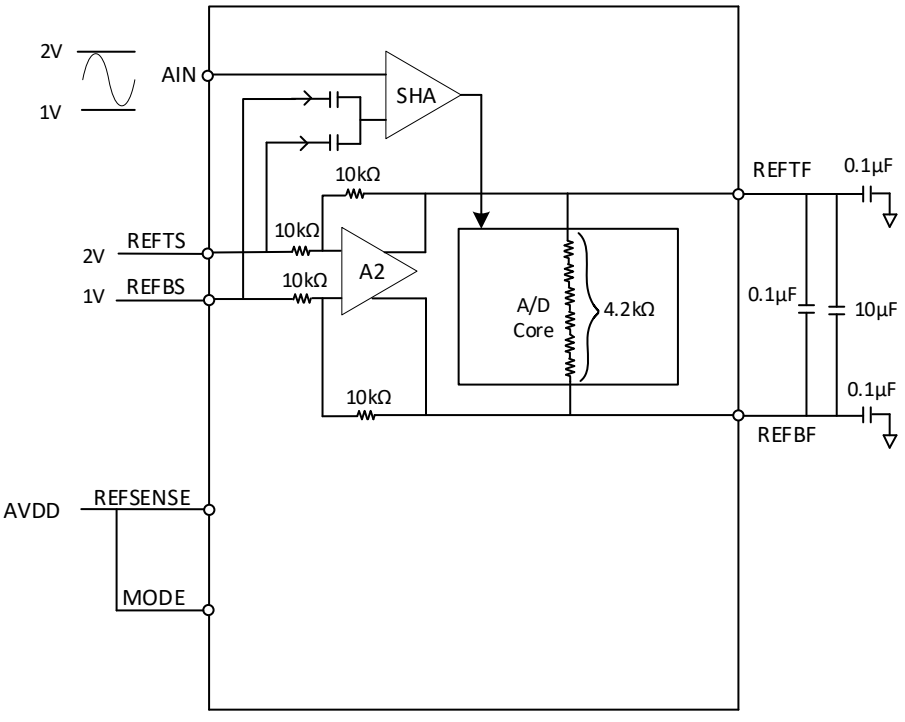


Figure 7. External Reference, 1V Input Range (Top/Bottom Mode)

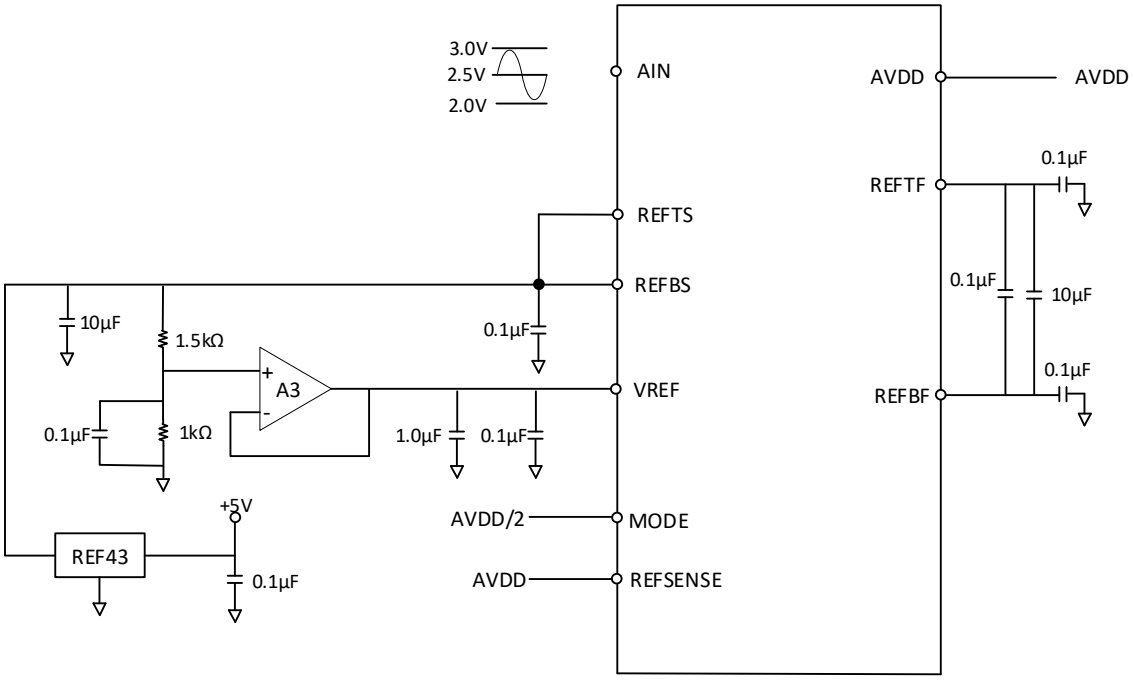


Figure 8. External Reference, 1V Input Range (Center Span Mode)

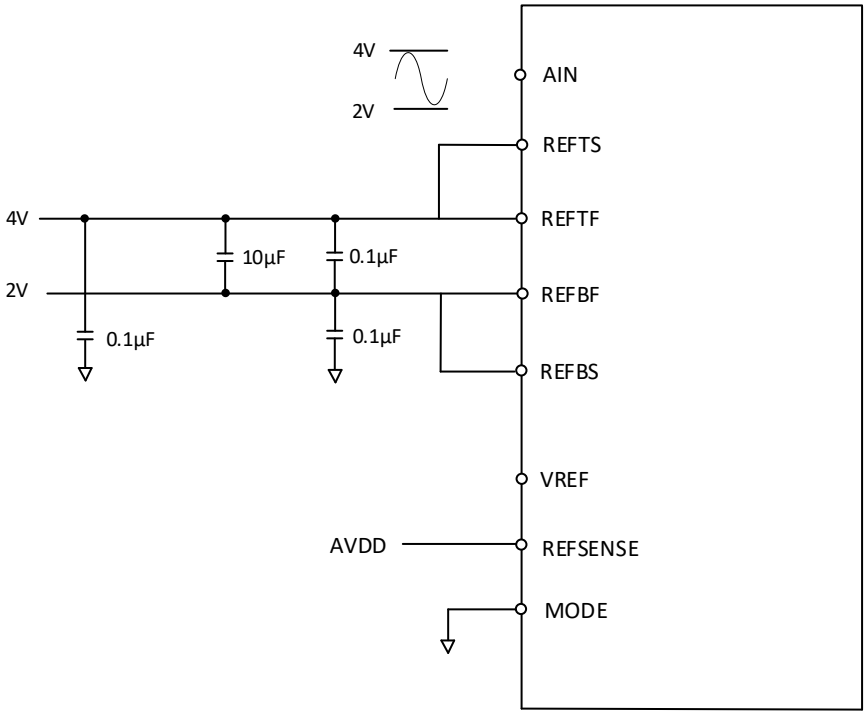


Figure 9a. External Reference, 2V Input Range (Top/Bottom Mode)

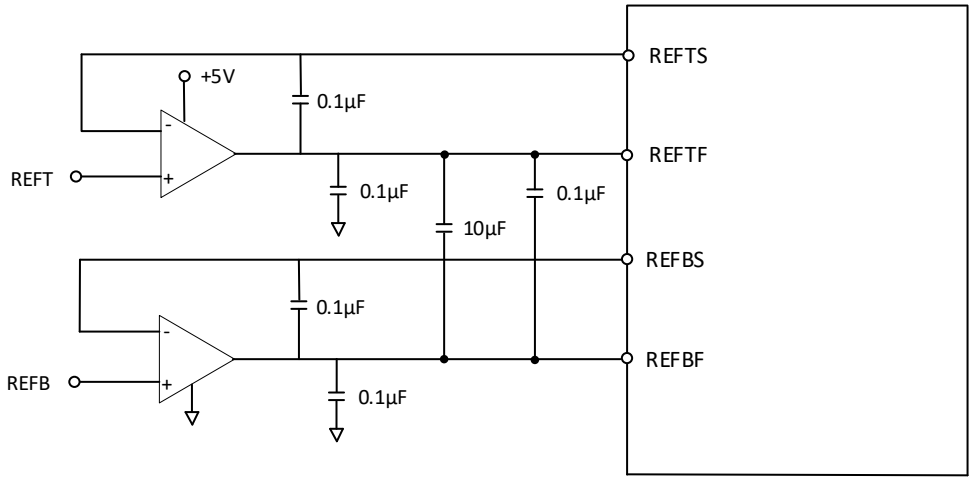


Figure 9b. Kelvin Connected External Reference Mode

Sleep Mode

The MS9280 can enter sleep mode by setting the STBY pin in logic high level and keeping the clock in low level. In this mode, the typical power dissipation is about 4mW. After STBY is low, the chip enters normal mode after 400ns.

Clamp Function

The MS9280 is integrated with clamp circuit to achieve AC-coupled input signal and video signal DC recovery internally. Figure 10 shows the internal clamp circuit and external control signals needed for clamp operation. In order to enable clamp, logic high-level is applied to the CLAMP pin, which will turn off SW1. The internal clamp amplifier operates in buffer mode. The DC voltage on the AIN pin is clamped to the voltage on CAMPLIN pin. After achieving expected clamp voltage, SW1 will be turned on because the CLAMP pin becomes low level. Ignoring the voltage change caused by input bias current, the input capacitor holds the clamped DC voltage until the next clamp interval arrives. To guarantee the closed-loop stability of the internal clamp amplifier, the recommended minimum input resistance is 10Ω.

The allowable voltage range of the CLAMPIN pin is decided by operation limits of internal clamp amplifier. And the recommended value between 0.5V and 2.5V.

The input capacitor depends on the sufficient capture time allowed by the input voltage AIN within the clamp interval and the minimum voltage drop between the clamp intervals. Specifically, the capture time when the switch is turned off is determined by the following formula:

$$t_{ACQ}=R_{IN}C_{IN}\ln\left(\frac{V_C}{V_E}\right)$$

Where, V_C is the voltage variation at both ends of capacitor. V_E is error voltage. V_C is the difference voltage between the initial DC input at the beginning of the clamp interval and the input clamp

voltage provided by the CLAMPIN pin. V_E is a system parameter, which is equal to the maximum allowable deviation of V_C. For example, 2V input level needs to be clamped at 1V DC level, the allowable deviation is 10mV, then V_C=1V, V_E=10mV. Once the suitable clamp level is obtained at the input, a very small voltage change is needed to ensure DC level deviation.

The voltage drop is calculated by the following formula:

$$dV=\frac{I_{BIAS}}{C_{IN}}(t)$$

Where, t is the clamp interval. Input bias current of the MS9280 is determined by sampling frequency Fs, reference center voltage (REFTS-REFBS)/2 and input voltage.

The voltage drop within the clamp interval is an important parameter. The minimum input capacitance is calculated based on needed voltage drop. Capture time - clamp pulse width is adjusted according to the selected minimum capacitance. In factual system, the trade-off is needed to be considered between capture time, clamp voltage drop and error voltage.

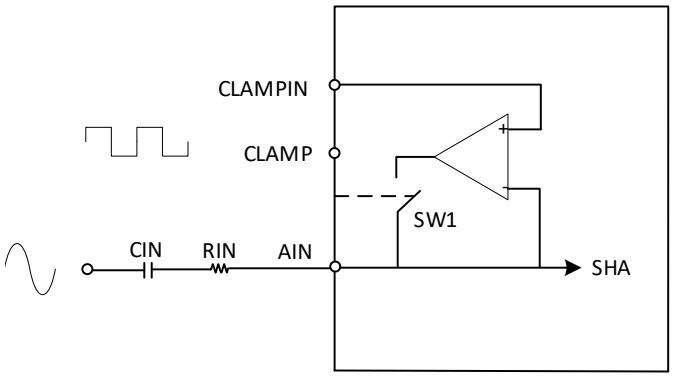


Figure 10a. Clamp Circuit

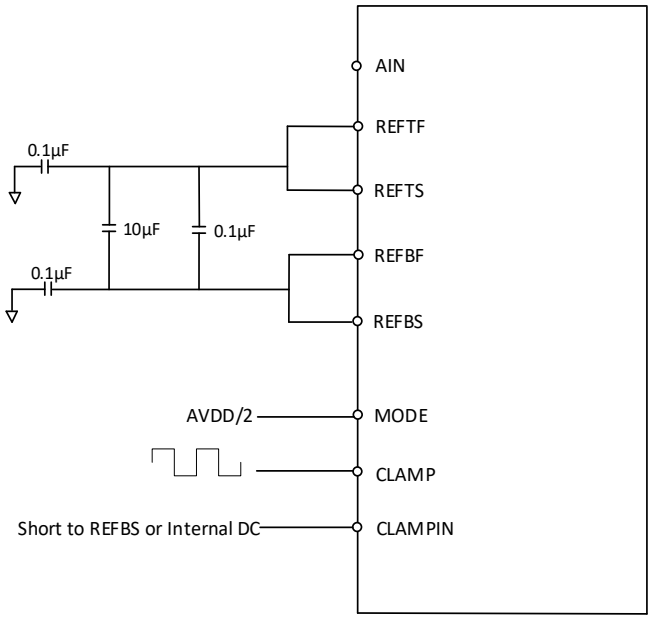


Figure 10b. Video Clamp Circuit

Driving Circuit of Analog Input

Figure 11 shows the equivalent analog input circuit. The MS9280 is integrated with a sample-and-hold amplifier internally. When the clock input is in low level, Switch 1, 2 are closed and Switch 3 is opened. Analog input signal charges the sampling capacitor CH. When the clock transits from low level to high level, Switch 1 and 2 are opened, placing the sample-and-hold amplifier in hold mode. Then Switch 3 is closed, the output of the amplifier is equal to the voltage stored on CH. When the clock transits from high level to low level, Switch 3 is opened first, then Switch 1 and 2 are closed, placing the sample-and-hold amplifier in track mode.

The structure of the sample-and-hold amplifier has requirements for the analog input driving ability. The pin capacitance CP and the hold capacitance CH are less than 5pF generally. The input signal source must be able to charge or discharge these capacitors to the voltage value required by 10bit accuracy in half of a clock cycle. When the sample-and-hold amplifier goes into track mode, the input signal source must charge or discharge capacitor CH from the stored voltage for last cycle to the new voltage. In the worst case, within half of clock cycle, the input signal provides the charging current. The on-resistance of the Switch 1 is the conversion of the maximum input signal peak of the sampling capacitor. This is equal to driving a low input impedance circuit. On the other hand, when the input signal source voltage is equal to the previously stored voltage, the hold capacitor requires no input current and the equivalent input impedance is extremely high.

Adding series resistor between the input signal source and the AIN pin can reduce the drive requirements of the signal source, as shown in figure 12. The bandwidth of the some particular applications limit the size of series resistor. The resistor should be limited to 20Ω or less to ensure the system characteristics. For the application with signal bandwidths less than the Nyquist rate, user can increase the resistance properly. Adding a shunt capacitor to ground can decrease the AC load impedance. The value of the capacitor depends on the source resistance and the required signal bandwidth.

The input range of the MS9280 is a function of the reference voltage. For the selection of input range, it is determined according to the different programming of the internal reference and external reference.

In many applications, especially for single power supply operation, AC coupling offers a convenient way of biasing the analog input signal at the proper signal range. Figure 13 shows a typical structure for AC-coupled analog input signal. The -3dB high-pass corner frequency is a very important consideration parameter. $f_{-3dB}=1/(2*pi*R2*C_{EQ})$, where C_{EQ} is the parallel combination of C1 and C2.

The choice of the resistor needs to be specially considered. The AC-coupled capacitor integrates the switch propagation characteristics, causing a net DC bias current to flow into the input. Bias current increases as the signal magnitude deviates from center reference voltage and sampling frequencies increase. When input signal is equal to reference center value, input bias current is lowest and offset error is generated $(R1+R2)*I_B$. If it is necessary to compensate this error, considering reducing R2 or adjusting VBIAS to meet the needed offset requirement.

DC coupling must be used in system application. Using operational amplifier to change the ground-referenced signal DC level to ensure that input signal is in the appropriate quantization range. Figure 14 shows an AD8041 circuit structure in non-inverting mode.

The MS9280 can adopt differential input signal mode. This structure can be achieved by shorting two inputs: REFTS and REFBS, as an differential input. Figure 15 shows the differential input mode of 1V P-P signal.

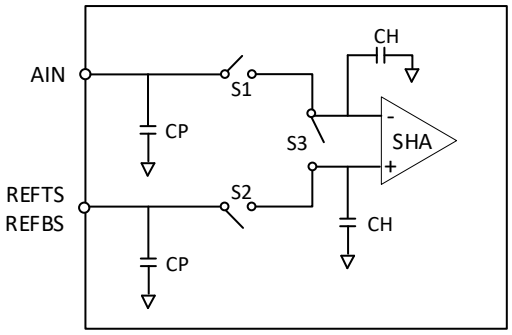


Figure 11. The MS9280 Equivalent Input Structure

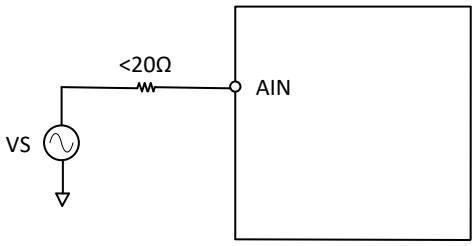


Figure 12. The MS9280 Simple Drive Circuit

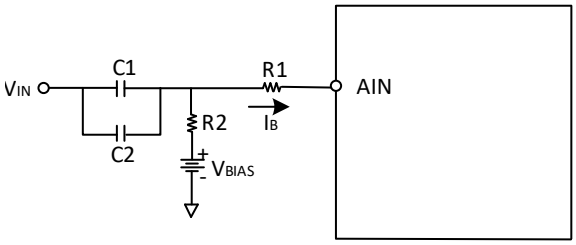


Figure 13. AC-Coupled Input

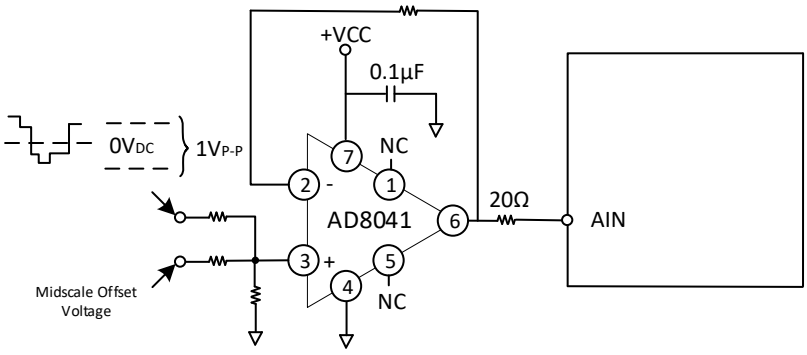


Figure 14. Bipolar Level Shift Structure

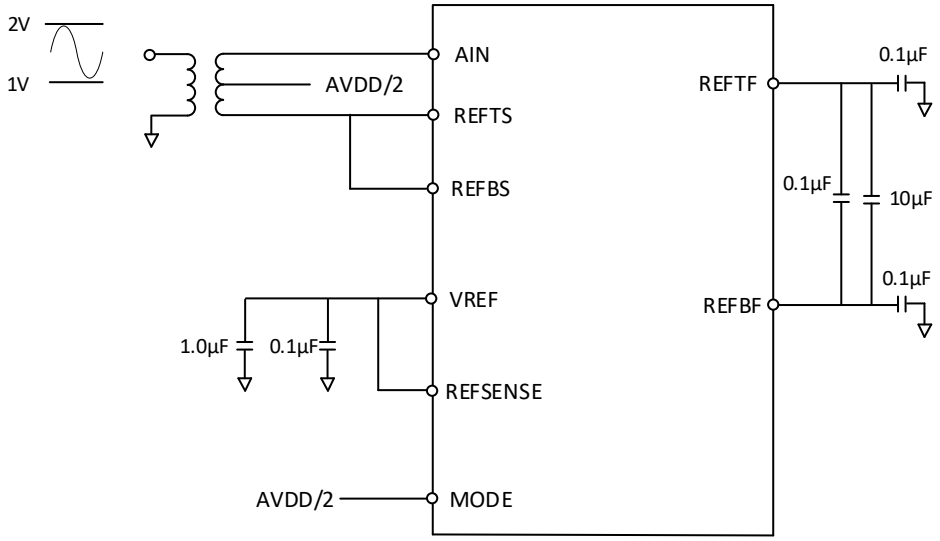


Figure 15. Differential Input Structure

Operating Mode of the AD876-8

The MS9280 can replace the AD876-8 series by pin configurations to reduce the system power dissipation using the AD876-8 originally. Figure 16 shows the pin configurations that the MS9280 replaces the AD876-8. By the REFSENSE pin grounding, the MODE pin floating and the CLAMP pin grounding, using external reference mode can replace the original AD876-8.

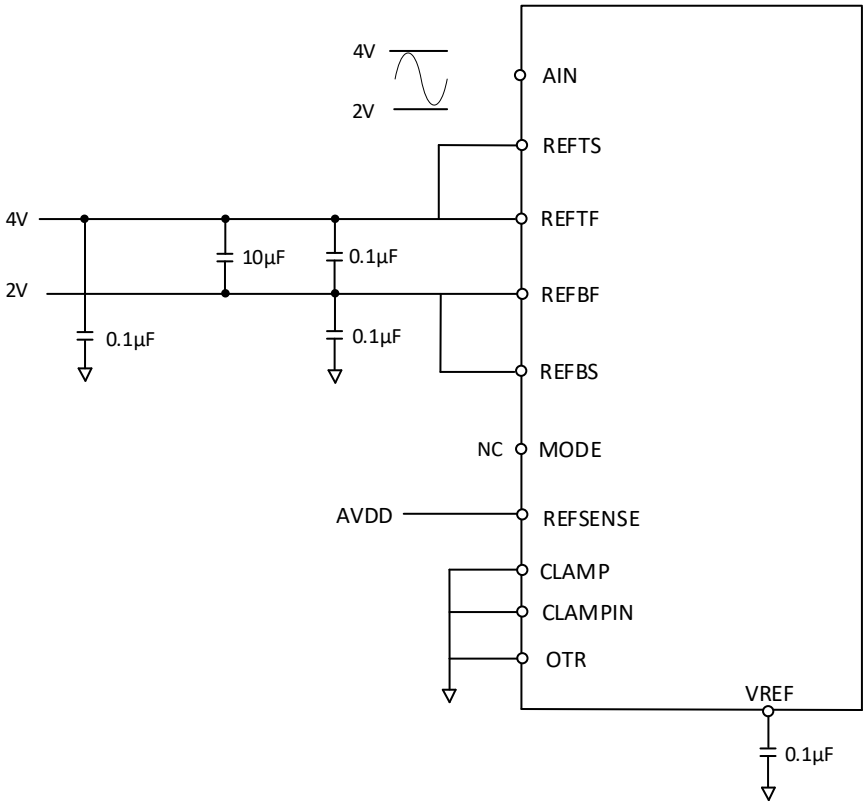


Figure 16. The AD876 Mode

Clock Input

The clock input of the MS9280 provides the circuit clock through internal inverting buffer. And the internal inverter is powered by the AVDD pin. This feature allows the clock to accommodate either +5V or +3.3V CMOS logic input signal and the input threshold voltage is AVDD/2.

The pipelined architecture of the MS9280 operates on both rising and falling edges of the clock. High-speed or advanced CMOS logic clock (HC/HCT, AC/ACT) is recommended for minimizing duty cycle variations. CMOS logic provides symmetrical voltage threshold levels and sufficient rising and falling times to support 35MSPS sampling operation. The highest clock frequency bit designed by the MS9280 is 35MHz. The higher clock frequency will weaken the system characteristics. Choosing the lower clock frequency can improve the system performance. The power dissipated by the output buffers is mainly proportional to clock frequency. The lower clock frequency can reduce power dissipation.

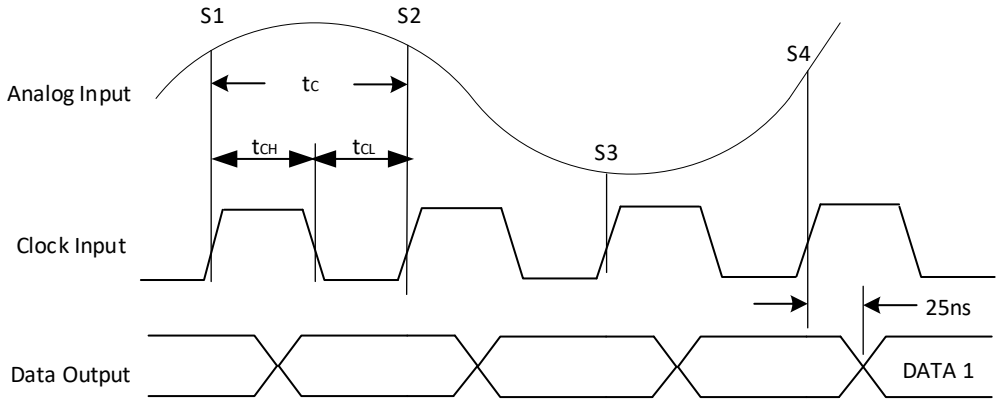


Figure 17. Timing Diagram

Digital Input and Output

Each of the MS9280 digital control inputs: THREE_STATE, STBY and CLK are all referenced to analog ground. The digital output is in straight binary format, as shown in Figure 18. When STBY is high and the CLK is disabled, the circuit is in low power dissipation mode and the static power dissipation drops to 5mW.

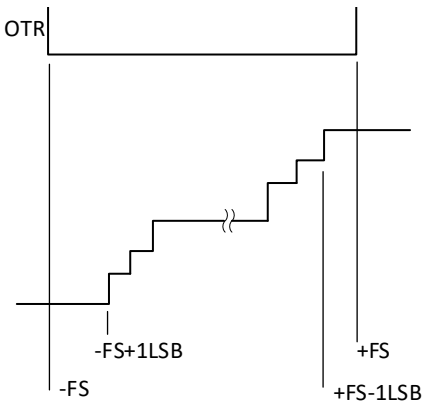


Figure 18. Data Output Format

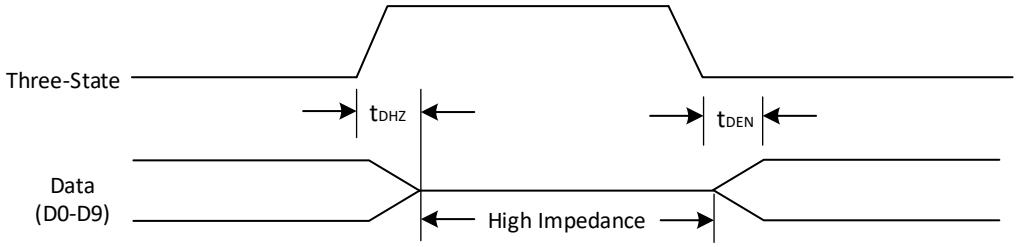
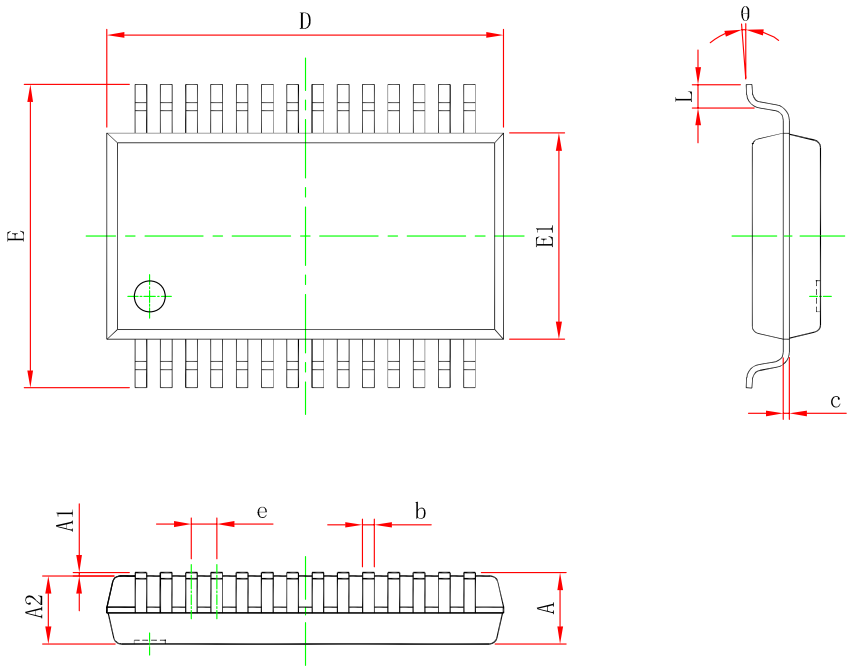


Figure 19. Three-State Timing Diagram

PACKAGE OUTLINE DIMENSIONS

SSOP28



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	-	2.000	-	0.079
A1	0.050	-	0.002	-
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	7.400	8.200	0.291	0.323
E1	5.000	5.600	0.197	0.220
e	0.650BSC		0.026BSC	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name: MS9280

Product Code: XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specification

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS9280	SSOP28	2000	1	2000	8	16000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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