- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 9.5 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Internal Look Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
 - **1000-V Charged-Device Model (C101)**

SN54LV163A . . . J OR W PACKAGE
SN74LV163A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{CLR}$	1	16	V_{CC}
CLK	2	15	RCO
A	3	14	Q_A
B	4	13	Q_B
C	5	12	Q_C
D	6	11	Q_D
ENP	7	10	ENT
GND	8	9	$\overline{LOAD}$
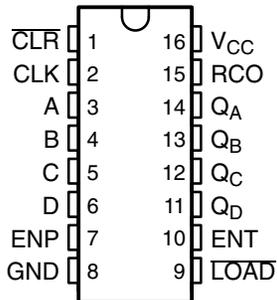
SN74LV163A . . . RGY PACKAGE
(TOP VIEW)

CLK	2	15	RCO
A	3	14	Q_A
B	4	13	Q_B
C	5	12	Q_C
D	6	11	Q_D
ENP	7	10	ENT

Top: $\overline{CLR}$ (1), V_{CC} (16)
Bottom: GND (8), $\overline{LOAD}$ (9)
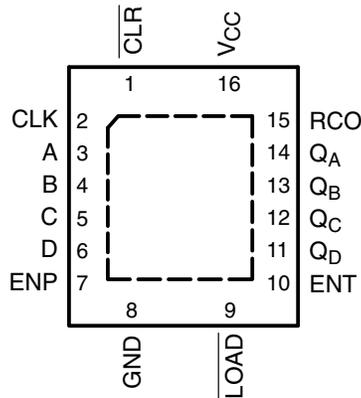
SN54LV163A . . . FK PACKAGE
(TOP VIEW)

Top: CLK, $\overline{CLR}$, NC, V_{CC}, RCO (3, 2, 1, 20, 19)

A	4	18	Q_A
B	5	17	Q_B
NC	6	16	NC
C	7	15	Q_C
D	8	14	Q_D

Bottom: ENP, GND, NC, $\overline{LOAD}$, ENT (9, 10, 11, 12, 13)
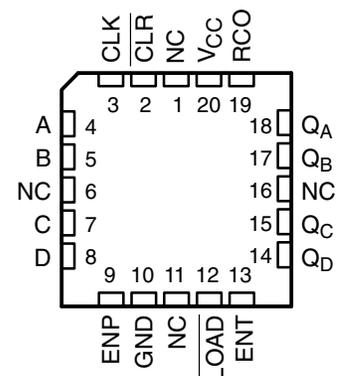
NC – No internal connection

description/ordering information

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN – RGY	Reel of 1000	SN74LV163ARGYR	LV163A
	SOIC – D	Tube of 40	SN74LV163AD	LV163A
		Reel of 2500	SN74LV163ADR	
	SOP – NS	Reel of 2000	SN74LV163ANSR	74LV163A
	SSOP – DB	Reel of 2000	SN74LV163ADBR	LV163A
	TSSOP – PW	Tube of 90	SN74LV163APW	LV163A
		Reel of 2000	SN74LV163APWR	
		Reel of 250	SN74LV163APWT	
	TVSOP – DGV	Reel of 2000	SN74LV163ADGVR	LV163A
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV163AJ	SNJ54LV163AJ
	CFP – W	Tube of 150	SNJ54LV163AW	SNJ54LV163AW
	LCCC – FK	Tube of 55	SNJ54LV163AFK	SNJ54LV163AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering information (continued)

The 'LV163A devices are 4-bit synchronous binary counters designed for 2-V to 5.5-V V_{CC} operation.

These synchronous, presettable counters feature an internal carry look ahead for application in high-speed counting designs. The 'LV163A devices are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the 'LV163A devices is synchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low after the next low-to-high transition of CLK, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily by decoding the Q outputs for the maximum count desired. The active-low output of the gate used for decoding is connected to $\overline{CLR}$ to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. ENP, ENT, and a ripple-carry output (RCO) are instrumental in accomplishing this function. Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

FUNCTION TABLE

| INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CLK	$\overline{QA}$	QB	QC	QD	
L	X	X	X	X	L	L	L	L	Reset to "0"
H	L	X	X		A	B	C	D	Preset data
H	H	X	L		No change				No count
H	H	L	X		No change				No count
H	H	H	H		Count up			Count
H	X	X	X		No change				No count

logic diagram (positive logic)
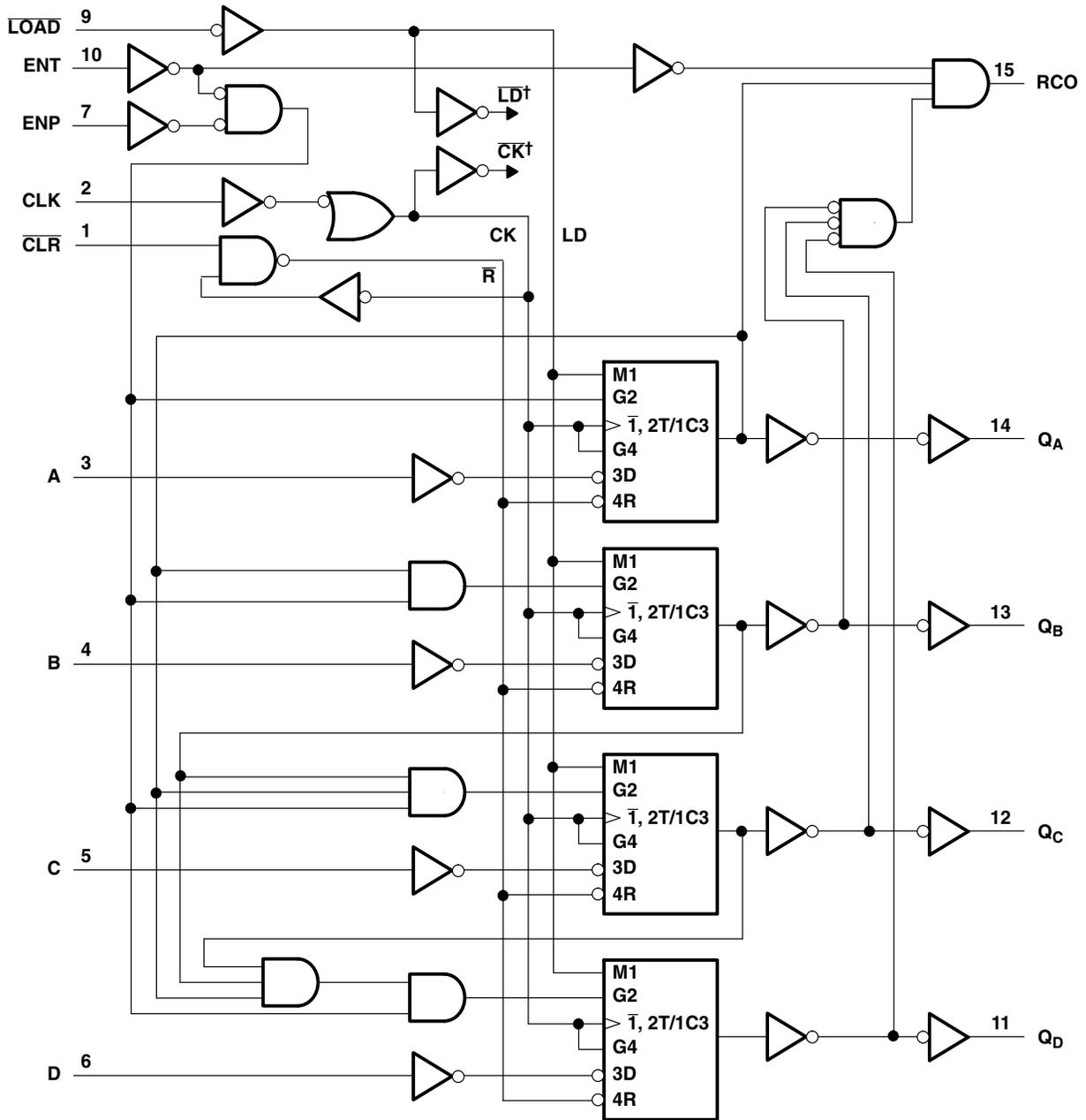
† For simplicity, routing of complementary signals $\overline{LD}$ and $\overline{CK}$ is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

logic diagram, each D/T flip-flop (positive logic)
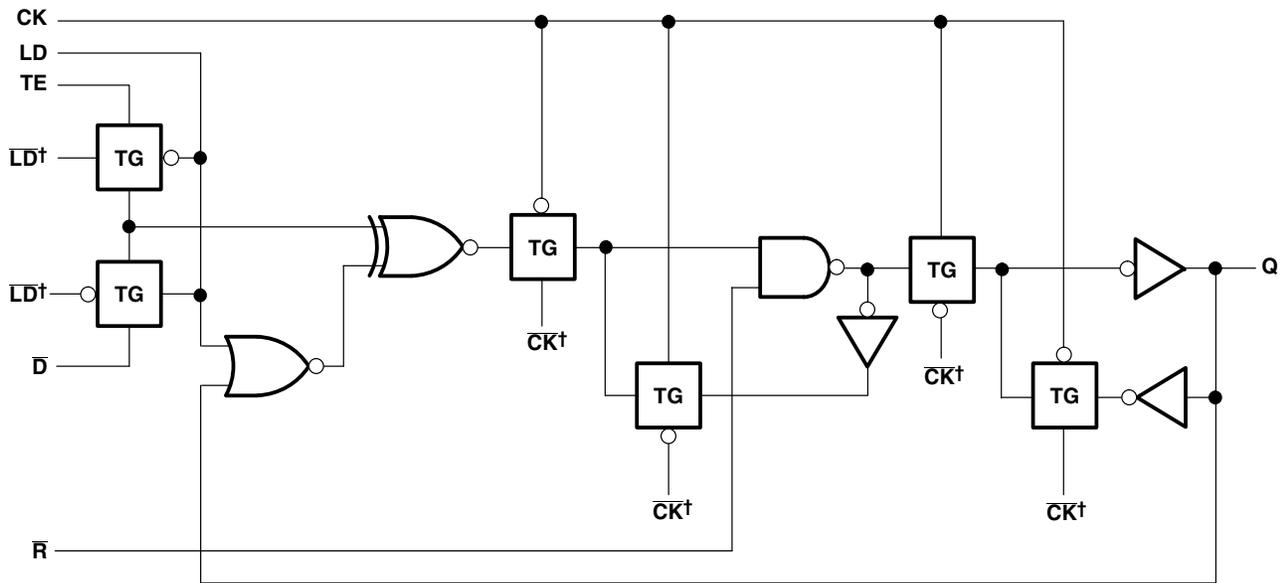
† The origins of $\overline{LD}$ and $\overline{CK}$ are shown in the overall logic diagram of the device.

typical clear, preset, count, and inhibit sequence

The following sequence is illustrated below:

1. Clear outputs to zero (synchronous)

2. Preset to binary 12

3. Count to 13, 14, 15, 0, 1, and 2

4. Inhibit
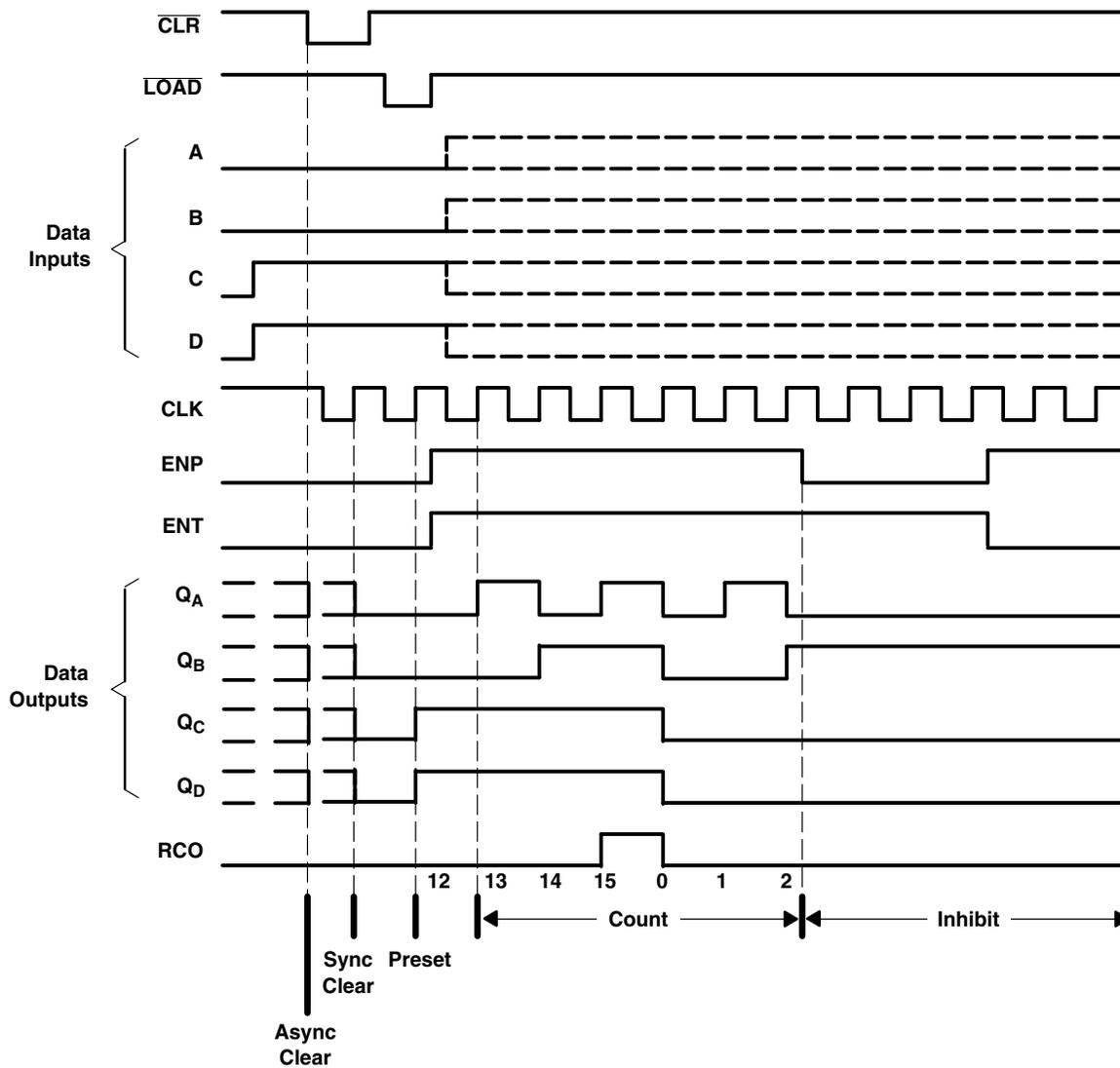
SN54LV163A, SN74LV163A
4-BIT SYNCHRONOUS BINARY COUNTERS

SCLS405F – APRIL 1998 – REVISED APRIL 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V

Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V

Output voltage range applied in high or low state, V_O (see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V

Voltage range applied to any output in the power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V

Input clamp current, I_{IK} (V_I < 0) . . . . –20 mA

Output clamp current, I_{OK} (V_O < 0) . . . . –50 mA

Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . $\pm$25 mA

Continuous current through V_{CC} or GND . . . . $\pm$50 mA

Package thermal impedance, θ_{JA} (see Note 3): D package . . . . 73°C/W

(see Note 3): DB package . . . . 82°C/W

(see Note 3): DGV package . . . . 120°C/W

(see Note 3): NS package . . . . 64°C/W

(see Note 3): PW package . . . . 108°C/W

(see Note 4): RGY package . . . . 39°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

TEXAS INSTRUMENTS

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recommended operating conditions (see Note 5)

			SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−6		−6	
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV163A			SN74LV163A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −6 mA	3 V	2.48			2.48			
	I_{OH} = −12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		1.8			1.8		pF

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SN54LV163A, SN74LV163A
4-BIT SYNCHRONOUS BINARY COUNTERS

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		7		7		7		ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$	6		6		6		ns
		Data (A, B, C, and D)	7.5		8.5		8.5		
		ENP, ENT	9.5		11		11		
		$\overline{LOAD}$ low	10		11.5		11.5		
t_h	Hold time, all synchronous inputs after CLK↑		1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		5		5		5		ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$	4		4		4		ns
		Data (A, B, C, and D)	5.5		6.5		6.5		
		ENP, ENT	7.5		9		9		
		$\overline{LOAD}$ low	8		9.5		9.5		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV163A		SN74LV163A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low		5		5		5		ns
t_{su}	Setup time before CLK↑	$\overline{CLR}$	3.5		3.5		3.5		ns
		Data (A, B, C, and D)	4.5		4.5		4.5		
		ENP, ENT	5		6		6		
		$\overline{LOAD}$ low	5		6		6		
t_h	Hold time, all synchronous inputs after CLK↑		1		1		1		ns

![Texas Instruments logo]

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50*	115*		40*		40		MHz
			C_L = 50 pF	30	90		25		25		
t_{pd}	CLK	Q	C_L = 15 pF		8.5*	16.2*	1*	19.5*	1	19.5	ns
		RCO (count mode)			9.1*	17*	1*	20.5*	1	20.5	
		RCO (preset mode)			12.1*	20.6*	1*	24.5*	1	24.5	
	ENT	RCO			8.7*	15.7*	1*	19*	1	19	
t_{pd}	CLK	Q	C_L = 50 pF		11	19.2	1	22.5	1	22.5	ns
		RCO (count mode)			11.9	20	1	23.5	1	23.5	
		RCO (preset mode)			14.6	23.6	1	27.5	1	27.5	
	ENT	RCO			11.7	18.7	1	22	1	22	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	80*	160*		70*		70		MHz
			C_L = 50 pF	55	125		50		50		
t_{pd}	CLK	Q	C_L = 15 pF		6.2*	12.8*	1*	15*	1	15	ns
		RCO (count mode)			6.8*	13.6*	1*	16*	1	16	
		RCO (preset mode)			8.8*	17.2*	1*	20*	1	20	
	ENT	RCO			6.5*	12.3*	1*	14.5*	1	14.5	
t_{pd}	CLK	Q	C_L = 50 pF		8	16.3	1	18.5	1	18.5	ns
		RCO (count mode)			8.8	17.1	1	19.5	1	19.5	
		RCO (preset mode)			10.7	20.7	1	23.5	1	23.5	
	ENT	RCO			8.2	15.8	1	18	1	18	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV163A		SN74LV163A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	135*	210*		115*		115		MHz
			C_L = 50 pF	95	160		85		85		
t_{pd}	CLK	Q	C_L = 15 pF		4.7*	8.1*	1*	9.5*	1	9.5	ns
		RCO (count mode)			5.2*	8.1*	1*	9.5*	1	9.5	
		RCO (preset mode)			6.4*	10.3*	1*	12*	1	12	
	ENT	RCO			4.9*	8.1*	1*	9.5*	1	9.5	
t_{pd}	CLK	Q	C_L = 50 pF		6.1	10.1	1	11.5	1	11.5	ns
		RCO (count mode)			6.6	10.1	1	11.5	1	11.5	
		RCO (preset mode)			7.8	12.3	1	14	1	14	
	ENT	RCO			6.3	10.1	1	11.5	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

PARAMETER		SN74LV163A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.2	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6:   Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	23.8	pF
			5 V	26	

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PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

From Output Under Test — Test Point

C_L (see Note A)

**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

From Output Under Test

$R_L = 1 \ k\Omega$ S1

C_L (see Note A)

○ V_{CC}
○ Open
○ GND

**LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \ \Omega$, $t_r ≤ 3$ ns, $t_f ≤ 3$ ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV163AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV163A	Samples
SN74LV163APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV163A	Samples
SN74LV163ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV163A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
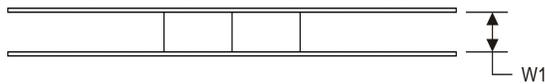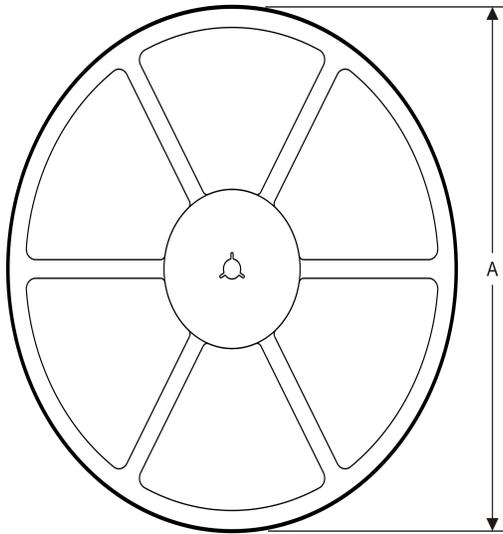
TAPE DIMENSIONS
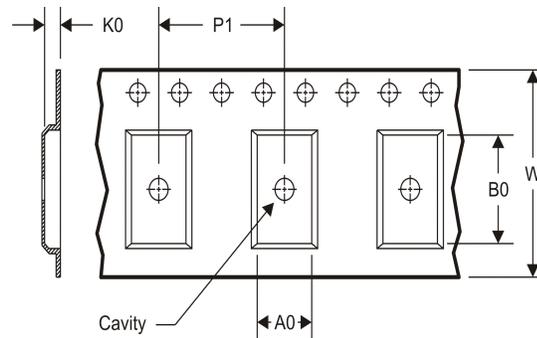
A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV163ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV163ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV163ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV163ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV163APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV163APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV163ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
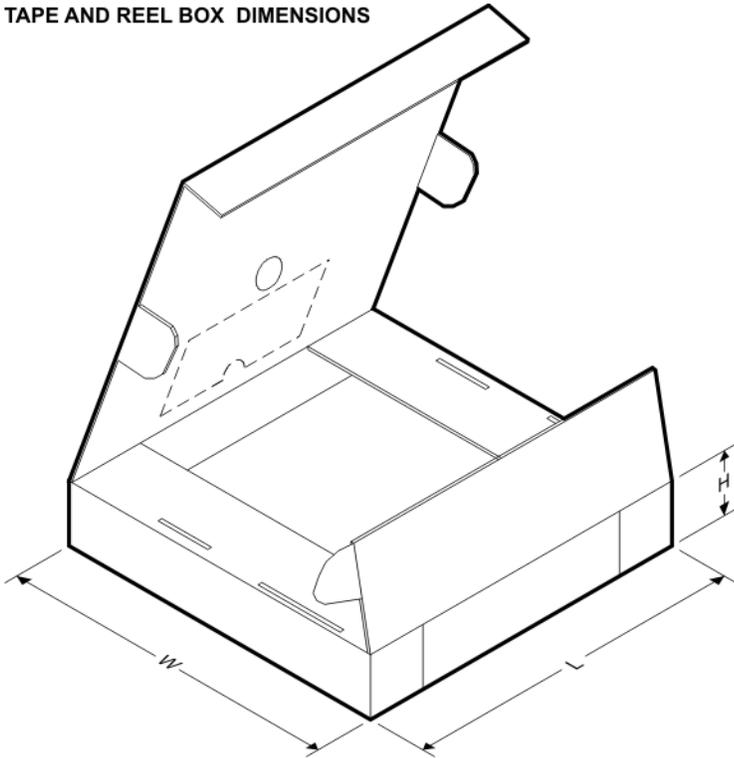
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV163ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV163ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV163ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV163ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV163APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV163APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV163ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN
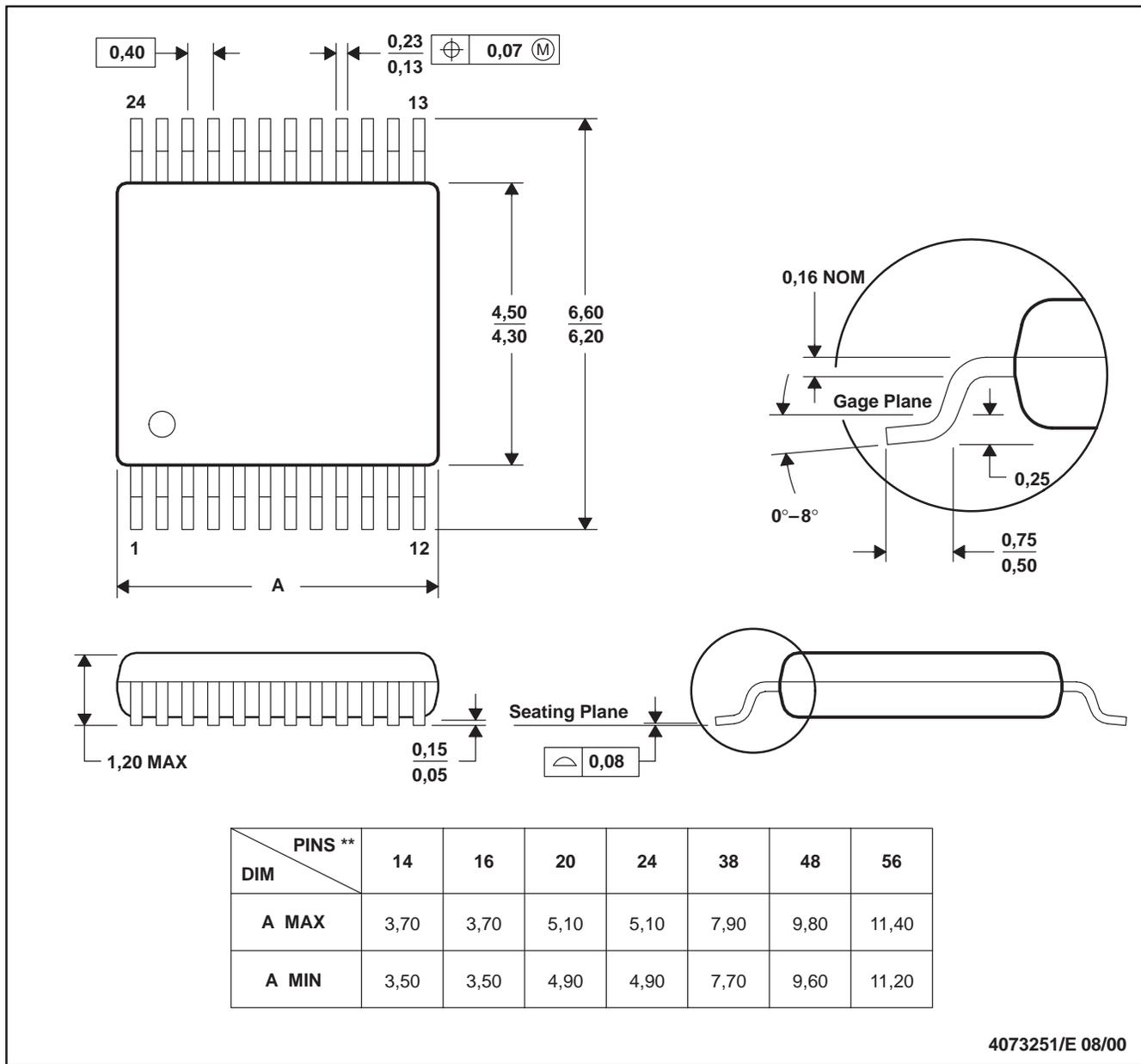
DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

$\triangle$D 4,50
                4,30

6,60
6,20

1   8

5,10
4,90

$\triangle$C

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10
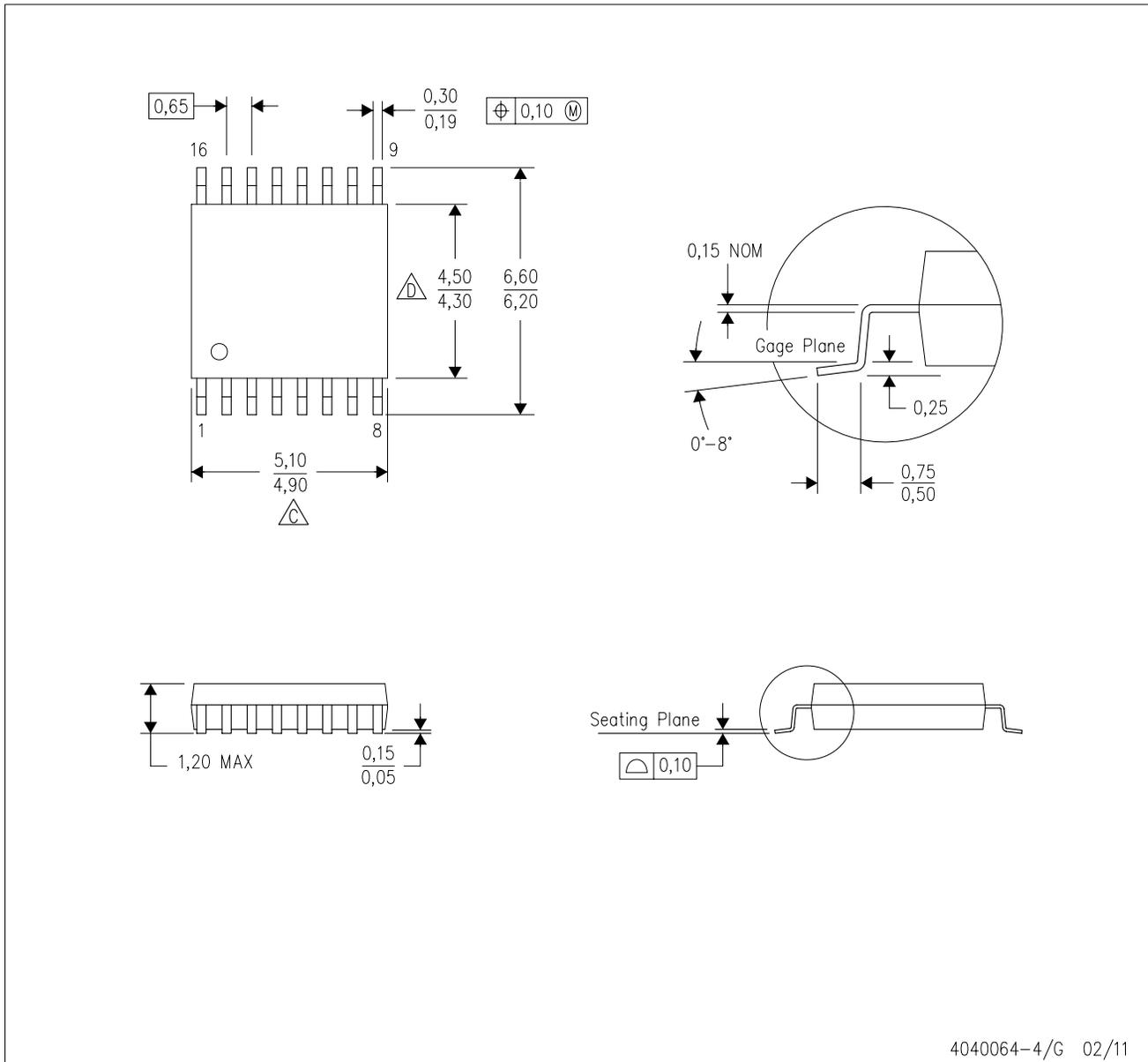
4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
          B.   This drawing is subject to change without notice.
         $\triangle$C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0,15 each side.
         $\triangle$D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
          E.   Falls within JEDEC MO−153

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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN
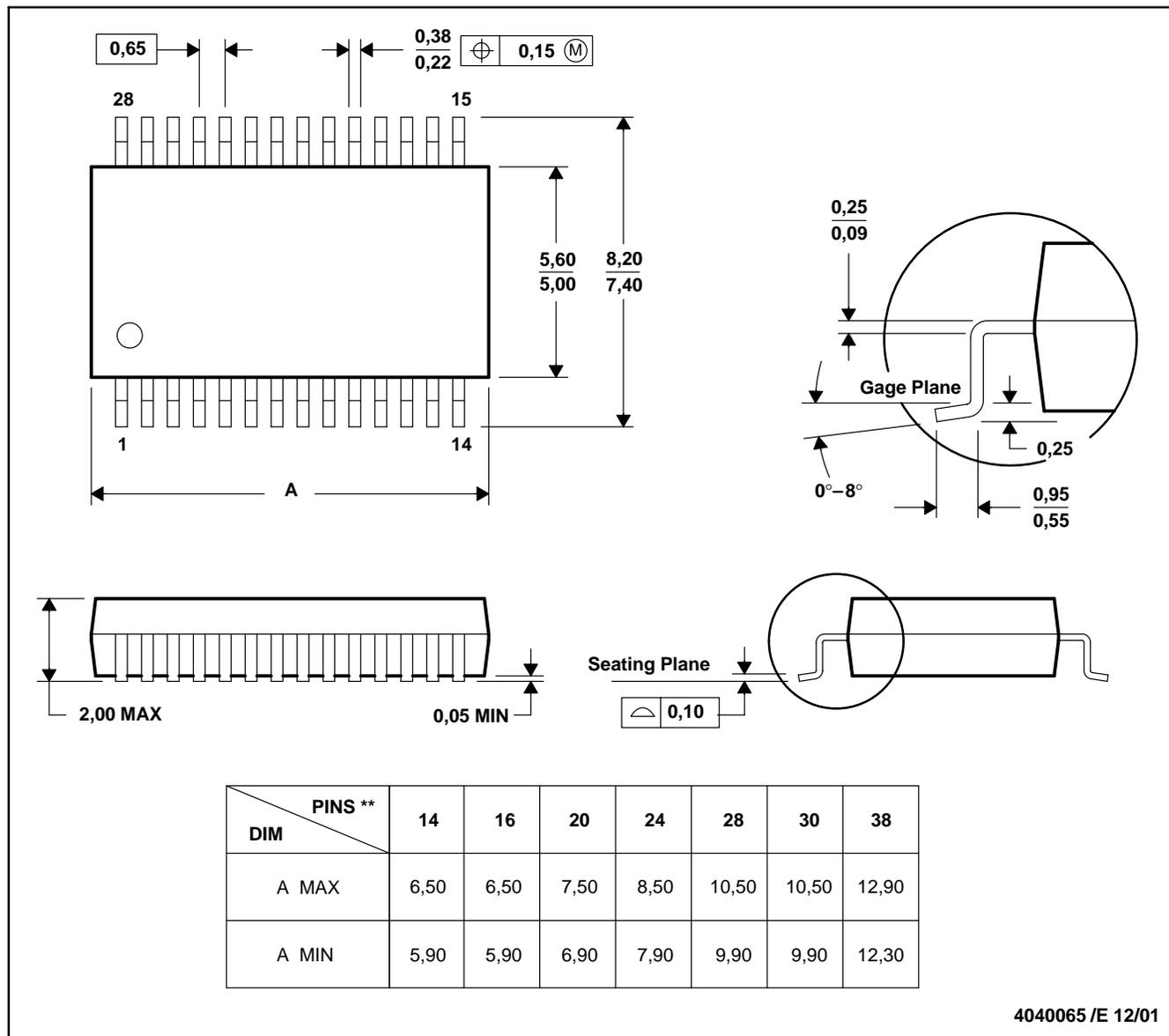
0,65

$\dfrac{0,38}{0,22}$ ⊕   0,15 Ⓜ

28   15

$\dfrac{5,60}{5,00}$ $\dfrac{8,20}{7,40}$

$\dfrac{0,25}{0,09}$

Gage Plane

0,25

0°−8°

$\dfrac{0,95}{0,55}$

1   14

A

2,00 MAX   0,05 MIN

Seating Plane

◁ 0,10

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD
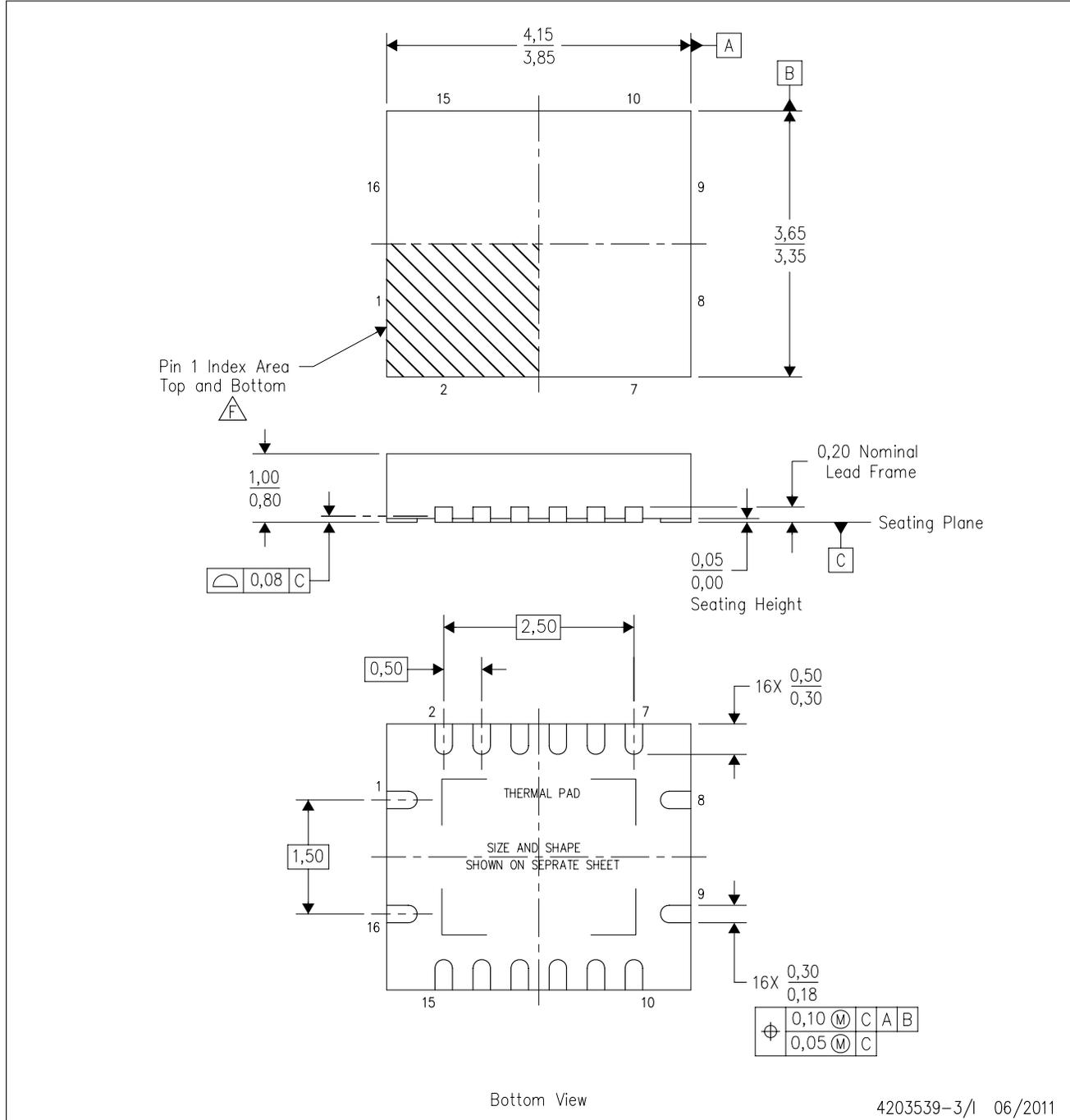
$\frac{4,15}{3,85}$ A

B

15   10

16   9

$\frac{3,65}{3,35}$

1   8

Pin 1 Index Area
Top and Bottom
F

2   7

0,20 Nominal
Lead Frame

$\frac{1,00}{0,80}$

Seating Plane

0,08 C

$\frac{0,05}{0,00}$
Seating Height

C

2,50

0,50

16X $\frac{0,50}{0,30}$

2   7

1   THERMAL PAD   8

1,50   SIZE AND SHAPE
SHOWN ON SEPRATE SHEET

16   9

15   10

16X $\frac{0,30}{0,18}$

⊕ | 0,10 Ⓜ | C | A | B
0,05 Ⓜ | C

Bottom View   4203539-3/I   06/2011

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M–1994.
         B.   This drawing is subject to change without notice.
         C.   QFN (Quad Flatpack No-Lead) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
              The Pin 1 identifiers are either a molded, marked, or metal feature.
         G.   Package complies to JEDEC MO–241 variation BA.

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RGY (R−PVQFN−N16)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
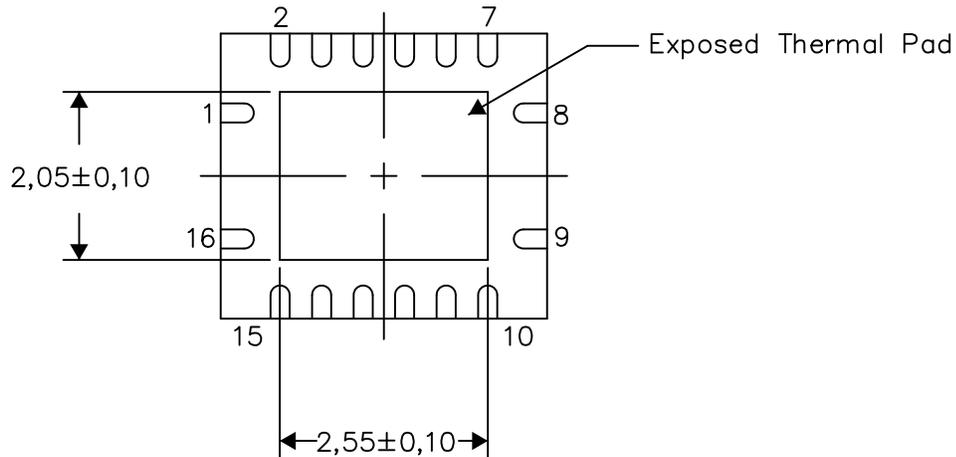
Bottom View

Exposed Thermal Pad Dimensions

4206353−3/P   03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)   PLASTIC QUAD FLATPACK NO-LEAD

Example Board Layout

4,80

Note D

4,30   2,60   2,55

1,50   2,05

0,85 X 16 PL.

0,28 X 16 PL.

10x0,50

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

4,75

4,25   2,65

1,50   0,82

1,07   0,30 x 2 PL

0,80 x 16 PL.

10x0,50   0,23 x 16 PL.

67% solder coverage by printed
area on center thermal pad

Non Solder Mask
Defined Pad

Example
Solder Mask Opening
(Note F)

0,08

R0,14   0,85

0,07   0,28

All Around

Example
Pad Geometry
(Note C)

Example Via Layout Design
may vary depending on constraints
(Note D, F)

1,00

1,00

6xØ0,3

4208122-3/P 03/14

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC-7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack
            QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.
            These documents are available at www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
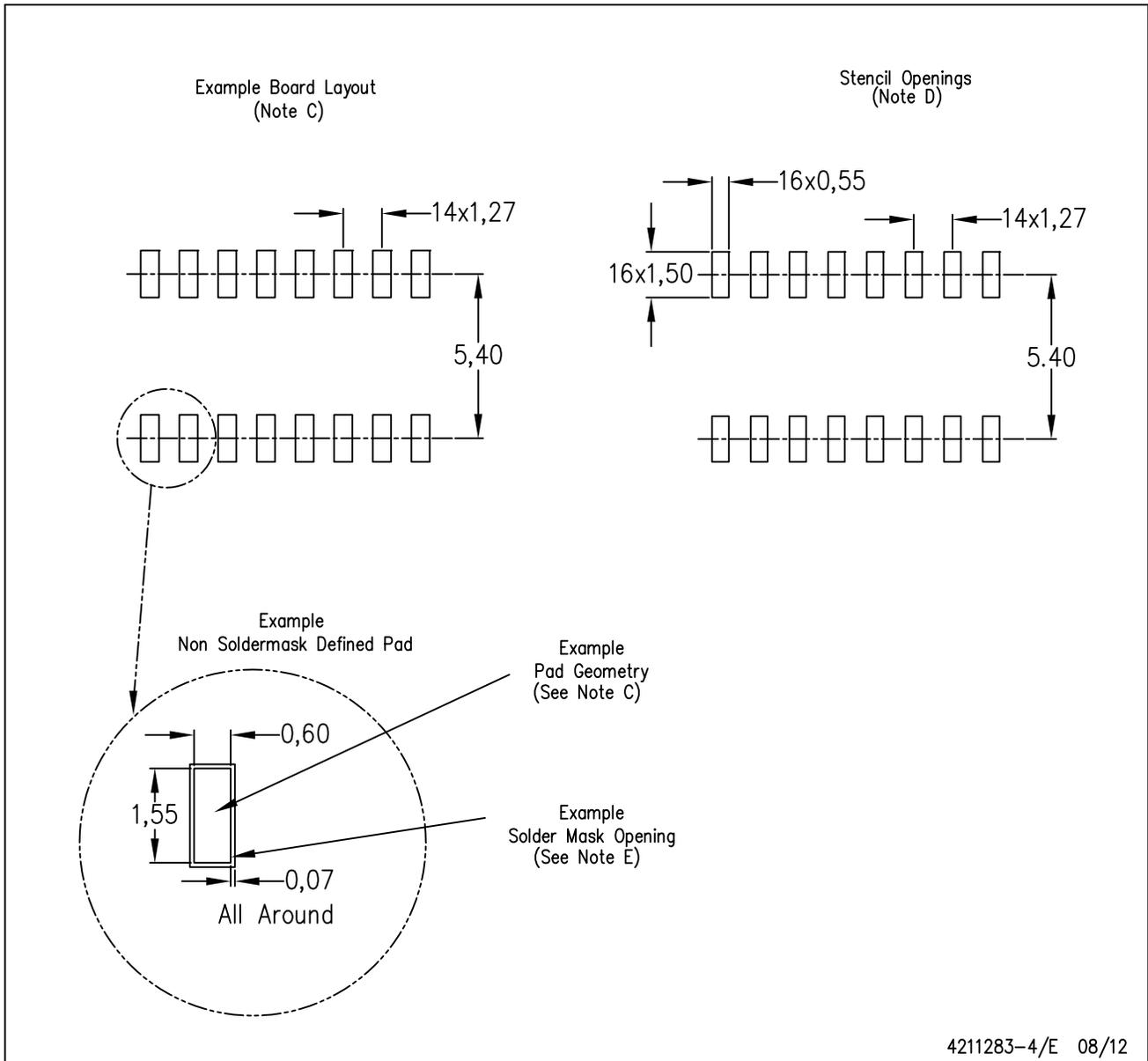
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D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

4040047-6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

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D (R-PDSO-G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

14x1,27

16x0,55

14x1,27

16x1,50

16x1,50

5,40

5.40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283-4/E   08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC-7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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MECHANICAL DATA

NS (R-PDSO-G)**
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE
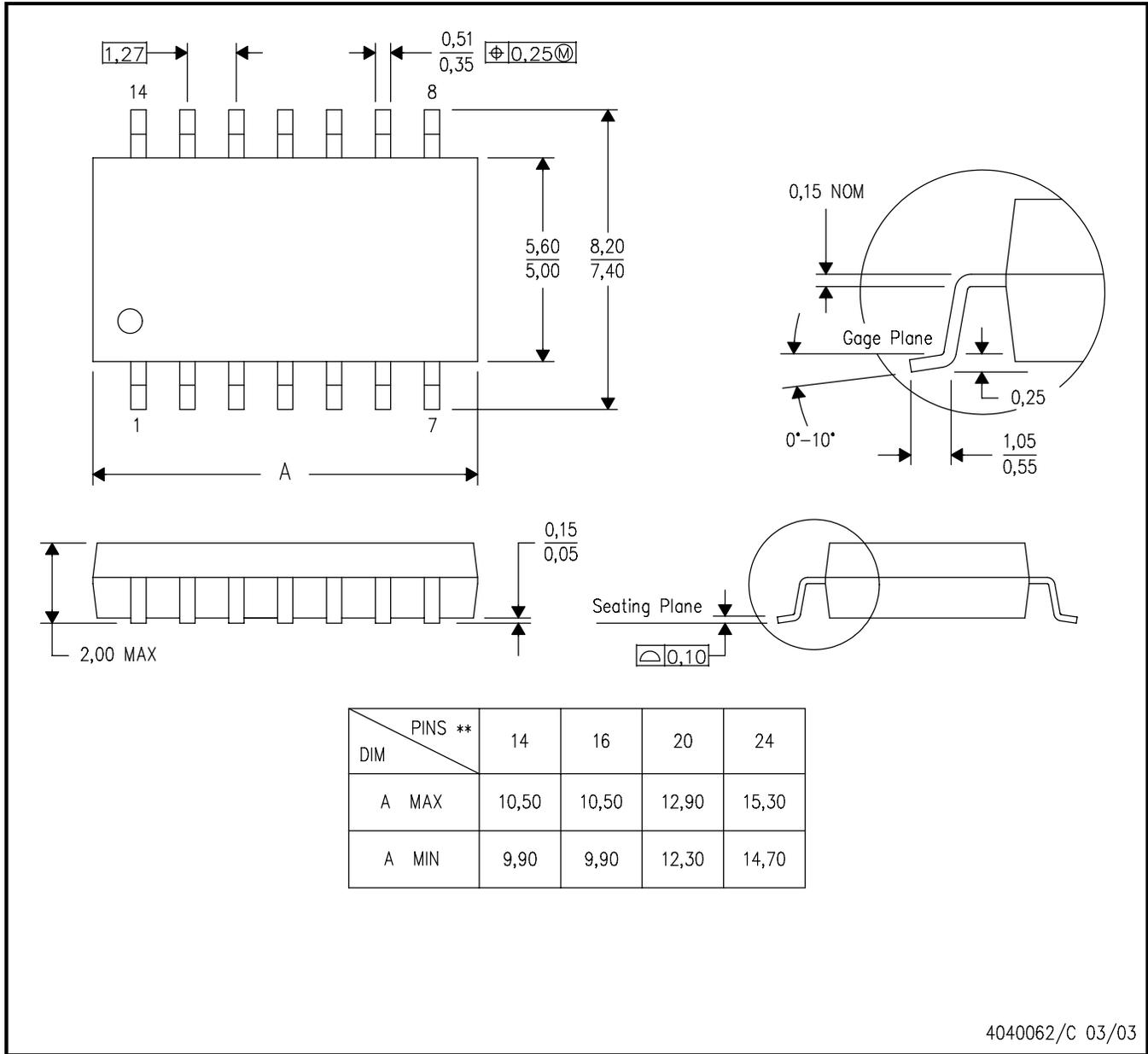
DIM	PINS **	14	16	20	24
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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