

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15\mathrm{V_{P-p}}$ can be achieved by digital signal amplitudes of $3-15\mathrm{V}$. For example, if $\mathrm{V_{DD}}=5\mathrm{V}$, $\mathrm{V_{SS}}=0\mathrm{V}$ and $\mathrm{V_{EE}}=-5\mathrm{V}$, analog signals from $-5\mathrm{V}$ to $+5\mathrm{V}$ can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $\mathrm{V_{DD}}-\mathrm{V_{SS}}$ and $\mathrm{V_{DD}}-\mathrm{V_{EE}}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs. A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and

an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

Features

- Wide range of digital and analog signal levels: digital 3-15V, analog to 15V_{p-p}
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD} V_{EE} = 15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at V_{DD}-V_{EE}=10V
- Logic level conversion for digital addressing signals of 3-15V (V_{DD}-V_{SS}=3-15V) to switch analog signals to 15 V_P-p (V_{DD}-V_{EE}=15V)
- \blacksquare Matched switch characteristics: $\Delta R_{ON}\!=\!5\Omega$ (typ.) for $V_{DD}\!-\!V_{EE}\!=\!15V$
- Very low quiescent power dissipation under all digitalcontrol input and supply conditions: 1 µW (typ.) at V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V
- Binary address decoding on chip

Connection Diagrams

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD}) -0.5 V_{DC} to $+18 \text{ V}_{DC}$ Input Voltage (V_{IN}) -0.5 V_{DC} to $\text{V}_{DD} + 0.5 \text{ V}_{DC}$ Storage Temperature Range (T_S) -65°C to $+150^{\circ}\text{C}$

Power Dissipation (P_D)

 Dual-In-Line
 700 mW

 Small Outline
 500 mW

 Lead Temp. (T_L) (soldering, 10 sec.)
 260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD}) $+5~\rm{V_{DC}~to}~+15~\rm{V_{DC}}$ Input Voltage (V_{IN}) $0V~\rm{to}~\rm{V_{DD}}~\rm{V_{DC}}$

Operating Temperature Range (T_A) 4051BM/4052BM/4053BM 4051BC/4052BC/4053BC

-55°C to +125°C -40°C to +85°C

DC Electrical Characteristics (Note 2)

| Symbol | Parameter | Con | ditions | −55°C | | + 25 ° | | | + 125°C | | Units |
|------------------|---|--|--|----------------|-------------------|----------------|-------|-------------------|----------------|-------------------|----------------|
| Syllibol | Parameter | Con | aitions | Min | Max | Min | Тур | Max | Min | Max | Ullits |
| I _{DD} | Quiescent Device Current | V _{DD} =5V V _{DD} =10V V _{DD} =15V | | | 5 10 20 | | | 5 10 20 | | 150 300 600 | μΑ μΑ μΑ |
| Signal In | puts (V _{IS}) and Outputs (V _C | os) | | | | | | | | | |
| R _{ON} | "ON" Resistance (Peak for V _{EE} ≤V _{IS} ≤V _{DD}) | $R_L = 10 \text{ k}\Omega$ (any channel selected) | $\begin{array}{l} V_{DD}\!=\!2.5V, \\ V_{EE}\!=\!-2.5V \\ \text{or } V_{DD}\!=\!5V, \\ V_{EE}\!=\!0V \end{array}$ | | 800 | | 270 | 1050 | | 1300 | Ω |
| | | | $\begin{array}{l} V_{DD}\!=\!5V \\ V_{EE}\!=\!-5V \\ \text{or } V_{DD}\!=\!10V, \\ V_{EE}\!=\!0V \end{array}$ | | 310 | | 120 | 400 | | 550 | Ω |
| | | | V_{DD} =7.5V, V_{EE} =-7.5V or V_{DD} =15V, V_{EE} =0V | | 200 | | 80 | 240 | | 320 | Ω |
| ΔR _{ON} | Δ"ON" Resistance Between Any Two Channels | $R_L = 10 \text{ k}\Omega$ (any channel selected) | $\begin{array}{l} V_{DD}\!=\!2.5V, \\ V_{EE}\!=\!-2.5V \\ \text{or } V_{DD}\!=\!5V, \\ V_{EE}\!=\!0V \end{array}$ | | | | 10 | | | | Ω |
| | | | $\label{eq:VDD} \begin{split} V_{DD}\!=\!5V, \\ V_{EE}\!=\!-5V \\ \text{or } V_{DD}\!=\!10V, \\ V_{EE}\!=\!0V \end{split}$ | | | | 10 | | | | Ω |
| | | | $\begin{array}{l} V_{DD}\!=\!7.5V, \\ V_{EE}\!=\!-7.5V \\ \text{or } V_{DD}\!=\!15V, \\ V_{EE}\!=\!0V \end{array}$ | | | | 5 | | | | Ω |
| | "OFF" Channel Leakage Current, any channel "OFF" | $V_{DD} = 7.5V,$ $O/I = \pm 7.5V, I.$ | $V_{EE} = -7.5V$ O = 0V | | ±50 | | ±0.01 | ±50 | | ±500 | nA |
| | "OFF" Channel Leakage | Inhibit = 7.5V | CD4051 | | ±200 | | ±0.08 | ±200 | | ±2000 | nA |
| | Current, all channels "OFF" (Common OUT/IN) | $V_{DD} = 7.5V,$ $V_{EE} = -7.5V,$ O/I = 0V, | CD4052 | | ±200 | | ±0.04 | ±200 | | ±2000 | nA |
| | | I/O= ±7.5V | CD4053 | | ±200 | | ±0.02 | ±200 | | ±2000 | nA |
| | Inputs A, B, C and Inhibit | | | I | | | | | | | |
| V _{IL} | Low Level Input Voltage | $\begin{aligned} &V_{EE}\!=\!V_{SS}R_L\!=\!\\ &I_{IS}\!<\!2\mu\text{A on al}\\ &V_{IS}\!=\!V_{DD}\text{thru}\\ &V_{DD}\!=\!5V\\ &V_{DD}\!=\!10V\\ &V_{DD}\!=\!15V \end{aligned}$ | OFF channels | | 1.5 3.0 4.0 | | | 1.5 3.0 4.0 | | 1.5 3.0 4.0 | > > > |
| V _{IH} | High Level Input Voltage | V _{DD} =5 V _{DD} =10 V _{DD} =15 | | 3.5 7 11 | | 3.5 7 11 | | | 3.5 7 11 | | V V V |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

| Symbol | Parameter | Conditions | | -40°C | | + 25°C | | | +85°C | | Units |
|------------------|--|---|---|----------------|-------------------|----------------|-------------------|-------------------|----------------|-------------------|----------------|
| Symbol | raiametei | 001 | iditions | Min | Max | Min | Тур | Max | Min | Max | Oille |
| I _{IN} | Input Current | V _{DD} =15V, V _{IN} =0V V _{DD} =15V, | V _{EE} =0V V _{EE} =0V | | -0.1 | | -10-5 | -0.1 | | -1.0 | μA |
| | | V _{IN} =15V | | | 0.1 | | 10-5 | 0.1 | | 1.0 | μΑ |
| I _{DD} | Quiescent Device Current | $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$ | | | 20 40 80 | | | 20 40 80 | | 150 300 600 | μΑ μΑ μΑ |
| Signal In | puts (V _{IS}) and Outputs (V _{OS} |) | | | | | | | | | |
| R _{ON} | "ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$) | $R_L = 10 \text{ k}\Omega$ (any channel selected) | $V_{DD} = 2.5V,$ $V_{EE} = -2.5V$ or $V_{DD} = 5V,$ $V_{EE} = 0V$ | | 850 | | 270 | 1050 | | 1200 | Ω |
| | | | $\begin{aligned} &V_{DD}\!=\!5V,\\ &V_{EE}\!=\!-5V\\ &\text{or }V_{DD}\!=\!10V,\\ &V_{EE}\!=\!0V \end{aligned}$ | | 330 | | 120 | 400 | | 520 | Ω |
| | | | $\begin{aligned} &V_{DD}\!=\!7.5\text{V},\\ &V_{EE}\!=\!-7.5\text{V}\\ &\text{or }V_{DD}\!=\!15\text{V},\\ &V_{EE}\!=\!0\text{V} \end{aligned}$ | | 210 | | 80 | 240 | | 300 | Ω |
| ΔR _{ON} | Δ"ON" Resistance Between Any Two Channels | $R_L = 10 \text{ k}\Omega$ (any channel selected) | $V_{DD} = 2.5V, \ V_{EE} = -2.5V \ or V_{DD} = 5V, \ V_{EE} = 0V$ | | | | 10 | | | | Ω |
| | | | $V_{DD} = 5V$ $V_{EE} = -5V$ or $V_{DD} = 10V$, $V_{EE} = 0V$ | | | | 10 | | | | Ω |
| | | | $V_{DD} = 7.5V, \ V_{EE} = -7.5V \ or V_{DD} = 15V, \ V_{EE} = 0V$ | | | | 5 | | | | Ω |
| | "OFF" Channel Leakage Current, any channel "OFF" | $V_{DD} = 7.5V$, $O/I = \pm 7.5V$, I | $V_{EE} = -7.5V$ /O=0V | | ±50 | | ±0.01 | ±50 | | ±500 | nA |
| | "OFF" Channel Leakage Current, all channels | Inhibit = 7.5V V _{DD} = 7.5V, | CD4051 | | ±200 | | ±0.08 | ±200 | | ±2000 | nA |
| | "OFF" (Common OUT/IN) | $V_{EE} = -7.5V,$ O/I=0V | | | ±200 | | ±0.04 | ±200 | | ±2000 | nA |
| Comtral | Innuita A. D. C. and Inhihit | $I/O = \pm 7.5V$ | CD4053 | | ±200 | | ±0.02 | ±200 | | ±2000 | nA |
| V _{IL} | Inputs A, B, C and Inhibit Low Level Input Voltage | V _{EE} =V _{SS} R _L | = 1 kO to Voo | T | | | | | | | |
| VIL | Low Level input voltage | | II OFF Channels | | 1.5 3.0 4.0 | | | 1.5 3.0 4.0 | | 1.5 3.0 4.0 | V V |
| V _{IH} | High Level Input Voltage | $V_{DD} = 5$ $V_{DD} = 10$ $V_{DD} = 15$ | | 3.5 7 11 | | 3.5 7 11 | | | 3.5 7 11 | | V V V |
| I _{IN} | Input Current | V _{DD} =15V, V _{IN} =0V V _{DD} =15V, | V _{EE} =0V V _{EE} =0V | | -0.1 0.1 | | -10 ⁻⁵ | -0.1 0.1 | | -1.0 1.0 | μA μA |

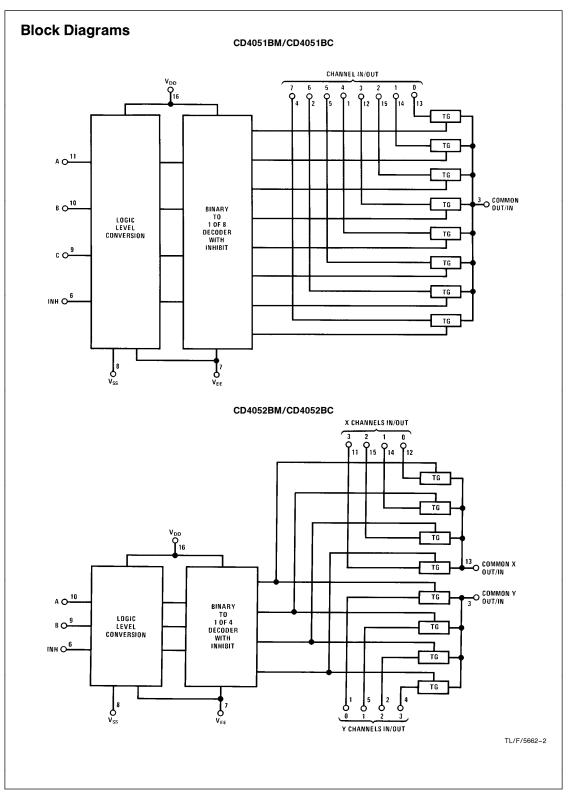
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

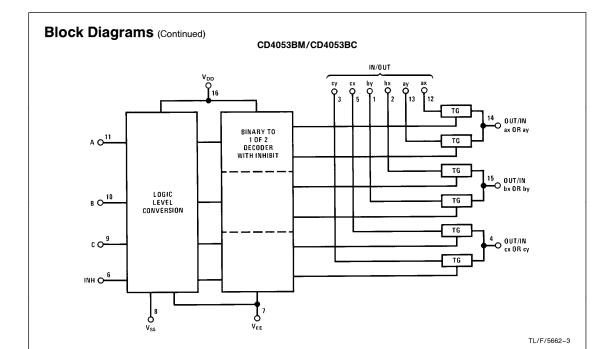
Note 2: All voltages measured with respect to $\ensuremath{V_{SS}}$ unless otherwise specified.

| Symbol | Parameter | Conditions | V _{DD} | Min | Тур | Max | Units |
|---------------------------------------|---|--|-------------------|-----|-------------------|--------------------|----------------|
| t _{PZH,} t _{PZL} | Propagation Delay Time from Inhibit to Signal Output (channel turning on) | $V_{EE}=V_{SS}=0V$ $R_{L}=1 \text{ k}\Omega$ $C_{I}=50 \text{ pF}$ | 5V 10V 15V | | 600 225 160 | 1200 450 320 | ns ns ns |
| t _{PHZ,} t _{PLZ} | Propagation Delay Time from Inhibit to Signal Output (channel turning off) | $V_{EE} = V_{SS} = 0V$ $R_L = 1 \text{ k}\Omega$ $C_L = 50 \text{ pF}$ | 5V 10V 15V | | 210 100 75 | 420 200 150 | ns ns ns |
| C _{IN} | Input Capacitance Control input Signal Input (IN/OUT) | | | | 5 10 | 7.5 15 | pF pF |
| C _{OUT} | Output Capacitance (common OUT/IN) | | | | | | |
| | CD4051 CD4052 CD4053 | V _{EE} =V _{SS} =0V | 10V 10V 10V | | 30 15 8 | | pF pF pF |
| C _{IOS} | Feedthrough Capacitance | | | | 0.2 | | pF |
| C_{PD} | Power Dissipation Capacitance | | | | | | |
| | CD4051 CD4052 CD4053 | | | | 110 140 70 | | pF pF pF |
| Signal In | puts (V _{IS}) and Outputs (V _{OS}) | | | | | | |
| | Sine Wave Response (Distortion) | $\begin{array}{l} R_L \! = \! 10 \text{ k}\Omega \\ f_{1S} \! = \! 1 \text{ kHz} \\ V_{1S} \! = \! 5 V_{p\text{-}p} \\ V_{EE} \! = \! V_{SI} \! = \! 0V \end{array}$ | 10V | | 0.04 | | % |
| | Frequency Response, Channel "ON" (Sine Wave Input) | $R_L = 1 \text{ k}\Omega, V_{EE} = 0V, V_{IS} = 5V_{p-p},$ $20 \log_{10} V_{OS}/V_{IS} = -3 \text{ dB}$ | 10V | | 40 | | MHz |
| | Feedthrough, Channel "OFF" | $R_L = 1 \text{ k}\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -40 \text{ dB}$ | 10V | | 10 | | MHz |
| | Crosstalk Between Any Two Channels (frequency at 40 dB) | $\begin{aligned} R_L &= 1 \text{ k}\Omega, V_{EE} = V_{SS} = 0 \text{V}, V_{IS}(A) = 5 \text{V}_{p\text{-}p} \\ 20 \log_{10} V_{OS}(B) / V_{IS}(A) &= -40 \text{ dB (Note 3)} \end{aligned}$ | 10V | | 3 | | MHz |
| t _{PHL} t _{PLH} | Propagation Delay Signal Input to Signal Output | $V_{EE} = V_{SS} = 0V$ $C_L = 50 \text{ pF}$ | 5V 10V 15V | | 25 15 10 | 55 35 25 | ns ns ns |
| Control I | nputs, A, B, C and Inhibit | | | | | | |
| | Control Input to Signal Crosstalk | $V_{EE}\!=\!V_{SS}\!=\!0$ V, $R_{L}\!=\!10~\text{k}\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V | 10V | | 65 | | mV (peak) |
| t _{PHL,} t _{PLH} | Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF") | V _{EE} =V _{SS} =0V C _L =50 pF | 5V 10V 15V | | 500 180 120 | 1000 360 240 | ns ns ns |

^{*}AC Parameters are guaranteed by DC correlated testing.

 $\textbf{Note 3:} \ \textbf{A, B are two arbitrary channels with A turned "ON" and B "OFF".}$



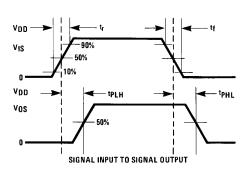


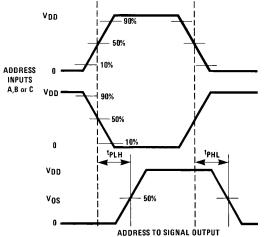
Truth Table

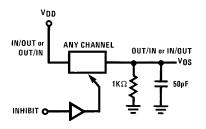
| INPUT STATES | | | | "ON" CHANNELS | | | | | |
|--------------|---|---|---|---------------|---------|------------|--|--|--|
| INHIBIT | С | В | Α | CD4051B | CD4052B | CD4053B | | | |
| 0 | 0 | 0 | 0 | 0 | 0X, 0Y | cx, bx, ax | | | |
| 0 | 0 | 0 | 1 | 1 | 1X, 1Y | cx, bx, ay | | | |
| 0 | 0 | 1 | 0 | 2 | 2X, 2Y | cx, by, ax | | | |
| 0 | 0 | 1 | 1 | 3 | 3X, 3Y | cx, by, ay | | | |
| 0 | 1 | 0 | 0 | 4 | | cy, bx, ax | | | |
| 0 | 1 | 0 | 1 | 5 | | cy, bx, ay | | | |
| 0 | 1 | 1 | 0 | 6 | | cy, by, ax | | | |
| 0 | 1 | 1 | 1 | 7 | | cy, by, ay | | | |
| 1 | * | * | * | NONE | NONE | NONE | | | |

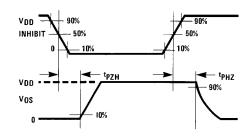
^{*}Don't Care condition.

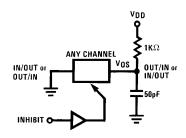


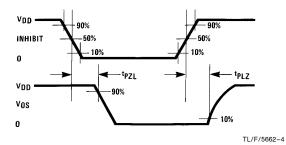










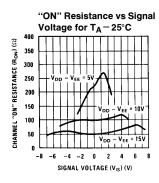


Special Considerations

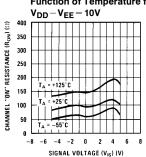
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must

not exceed 0.6V at $T_A{\leq}$ 25°C, or 0.4V at $T_A{>}$ 25°C (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

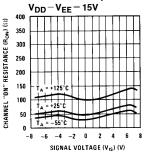
Typical Performance Characteristics



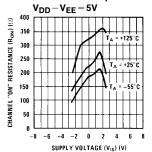
"ON" Resistance as a Function of Temperature for



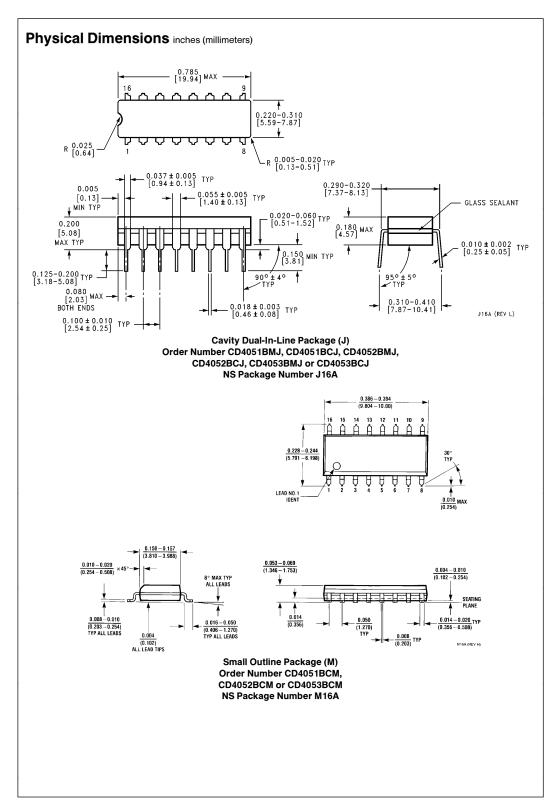
"ON" Resistance as a Function of Temperature for

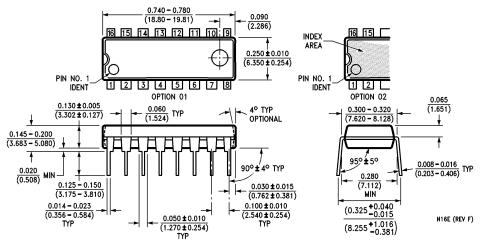


"ON" Resistance as a Function of Temperature for



TL/F/5662-5





Molded Dual-In-Line Package (N) Order CD4051BM, CD4051BC, CD4052BM, CD4052BC, CD4053BM, CD4053BC NS Package Number N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor

National Semiconducto Corporation 1111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018

National Semiconductor Europe

Fax: (+49) 0-180-530 85 86 Fax: (+49) U-18U-35U oo oo Email: onjwege etevm2.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tei: (+49) 0-180-532 78 32 Français Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80 **National Semiconductor**

Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960

National Semiconductor

Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408