# SN74AHC1G32-Q1
SINGLE 2-INPUT POSITIVE-OR GATE

SCLS544A – SEPTEMBER 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Operating Range of 2 V to 5.5 V

- Max t_{pd} of 6.5 ns at 5 V
- Low Power Consumption, 10-μA Max I_{CC}
- $\pm$8-mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17

description/ordering information

The SN74AHC1G32 is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

**DBV OR DCK PACKAGE
(TOP VIEW)**

```
      A [ 1      5 ] V_CC
      B [ 2
    GND [ 3      4 ] Y
```
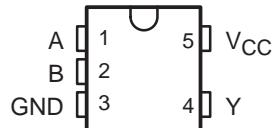
ORDERING INFORMATION[†]

T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING[§]
–40°C to 105°C	SOT (SOT-23) – DBV	Reel of 3000	SN74AHC1G32TDBVRQ1	A32_
	SOT (SC-70) – DCK	Reel of 3000	SN74AHC1G32TDCKRQ1	AG_

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
[§] The actual top-side marking has one additional character that designates the wafer fab / assembly site.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

logic diagram (positive logic)


```
A  1 ──┐
       ├──╲
       │   ╲──── 4  Y
B  2 ──┘   ╱
       ├──╱
```


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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	105	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25°C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50\ \mu A$	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4\ mA$	3 V	2.58			2.48		
	$I_{OH} = -8\ mA$	4.5 V	3.94			3.8		
V_{OL}	$I_{OL} = 50\ \mu A$	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	$I_{OL} = 4\ mA$	3 V			0.36		0.44	
	$I_{OL} = 8\ mA$	4.5 V			0.36		0.44	
I_I	$V_I = 5.5\ V$ or GND	0 V to 5.5 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, $\quad I_O = 0$	5.5 V		1			10	μA
C_i	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	$C_L = 50\ pF$		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25°C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	$C_L = 50\ pF$		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $\quad f = 1\ MHz$	14	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.
   E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AHC1G32TDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	A32U	Samples
SN74AHC1G32TDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	AGU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF SN74AHC1G32-Q1 :

- Catalog: SN74AHC1G32

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS
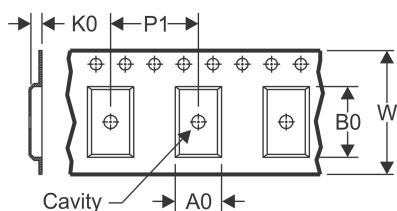
A0	Dimension designed to accommodate the component width	
B0	Dimension designed to accommodate the component length	
K0	Dimension designed to accommodate the component thickness	
W	Overall width of the carrier tape	
P1	Pitch between successive cavity centers	

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
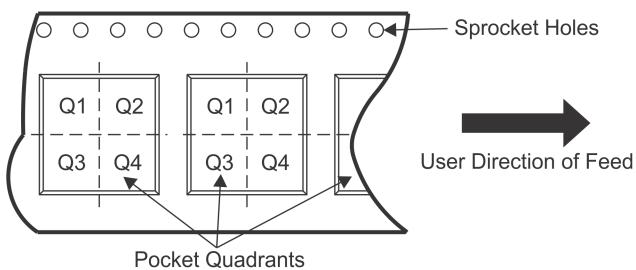
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G32TDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G32TDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS
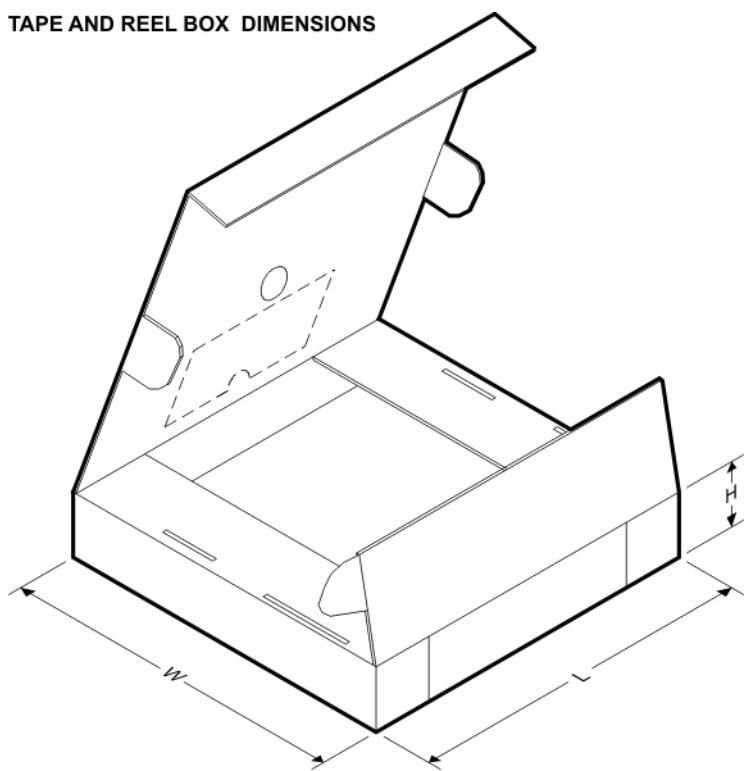
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G32TDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0
SN74AHC1G32TDCKRQ1	SC70	DCK	5	3000	203.0	203.0	35.0

DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

5   4

2,40
1,80

1,40
1,10

Pin 1
Index Area

1   3

0,65

5X 0,30
0,15

1,30

⊕ 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

0,10 0,10
0,00

Seating Plane
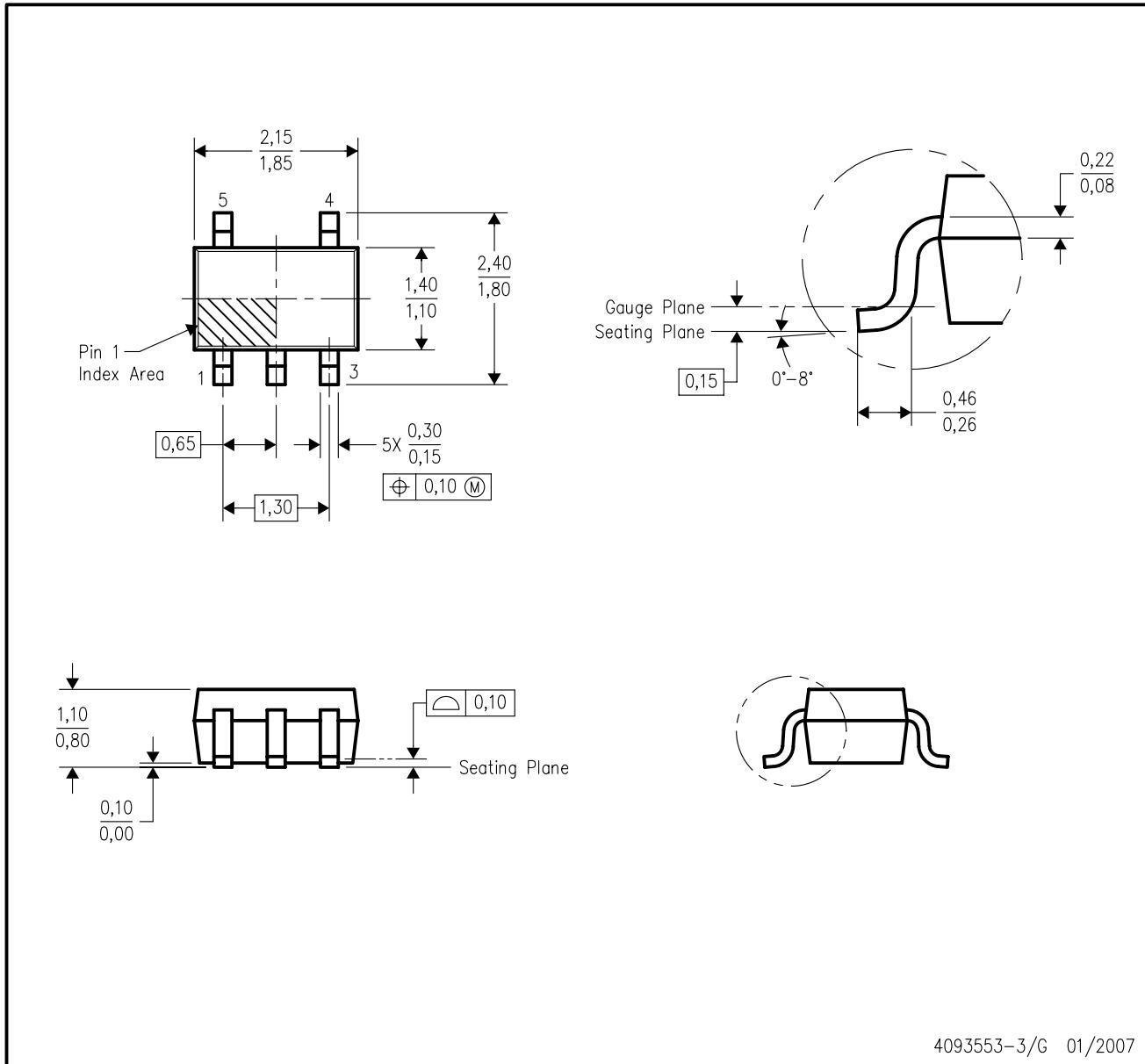
4093553−3/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AA.

DCK (R-PDSO-G5)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
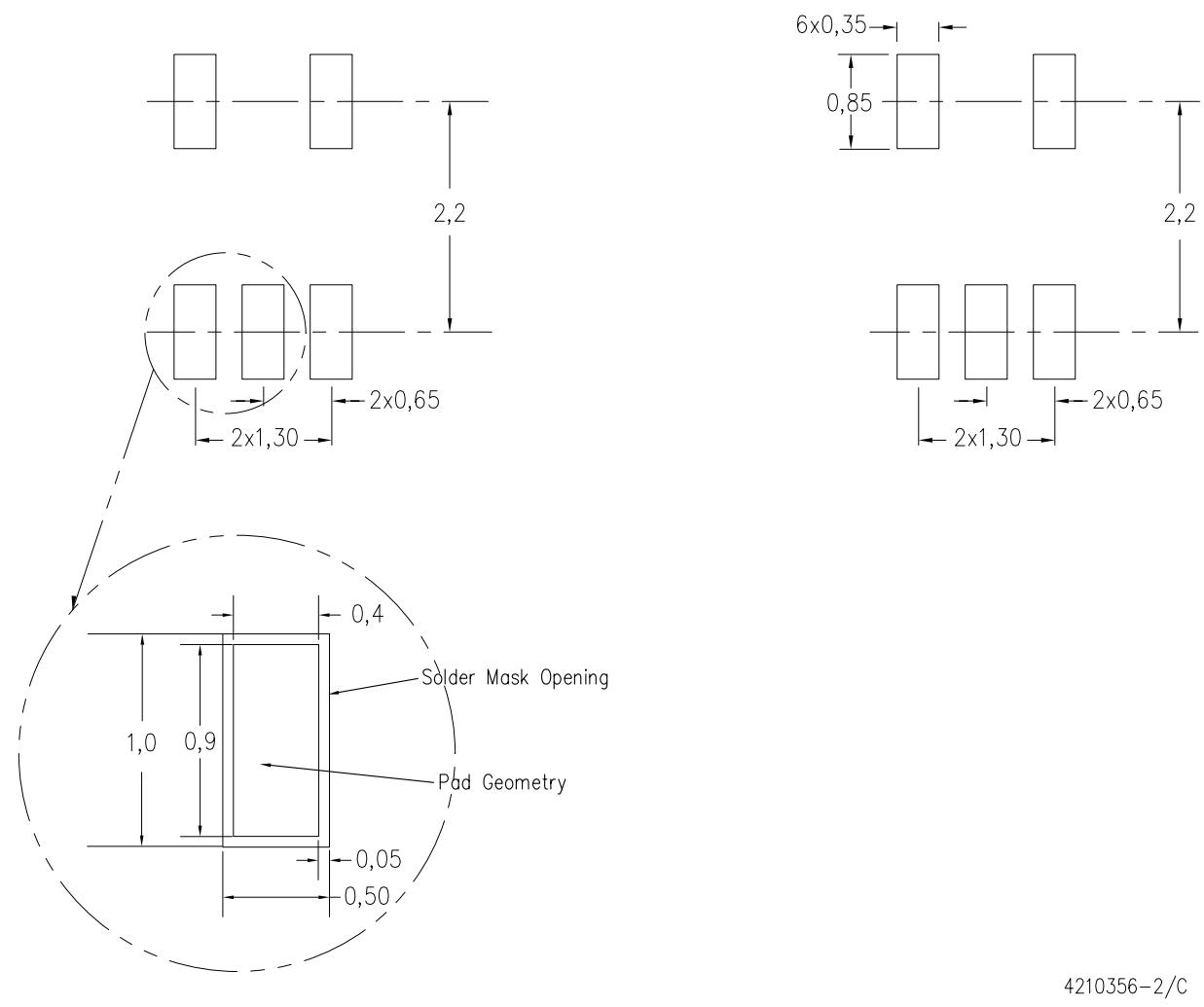
6x0,35

0,85

2,2

2x0,65

2x1,30

2,2

2x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356-2/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC-7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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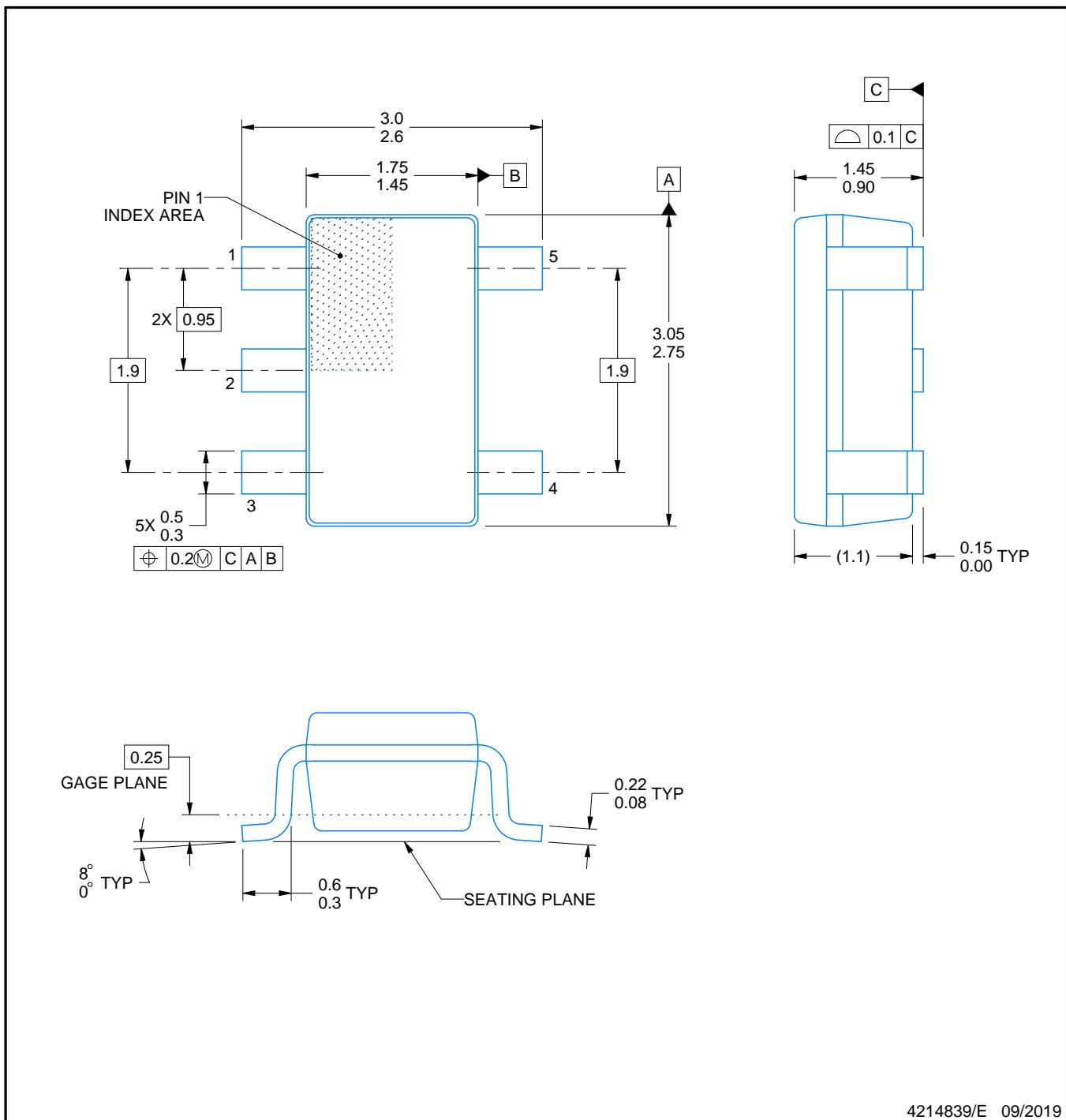
4214839/E   09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

PKG ℄

5X (1.1)

1

5X (0.6)

5

SYMM ℄

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)
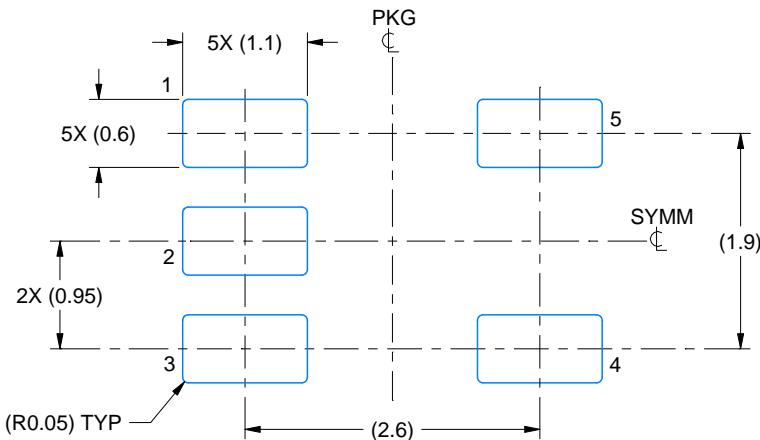
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED
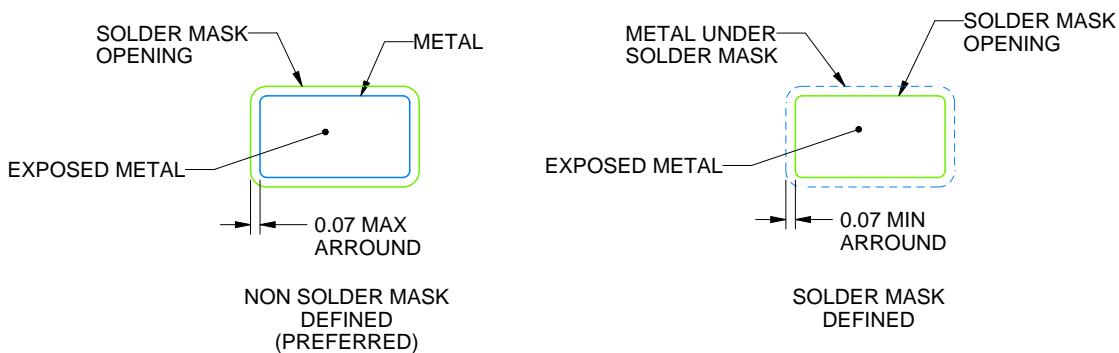
SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
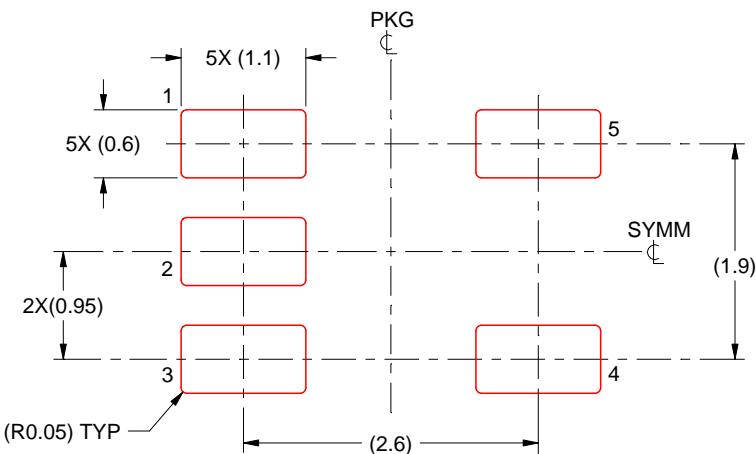
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E   09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
8. Board assembly site may have different recommendations for stencil design.