300-mA, Sub-Bandgap Output Voltage, Low-I_Q, Low-Dropout Regulator

FEATURES

- **2% Accuracy**
- **Low I_Q: 35 μA**
- **Fixed-Output Voltage Combinations Possible from 0.7 V to 1.15 V(1)**
- **High PSRR: 68 dB at 1 kHz**
- **Stable with Effective Capacitance of 0.1 μF(2)**
- **Thermal Shutdown and Overcurrent Protection**
- **Packages: SOT23-5, 1,5-mm × 1,5-mm SON-6**

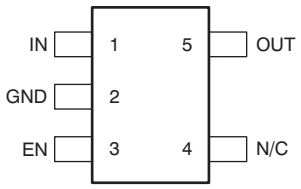
(1) For output voltage of 1.2 V and higher, see the TLV702 family of devices.

(2) See the *Input and Output Capacitor Requirements* in the Application Information section.

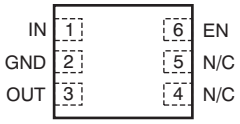
APPLICATIONS

- **Wireless Handsets**
- **Smart Phones, PDAs**
- **MP3 Players**
- **ZigBee® Networks**
- **Bluetooth® Devices**
- **Li-Ion Operated Handheld Products**
- **WLAN and Other PC Add-on Cards**

TLV712xxDBV
SOT23-5
(TOP VIEW)



TLV712xxDSE
SON-6
(TOP VIEW)



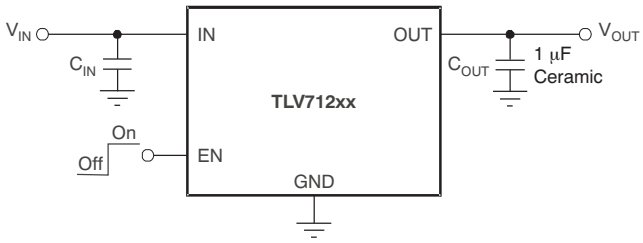
DESCRIPTION

The TLV712xx series of low-dropout linear regulators (LDOs) are low quiescent current devices with excellent line and load transient performance. These devices provide sub-bandgap output voltages; that is, output voltages less than 1.2 V all the way down to 0.7 V. Therefore, these LDOs can be used to power processors with operating voltages less than 1.2 V. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 μF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV712xxP series also provides an active pull-down circuit to quickly discharge the outputs.

The TLV712xx series of LDO linear regulators are available in SOT23-5 and 1,5-mm x 1,5-mm SON-6 packages.



Typical Application Circuit
(Fixed-Voltage Versions)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION (1)

PRODUCT	V_{OUT} (2)
TLV712**xx(x)***Pyyyz*	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 09 = 0.9 V; 085 = 0.85 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.7 V to 1.15 V in 50-mV increments are available. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	+6.0	V
	EN	–0.3	+6.0	V
	OUT	–0.3	+5.0	V
Current (source)	OUT	Internally limited		
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DBV	200°C/W	500 mW	275 mW	200 mW
DSE	180°C/W	555 mW	305 mW	222 mW

(1) For board details, see the *Thermal Information* section.

ELECTRICAL CHARACTERISTICS

At V_{IN} = 2.0 V, I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1.0 μF, and T_J = –40°C to +125°C, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.0		5.5	V
V_{OUT}	DC output accuracy		–20	6	+20	mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	2 V ≤ V_{IN} ≤ 5.5 V,		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 300 mA		1	15	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	μA
		I_{OUT} = 300 mA		370		μA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V		400		nA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V, T_J = –40°C to +85°C		1	2	μA
PSRR	Power-supply rejection ratio	f = 1 kHz		68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{OUT} = 0.7 V		30		μV_{RMS}
t_{STR}	Startup time(1)	I_{OUT} = 300 mA		100		μs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		μA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
$R_{DISCHARGE}$	Active pull-down resistance (TLV712xxP only)	V_{EN} = 0 V		120		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+165		°C
		Reset, temperature decreasing		+145		°C
T_J	Operating junction temperature		–40		+125	°C

(1) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAMS

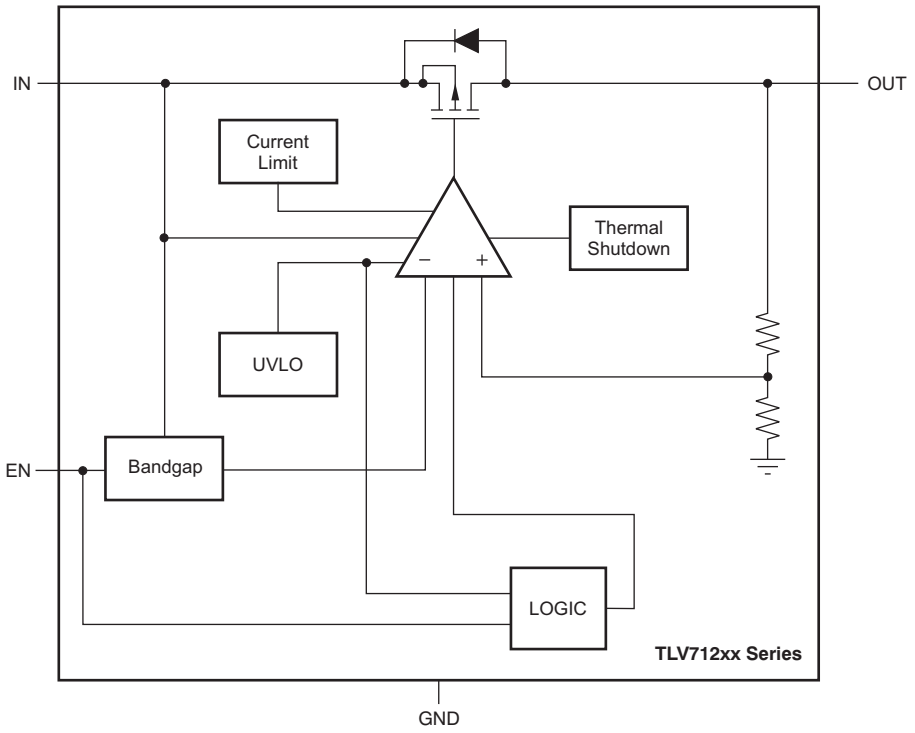


Figure 1. TLV712xx

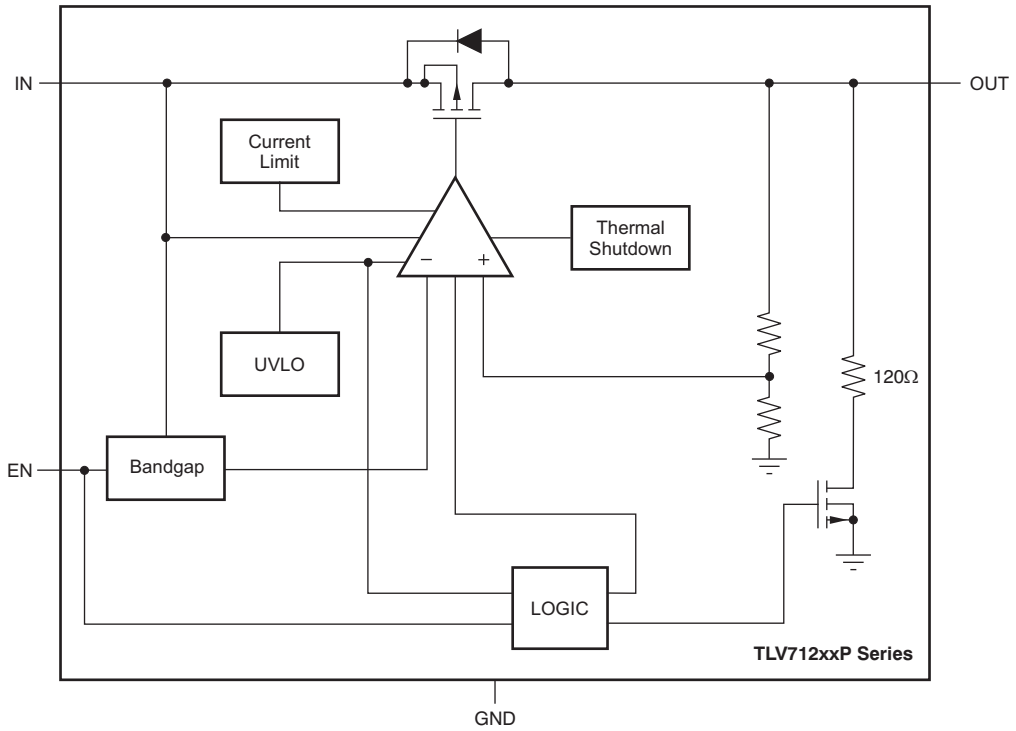
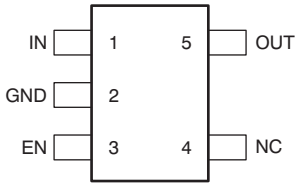


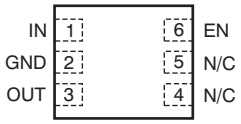
Figure 2. TLV712xxP

PIN CONFIGURATIONS

DBV PACKAGE
SOT23-5
(TOP VIEW)



DSE PACKAGE(1)
SON-6
(TOP VIEW)



(1) Preview package option.

PIN DESCRIPTIONS

NAME	SOT23-5 DBV	SON-6 DSE	DESCRIPTION
IN	1	1	Input pin. A small 1-μF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	2	Ground pin
EN	3	6	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 μA, nominal. For TLV712xxP, output voltage is discharged through an internal 120-Ω resistor when device is shut down.
NC	4	4, 5	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	3	Regulated output voltage pin. A small 1-μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 2.0 V, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION

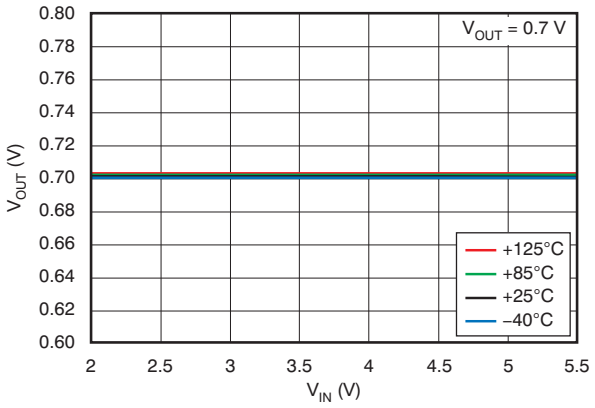


Figure 3.

LOAD REGULATION

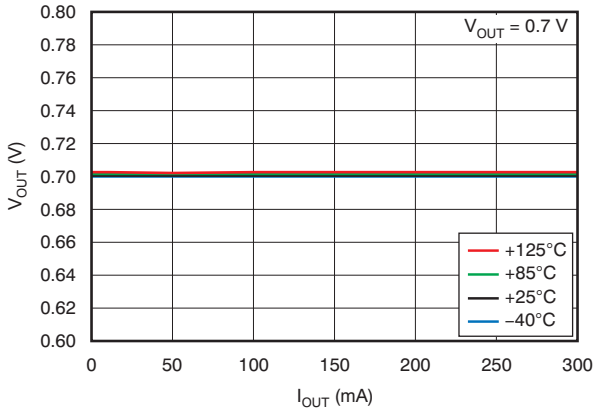


Figure 4.

OUTPUT VOLTAGE vs TEMPERATURE

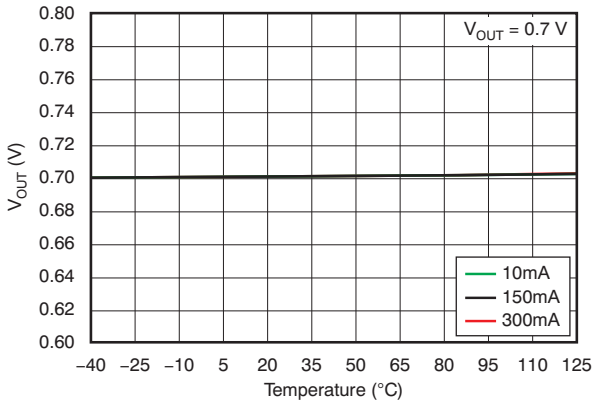


Figure 5.

GROUND PIN CURRENT vs INPUT VOLTAGE

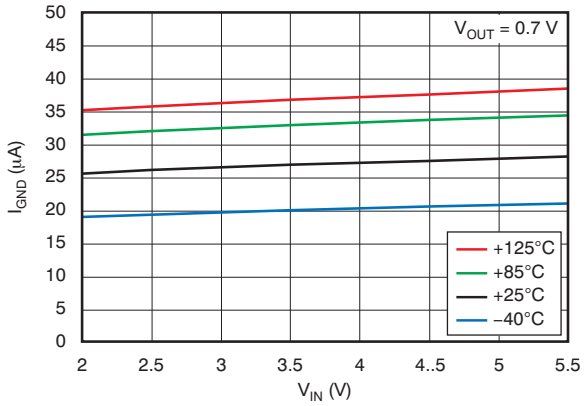


Figure 6.

GROUND PIN CURRENT vs LOAD

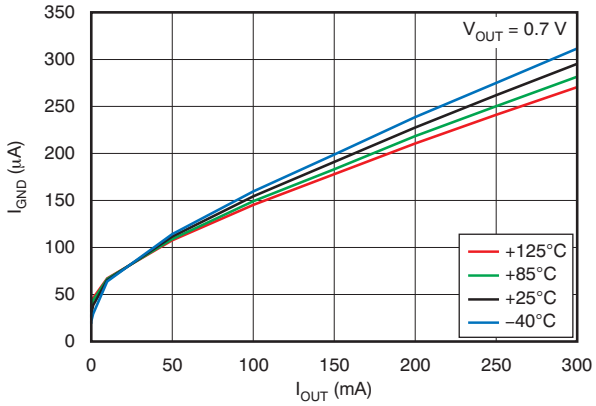


Figure 7.

GROUND PIN CURRENT vs TEMPERATURE

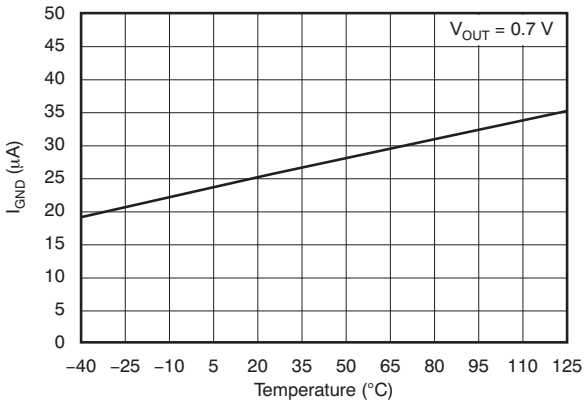


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 2.0 V, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = +25°C.

SHUTDOWN CURRENT vs INPUT VOLTAGE

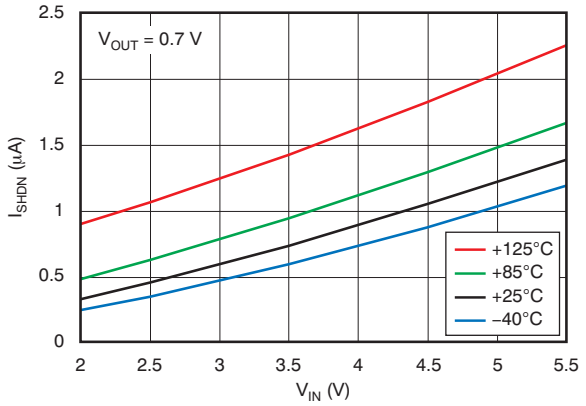


Figure 9.

CURRENT LIMIT vs INPUT VOLTAGE

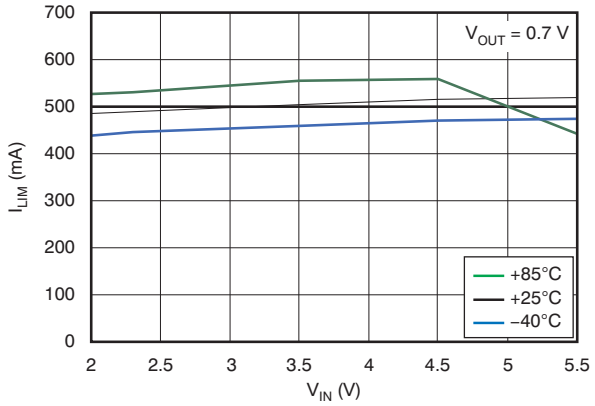


Figure 10.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

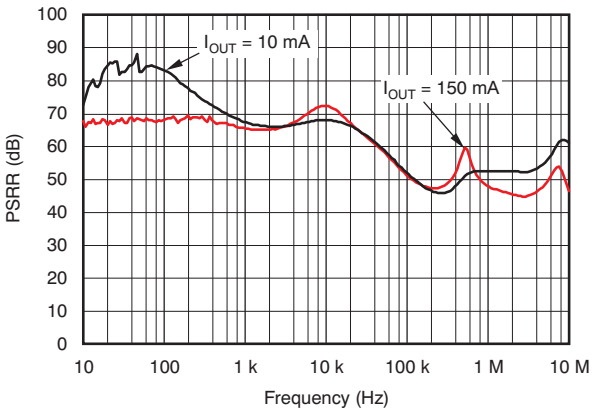


Figure 11.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

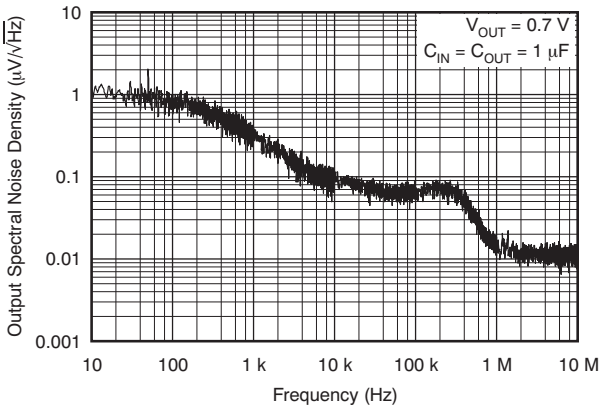


Figure 12.

LOAD TRANSIENT RESPONSE

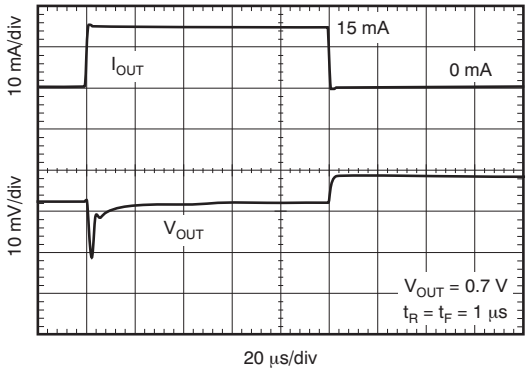


Figure 13.

LOAD TRANSIENT RESPONSE

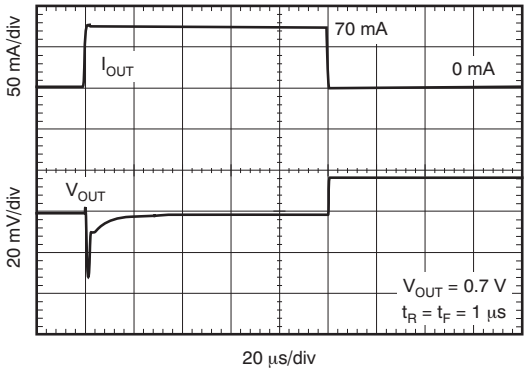


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 2.0 V, I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 μF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD TRANSIENT RESPONSE

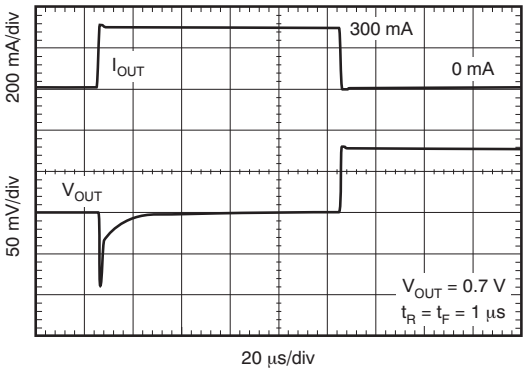


Figure 15.

LINE TRANSIENT RESPONSE

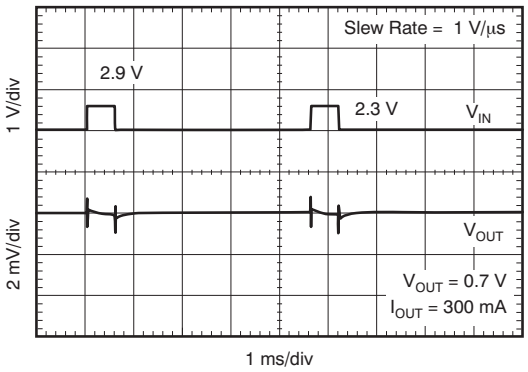


Figure 16.

LINE TRANSIENT RESPONSE

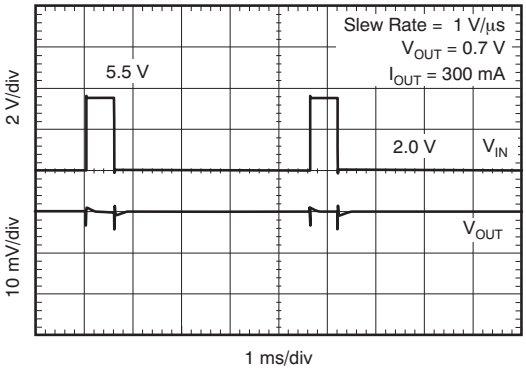


Figure 17.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

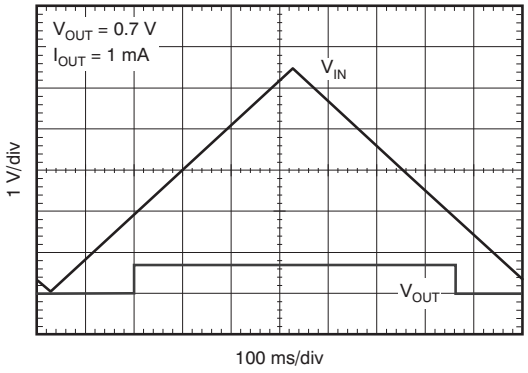


Figure 18.

APPLICATION INFORMATION

GENERAL DESCRIPTION

The TLV712xx belongs to a new family of next-generation value LDO regulators. These devices offer sub-bandgap output voltages; that is, output voltages from 1.2 V all the way down to 0.7 V. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0-μF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV712xx is designed to be stable with an *effective capacitance* of 0.1 μF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-μF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications.

NOTE: Using a 0.1-μF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 μF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-μF to 1.0-μF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-μF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV712xx internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates ($V_{IN} – V_{OUT}$) × I_{LIMIT} until thermal shutdown is triggered and the device turns off. As the device cools, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The PMOS pass element in the TLV712xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9 V. This relatively lower voltage value required to turn on the LDO can also be used to power the device when it is connected to a GPIO of a newer processor, where the GPIO Logic 1 voltage level is lower than that of traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

The TLV712xxP version has internal active pull-down circuitry that discharges the output with a time constant of:

$$\tau = \frac{(120 \bullet R_L)}{(120 + R_L)} \bullet C_{OUT} \quad (1)$$

where:

- R_L = Load resistance
- C_{OUT} = Output capacitor

DROPOUT VOLTAGE

The TLV712xx uses a PMOS pass transistor to achieve low dropout. For the complete output voltage range of 0.7 V to 1.2 V, the device can supply 300 mA with a rated minimum input voltage of 2.0 V. Note that the dropout voltage specification is not relevant for the TLV712xx family of devices because the output voltage range of the device does not exceed 1.2 V and the minimum input voltage for the device is 2.0 V.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV712xx uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV712xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV712xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Thermal performance data for TLV712xx were gathered using the TLV700 evaluation module (EVM), a two-layer board with two ounces of copper per side. The dimensions and layout for the SOT23-5 package EVM are shown in Figure 19 and Figure 20. Corresponding thermal performance data are given in Table 1. Note that this board has provision for soldering not only the SOT23-5 package on the bottom layer, but also an SC-70 package on the top layer. The dimensions and layout of the SON-6 (DSE) package EVM are shown in Figure 21 and Figure 22. Corresponding thermal performance data are given in Table 1. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV712xx are available from the Texas Instruments web site at www.ti.com. The recommended land pattern for the DBV and DSE packages are shown in Figure 23 and Figure 24 respectively.

Table 1. EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DBV	200°C/W	500 mW	275 mW	200 mW
DSE	180°C/W	555 mW	305 mW	222 mW

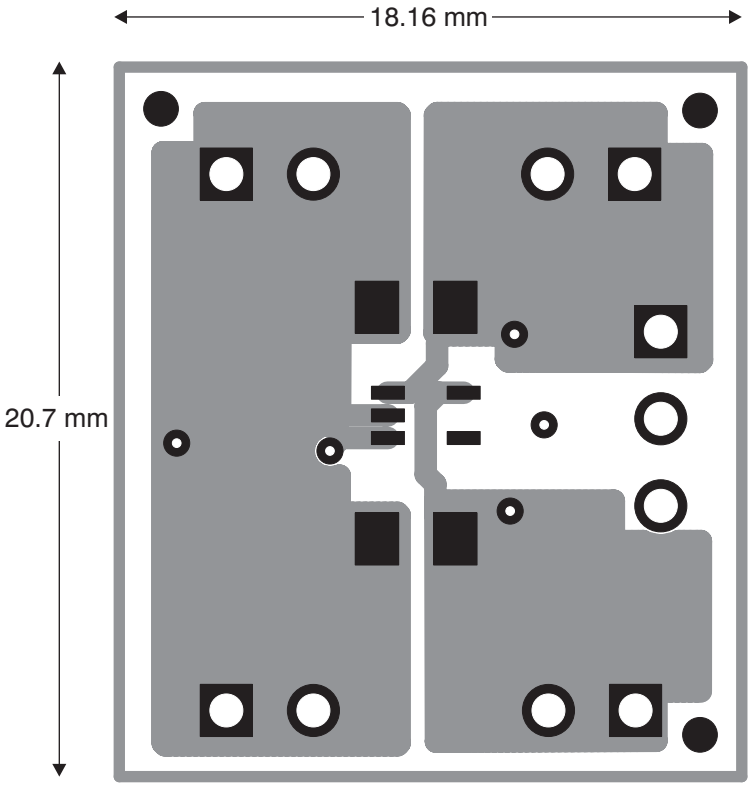


Figure 19. SOT23-5 EVM Top Layer

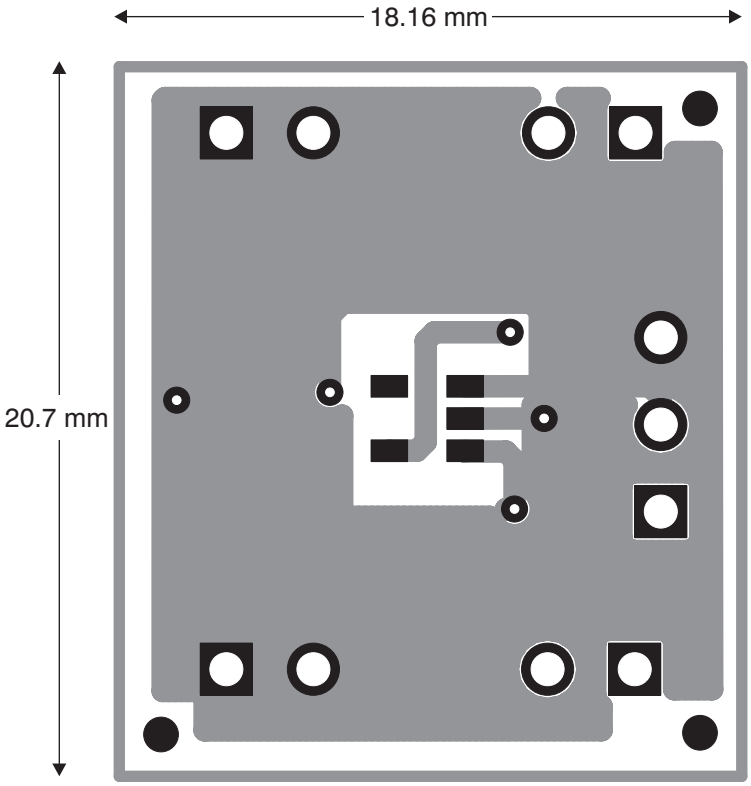


Figure 20. SOT23-5EVM Bottom Layer

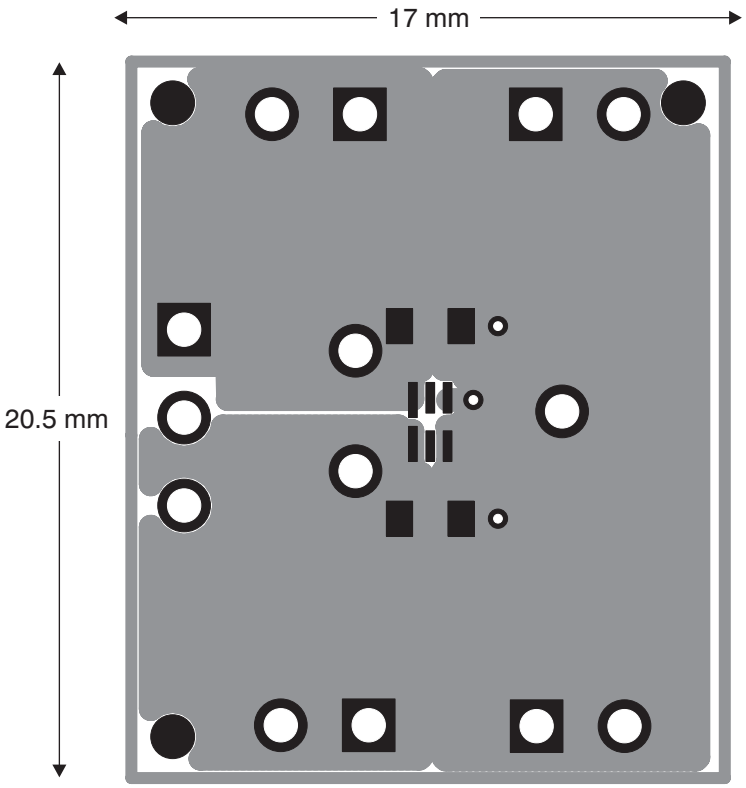


Figure 21. DSE EVM Top Layer

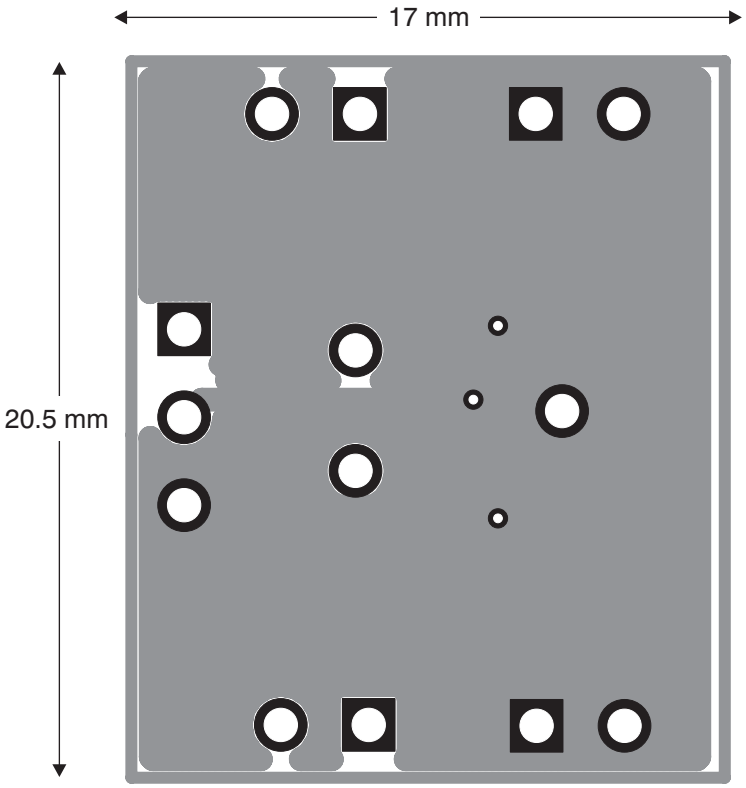
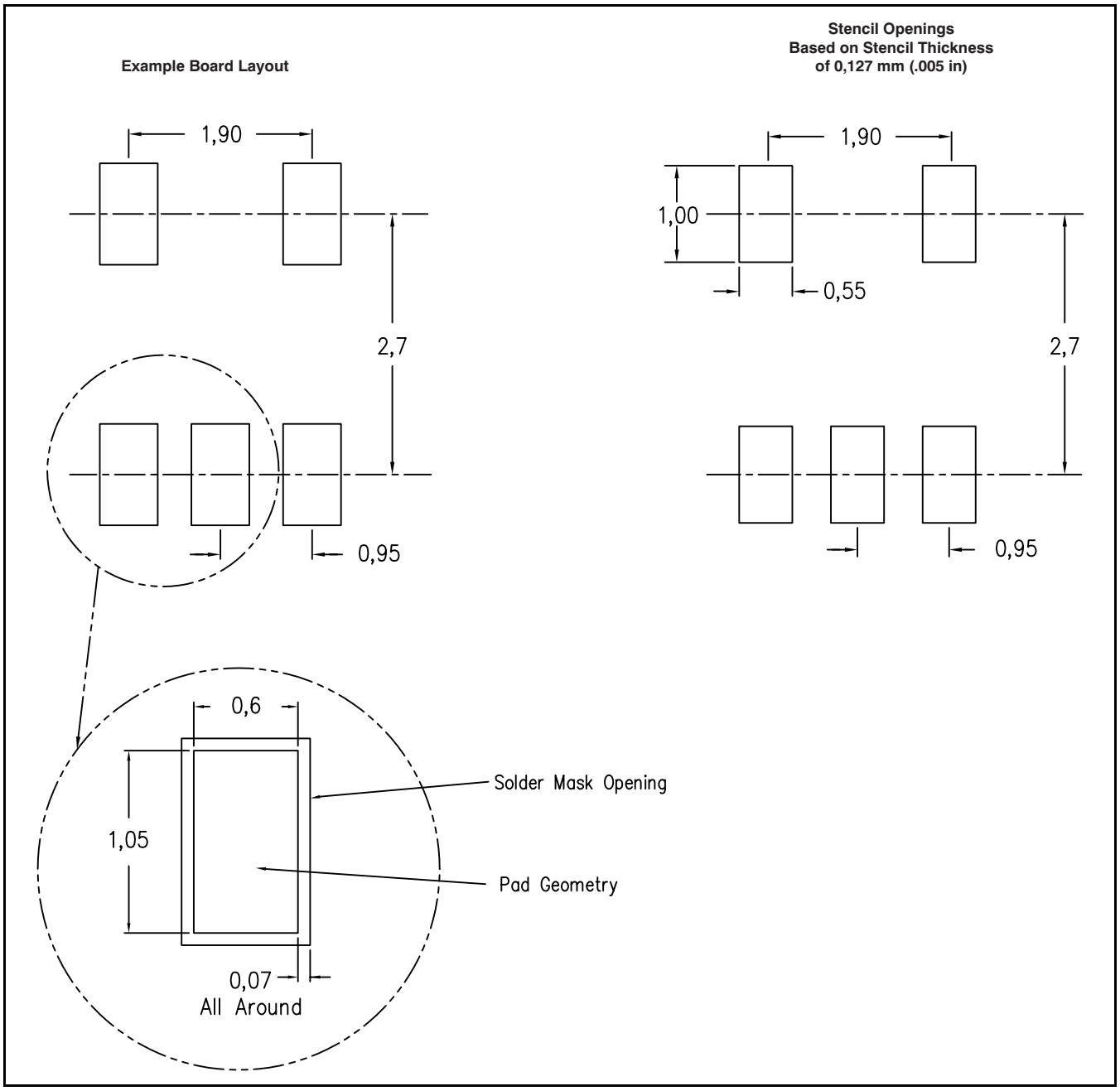


Figure 22. DSE EVM Bottom Layer



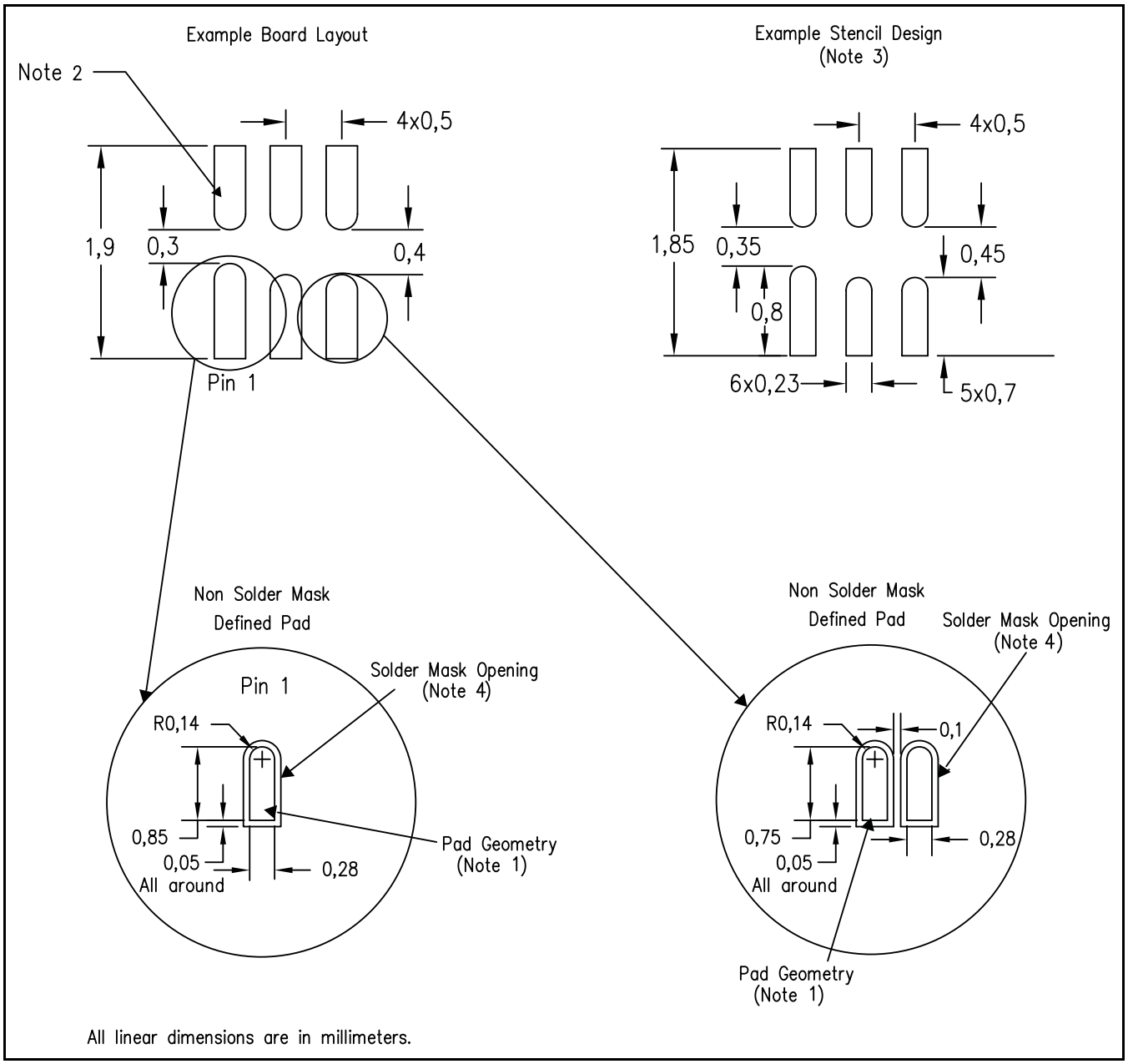
(1) All linear dimensions are in millimeters.

(2) Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

(3) Publication IPC-7351 is recommended for alternate designs.

(4) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric load solder paste. Refer to IPC-7525 for other stencil recommendations.

Figure 23. Recommended Land Pattern for DBV Package



(1) Publication IPC-7351 is recommended for alternate designs.

(2) For more information, refer to TI application notes SCBA017 and SLUA271 (*Quad Flatpack No-Lead Logic Packages* and *QFN/SON PCB Attachment*, respectively) for specific thermal information, via requirements, and additional recommendations for board layout. These documents are available at the Texas Instruments web site (http://www.ti.com) by searching for the literature number.

(3) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.

(4) Customers should contact their board fabrication site for minimum solder mask tolerances between signal pads.

Figure 24. Recommended Land Pattern for DSE Package

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September, 2010) to Revision A **Page**

- Added SON package description to *Features* list 1
- Added SON-6 package (preview) pin drawing to front page 1
- Revised last paragraph of *Description* section to include information about DSE package 1
- Updated *Ordering Information* table 2
- Revised *Dissipation Ratings* table to show DSE package information 2
- Added DSE package pinout (preview) and pin configuration information 5
- Updated *Package Mounting* and *Power Dissipation* sections to reflect DSE package information 10
- Added Figure 21 and Figure 22 12
- Added Figure 24 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71209DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVO	Samples
TLV71209DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QVO	Samples
TLV71210DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAR	Samples
TLV71210DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SAR	Samples
TLV71210DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RX	Samples
TLV71210DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RX	Samples
TLV71211DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDK	Samples
TLV71211DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDK	Samples
TLV71211DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	YI	Samples
TLV71211DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	YI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

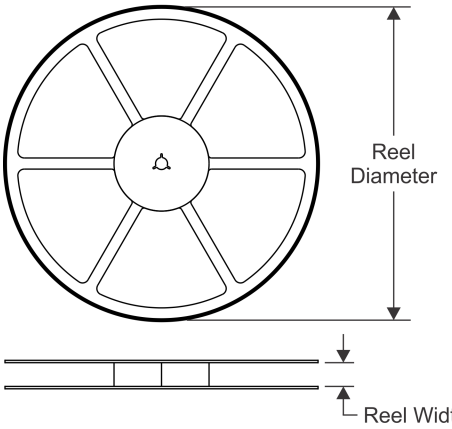
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

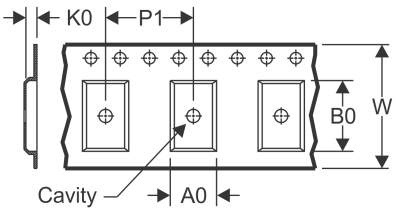
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

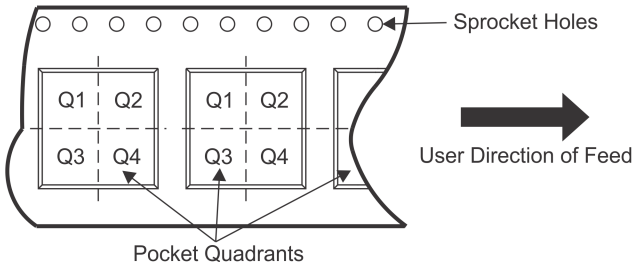


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

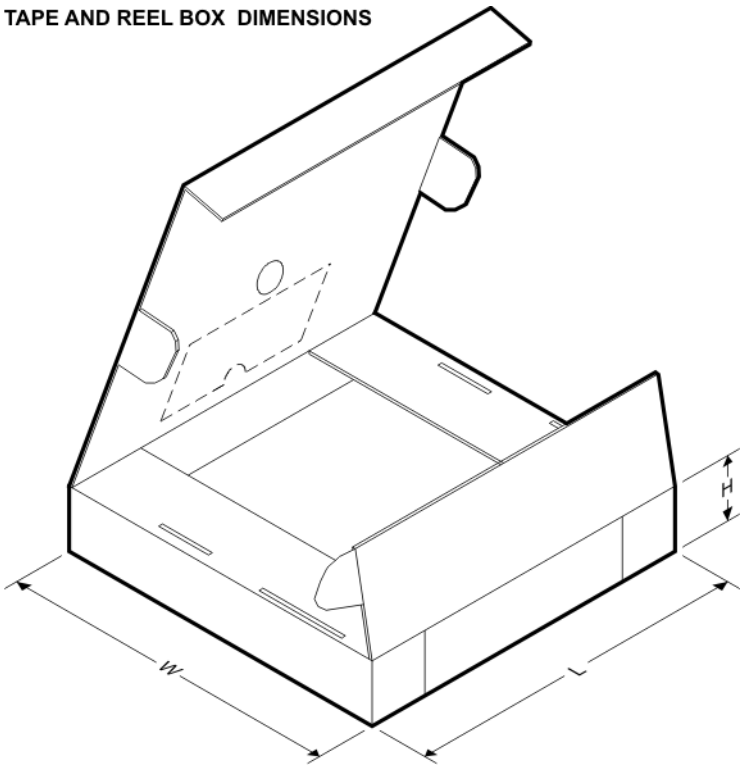
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71209DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71209DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71209DBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
TLV71209DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71210DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71210DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71210DBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71210DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71210DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71210DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71211DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71211DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TLV71211DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71211DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71211DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71211DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

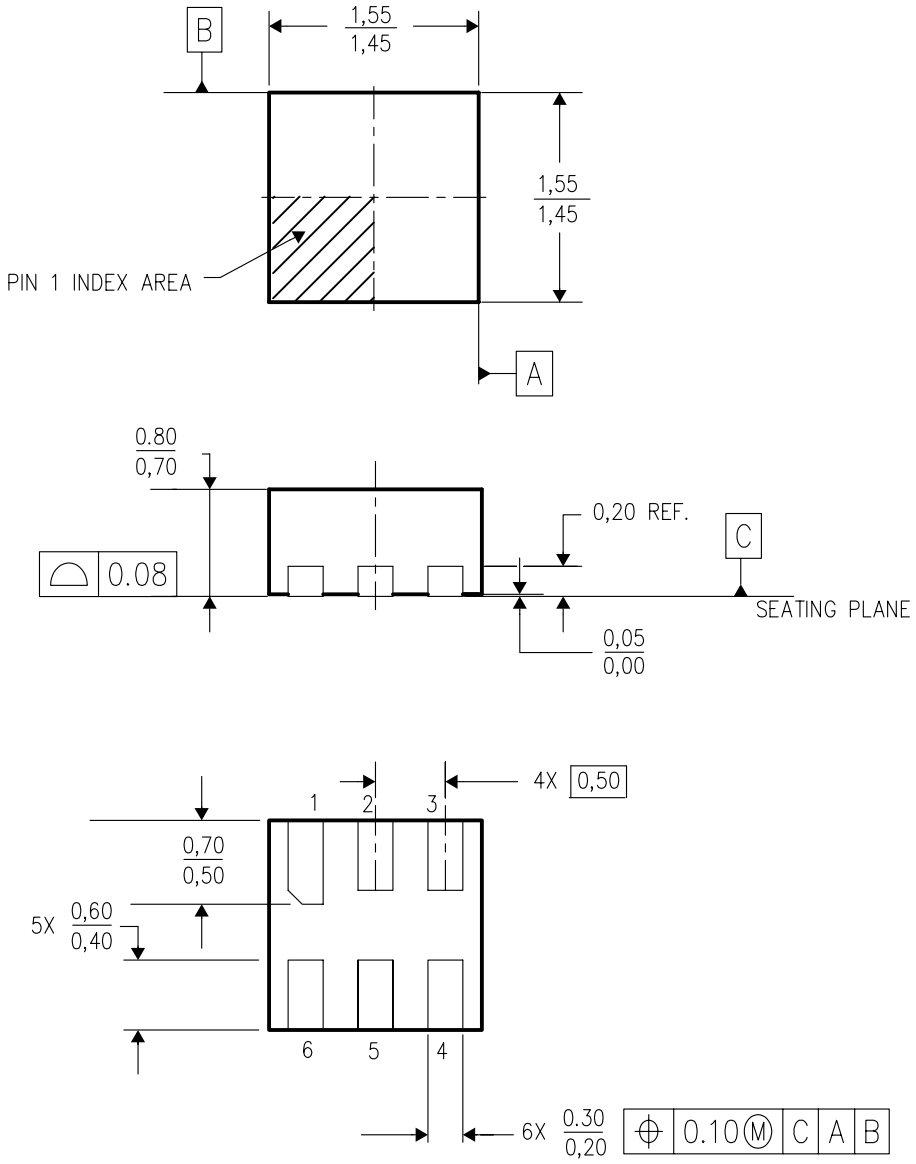
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71209DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV71209DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71209DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71209DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV71210DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71210DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV71210DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV71210DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV71210DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV71210DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV71211DBVR	SOT-23	DBV	5	3000	183.0	183.0	20.0
TLV71211DBVT	SOT-23	DBV	5	250	183.0	183.0	20.0
TLV71211DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV71211DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV71211DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV71211DSET	WSON	DSE	6	250	203.0	203.0	35.0

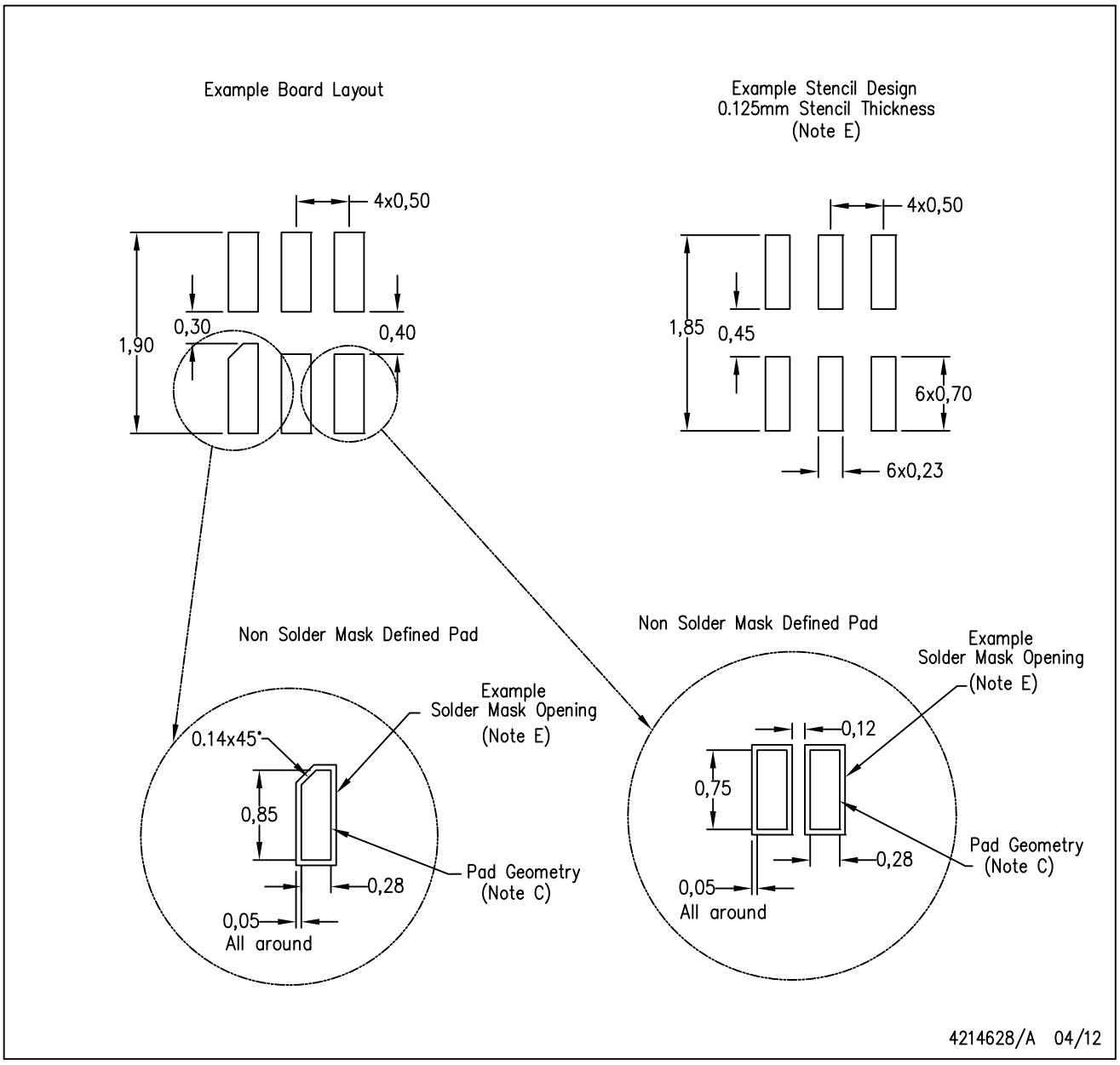
DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

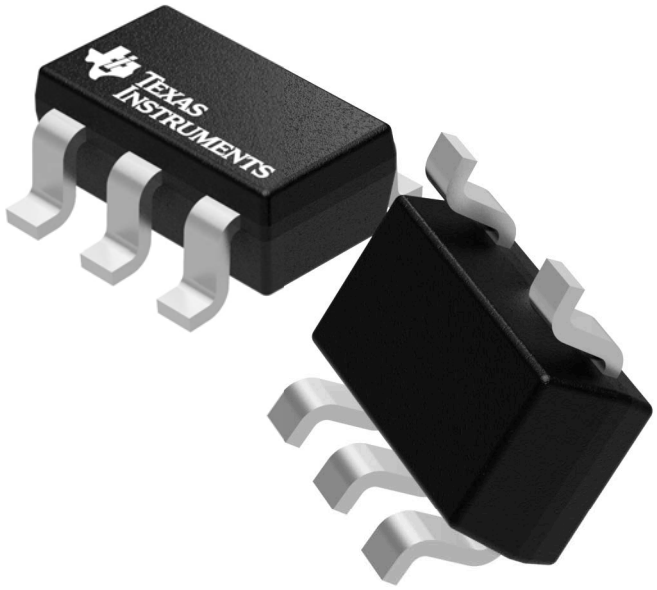
DSE (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



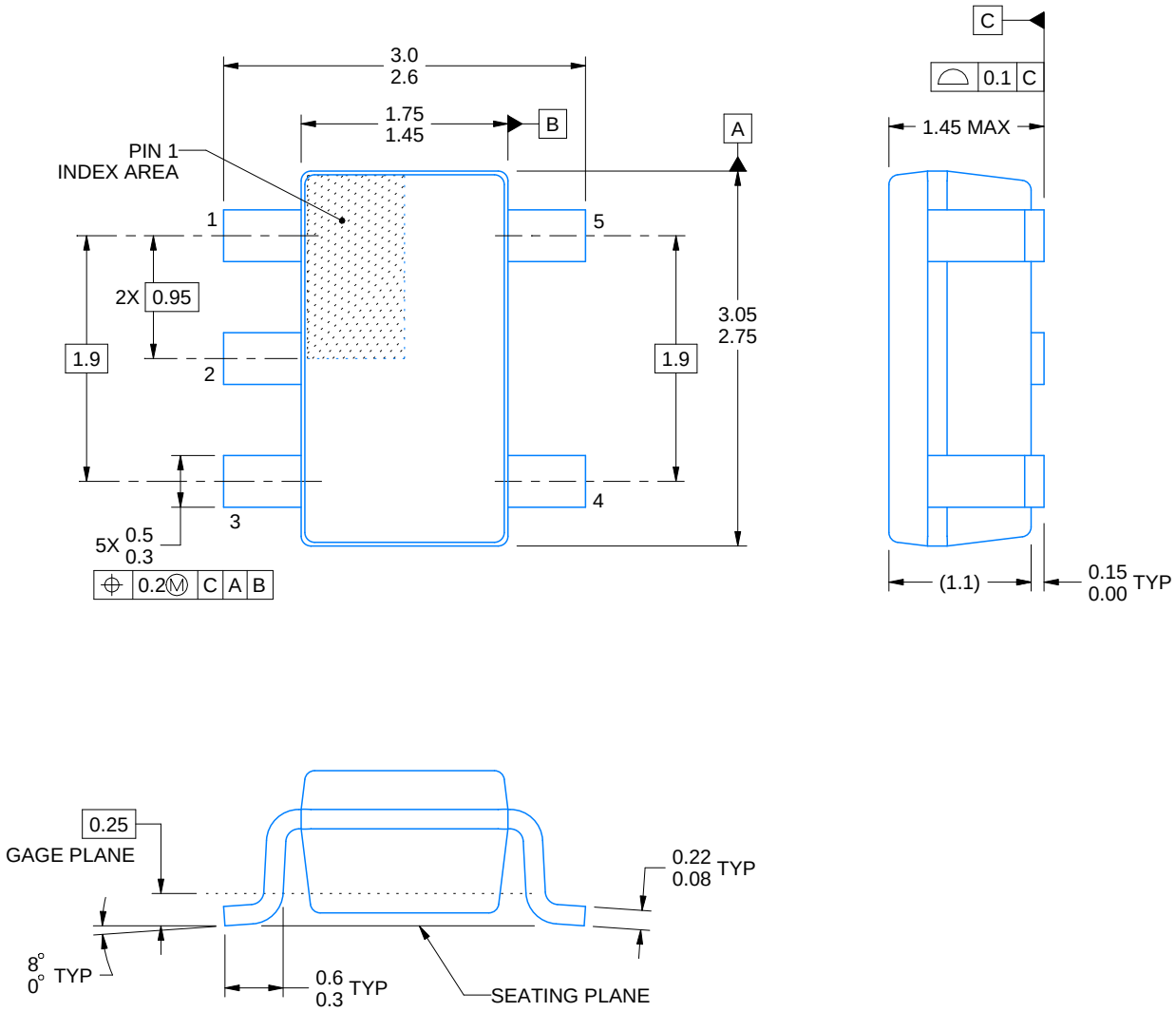
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

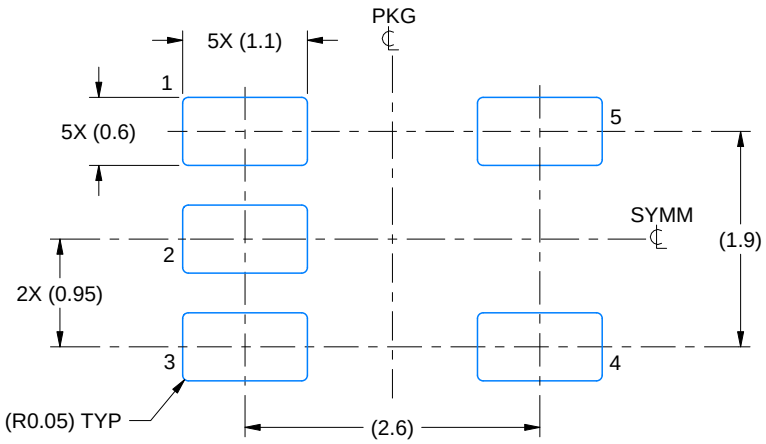
SMALL OUTLINE TRANSISTOR



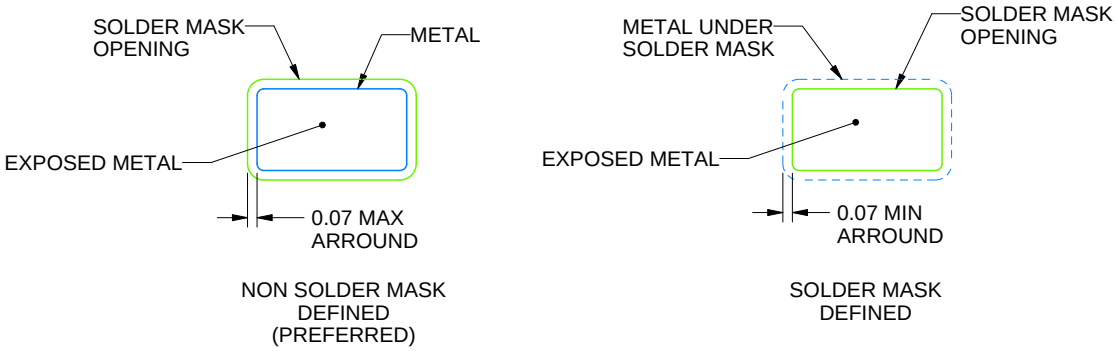
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

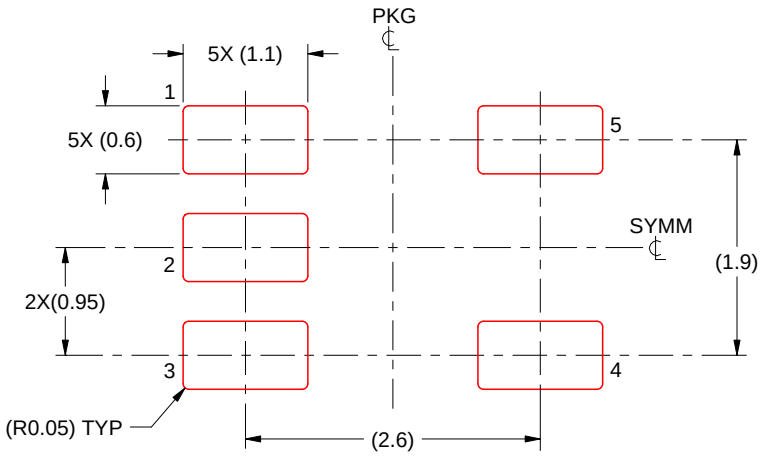


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

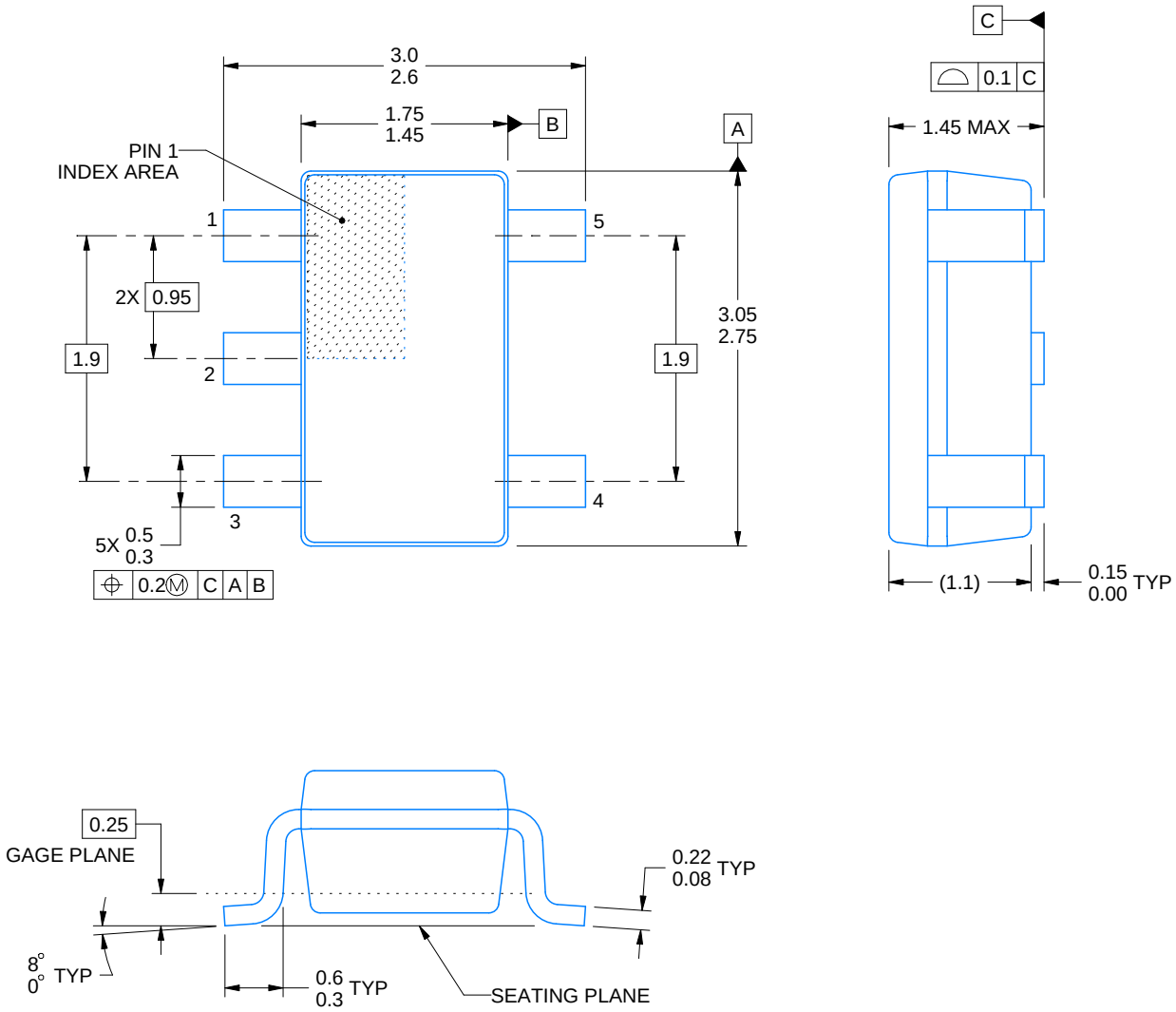
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

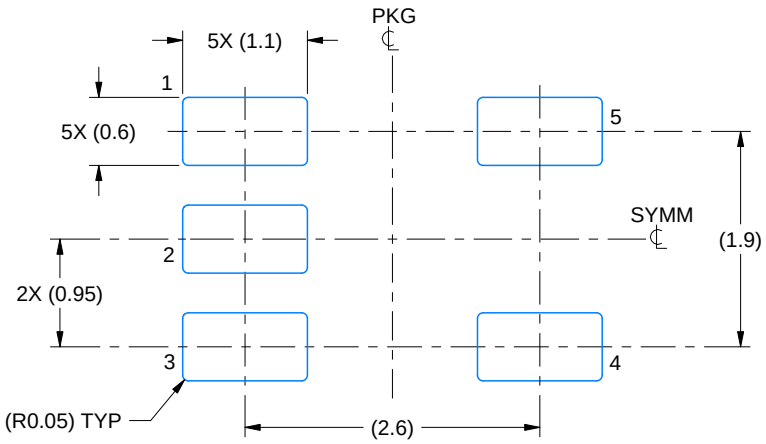
SMALL OUTLINE TRANSISTOR



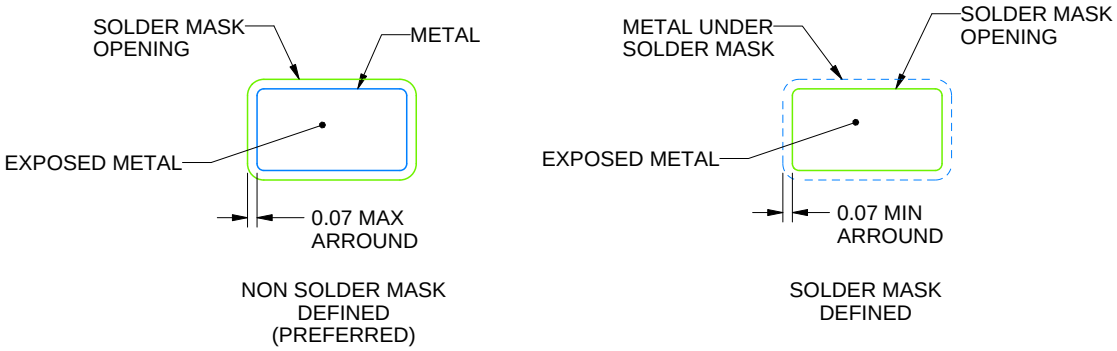
4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

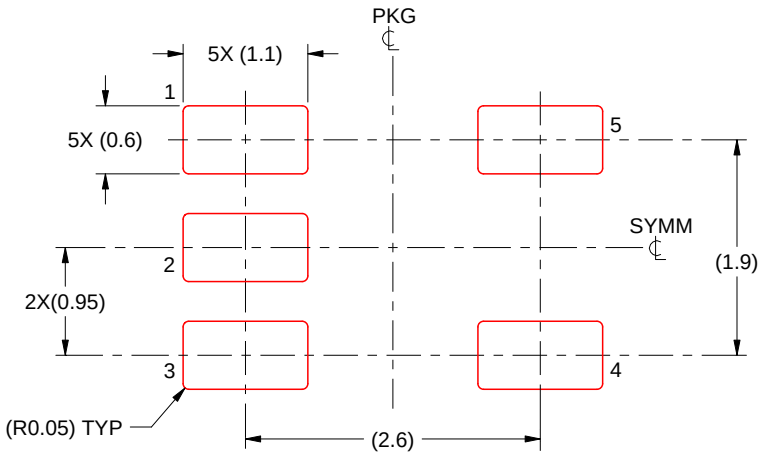


SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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