Features

- Recision supply voltage monitor
  2.63 V (CBM706P, CBM706R, CBM708R)
  2.93 V (CBM706S, CBM708S)
  3.08 V (CBM706T, CBM708T)
- 100 µA quiescent current
- 200 ms reset pulse width
- Debounced manual reset input (MR)
- Independent watchdog timer
- 1.6 sec timeout (CBM706P, CBM706R, CBM706S,CBM706T)
- Voltage monitor for power fail or low battery warning
- Guaranteed RESET valid with V_{CC} = 1 V
- Superior upgrade for CBM706P/R/S/T, CBM708R/S/T

Applications

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Critical microprocessor monitoring
- Battery operated systems
- Portable instruments

General Description

The CBM706P/ CBM706R/ CBM706S/ CBM706T and the CBM708R/ CBM708S/ CBM708T microprocessor supervisory circuits are suitable for monitoring either 3 V or 3.3 V power supplies.

The CBM706P/ CBM706R/ CBM706S/CBM706T provide power supply monitoring circuitry that generate a reset output during power-up, power-down, and brownout conditions. The reset output remains operational with V_{CC} as low as 1 V. Independent watchdog monitoring circuitry is also provided. This activates if the watchdog input does not toggle within 1.6 sec.

In addition, there is a 1.25 V threshold detector for a power fail warning, low battery detection, or to monitor an additional power supply. An active low debounced MR input is also included.

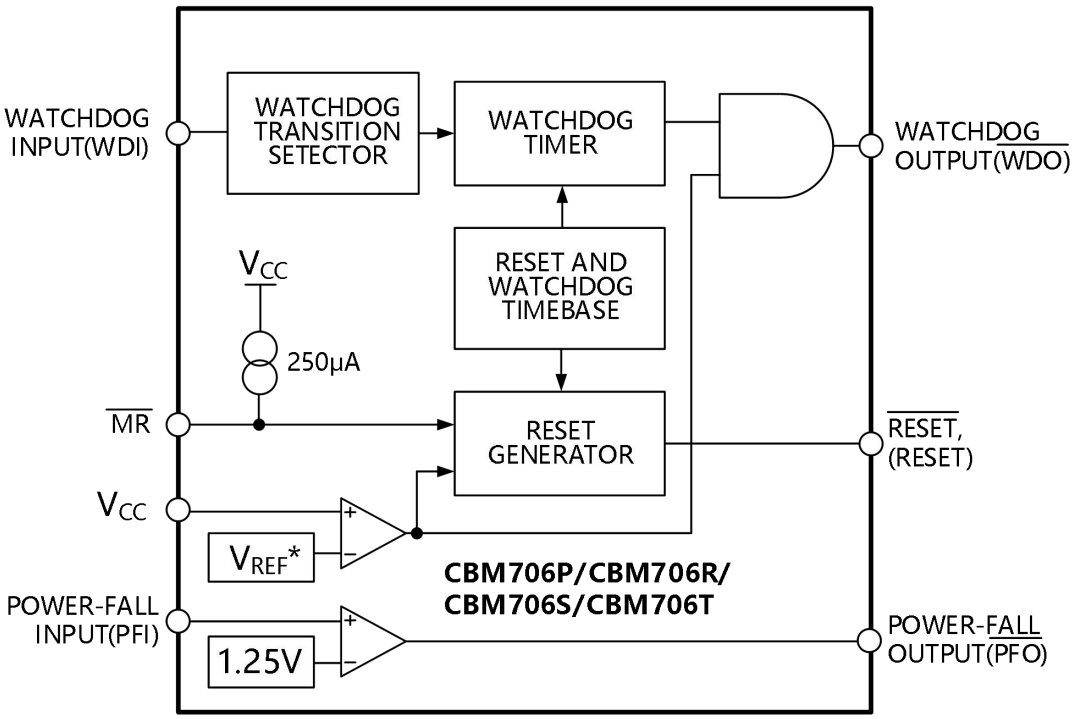
The CBM706R, CBM706S, and CBM706T are identical except for the reset threshold monitor levels, which are 2.63V, 2.93V,and 3.08 V, respectively. The CBM706P is identical to the CBM706R in that the reset threshold is 2.63 V. It differs only in that it has an active high reset output.

The CBM708R/CBM708S/CBM708T provide similar functio-nality as the CBM706R/ CBM706S/ CBM706T and only differ in that a watchdog timer function is not available. Instead, an active high reset output (RESET) is provided in addition to the active low (RESET) output.

All devices are available in narrow 8-lead MSOP and 8-lead SOP packages.

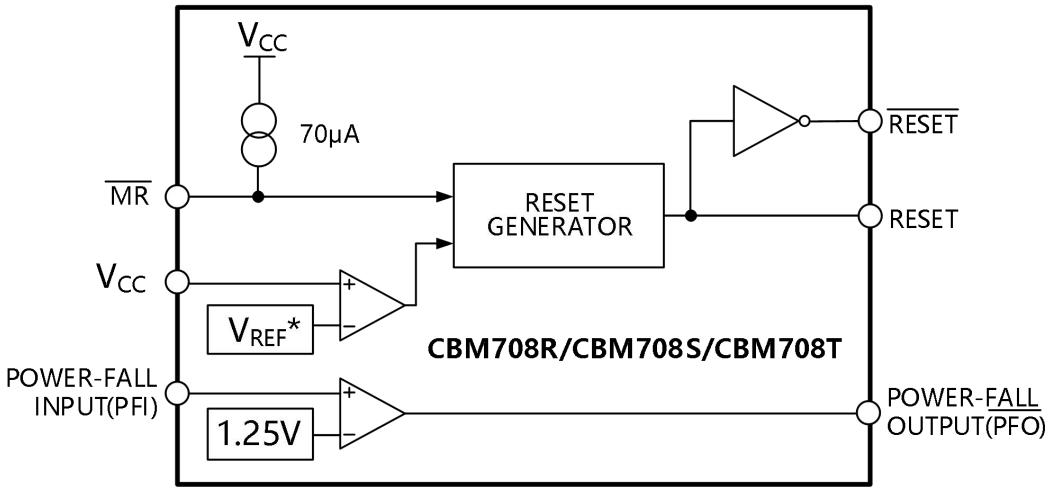
CATALOG

Functional Block Diagrams



*VOLTAGE REFERENCE = 2.63V (P/R), 2.93V (S), 3.08V (T)

Figure 1. CBM706P/CBM706R/CBM706S/CBM706T



* VOLTAGE REFERENCE = 2.63V (R), 2.93V (S), 3.08V (T)

Figure 2. CBM708R/CBM708S/CBM708T

Specifications

V_{CC} = 2.70 V to 5.5 V (CBM706P/CBM706R/CBM708R), V_{CC} = 3.0 V to 5.5 V (CBM70XS), V_{CC} =3.15 V to 5.5 V (CBM70XT), T_A = T_{MIN} to T_{MAX} unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		100	500	μA	V_{CC} < 3.6 V
			500	μA	V_{CC} < 5.5 V
LOGIC OUTPUT					
Reset Threshold(V_{RST})	2.55	2.63	2.70	V	CBM706P/CBM706R/CBM708R
	2.85	2.93	3.00	V	CBM706S/CBM708S
	3.00	3.08	3.15	V	CBM706T/CBM708T
Reset Threshold Hysteresis		20		mV	
Reset Pulse Width	160	200	280	ms	CBM706P/CBM706R/CBM708R, V_{CC}=3V
					V_{CC} = 3.3 V
		200		ms	V_{CC} = 5.0 V
RESET OUTPUT VOLTAGE (CBM706R/CBM708R/CBM706S/CBM708S/CBM706T/CBM708T)					
V_{OH}	0.8 × V_{CC}			V	V_{RST}(max)<V_{CC}<3.6V, I_{SOURCE}=500μA
V_{OL}			0.3	V	V_{RST}(max)<V_{CC}<3.6V, I_{SINK} = 1.2mA
V_{OH}	V_{CC}−1.5V			V	4.5V<V_{CC}<5.5V, I_{SOURCE} = 800μA
V_{OL}			0.4	V	4.5V<V_{CC}<5.5V, I_{SINK} = 3.2 mA
V_{OL}			0.3	V	V_{CC}=1V, I_{SINK} = 100μA
RESET OUTPUT VOLTAGE (CBM706P)					
V_{OH}	V_{CC}−0.6 V			V	V_{RST}(max)<V_{CC}<3.6V, I_{SOURCE}=215μA
V_{OL}			0.3	V	V_{RST}(max)<V_{CC}<3.6V, I_{SINK}=1.2mA
V_{OH}	V_{CC}−1.5V			V	4.5V<V_{CC}<5.5V, I_{SOURCE}=800μA
V_{OL}			0.4	V	4.5V<V_{CC}<5.5V, I_{SINK}=3.2mA
RESET OUTPUT VOLTAGE (CBM708R/CBM708S/CBM708T)					
V_{OH}	0.8 × V_{CC}			V	V_{RST}(max)<V_{CC}<3.6V, I_{SOURCE}=500μA

V_{OL}			0.3	V	V_{RST}(max)<V_{CC}<3.6V, I_{SINK}=500μA
V_{OH}	V_{CC}−1.5V			V	4.5V<V_{CC}<5.5V, I_{SOURCE}=800μA
V_{OL}			0.4	V	4.5V<V_{CC}<5.5V, I_{SINK}=1.2mA
WATCHDOG INPUT (CBM706P/CBM706R/CBM706S/CBM706T)					
Watchdog Timeout Period	1.00	1.60	2.25	sec	CBM706P/CBM706R: V_{CC}=3V
					CBM706S/CBM706T: V_{CC}=3.3V
					V_{IL}=0.4V, V_{IH}=V_{CC}×0.8 V
WDI Pulse Width	100			ns	V_{RST}(max)<V_{CC}<3.6 V
	50			ns	4.5V<V_{CC}<5.5 V
WDI Input Threshold					
V_{IL}			0.6	V	V_{RST}(max)<V_{CC}<3.6V
V_{IH}	0.7 × V_{CC}			V	V_{RST}(max)<V_{CC}<3.6V
V_{IL}			0.8	V	V_{CC}=5.0V
V_{IH}	3.5			V	V_{CC}=5.0V
WDI Input Current	-1.0	-0.63	1.0	μA	WDI=0V
	-10	16.5	20	μA	WDI=V_{CC}
WDO OUTPUT VOLTAGE					
V_{OH}	0.8×V_{CC}			V	V_{RST}(max)<V_{CC}<3.6V, I_{SOURCE}=500μA
	V_{CC}−1.5V			V	4.5V<V_{CC}<5.5V, I_{SOURCE}=800μA
V_{OL}			0.3	V	V_{RST}(max)<V_{CC}<3.6V, I_{SINK}=500μA
			0.6	V	4.5V<V_{CC}<5.5V, I_{SINK}=1.2mA
MANUAL RESET INPUT					
MR Pull-Up Current (MR=0V)	25	70	250	μA	V_{RST}(max)<V_{CC}<3.6V
	100	250	600	μA	4.5V<V_{CC}<5.5V
MR Pulse Width	500			ns	V_{RST}(max)<V_{CC}<3.6V
	150			ns	4.5V<V_{CC}<5.5V
MR INPUT THRESHOLD					
V_{IL}			0.6	V	V_{RST}(max)<V_{CC}<3.6V
V_{IH}	0.7×V_{CC}			V	V_{RST}(max)<V_{CC}<3.6V
V_{IL}			0.8	V	4.5V<V_{CC}<5.5V
V_{IH}	2.0			V	4.5V<V_{CC}<5.5V
MR To Reset Output Delay			750	ns	V_{RST}(max)<V_{CC}<3.6V

			250	ns	4.5V<V_{CC}<5.5V
POWER FAIL INPUT					
PFI Input Threshold	1.2	1.25	1.3	V	CBM706P/CBM706R/CBM708R, V_{CC}=3V CBM706S/CBM708S/CBM706T/CBM708T,
PFI Input Current	-25	+0.01	+25	nA	V_{CC}=3.3V, PFI falling
PFO OUTPUT VOLTAGE					
V_{OH}	0.8×V_{CC}			V	V_{RST}(max)<V_{CC}<3.6V, I_{SOURCE}=500μA
V_{OL}			0.3	V	V_{RST}(max)<V_{CC}<3.6V, I_{SINK}=1.2mA
V_{OH}	V_{CC}−1.5V			V	4.5V<V_{CC}<5.5V, I_{SOURCE}=800μA
V_{OL}			0.4	V	4.5V<V_{CC}<5.5V, I_{SINK}=3.2mA

Absolute Maximum Ratings

T_A = 25°C, unless otherwise noted.

Table 2

Parameter	Rating
V_{CC}	−0.3 V to +6 V
All Other Inputs	−0.3V to V_{CC}+0.3V
Input Current	
V_{CC}	20mA
GND	20mA
Digital Output Current	20mA
Power Dissipation, N-8 PDIP	727mW
θ_{JA} Thermal Impedance	135℃/W
Power Dissipation, R-8 SOIC	470mW
θ_{JA} Thermal Impedance	110℃/W
Operating Temperature Range	
Industrial (Version A)	-40℃ to +85℃
Lead Temperature (Soldering,10 sec)	300℃
Vapor Phase (60 sec)	215℃
Infrared (15 sec)	220℃
Storage Temperature Range	-65℃ to +150℃
ESD Rating	>4.5kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD SENSIYIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Pin Configurations And Function Descriptions

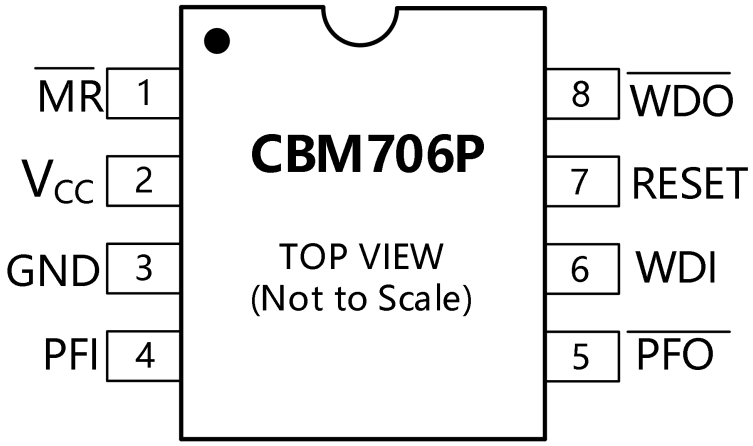


Figure 3. CBM706P

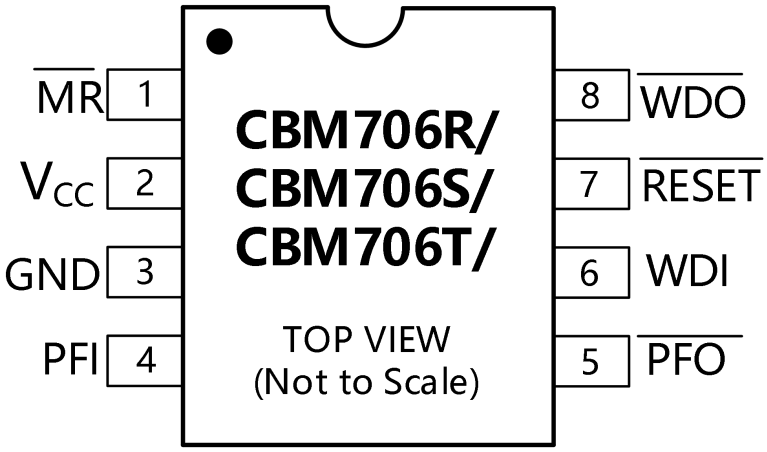


Figure 4. CBM706R/CBM706S/CBM706T

Table3. (CBM706P/CBM706R/CBM706S/CBM706T)

Pin No.	Mnemonic	Description
1	$\overline{MR}$	Manual Reset Input. When to ken below 0.6 V, a RESET/$\overline{RESET}$ is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch because it is internally debounced. An internal 70 IJA pull-up current holds the input High when floating.
2	V_{CC}	Power Supply Input. Place a 0.lμF decoupling capacitor between the Vcc and GND pins.
3	GND	Ground. Ground reference for all signals (0V).
4	PFI	Power Fail Input. PFI is the noninverting input to the power fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI connects to GND.
5	$\overline{PFO}$	Power Fail Output. $\overline{PFO}$ is the output from the power fail comparator. It goes low when PFl is less than 1.25 V.
6	WDI	Watchdog Input. lf WDI remains either High or low for longer than the watchdog timeout period, the watchdog output, $\overline{WDO}$, goes low. The timer resets with each transition at the WDl input. Either a high to low or a low to high transition clears the counter.The internal timer is also cleared whenever reset is asserted.
7(CBM706R/CBM706S/ ADM706T Only)	$\overline{RESET}$	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It is triggered either by Vcc being below the reset threshold or by a low signal on the $\overline{MR}$ input. $\overline{RESET}$ remains low whenever Vcc is below the reset threshold. lt remains low for 200ms after Vcc goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to MR.
7(CBM706P Only)	RESET	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{RESET}$.
8	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low if the internal watchdog timer times out as a result of inactivity on the WDI input. lt remains low until the watchdog timer is cleared $\overline{WDO}$ also goes low during low line conditions. Whenever Vcc is below the reset threshold, $\overline{WDO}$ remains low. As soon as Vcc goes above the reset threshold, $\overline{WDO}$ goes high immediately.

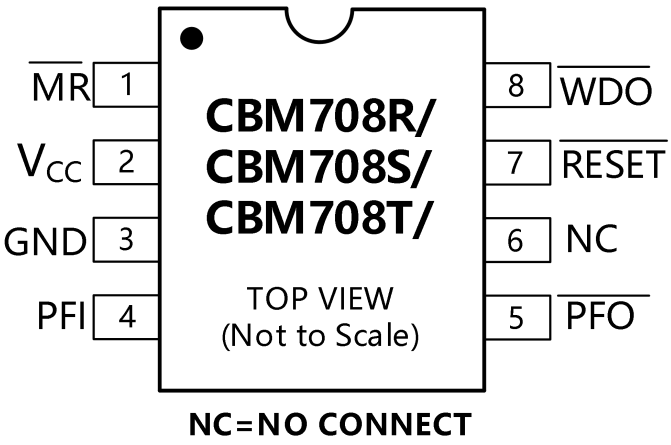


Figure 5. CBM708R/CBM708S/CBM708T

Table 4. (CBM708R/CBM708S/CBM708T)

Pin No.	Mnemonic	Description
1	$\overline{MR}$	Manual Reset Input. When taken below 0.6V, a RESET/ $\overline{RESET}$ is generated. $\overline{MR}$ can be driven from TTL, CMOS logic, or from a manual reset switch because it is internally debounced. An internal 70 UA pull-up current holds the input high when floating.
2	V_{CC}	Power Supply Input. Place a 0.1 μF decoupling capacitor between the Vcc and GND pins.
3	GND	Ground. Ground reference for all signals (0V).
4	PFI	Power Fail Input. PFI is the noninverting input to the power fail comparator. When PFI is less than 1.25 V, $\overline{PFO}$ goes low. If unused, PFI connects to GND.
5	$\overline{PFO}$	Power Fail Output. $\overline{PFO}$ is the output from the power fail comparator. It goes low when PFI is less than 1.25 V.
6	NC	No Connect.
7	$\overline{RESET}$	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It is triggered either by Vcc being below the reset threshold or by a low signal on the $\overline{MR}$ input. $\overline{RESET}$ remains low whenever Vcc is below the reset threshold. It remains low for 200ms after Vcc goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout does not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to MR.
8	RESET	Logic Output. RESET is an active high output suitable for systems that use active high reset logic. It is the inverse of $\overline{RESET}$.

Typical Performance Characteristics

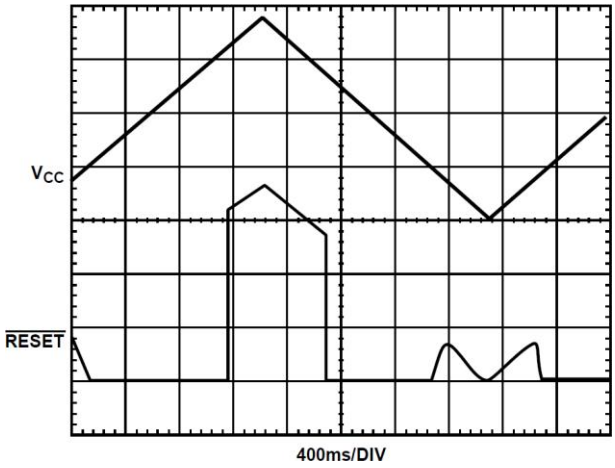


Figure 6. CBM706R/CBM706S/CBM706T and the CBM708R/CBM708S/CBM708T RESET Output Voltage vs. Supply Voltage

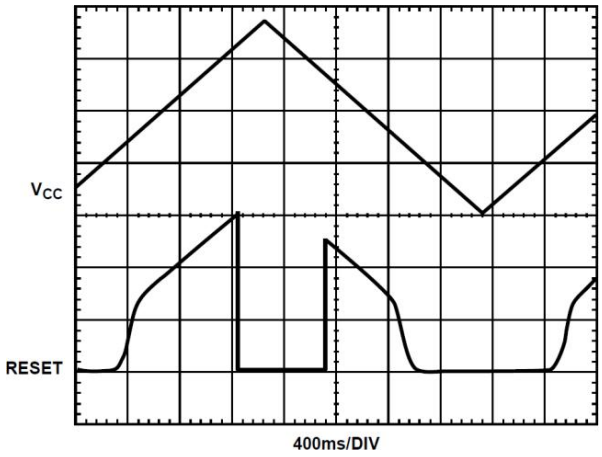


Figure 7. RESET Output Voltage vs. Supply Voltage

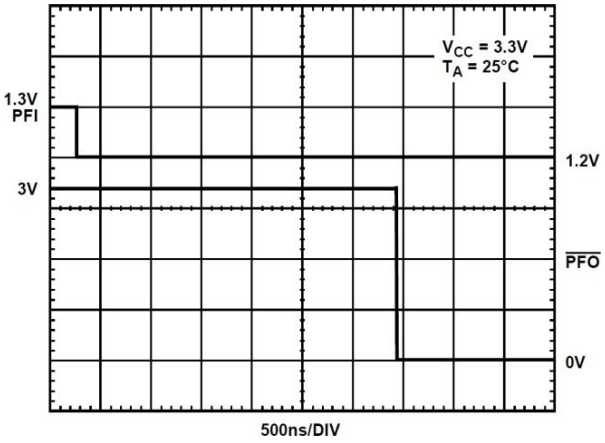


Figure 8. PFI Assertion Response Time

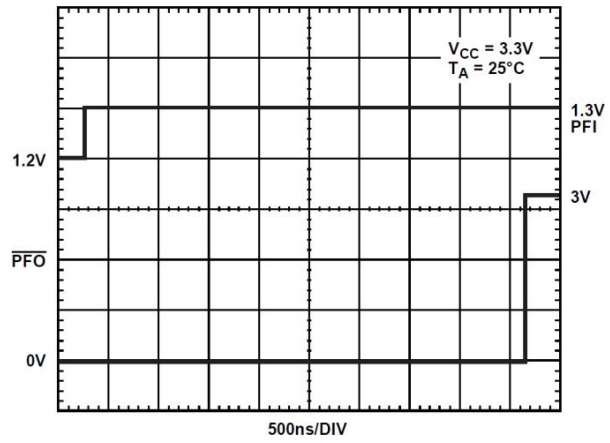


Figure 9. PFI Deassertion Response Time

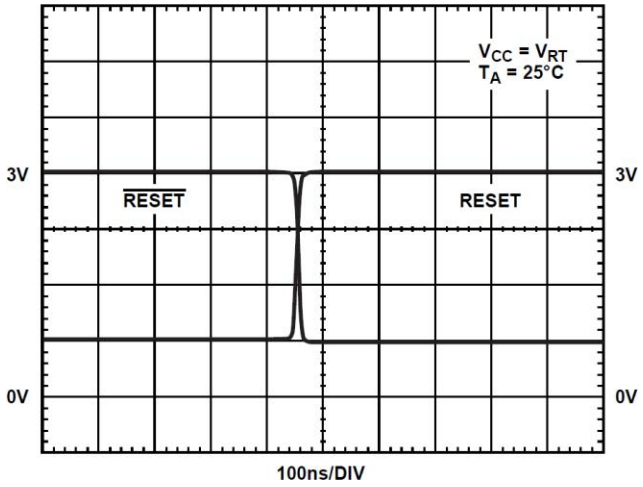


Figure 10. RESET, RESET Assertion

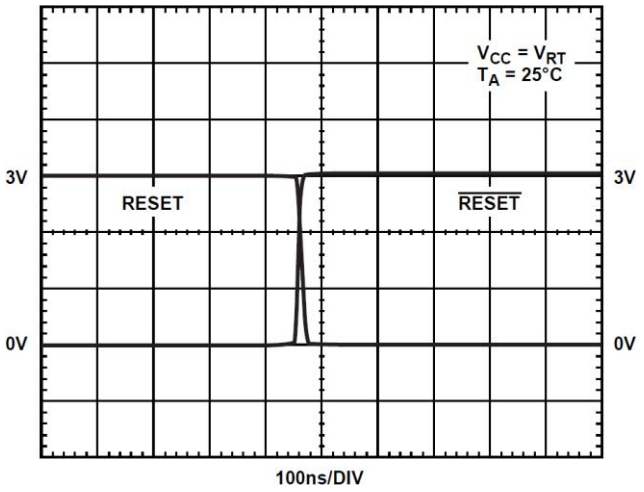


Figure 11. RESET, RESET Deassertion

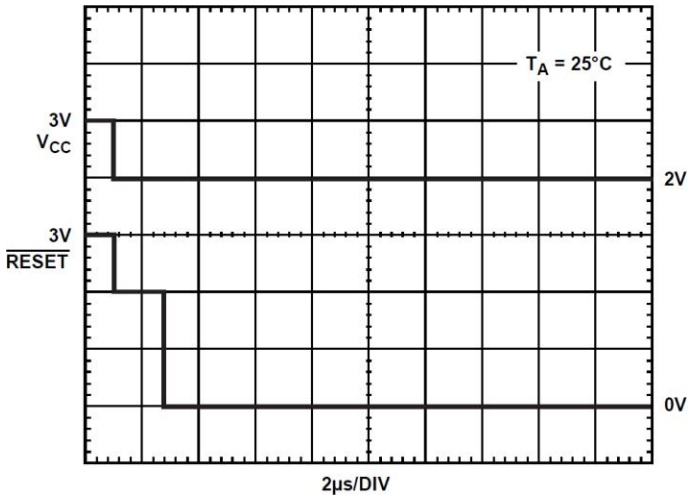
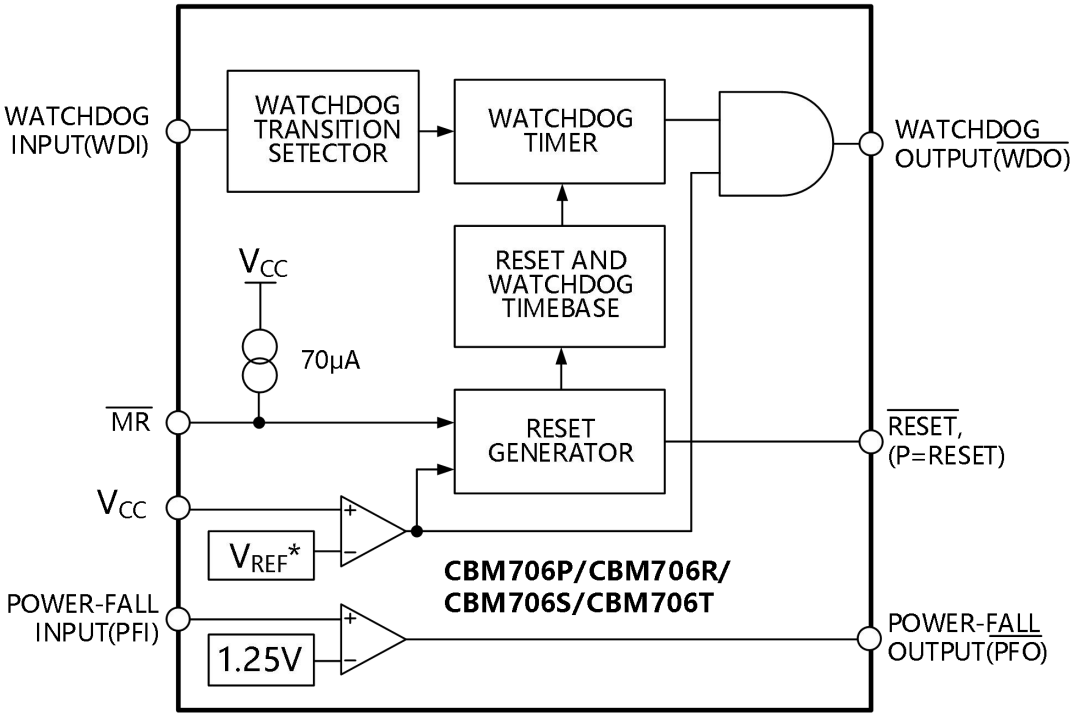


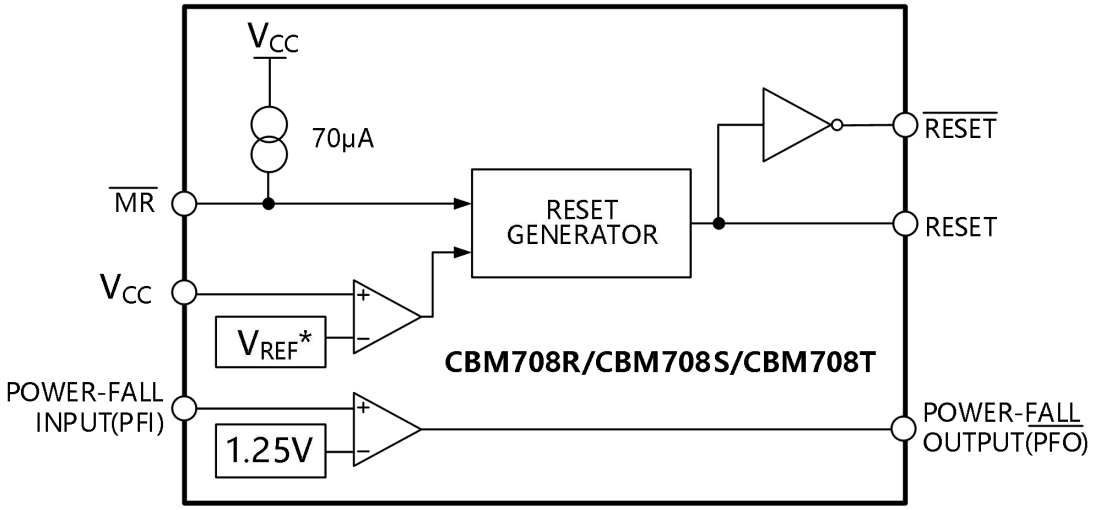
Figure 12. CBM706R/CBM706S/CBM706T
and the CBM708R/CBM708S/CBM708T
RESET Response

● Circuit Information



*VOLTAGE REFERENCE = 2.63V (P/R), 2.93V (S), 3.08V (T)

Figure 13. CBM706P/CBM706R/CBM706S/CBM706T Functional Block Diagram



* VOLTAGE REFERENCE = 2.63V (R), 2.93V (S), 3.08V (T)

Figure 14. CBM708R/CBM708S/CBM708T Functional Block Diagram

- **Power Fail Reset Output**

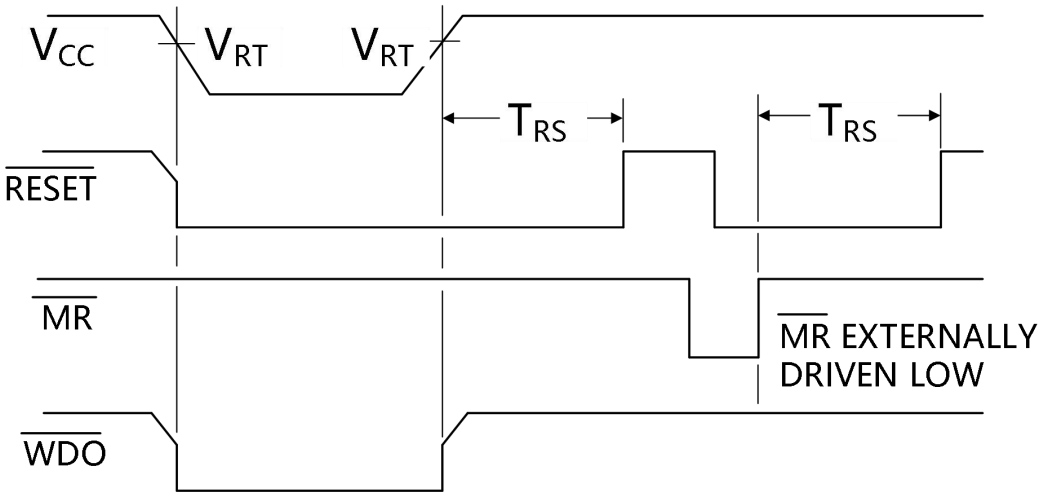
The reset output provides a reset (RESET or RESET) output signal to the microprocessor whenever the VCC input is below the reset threshold. The actual reset threshold voltage is dependent on whether a P, R, S, or T suffix device is used. An internal timer holds the reset output active for 200 ms after the voltage on VCC rises above the threshold. This is intended as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset line is similarly activated and remains active for 200 ms after the supply recovers. If another interruption occurs during an active reset period, the reset timeout period continues for an additional 200 ms.

The reset output is guaranteed to remain valid with VCC as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply starts up.

The CBM706P provides an active high RESET signal; the CBM706R/CBM706S/CBM706T provide an active low RESET signal; and the CBM708R/CBM706S/CBM706T provide both RESET and RESET.

- **Manual Reset**

The MR input allows other reset sources, such as a manual reset switch, to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typical). The MR input is TTL-/CMOS-compatible; it can also be driven by any logic reset output. If unused, the MR input can be tied high or left floating.



NOTES: RESET = COMPLEMENT OF RESET

Figure 15. RESET, MR, and WDO Timing

- **Watchdog Timer (CBM706P/CBM706R/ CBM706S/CBM706T)**

The watchdog timer circuit monitors the activity of the microprocessor to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the watchdog input (WDI) line. If this line is not toggled within the timeout period (1.6 sec), the watchdog output (WDO) is driven low. The WDO output is connected to a nonmaskable interrupt (NMI) on the processor. Therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine is used to rectify the problem.

The watchdog timer is cleared either by a high to low or by a low to high transition on WDI. Pulses as narrow as 50 ns are detected. The timer is also cleared by RESET/RESET going active. Therefore, the watchdog timeout period begins after reset goes inactive.

When VCC falls below the reset threshold, WDO is forced low whether or not the watchdog timer has timed out. Normally, this generates an interrupt, but it is overridden by RESET/RESET going active.

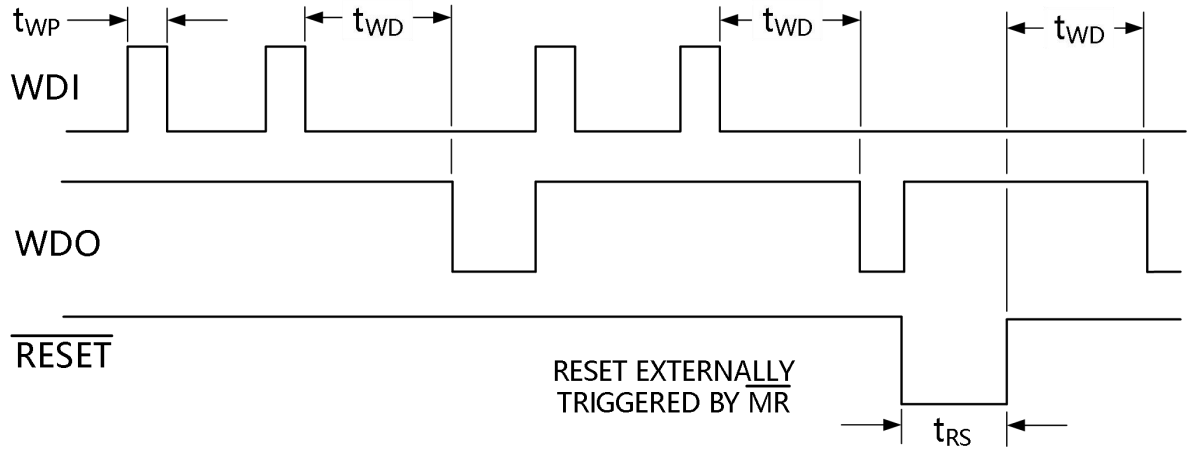


Figure 16. Watchdog Timing

- **Power Fail Comparator**

The power fail comparator is an independent comparator that monitors the input power supply. The inverting input of the comparator internally connects to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input monitors the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output (PFO) goes low, indicating a power failure. For early warning of power failure, the comparator monitors the preregulator input by choosing an appropriate resistive divider network. The PFO output interrupts the processor to implement a shutdown procedure before the power is lost.

As the voltage on the PFI pin is limited to V_{CC} + 0.3 V, it is recommended to connect the PFI pin with a Schottky diode to the RESET pin, as shown in Figure 17. This helps with clamping the PFI pin voltage during device power up and operation.

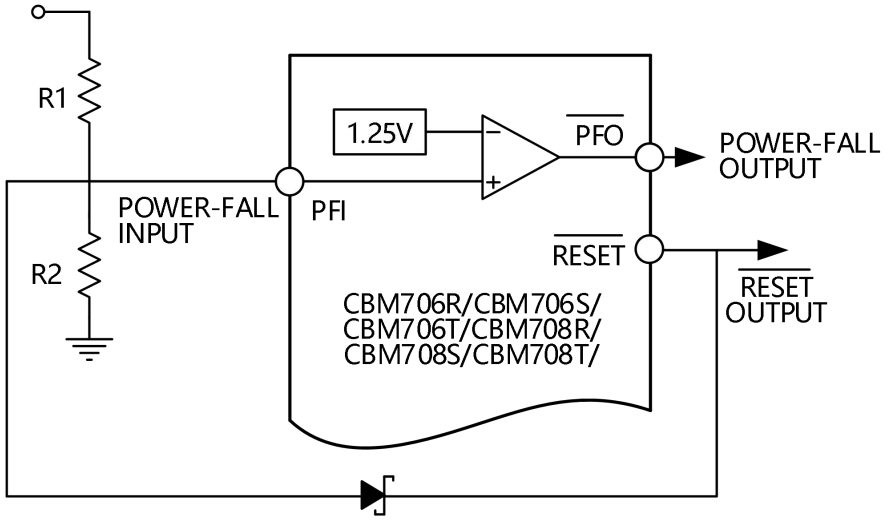


Figure 17. Power Fail Comparator

- **Adding Hysteresis To The Power Fail Comparator**

For increased noise immunity, hysteresis can be added to the power fail comparator. Because the comparator circuit is non-inverting, hysteresis is added simply by connecting a resistor between the PFO output and the PFI input as shown in Figure 18. When PFO is low, Resistor R3 sinks current from the summing junction at the PFI pin. When PFO is high, Resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity is achieved by connecting a capacitor between PFI and GND.

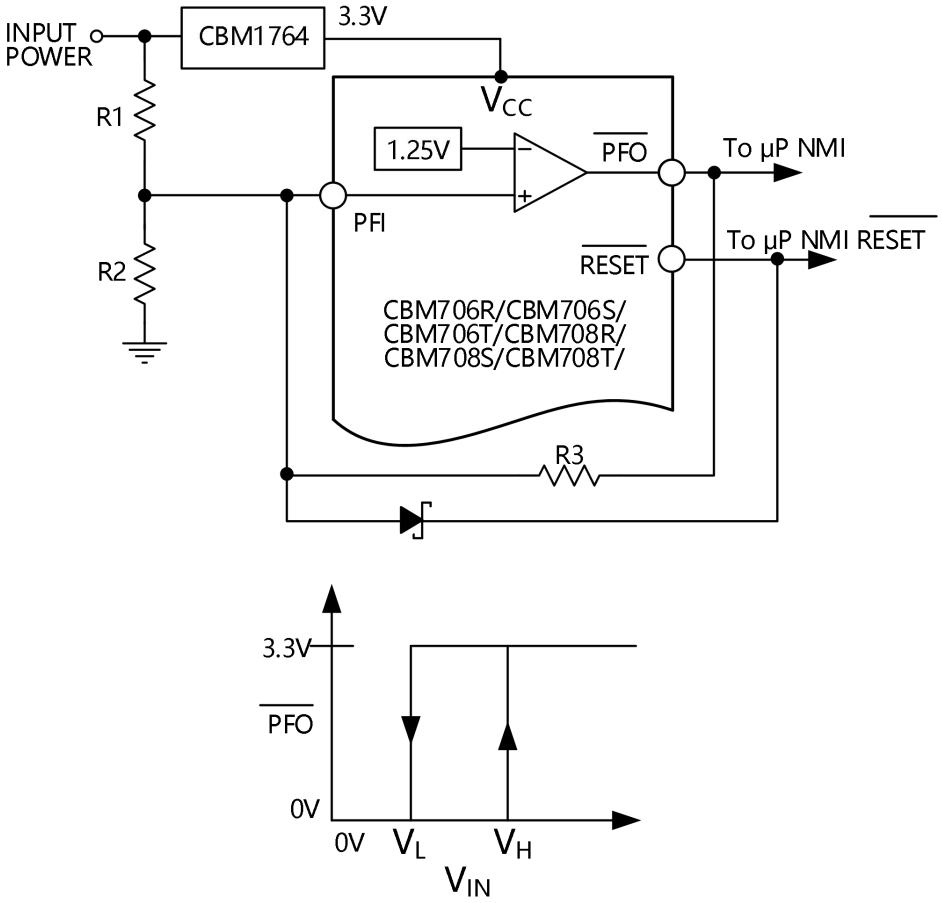


Figure 18. Adding Hysteresis to the Power Fail Comparator

$$V_H = 1.25[1 + \left(\frac{R2 + R3}{R2 \times R3}\right) R1]$$

$$V_L = 1.25 + R1\left(\frac{1.25}{R2} - \frac{V_{CC} - 1.25}{R3}\right)$$

$$V_{MID} = 1.25(\frac{R1 + R2}{R2})$$

- **Valid Reset Below 1V VCC**

The CBM706R/CBM706S/CBM706T, CBM708R/CBM708S/ CBM708T are guaranteed to provide a valid reset level with V_{CC} as low as 1 V. Refer to the Typical Performance Characteristics section. As V_{CC} drops below 1 V, the internal transistor does not have sufficient drive to hold it on so the voltage on RESET is no longer held at 0 V. A pull-down resistor, as shown in Figure 19, can connect externally to hold the line low if it is required.

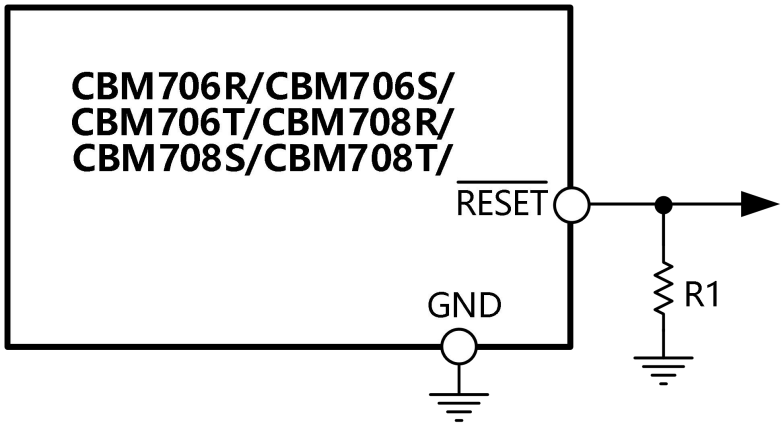


Figure 19. RESET Valid Below 1V

- **Applications Information**

A typical operating circuit is shown in Figure 20. The unregulated dc input supply is monitored using the PFI input via the resistive divider network. Resistor R1 and Resistor R2 are to be selected so that when the supply voltage drops below the desired level (for example, 5 V), the voltage on PFI drops below the 1.25 V threshold, thereby generating an interrupt to the microprocessor. Monitoring the preregulator input gives additional time to execute an orderly shutdown procedure before power is lost.

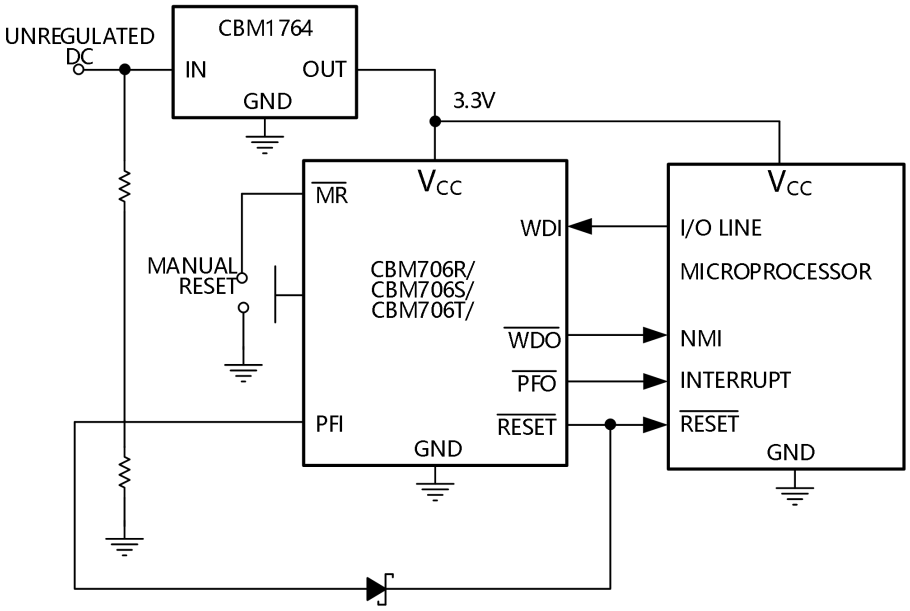


Figure 20. Typical Application Circuit

Microprocessor activity is monitored using the WDI input. This is driven using an output line from the processor. The software routines toggle this line at least once every 1.6 sec. If a problem occurs and this line is not toggled, WDO goes low and a nonmask-able interrupt is generated. This interrupt routine is to be used to clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, the WDO output is to be connected to the input as shown in Figure 21.

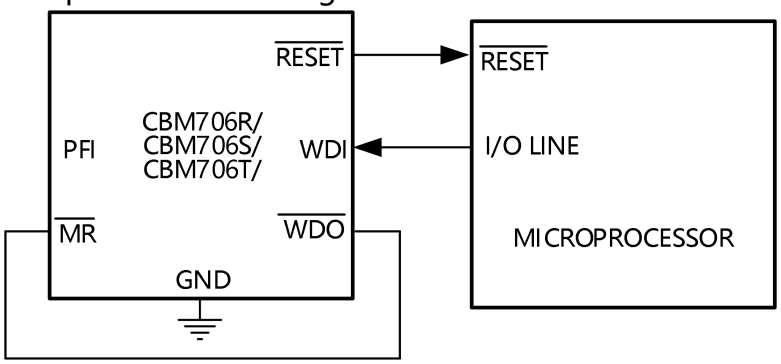


Figure 21. RESET From WDO

- **Monitoring Additional Supply Levels**

It is possible to use the power fail comparator to monitor a second supply as shown in Figure 22. The two sensing resistors, R1 and R2, are selected such that the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. The PFO output can connect to the MR input so a reset generates when the supply drops out of tolerance. In this case, if either supply drops out of tolerance, a reset is generated.

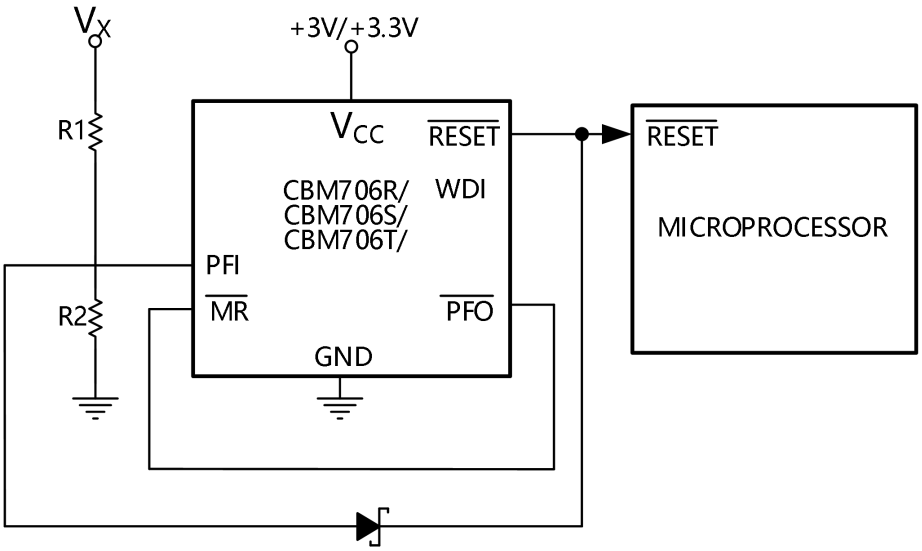


Figure 22. Monitoring 3 V/3.3 V and an Additional Supply V_X

- **Microppocessor With Bidirectional Reset**

To prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor is to be inserted between the CBM706R/CBM706S/CBM706T, CBM708R/CBM708S/ CBM708T RESET output pin and the microprocessor reset pin. This limits the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, it must be buffered as shown in Figure 23.

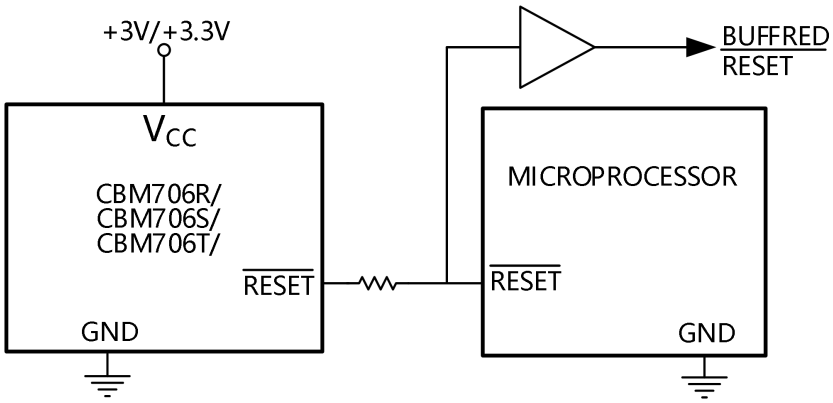
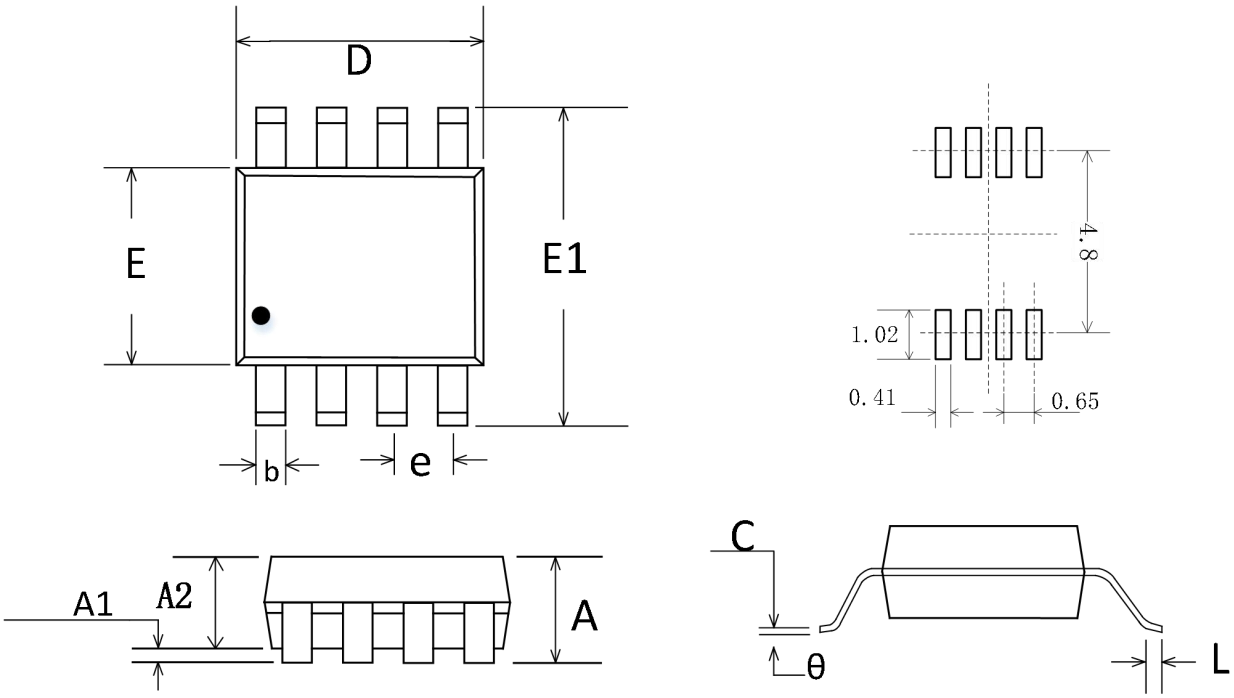


Figure 23. Bidirectional Input/Output RESET

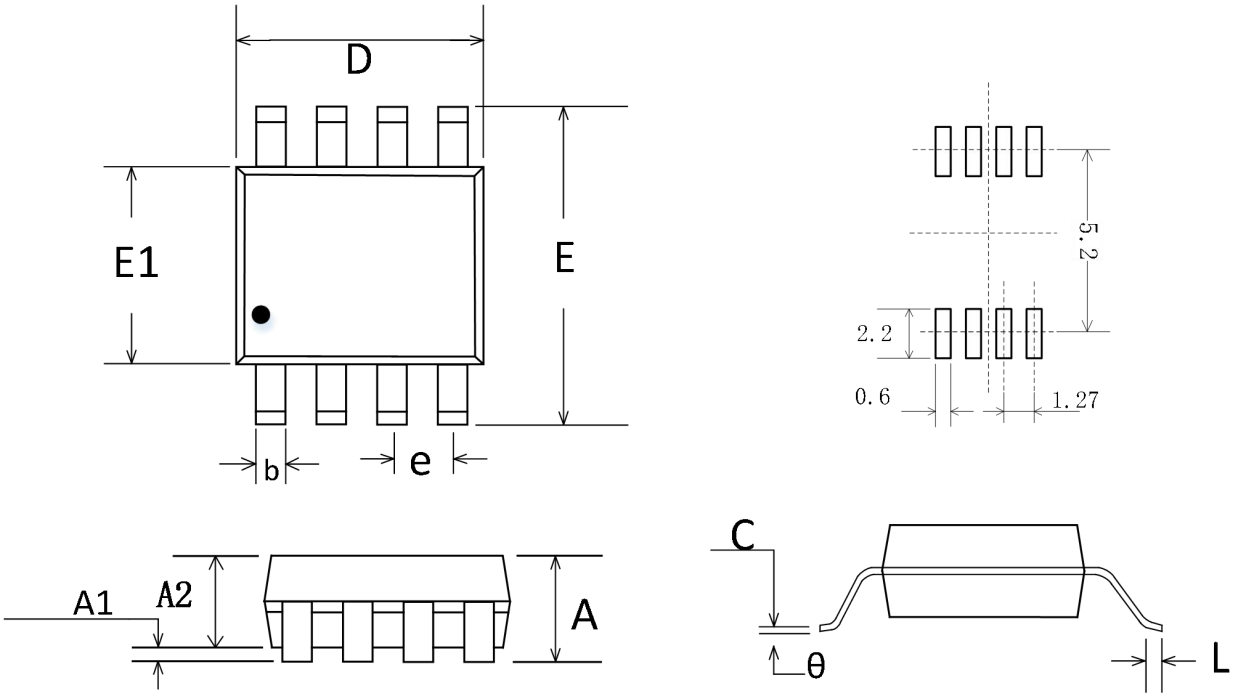
Package Information

MSOP-8



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

SOIC-8(SOP8)



Symbol	Dimensions In Millimeters		Dimensions Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package/Ordering Information

PRODUCT	ORDERING NUMBER	TEMPRANGE	PACKAGE	PAKEAGE MARKING	TRANSPOT MEDIA,QUANTILY
CBM706P	CBM706PAS8	-40℃~85℃	SOIC-8(SOP8)	CBM706P	Tape and Reel, 2500
	CBM706PAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM706P	Tape and Reel, 3000
	CBM706PAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM706P	Tape and Reel, 4000
	CBM706PMS8	-40℃~85℃	MSOP-8	706PM	Tape and Reel, 3000
CBM706R	CBM706RAS8	-40℃~85℃	SOIC-8(SOP8)	CBM706R	Tape and Reel, 2500
	CBM706RAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM706R	Tape and Reel, 3000
	CBM706RAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM706R	Tape and Reel, 4000
	CBM706RMS8	-40℃~85℃	MSOP-8	706RM	Tape and Reel, 3000
CBM706S	CBM706SAS8	-40℃~85℃	SOIC-8(SOP8)	CBM706S	Tape and Reel, 2500
	CBM706SAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM706S	Tape and Reel, 3000
	CBM706SAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM706S	Tape and Reel, 4000
	CBM706SMS8	-40℃~85℃	MSOP-8	706SM	Tape and Reel, 3000
CBM706T	CBM706TAS8	-40℃~85℃	SOIC-8(SOP8)	CBM706T	Tape and Reel, 2500
	CBM706TAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM706T	Tape and Reel, 3000
	CBM706TAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM706T	Tape and Reel, 4000
	CBM706TMS8	-40℃~85℃	MSOP-8	706TM	Tape and Reel, 3000
CBM708R	CBM708RAS8	-40℃~85℃	SOIC-8(SOP8)	CBM708R	Tape and Reel, 2500
	CBM708RAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM708R	Tape and Reel, 3000
	CBM708RAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM708R	Tape and Reel, 4000
	CBM708RMS8	-40℃~85℃	MSOP-8	708RM	Tape and Reel, 3000
CBM708T	CBM708TAS8	-40℃~85℃	SOIC-8(SOP8)	CBM708T	Tape and Reel, 2500
	CBM708TAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM708T	Tape and Reel, 3000
	CBM708TAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM708T	Tape and Reel, 4000
	CBM708TMS8	-40℃~85℃	MSOP-8	708TM	Tape and Reel, 3000

CBM708S	CBM708SAS8	-40℃~85℃	SOIC-8(SOP8)	CBM780S	Tape and Reel, 2500
	CBM708SAS8-RL	-40℃~85℃	SOIC-8(SOP8)	CBM780S	Tape and Reel, 3000
	CBM708SAS8-REEL	-40℃~85℃	SOIC-8(SOP8)	CBM780S	Tape and Reel, 4000
	CBM708SMS8	-40℃~85℃	MSOP-8	708SM	Tape and Reel, 3000