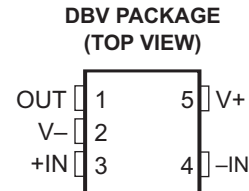


# 1.8-V MICROPOWER CMOS OPERATIONAL AMPLIFIER ZERO-DRIFT SERIES

Check for Samples: [OPA333-Q1](#)

## FEATURES

- Qualified for Automotive Applications
- Low Offset Voltage: 10  $\mu\text{V}$  (Max)
- 0.01-Hz to 10-Hz Noise: 1.1  $\mu\text{V}_{\text{PP}}$
- Quiescent Current: 17  $\mu\text{A}$
- Single-Supply Operation
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input/Output
- MicroSize SOT23 (DBV) Package

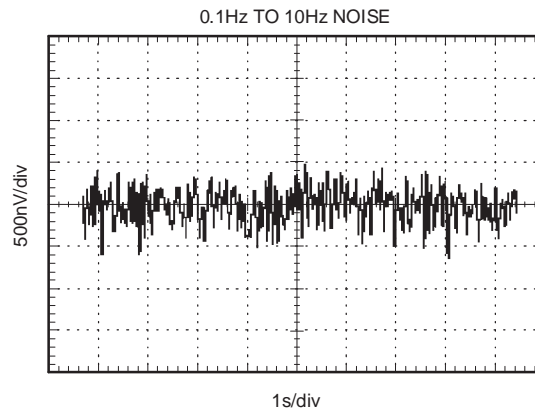


## DESCRIPTION/ORDERING INFORMATION

The OPA333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10  $\mu\text{V}$  max) and near-zero drift over time and temperature. These miniature, high-precision, low-quiescent-current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as 1.8 V ( $\pm 0.9$  V) and up to 5.5 V ( $\pm 2.75$  V) may be used. They are optimized for low-voltage single-supply operation.

The OPA333 family offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

The OPA333 (single version) is available in the SOT23-5 package.



## ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOT23 – DBV	Reel of 2500	OPA333QDBVRQ1	QCNQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage		7	V
Signal input terminals, voltage <sup>(2)</sup>	-0.3	(V+) + 0.3	V
Output short circuit <sup>(3)</sup>		Continuous	
Operating temperature range	-40	125	°C
Storage temperature range	-65	150 <sup>(4)</sup>	°C
Junction temperature		150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short circuit to ground, one amplifier per package
- (4) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

**ELECTRICAL CHARACTERISTICS:  $V_S = 1.8\text{ V to }5.5\text{ V}$** 
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ .

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$ ,  $V_{CM} = V_S/2$ ,  $V_{OUT} = V_S/2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>					
Input offset voltage	$V_{OS}$ $V_S = 5\text{ V}$		2	10	$\mu\text{V}$
<b>vs temperature</b>	$dV_{OS}/dT$ $V_S = 5\text{ V}$		<b>0.5</b>		$\mu\text{V}/^\circ\text{C}$
<b>vs power supply</b>	<b>PSRR</b> $V_S = 1.8\text{ V to }5.5\text{ V}$		<b>1</b>	<b>6</b>	$\mu\text{V/V}$
Long-term stability <sup>(1)</sup>			(1)		
Channel separation, dc			0.1		$\mu\text{V/V}$
<b>INPUT BIAS CURRENT</b>					
Input bias current	$I_B$		$\pm 70$	$\pm 200$	$\text{pA}$
<b>over Temperature</b>			<b><math>\pm 200</math></b>		<b><math>\text{pA}</math></b>
Input offset current	$I_{OS}$		$\pm 140$	$\pm 400$	$\text{pA}$
<b>NOISE</b>					
Input voltage noise, $f = 0.01\text{ Hz to }1\text{ Hz}$			0.3		$\mu\text{V}_{PP}$
Input voltage noise, $f = 0.1\text{ Hz to }10\text{ Hz}$			1.1		$\mu\text{V}_{PP}$
Input current noise, $f = 10\text{ Hz}$	$i_n$		100		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b>					
Common mode voltage range	$V_{CM}$	$(V-) - 0.1$		$(V+) + 0.1$	V
<b>Common-Mode Rejection Ratio</b>	<b>CMRR</b> $(V-) - 0.1\text{ V} < V_{CM} < (V+) + 0.1\text{ V}$	<b>106</b>	<b>130</b>		<b>dB</b>
<b>INPUT CAPACITANCE</b>					
Differential			2		pF
Common mode			4		pF
<b>OPEN-LOOP GAIN</b>					
Open-loop voltage gain	$A_{OL}$ $(V-) + 100\text{ mV} < V_O < (V+) - 100\text{ mV},$ $R_L = 10\text{ k}\Omega$	<b>106</b>	<b>130</b>		<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain-bandwidth product	GBW $C_L = 100\text{ pF}$		350		kHz
Slew rate	SR $G = 1$		0.16		$\text{V}/\mu\text{s}$
<b>OUTPUT</b>					
Voltage output swing from rail	$R_L = 10\text{ k}\Omega$		30	50	mV
<b>over temperature</b>	<b><math>R_L = 10\text{ k}\Omega</math></b>			<b>85</b>	<b>mV</b>
Short-circuit current	ISC		$\pm 5$		mA
Capacitive load drive	CL				
<sup>(2)</sup> Open-loop output impedance	$f = 350\text{ kHz}, I_O = 0$		2		k $\Omega$
<b>POWER SUPPLY</b>					
Specified voltage range	$V_S$	1.8		5.5	V
Quiescent current per amplifier	$I_Q$ $I_O = 0$		17	25	$\mu\text{A}$
<b>over temperature</b>				<b>30</b>	<b><math>\mu\text{A}</math></b>
Turn-on time	$V_S = 5\text{ V}$		100		$\mu\text{s}$

(1) 300-hour life test at  $150^\circ\text{C}$  demonstrated randomly distributed variation of approximately  $1\ \mu\text{V}$ .

(2) See Typical Characteristics

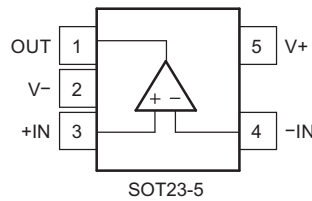
**ELECTRICAL CHARACTERISTICS:  $V_S = 1.8\text{ V to }5.5\text{ V}$  (continued)**

**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ\text{C to }125^\circ\text{C}$ .

At  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S/2$ ,  $V_{CM} = V_S/2$ ,  $V_{OUT} = V_S/2$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TEMPERATURE RANGE</b>					
Specified range		-40		125	°C
Operating range		-40		125	°C
Storage range		-65		150	°C
Thermal resistance	$\theta_{JA}$				
SOT23-5			200		°C/W

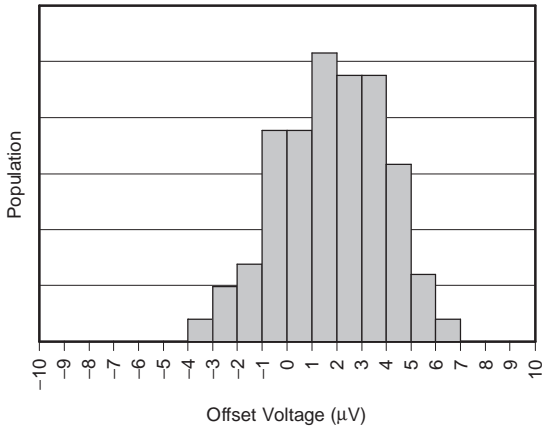
**PIN CONFIGURATION**



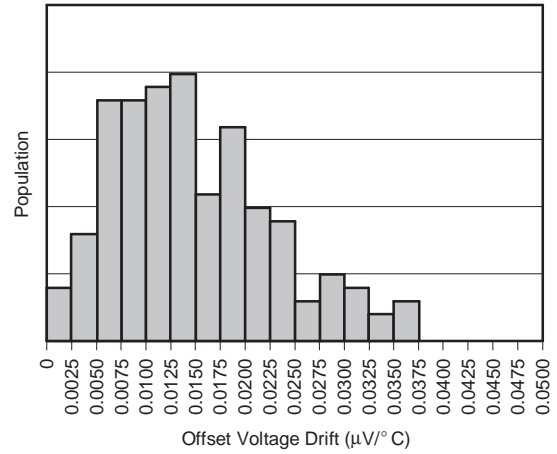
TYPICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{ V}$ , and  $C_L = 0\text{ pF}$  (unless otherwise noted)

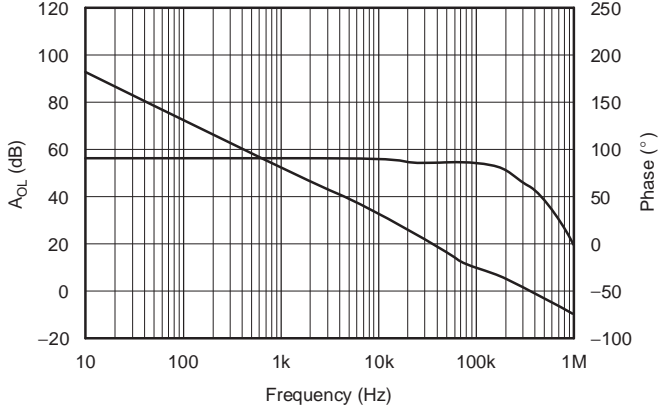
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



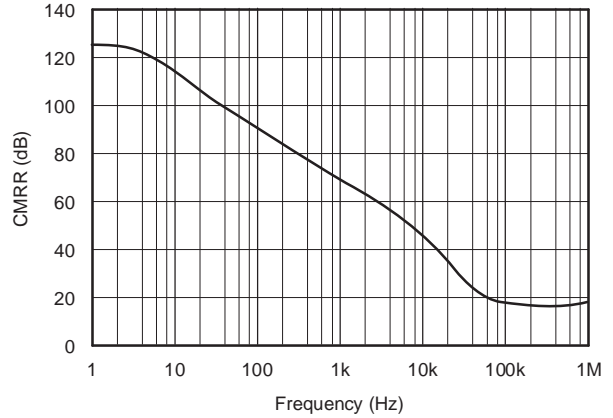
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



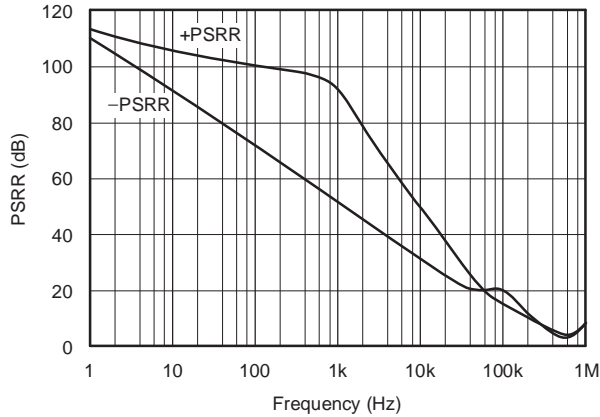
OPEN-LOOP GAIN vs FREQUENCY



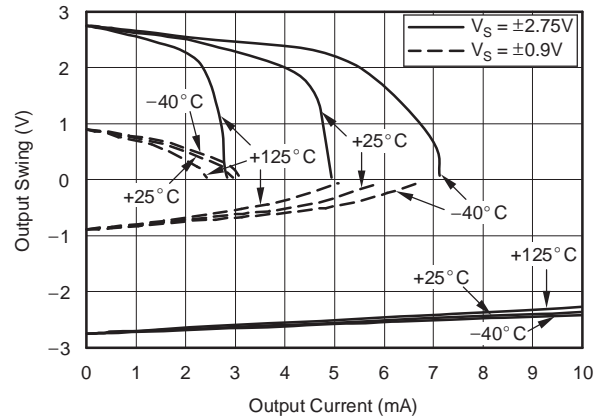
COMMON-MODE REJECTION RATIO vs FREQUENCY



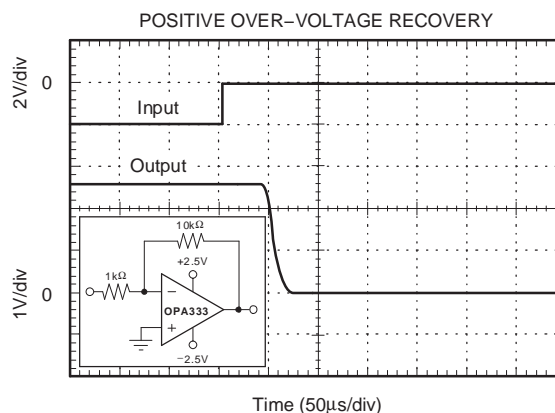
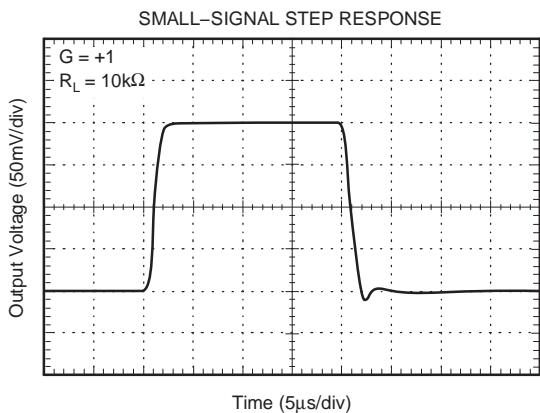
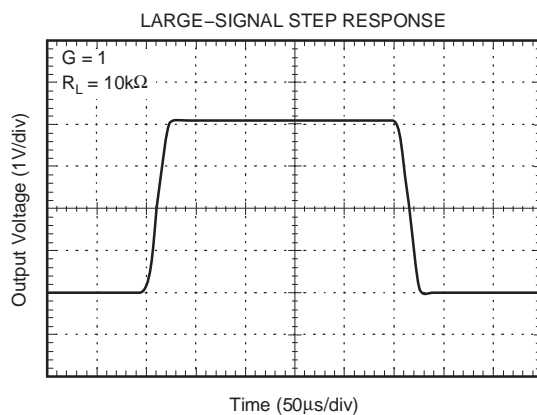
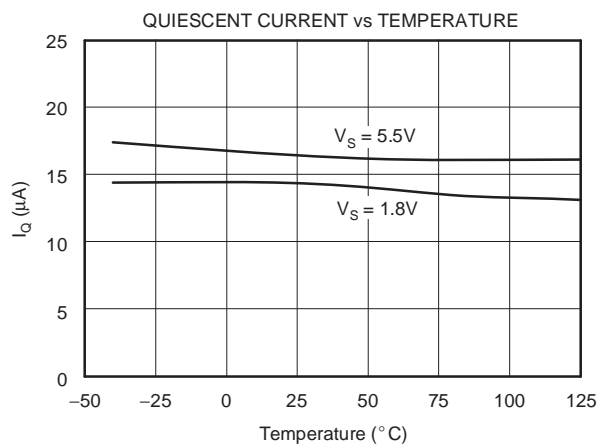
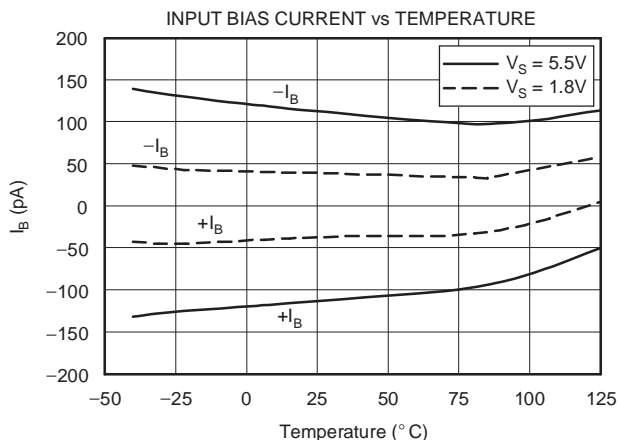
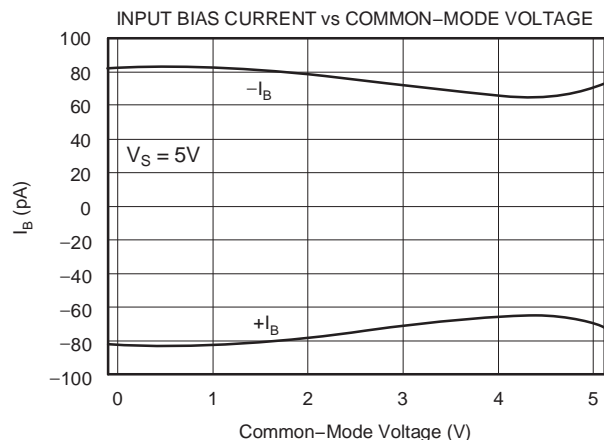
POWER-SUPPLY REJECTION RANGE vs FREQUENCY



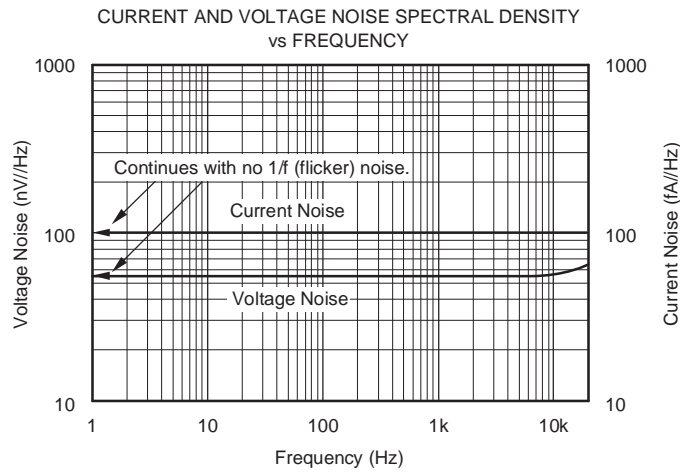
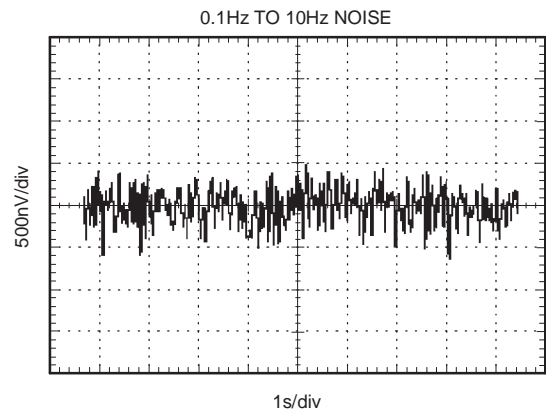
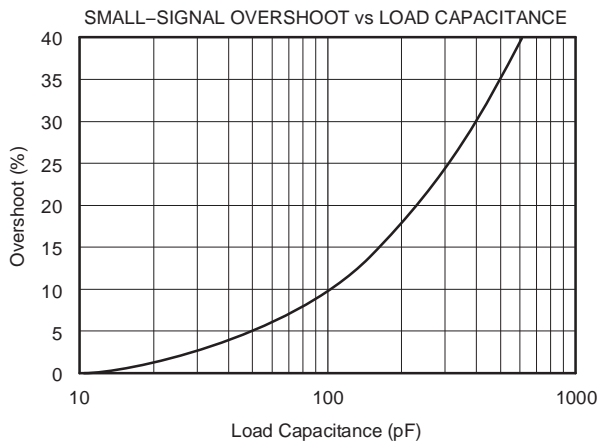
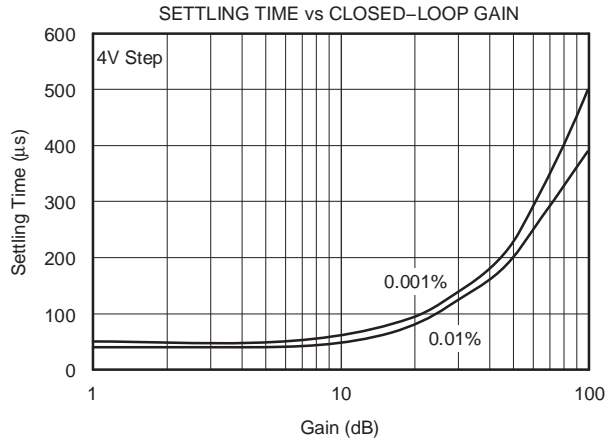
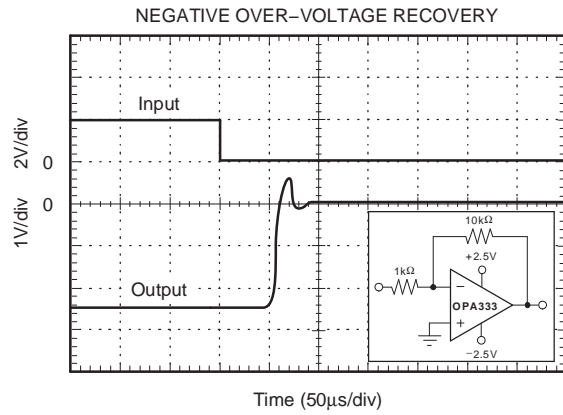
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



**TYPICAL CHARACTERISTICS (continued)**



TYPICAL CHARACTERISTICS (continued)



## APPLICATION INFORMATION

The OPA333 is unity-gain stable and free from unexpected output phase reversal. They use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by ensuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals)
- Thermally isolate components from power supplies or other heat sources
- Shield op amp and input circuitry from air currents, such as cooling fans

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1  $\mu\text{V}/^\circ\text{C}$  or higher, depending on materials used.

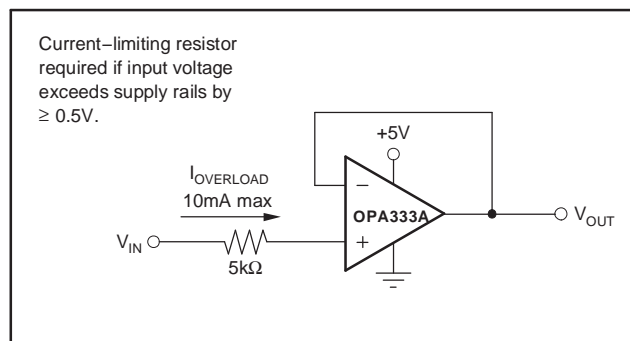
### Operating Voltage

The OPA333 op amp operates over a power-supply range of 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

### Input Voltage

The OPA333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor (see Figure 1).



**Figure 1. Input Current Protection**

### Internal Offset Correction

The OPA333 op amp uses an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8  $\mu\text{s}$  using a proprietary technique. Upon power up, the amplifier requires approximately 100  $\mu\text{s}$  to achieve specified  $V_{\text{OS}}$  accuracy. This design has no aliasing or flicker noise.



## Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 2).

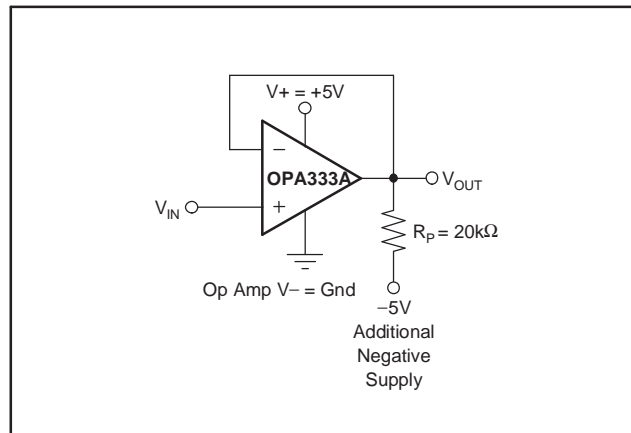


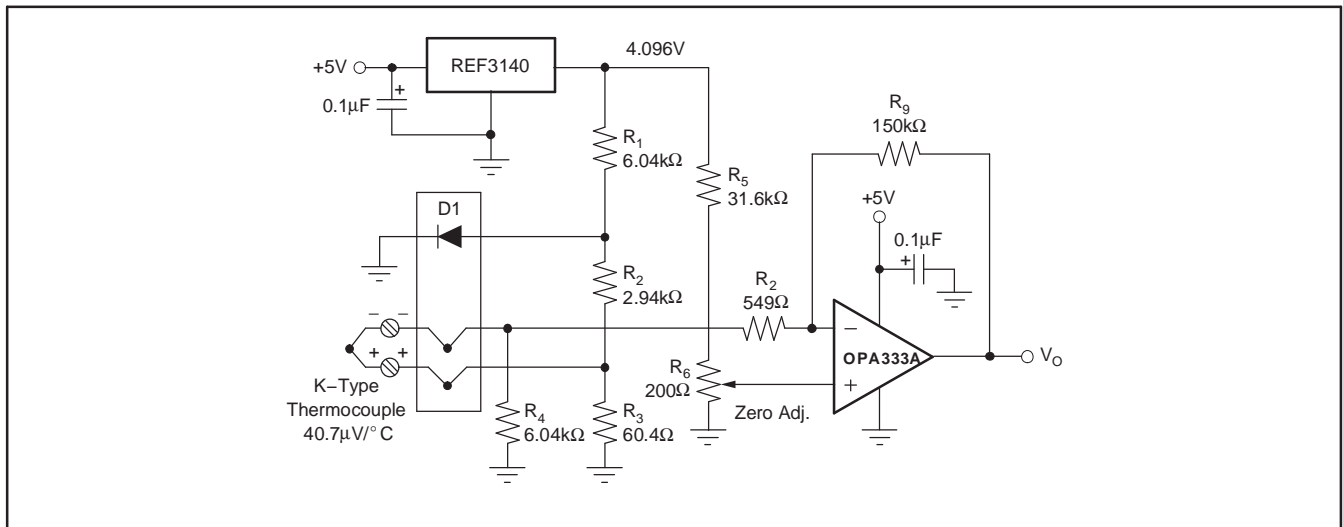
Figure 2.  $V_{OUT}$  Range to Ground

The OPA333 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

## General Layout Guidelines

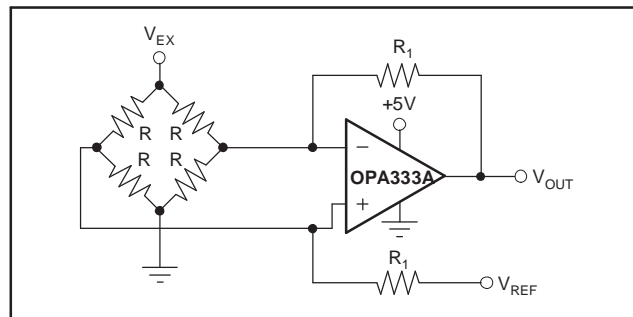
Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333 has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may still cause varying offset levels.



**Figure 3. Temperature Measurement**

Figure 4 shows the basic configuration for a bridge amplifier.



**Figure 4. Single Op-Amp Bridge Amplifier**

A low-side current shunt monitor is shown in Figure 5.  $R_N$  are operational resistors used to isolate the ADS1100 from the noise of the digital I<sup>2</sup>C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.

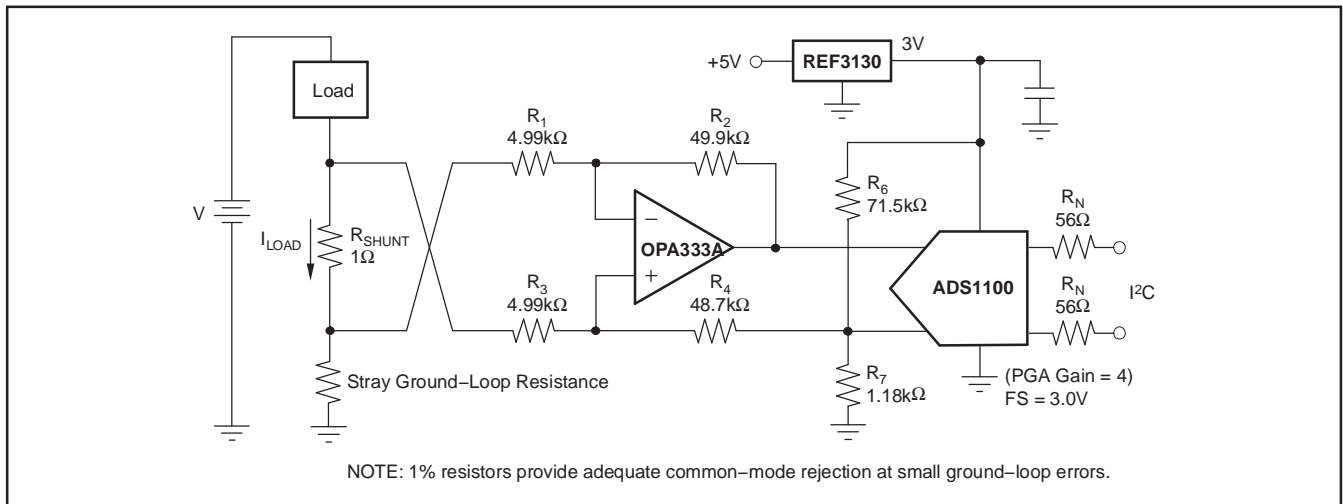


Figure 5. Low-Side Current Monitor

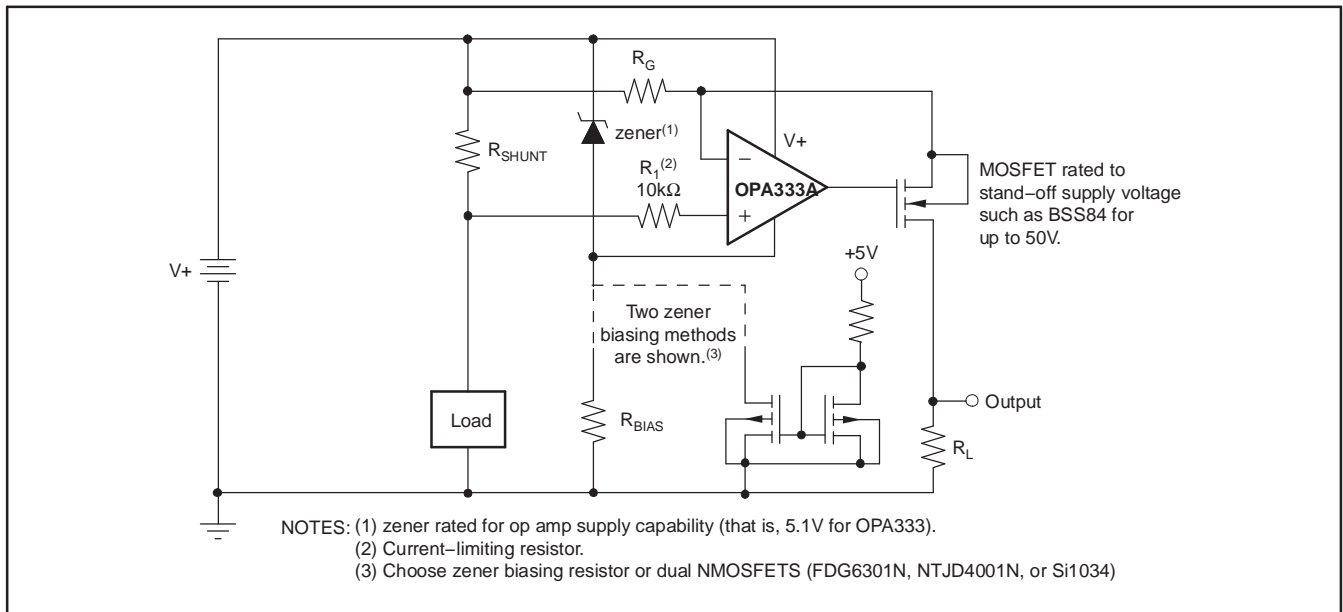


Figure 6. High-Side Current Monitor

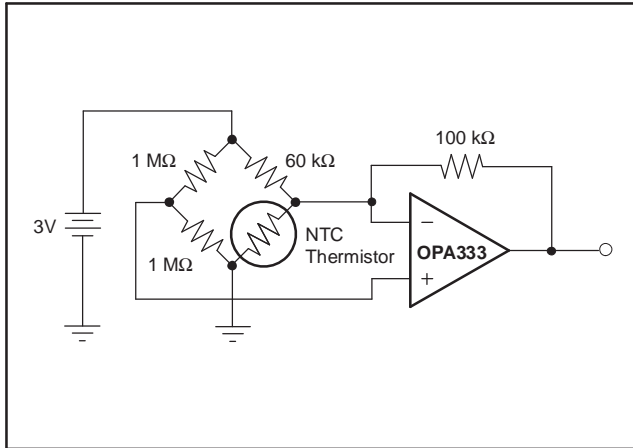


Figure 7. Thermistor Measurement

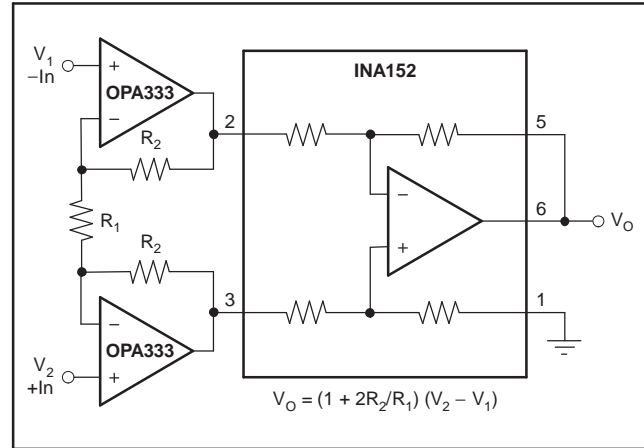


Figure 8. Precision Instrumentation Amplifier

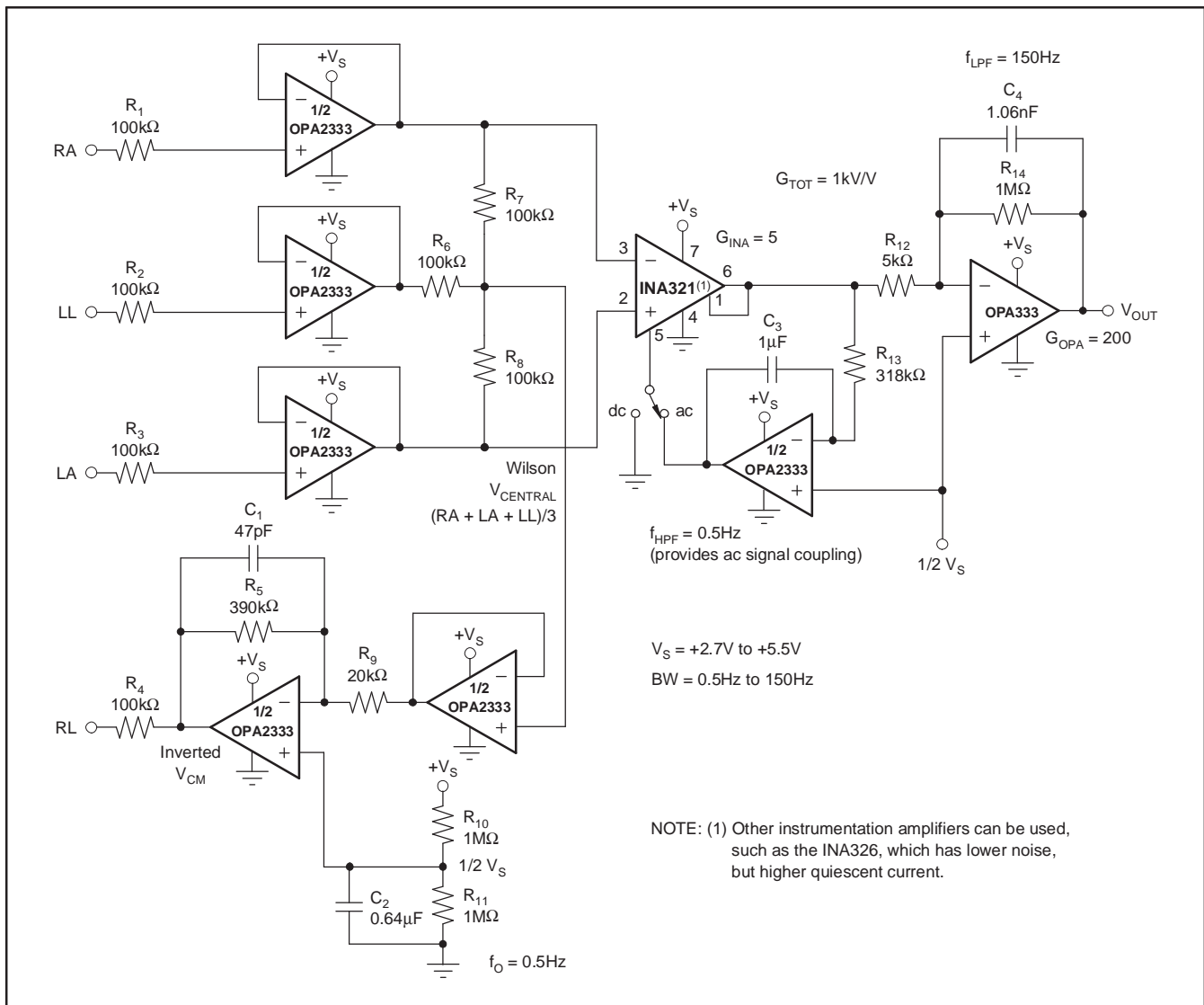


Figure 9. Single-Supply, Very-Low-Power ECG Circuit

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA333AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QCNQ	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA333-Q1 :**

- Catalog: [OPA333](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA333AQDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA333AQDBVRQ1	SOT-23	DBV	5	3000	203.0	203.0	35.0



## GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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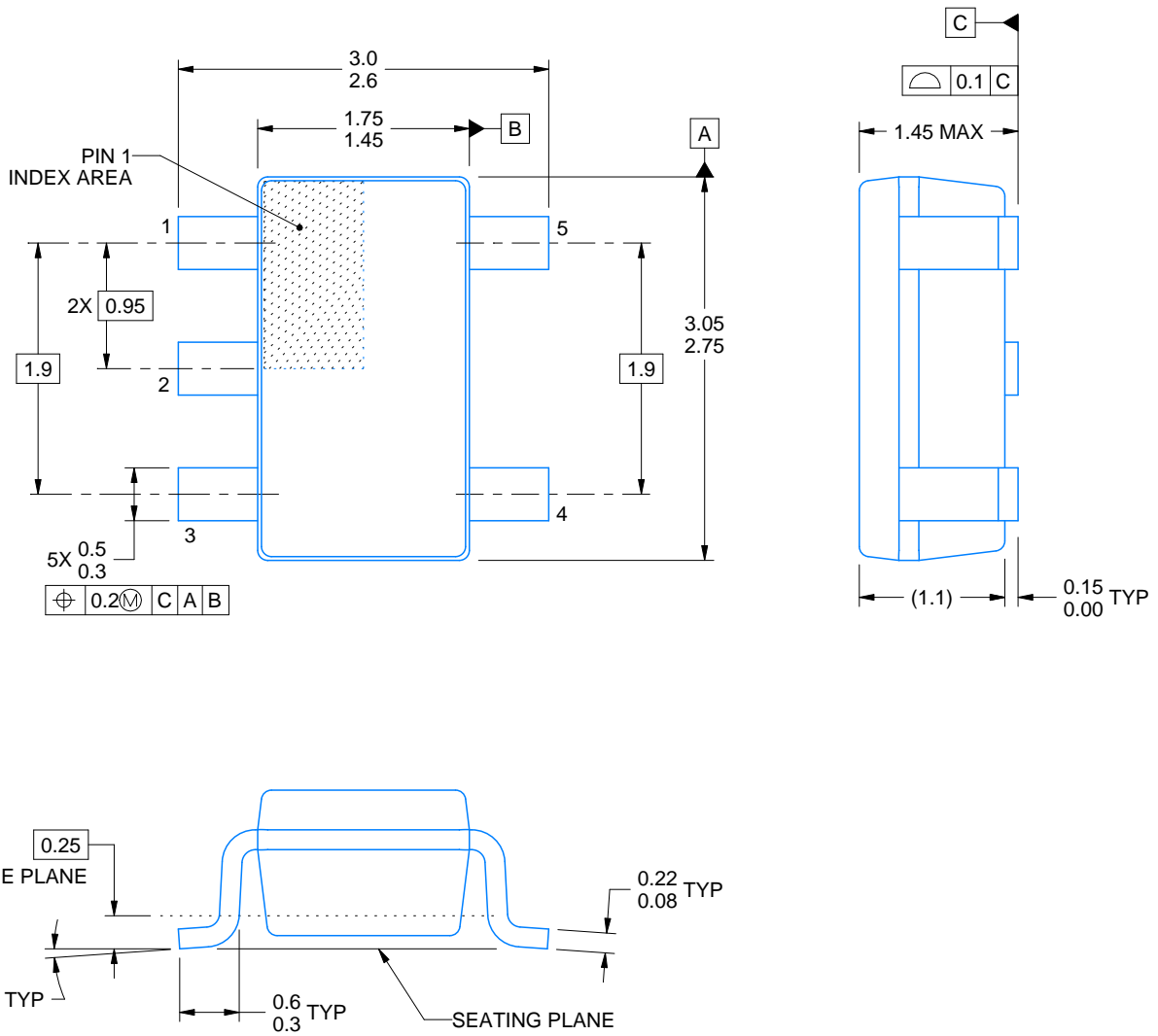
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

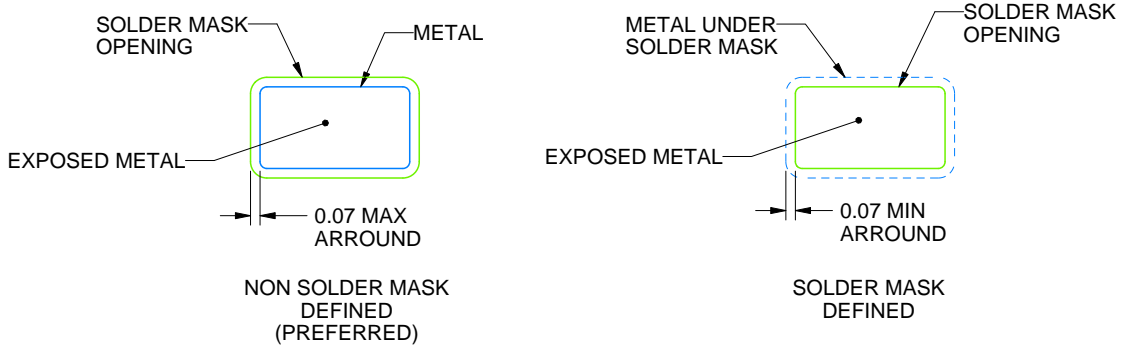
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

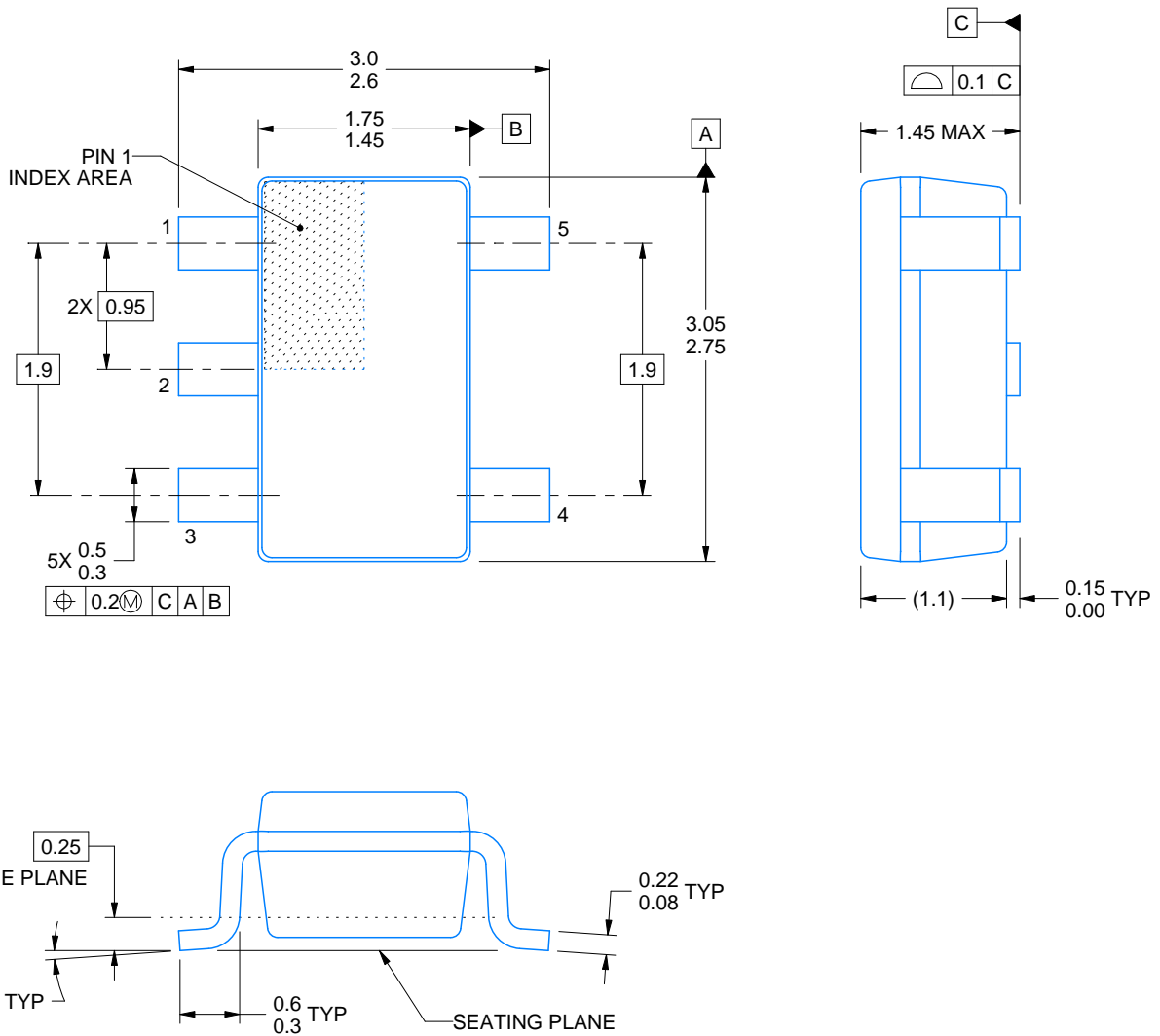
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

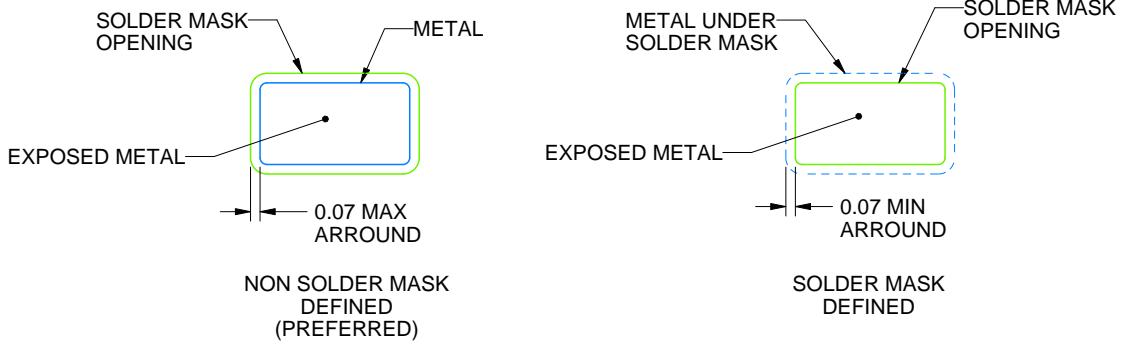
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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