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FDG6306P

P-Channel 2.5V Specified PowerTrench^o MOSFET

General Description

This PChannel 2.5V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications wth a wide range of gate drive voltage (2.5V - 12V).

Applications

- Battery management
- · Load switch

Features

- -0.6 A, -20 V. $R_{DS(ON)} = 420 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$ $R_{DS(ON)} = 630 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Low gate charge
- + High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$
- Compact industry standard SC70-6 surface mount package



The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

Symbol		Parameter		Ratings	Units	
V _{DSS}	Drain-Sourc	e Voltage		-20	V	
V _{GSS}	Gate-Source	Gate-Source Voltage		± 12	V	
Ь	Drain Currer	nt – Continuous	(Note 1)	-0.6	A	
		– Pulsed		-2.0		
PD	Power Dissi	pation for Single Oper	ation (Note 1)	0.3	W	
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to +150		
R _{0JA} Packag		sistance, Junction-to-A	· · · ·	415	°C/W	
Device Marking		Device	Reel Size	Tape width	Quantity	
Device	5	Donico		•	quantity	

June 2016

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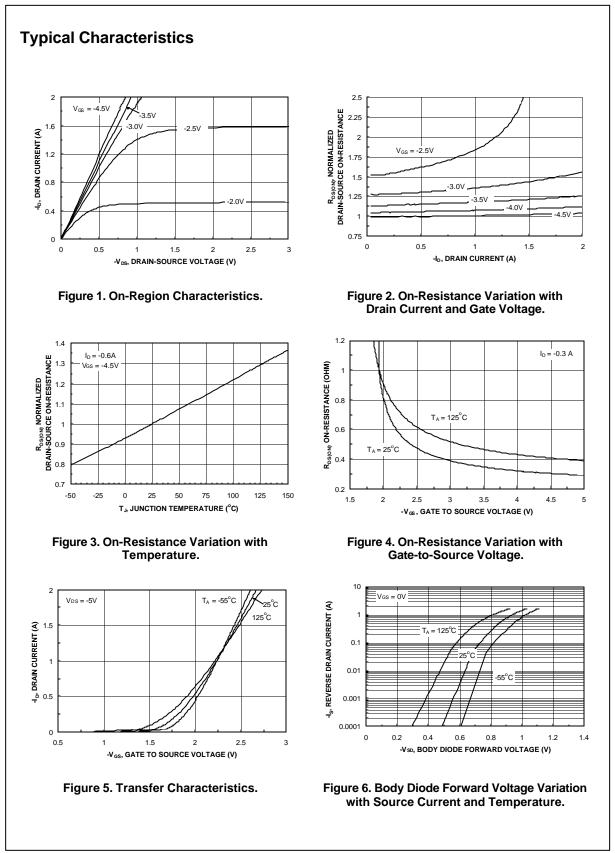
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-20			V
<u>ΔBVbss</u> ΔTj	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$, Referenced to 25°C		-14		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
GSSF	Gate-Body Leakage, Forward	$V_{GS} = -12 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
GSSR	Gate–Body Leakage, Reverse	$V_{GS} = 12 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA
On Cha	acteristics (Note 2)					•
V _{GS(th)}	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = -250 \; \mu\text{A}$	-0.6	-1.2	-1.5	V
<u>ΔVgs(th)</u> ΔTj	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{l} V_{GS} = -4.5 \; V, \; I_D = -0.6 \; A \\ V_{GS} = -2.5 \; V, \; I_D = -0.5 \; A \\ V_{GS} = -4.5 \; V, \; I_D = -0.6 \; A, \; T_J \!=\! 125^\circ \! C \end{array} $		300 470 400	420 630 700	MΩ
D(on)	On–State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$	-2			A
9 _{FS}	Forward Transconductance	$V_{DS} = -5 V$, $I_D = -0.6 A$		1.8		S
Dynami	c Characteristics					
Ciss	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$		114		pF
Coss	Output Capacitance	f = 1.0 MHz		24		pF
Crss	Reverse Transfer Capacitance			9		pF
Switchi	ng Characteristics (Note 2)					
d(on)	Turn–On Delay Time	$V_{DD} = -10 V, I_D = 1 A,$		5.5	11	ns
r	Turn–On Rise Time	$V_{GS} = -4.5 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		14	25	ns
d(off)	Turn–Off Delay Time			6	12	ns
f	Turn-Off Fall Time			1.7	3.4	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_D = -0.6 \text{ A},$		1.4	2.0	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 V$		0.3		nC
Q _{gd}	Gate–Drain Charge			0.4		nC
Drain–S	ource Diode Characteristic	s and Maximum Ratings				
S	Maximum Continuous Drain-Source				-0.25	A
√ _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 V$, $I_{S} = -0.25 A$ (Note 2)		-0.77	-1.2	V

the drain pins. R_{BJA} is guaranteed by design while R_{BJA} is determined by the user's board design. $R_{\text{BJA}} = 415^{\circ}$ C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%

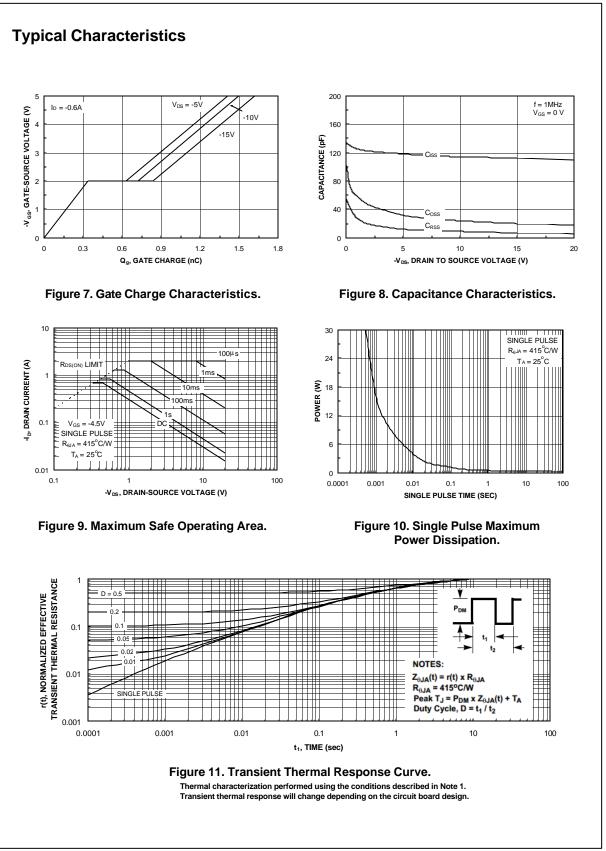
FDG6306P Rev 1.3 (W)

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