M61571AFP

2 × 50W Digital Audio Power Amplifier

REJ03F0118-0300
Rev.3.0
Dec 22, 2005

Description

M61571AFP is a Digital power amplifier IC developed for home audio.

M61571AFP can realize maximum Power 50W × 2ch(VD = 21V,THD = 10%, BTL) at 4 Ω load.

It is possible to replace from the conventional analog amplifier system to the digital amplifier system easily.

Features

- Output power Maximum Rating: 50W at RL = 4Ω,VD = 21V,THD = 10%, BTL; 37W at RL = 4Ω,VD = 18V,THD = 10%, BTL
- The RENESAS original circuits realize low noise and low distortion characteristics.
- Built-in the 2 channels (BTL) output drivers by Nch-MOS FET.
- High power efficiency
- High speed switching
- Package: Power SSOP with 52pin (52P9F)

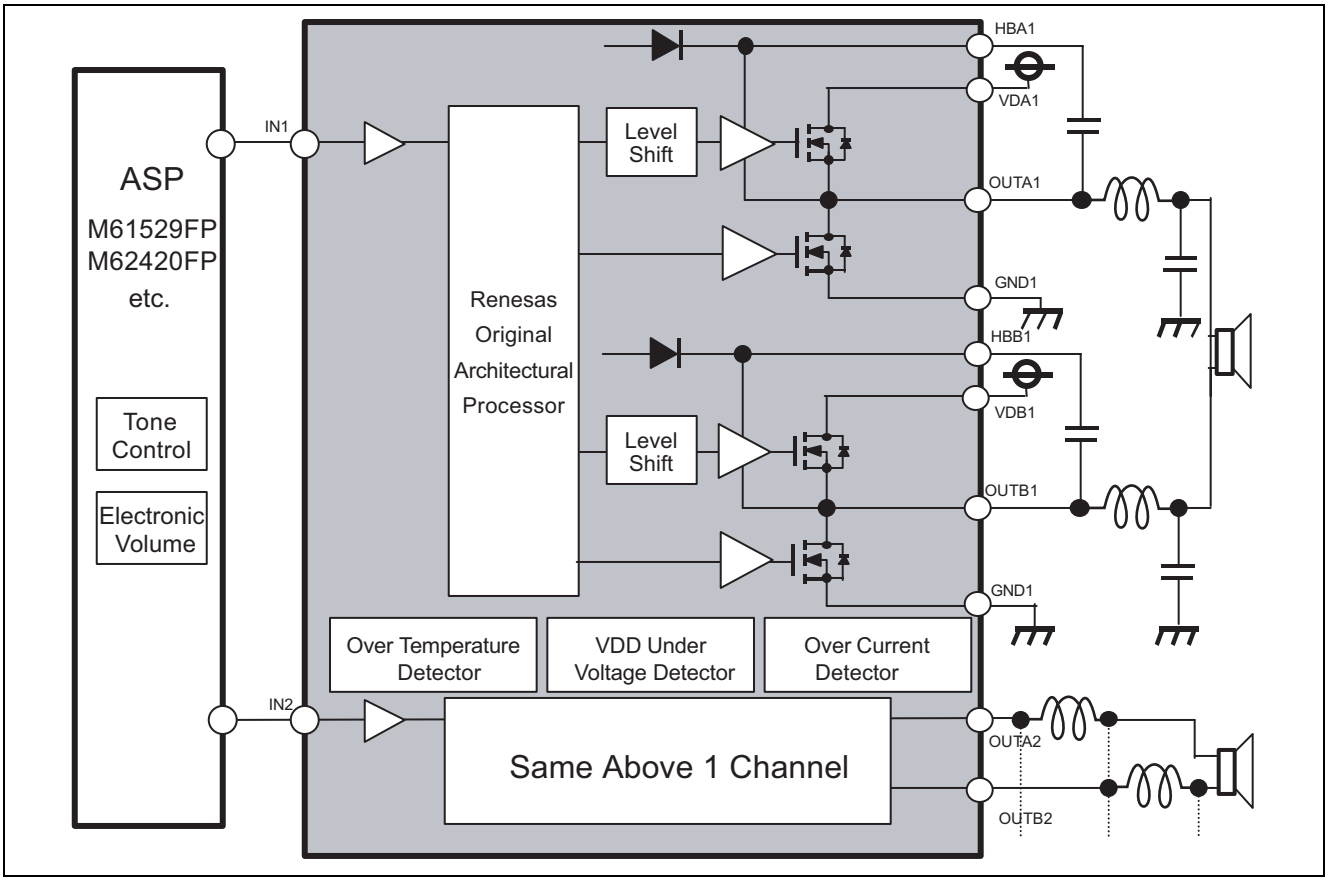
Applications

- Home audio, TV, PDP, LCD Monitor etc.

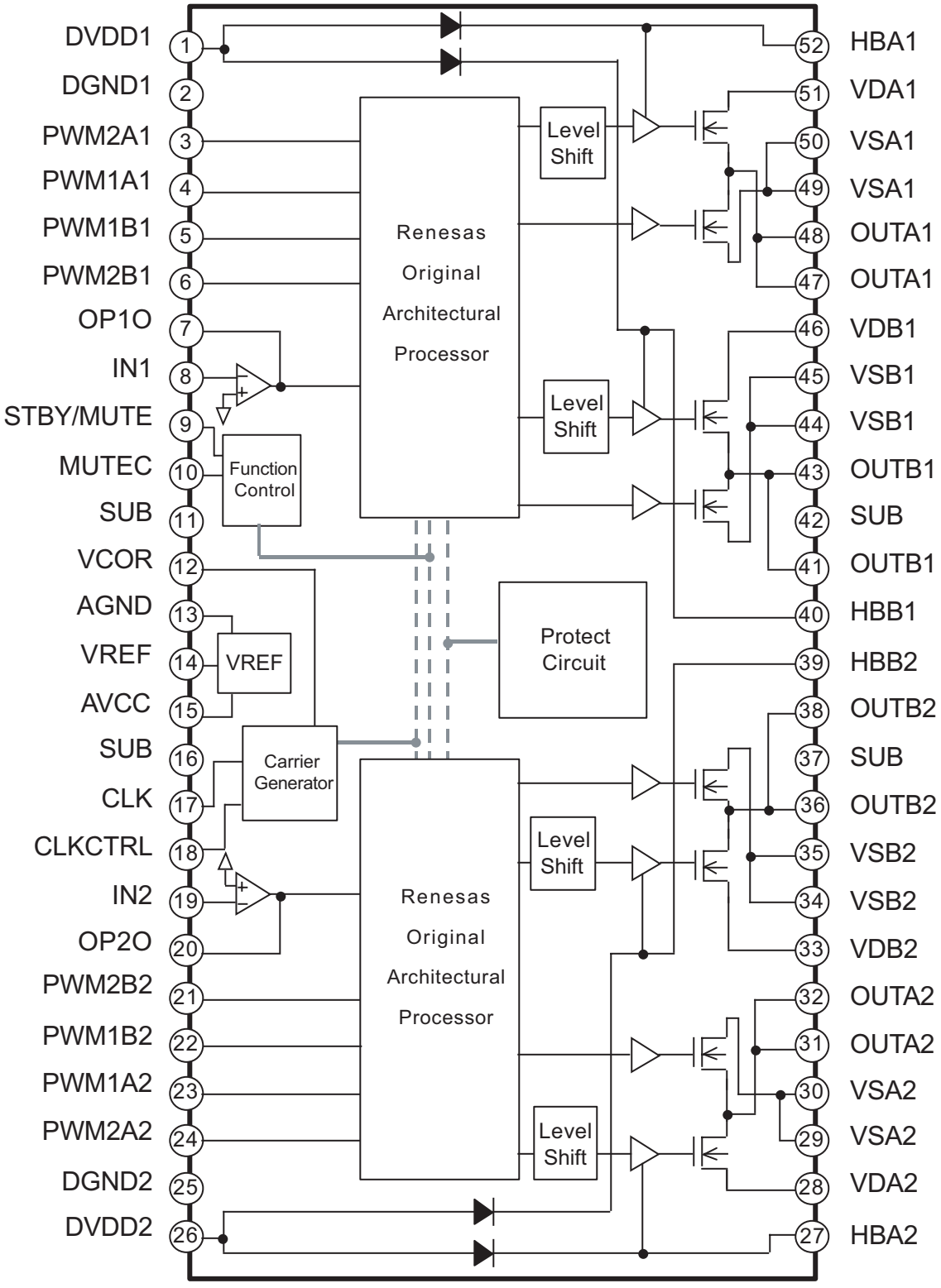
Recommended Operating Conditions

- Power supply voltage for analog & pre-driver stage: Rating 10V
- Power supply voltage for power stage: Rating 18V,
  Recommended operation supply voltage range: from 10V to 21V
- Speaker impedance: operating from 4 to 8Ω

System Block Diagram



Pin Layout and Internal Block Diagram



Top View (Facing up Heat Spreader)

Pin Description

	No.	Symbol	Description
CH1 power block	49, 50	VSA1	CH1-A block: Ground pin for power output stage
	47, 48	OUTA1	CH1-A block: Power output pin
	51	VDA1	CH1-A block: Power supply pin for power output stage (VD is supplied)
	52	HBA1	CH1-A block: Capacitor connection pin for bootstrap on "H" side
	44, 45	VSB1	CH1-B block: Ground pin for power output stage
	41, 43	OUTB1	CH1-B block: Power output pin
	46	VDB1	CH1-B block: Power supply pin for power output stage (VD is supplied)
	40	HBB1	CH1-B block: Capacitor connection pin for bootstrap on "H" side
	2	DGND1	CH1 Ground pin for digital pre-driver stage
	1	DVDD1	CH1 Power supply pin for digital pre-driver stage (DVDD=10V supply)
CH2 power block	29, 30	VSA2	CH2-A block: Ground pin for power output stage
	31, 32	OUTA2	CH2-A block: Power output pin
	28	VDA2	CH2-A block: Power supply pin for power output stage (VD is supplied)
	27	HBA2	CH2-A block: Capacitor connection pin for bootstrap on "H" side
	34, 35	VSB2	CH2-B block: Ground pin for power output stage
	36, 38	OUTB2	CH2-B block: Power output pin
	33	VDB2	CH2-B block: Power supply pin for power output stage (VD is supplied)
	39	HBB2	CH2-B block: Capacitor connection pin for bootstrap on "H" side
	25	DGND2	CH2 Ground pin for digital pre-driver stage
	26	DVDD2	CH2 Power supply pin for digital pre-driver stage (DVDD=10V supply)
Analog block	8	IN1	CH1 Analog signal input pin
	7	OP1O	CH1 Amp output
	4	PWM1A1	CH1-A block PWM generate pin1
	3	PWM2A1	CH1-A block PWM generate pin2
	5	PWM1B1	CH1-B block PWM generate pin1
	6	PWM2B1	CH1-B block PWM generate pin2
	19	IN2	CH2 Analog signal input pin
	20	OP2O	CH2 Amp output
	23	PWM1A2	CH2-A block PWM generate pin1
	24	PWM2A2	CH2-A block PWM generate pin2
	22	PWM1B2	CH2-B block PWM generate pin1
	21	PWM2B2	CH2-B block PWM generate pin2
	15	AVCC	Analog Block: Power supply pin (AVCC=10V supply)
	14	VREF	Analog Block: Reference voltage pin
	13	AGND	Analog Block: Ground
Common	18	CLKCNTL	Pin for frequency setting of internal carrier generator
	17	CLK	Clock Input/Output pin
	12	VCOR	Carrier frequency controlled pin
	10	MUTEC	Capacitor connection pin for mute control
	9	STBY/ MUTE	Stand-by/ Mute control input pin
	11, 16, 37, 42	SUB	SUB terminal of IC is connected to exposed heat sink pad.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Condition	
HBA*, HBB* Maximum supply voltage	HBmax	40	V	HBA*, HBB* Pin Voltage	DC
		50			AC: under 100ns of pulse width
VD* Maximum supply voltage	VDmax	25	V	VD* Power Supply Voltage	DC
		40			AC: under 100ns of pulse width
Absolute maximum rating voltage	VDDmax	16	V	VDD* power supply voltage	
Power dissipation	Pd	7.5	W	Ideal heat dissipation condition at Ta = 75°C	
Thermal resistance	θjc	10	°C/W	from junction to case	
Junction temperature	Tj	150	°C		
Operating ambient temperature	Ta	–20 to +75	°C		
Storage temperature	Tstg	–40 to +125	°C		

Note: * marks mean the number of channel 1 to 2.

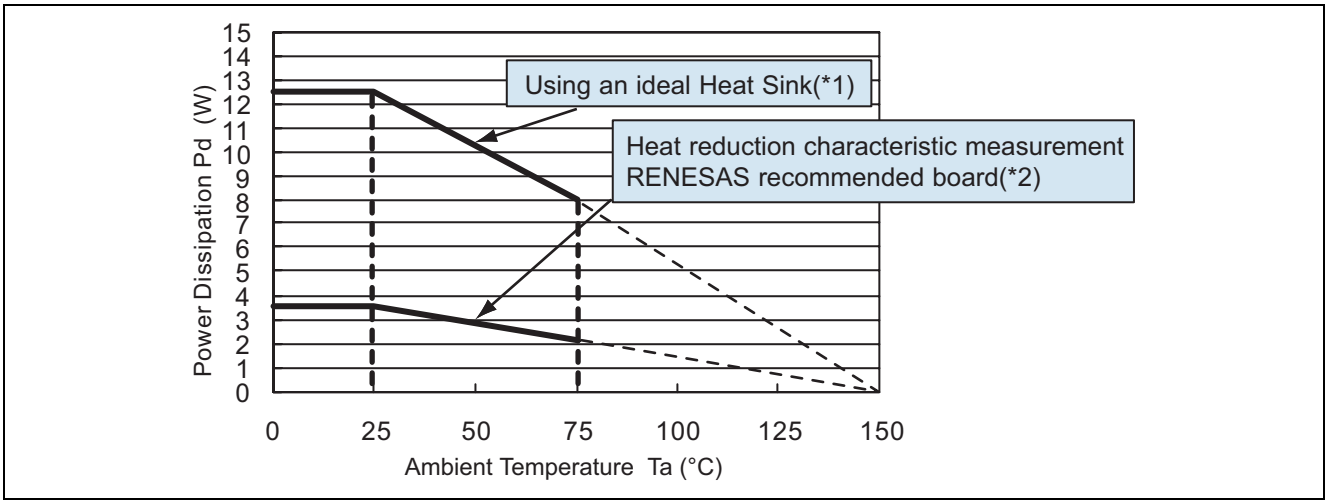
Notes regarding this product

Notes: 1. This product may generate heat, even while operating normally, and it may become high temperature. This product may seldom become high temperature further by the poor property, failure, etc. not only including peripheral parts.
Moreover, since it is used for the last stage of a product, and that one may be damaged according to an external factor, please fully take into consideration in use!
This product is designed on the assumption that a consumer product. Please be sure to use it within the heat dissipation condition of this specification. If heat dissipation condition becomes fall, there is fear of damage on a fall or abnormalities of the performance.

2. If the instant peak value of the VD power supply current exceeds 8A per channel (design value), included over current protector will the PWM operation. It is unnecessary to supply more over this current value, please mind.
The maximum current value at typical 4Ω operation is a little less than 3.5A.
When you use it, please take notice the stability of supply voltage that each terminal power does not exceed rated value.

3. This product includes a MOS transistor and a CMOS logic circuit.
Since there are possibilities generated in a MOS transistor or a CMOS logic circuit, such as destruction and a latch up, please set for use it and be careful of it like a MOS transistor or the CMOS logic LSI.

Thermal Derating



(Reference data)

*1. Maximum output power Pd = 12.5W under Ta = 25°C, using an ideal Heat Sink

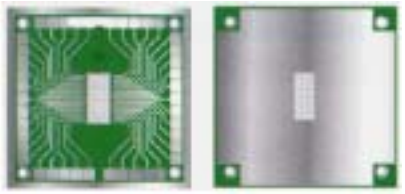
*2. Renesas recommended board specification

(Board specification)

- Material: Glass epoxy FR-4
- Size: 70 × 70 mm
- Thickness: t = 1.6 mm

(Wiring specification of 1/2 layer)

- Material: Copper
- Thickness: t = 18 µm



1st layer(Top View) 2nd layrer(Back View)

Note: Please be sure to use it within the heat dissipation condition of this specification. If heat dissipation condition becomes fall, there is fear of damage on a fall or abnormalities of the performance.

Recommended Operating condition

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Power supply voltage for power output stage	VD*	AVCC	18	21	V	VD* (pins 28,33,46,51)
Power supply voltage for digital pre-driver stage	DVDD*	9	10	11	V	DVDD1 (pin 1), DVDD2 (pin 26)
Power supply voltage for analog stage	AVCC	9	10	11	V	AVCC (pin 15)
Control voltage of low level	VL	0	—	1	V	pin 9, AVCC = 10V
Control voltage of middle level	VM	2.3	—	5.5	V	pin 9, AVCC = 10V
Control voltage of high level	VH	7.5	—	AVCC	V	pin 9, AVCC = 10V

Note:
1. * marks mean the number of channel 1 to 2.
2. Please use DVDD and AVCC on same voltage.
3. ”Absolute maximum rating” means the limitation value to available to let the device destroyed.
4. "Recommended operation conditions" indicates the conditions as which a device functions correctly. However, this doesn’t guarantee the specific performance limit.
5. Moreover, "Electronic characteristics" is the electric specification of DC and AC which guarantees the specific performance limit, when the examination conditions indicated are fulfilled. Although the specification as which the limit value is not specified among parameters is not guaranteed, central value (TYP) serves as an index, which shows the performance of a device

   This is because these parameters are greatly dependent on evaluation board layout design / specification parts / power supply section design, and is a standard value in the board /parts of our company’s specification

Electronic Characteristics

(Unless otherwise noted,
Ta=25°C, VD=18V, DVDD,AVCC=10V, Gv=18dB, Carrier Frequency=550kHz,, f = 1kHz, RL=4Ω)

DC Characteristics

Parameter		Symbol	Limit			Unit	Measurement Condition
			Min	Typ	Max		
Circuit current							
VD Circuit current		IVD		16	35	mA	No signal (Power stage)
VDD Circuit current		IVDD		60	100	mA	No signal (Pre-driver + Analog)
Stand-by Circuit current		ISTVD		80	250	μA	Stand-by
Under voltage detection							
Detection level of under-voltage		AVCCR	5.5	6.0	7.0	V	Between VDD and GND
Under-voltage hysteresis voltage		AVCCH		1		V	Detection → Recovery
Heating detection							
Temperature of protection starting		TPRH		150		°C	Note 1
Temperature of protection release		TPRL		130		°C	
Over current detection							
Over current detection value		IMAX		8		A	
Output ON resistance of power MOS							
Output ON resistance	H side	Ron		300		mΩ	IF=100mA
	L side			280		mΩ	IF=100mA

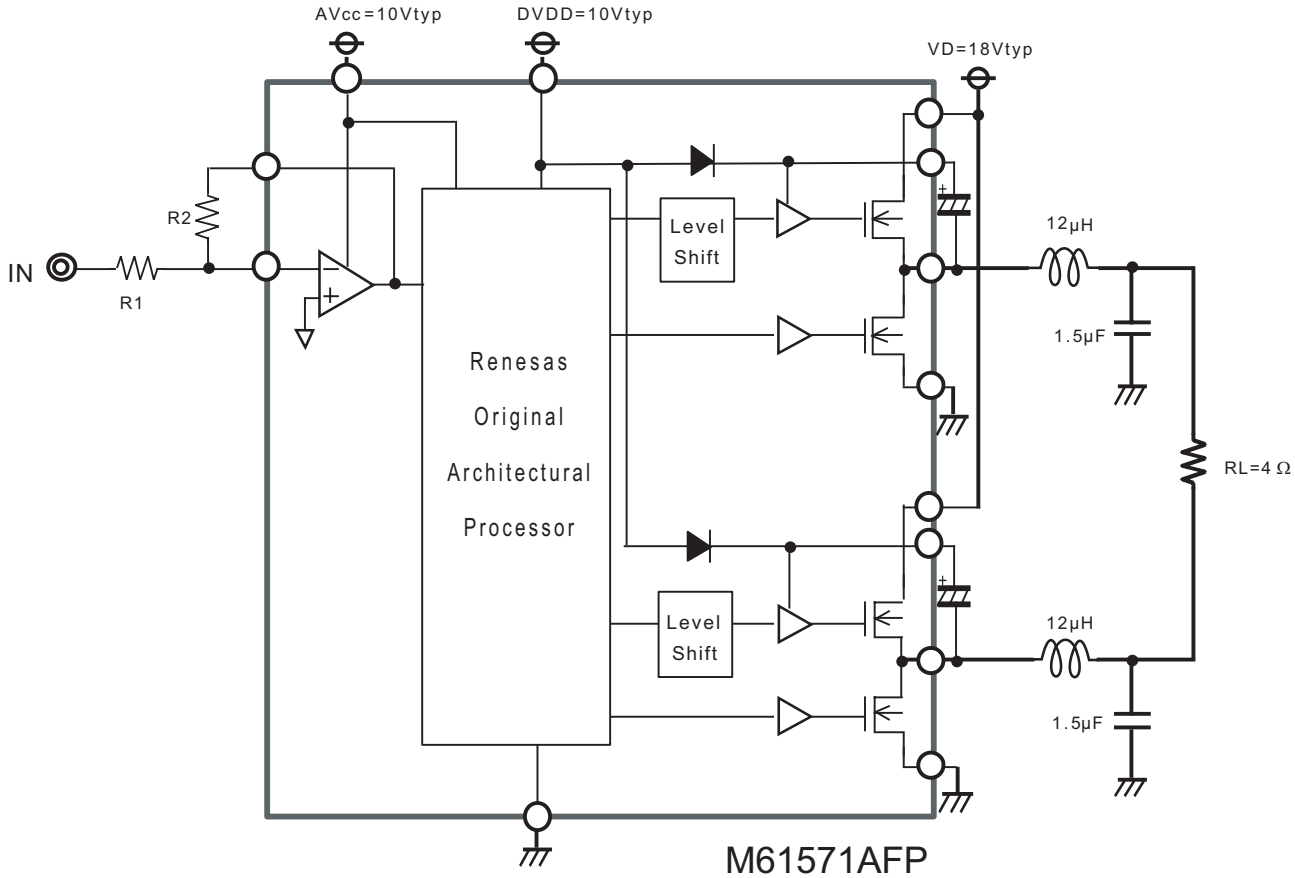
Note 1: The detection temperature of a heat detection circuit is the objective value at designing, and it does not guarantee the detection value. (These measurements are not checked by the temperature test.)

AC Characteristics

Parameter	Symbol	Limit			Unit	Measurement Condition
		Min	Typ	Max		
Output power1	Po1		37		W	THD + N = 10% 400HzHPF, 30kHzLPF
Output power2	Po2		30		W	THD + N = 1% 400HzHPF, 30kHzLPF
Maximum output power	Pomax		50		W	VD = 21V, THD + N = 10%, 30kHzLPF 400HzHPF
Total harmonic distortion	THD + N		0.02	0.1	%	Po = 15W, 400HzHPF, 30kHzLPF
Output noise level	No		50	100	μVrms	A-Weighted filter
Gain voltage	Gv	16	18	20	dB	Po = 1W, Analog block: Gv = 0dB
Mute level	Mute		85		dB	
Channel balance	CBAL	–0.5	0	+0.5	dB	Po = 1W, Analog block: Gv = 0dB
Ripple rejection ratio	PSRR		60		dB	Vripple = 400mV, Fi = 1kHz
Power efficiency	Eff		85		%	Po = 30W, Fi = 1kHz, at 1ch input

Functional Explanation

1. System Block Diagram / 1ch



System Total Gain

$$Gv = 20\log\left(\frac{R2}{R1}\right) + 12 + 6 \quad [\,dB\,]$$

Analog Stage Gain | Internal Gain | BTL

When R1=20kΩ, R2=75kΩ

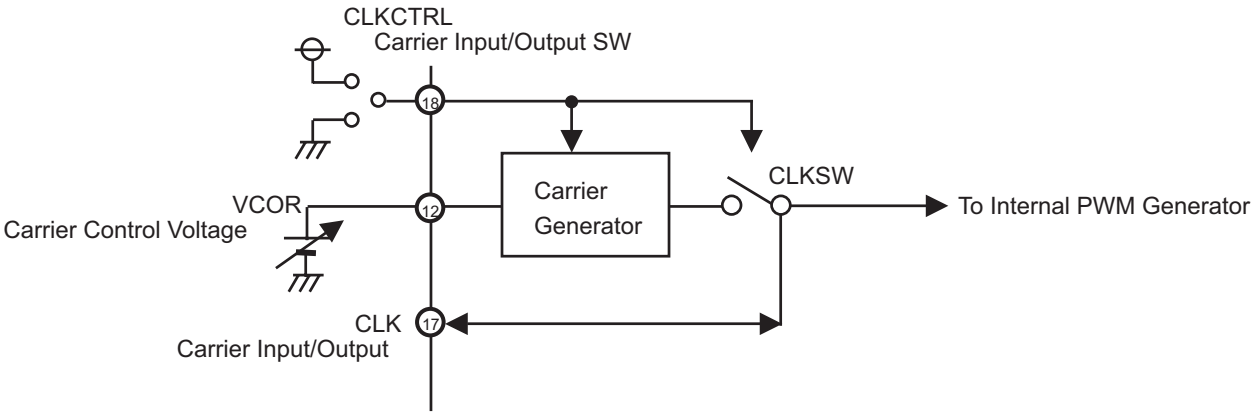
Gv = 29.5dB

2. Carrier Generator

This IC is built-in the functions for (1) changing a carrier frequency and (2) switching the master/slave mode. These functions can perform easily improvement adjustment of efficiency / performance / EMI performance. And, the measure is possible also for the beat problem which originates in the carrier frequency gap in the case of carrying out two or more simultaneous operation of this IC by the multi-channel system etc.

(1) The setting method of Carrier frequency

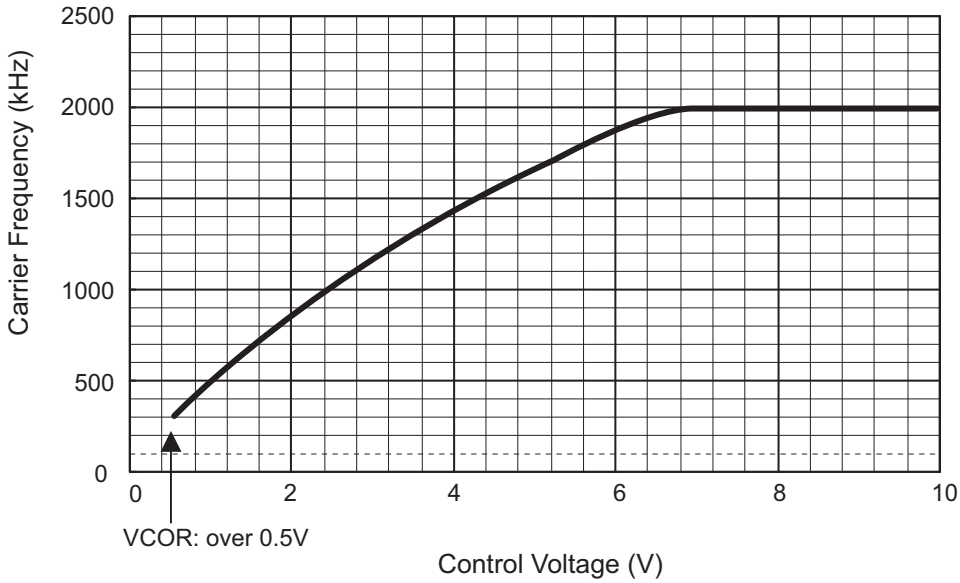
It is possible to set up the reference clock of PWM generator by controlled DC voltage of VCOR (12pin).
That is able to change the frequency value from 300kHz to 2.0MHz.
However, please evaluate enough in the case of use the carrier frequency under our recommendation value (550kHz).
In the case of the conditions which made low carrier frequency and high supply voltage, please be careful for that PWM modulating operation may become unstable.



<Reference Data>

Carrier Control Voltage(12pin DC Voltage) vs Carrier Frequency

<Condition> VD=18V, Vcc=10V, Ta=27°C, RL=4Ω



(2) The setting method of Carrier signal I/O

18pin: The mode control of a career generation circuit of operation by setup of CLKCTRL pin.

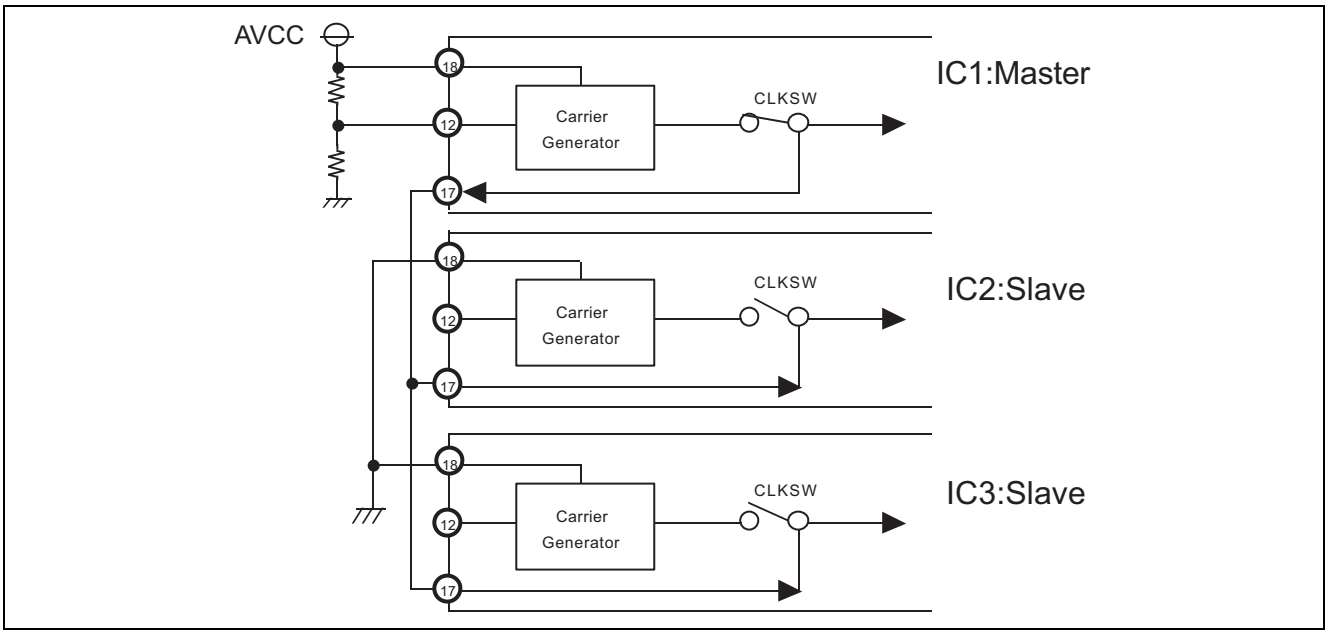
The control mode has the two modes, the master mode which outputs the carrier signal generated in internal VCO to CLK terminal (17pin : CLK), and the slave mode which stops internal VCO and receives the carrier of a master chip from CLK terminal (17pin : CLK).

The control table for operation mode

CLKCNTL	CLK	CLKSW	Operation Mode
AVCC	Output	ON	Master mode: Internal VCO generates carrier and sends it to slave chips.
AGND	Input	OFF	Slave mode: It receives carrier from other master chip.

Note: When using two or more M61571AFP, It is possible to generate a master clock from one IC and to operate other ICs using the clock. The beat generated by the difference of the carrier frequency of each IC can be prevented.

In the case of multi channel use



3. Function Control

This IC has Stand-by /Mute function and it is possible to control by changing the voltage of 9pin: STBY/MUTE.

(1) Function setting

9 pin: Stand-by/Mute	Operating Condition	Output FET Condition
L	Stand-by	Hi-Z
M	Mute	Duty = 50%
H	Normal operation	Normal operation

(a) Stand-by

While cutting off the output of all output MOSFET and muting the music play, the standby current can be made into the minimum.

Moreover, at the standby mode all circuits except for the standby circuit stop completely and also stop the pulse modulation signal. So, an output noise isn't generated.

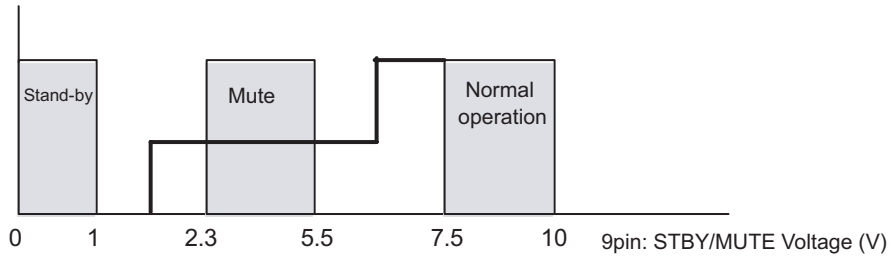
(b) Mute

It mutes an output signal at the same time it mutes an input signal. However, the pulse modulation signal outputs by 50% duty. (Mute level: 85dB typ.)

If it turns on the mute for preventing a shock noise, it will shift to the mute status smoothly.

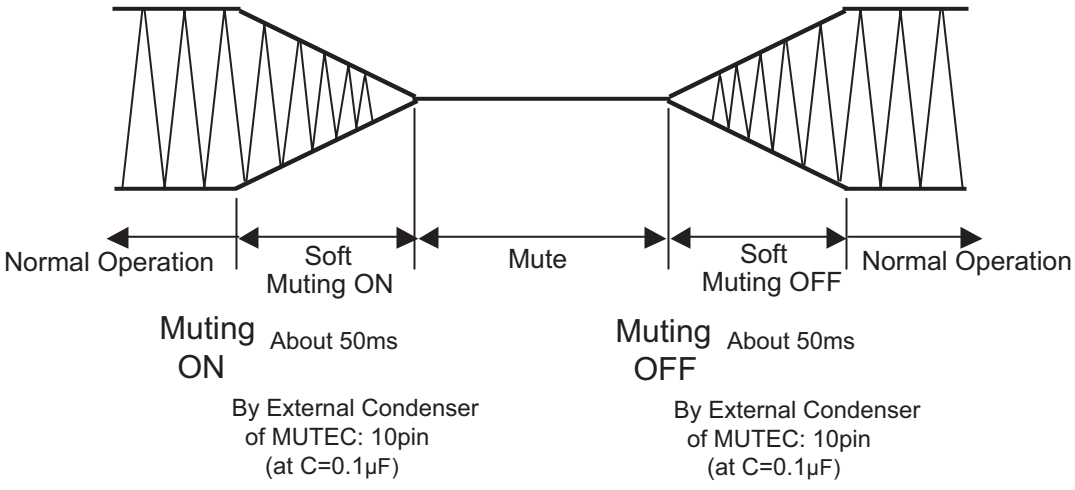
(Soft muting function)

(2) 9pin: STBY/ MUTE Control voltage range



(3) Soft Muting

The time of Soft Muting is decided by the external capacitor of 10pin: MUTEC. When C = 0.1µF, this becomes about 50ms. We recommend the setting over 0.1µF (50ms) for preventing shock sound.



4. Protection Circuit

When M61571AFP detects some protect factor, it has built-in the various protection circuits.

(1) Over Current Protection Circuit

This circuit protects by detecting the unusual over current of Output Power FETs. The detection current values are 8A(typ).

If over current protection circuit are operated, M61571AFP makes all output FETs to " Hi-Z" state and output pins to "Open".

(2) Over Temperature Protection Circuit

This circuit detects unusual over temperature and protects IC (chip). It operates before reach out to thermal run away such as internal junction temperature and the protection circuit operates until it falls to the temperature of hysteresis condition.

When over temperature protection circuit is operated, it makes all output FET to " Hi-Z" state and output pins to "Open".

Protection start temperature: 150ºC typ Protection restore temperature: 130ºC typ

(3) Under Voltage Protection Circuit

This circuit detects an unusual under voltage of analog pre stage power supply and protects. When under voltage detected, it makes all output FET to " Hi-Z" state and output pins to "Open".

When the transient at power ON, the power supply of AC line falls, the load impedance changes and the supply voltage falls temporarily, this is the function committed effectively and it is possible to prevent unusual destruction and to make POP sound by the unusual output into the minimum

Under voltage detection voltage: 6.0V(typ)

Under voltage release voltage: 7.0V(typ)

(4) The table of protection circuit operation

Protection Mode	Protect Condition	Output Stage Condition
Over current protection	Detection current: 8A typ	Hi-Z
Over temperature protection	Protection starting: 150ºC typ Protection release: 130ºC typ	Hi-Z
AVCC under voltage	Detection voltage: 6.0V Release voltage: 7.0V	Hi-Z

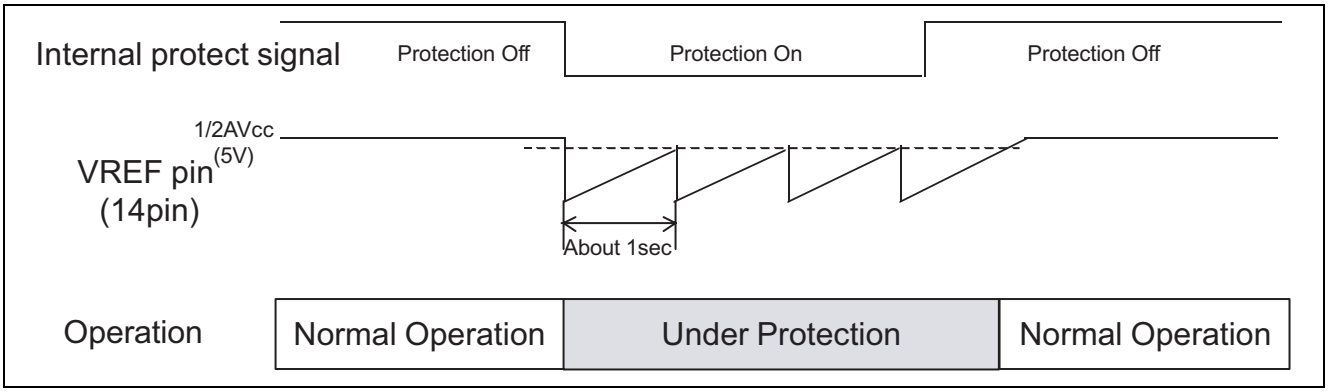
(5) The restoring from a protection state

- At the case of over current protection, over temperature protection and under voltage protection

The restoring from a protection state is performed automatically. While the protection is operating, restoring to normal operation is usually performed for every constant time.

Then, if protection conditions are canceled, it returns to normal operation, if operation is not canceled, a protection state will usually be continued. The cycle of return operation is decided by capacity value of the capacitor linked to 14pin: VREF, and becomes about 1 second at the time of 47µF (design value).

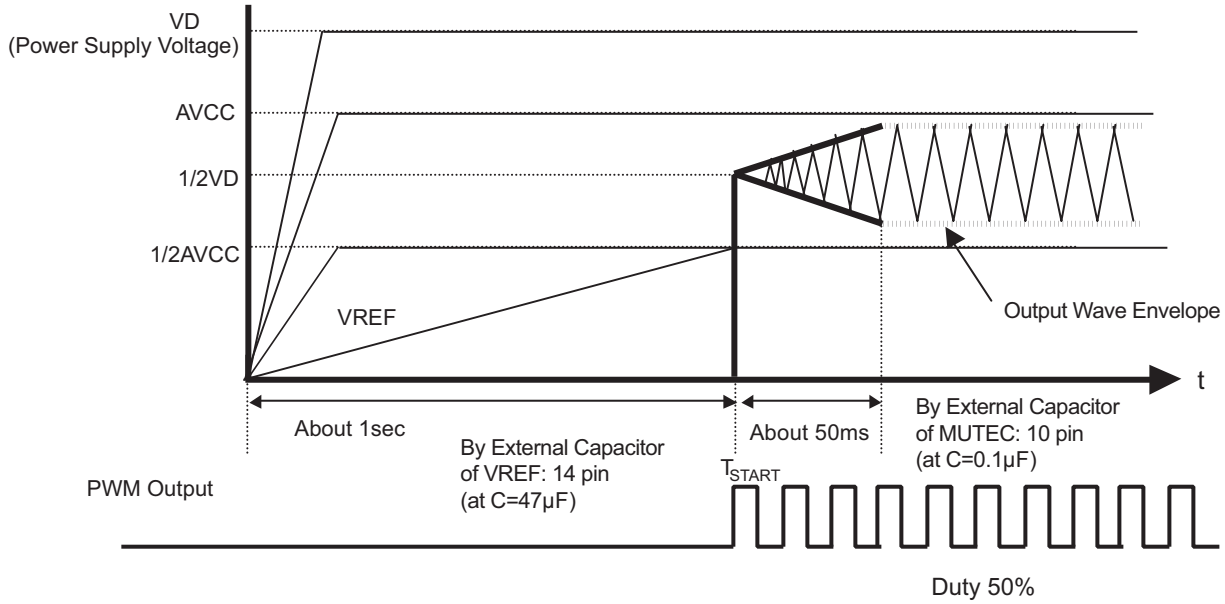
For stable operation, we recommend over 10µF as a capacitor value. The protection state can monitor in this oscillation condition of REF terminal. (Refer to the following figure about the restoring sequence)



Notes at the time of Power ON and Power OFF

When the power ON, M61571AFP automatically operates the soft mute release from the mute state by the following sequence.

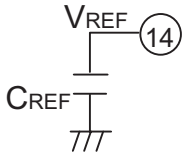
Timing at the power ON



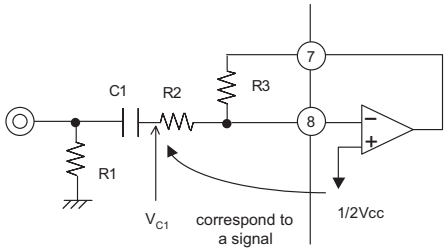
T_{START} means the time by reached VREF to 1/2Avcc and determined automatically by the value of capacitor C_{REF} connected to external parts according to the following formula.

$$T_{START} = \frac{C_{REF} \cdot AV_{CC}}{500 \times 10^{-6}} \quad (sec)$$

When V_{CC}=10V and C_{REF}=47µF, T_{START}=940ms(Typ)

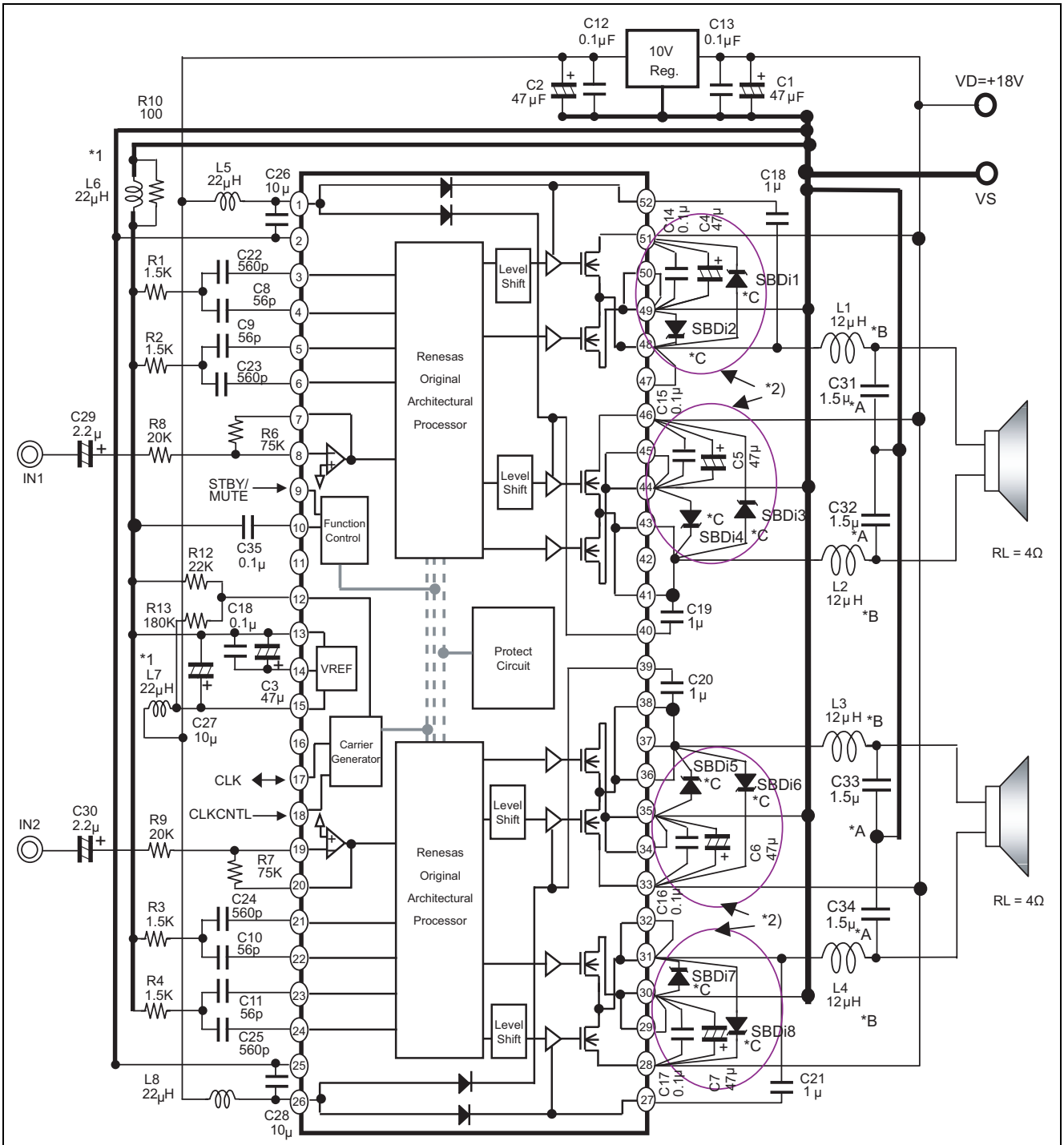


Condition 1) It is necessary to set a system as a stable state by completing to charge of the input coupling capacitor C1 by T_{START}.



$$T_{VC1} = 1.7 \times (C_1(R_1+R_2)) < T_{START}$$

The example of an application circuit



*1: In the case of a substrate design, I recommend arranging in advance on the point near IC of a power supply and a GND line. So, an improvement of an audio performance (distortion and noise) and an EMI performance can be expected. The can delete, if satisfactory by prior evaluation.

*2: Since high frequency big current flows to this capacitor and diode, please arrange to an output terminal and the power supply terminal directly and consider at the time of a layout design to become the smallest possible loop. Otherwise, it becomes the cause of malfunction, performance aggravation, and destruction.

Special External Parts Lists

	Parts No.	Parts Name	Type Name	Pcs
A	C31, 32, C33, C34	C-FILM	1.5μ-50V	4
B	L1, L2, L3, L4	CHOKE-COIL	12μH 7G09B-120M(SAGAMI ELEC CO., LTD.)	4
C	SBDi1,2,3,4,5,6,7,8	DIODE (Shot key barrier)	RB160L40 (made by RHOM)	8

(Note1) Choke coil(*B) are consisted of Second Butterworth LPF in a pair with the capacitor(*A) of from C31 to C34, it is expressed with cut off frequency fc = 1/(2*3.14√LC).
Since they are the important parts which determine EMI performance and audio performance, please select after sufficient examination EMI.
Especially, in order to gather electric power efficiency, we recommend the small thing of DC resistance. Moreover, when excitation current is taken into consideration, it sets at carrier frequency the o'clock of 550kHz, and it is 12μH (I recommend constituting above H.).
When use is carried out on high carrier frequency, it is possible to use a still smaller choke coil.

Notes about mounting

a) Reduction of high frequency impedance for digital GND

At digital GND for pre-driver (2pin and 25pin : DGND terminal) the very big pulse current for high frequency is flowing in order to carry out the high-speed drive of the output power MOS transistor. Therefore, if the board layout design of this digital GND is bad, the high frequency noise from this PWM oscillation becomes large and has a bad influence on function operation and the analog circuit of the internal circuits. So, this may cause malfunction, performance degradation and destruction. In order to reduce the influence of this high frequency noise, it is very effective to lower the high frequency impedance of GND pattern, and we recommend to make GND pattern of a digital system to thickly GND.

b) Disposal of SUB terminal (11, 16, 37, 42 pins)

This IC has 4 pins of SUB terminal (11, 16, 37 and 42pin) and connects to the substrate (substrate: chip back) of IC chip. The leakage current of the high frequency generated at the timing of the edge of PWM may flow into this terminal. If the impedance of the substrate is high, noise level may become large and the parasitism transistor inside IC may operate, and malfunction may be caused.
In order to avoid this, it is effective to reduce the impedance as much as possible. We recommend to connect each SUB terminal to GND which the high frequency impedance is low (DGND of the thickly GND of recommendation by a clause)

c) Disposal of analog GND

In order to reduce interference from the output power stage's GND (VS terminal of each bridge) and pre-driver stage of digital GND (DGND terminal) as much as possible, please connect analog GND by one point at the electric supply GND point, and consider as wiring without a common impedance. Moreover, we recommend to insert a coil/resistance (L6, R10) which separates between the GND electric supply point and high frequency if needed.

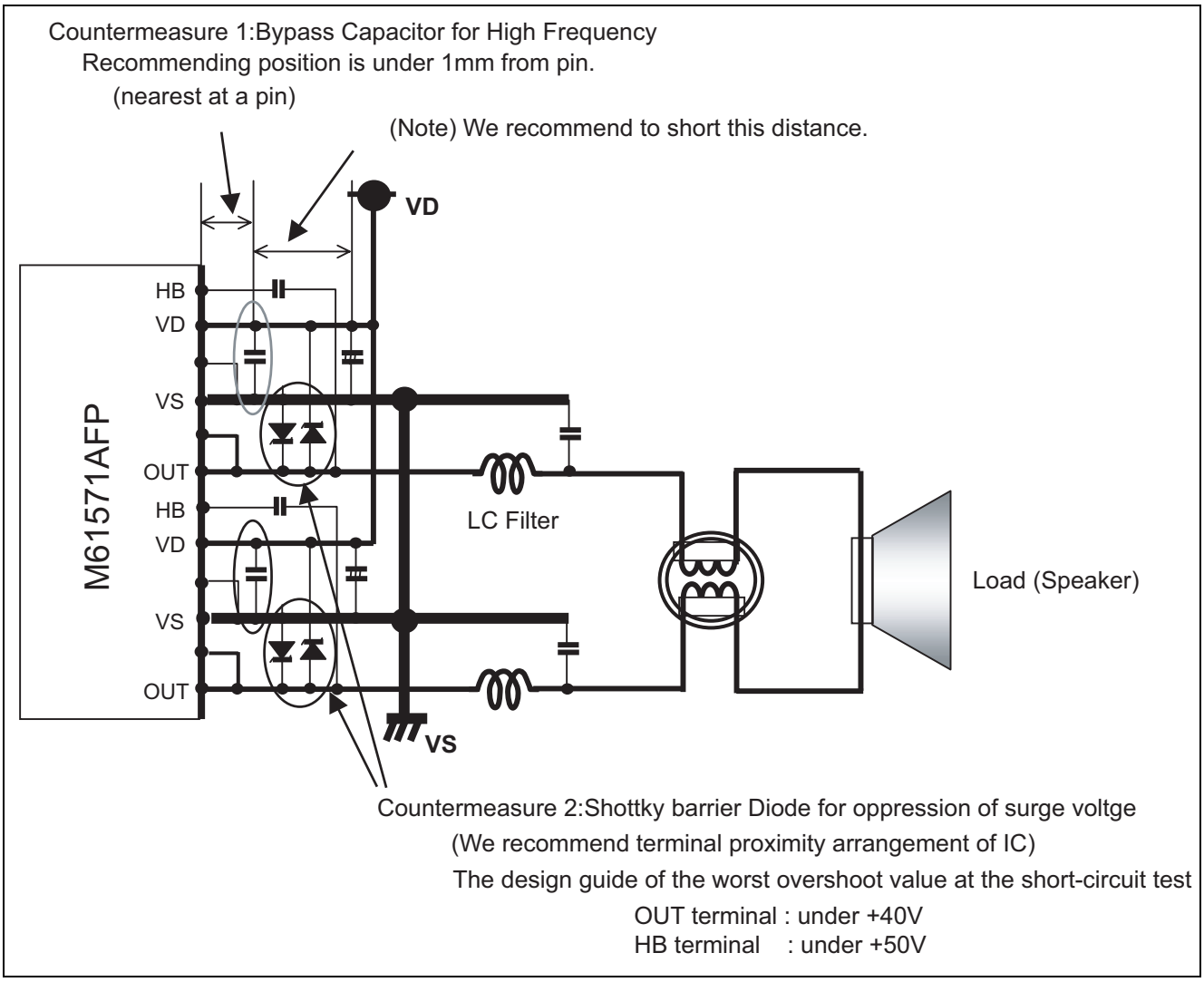
d) Destructive measure

Although this IC built in various protection circuits, there is a case which the unusual current occurs in output terminal at the time of a load short circuit, the output ground short and PWM operation starting. In this case, the overshoot of PWM output becomes very large. If this voltage becomes over absolute maximum supply voltage, there is a case where IC breaks. So, please design the board layout which the voltage for each terminal becomes less than the absolute maximum ratings' supply voltage (5page).

In addition, please design that a guide of maximum over shoot is PWM output=under 40V and HB (Bootstrap) terminal=under 50V.

The typical example of an overshoot measure

(1) The bypass capacitor (Laminated ceramic capacitor) from the power supply of output power transistor (VD) to GND (VS) is arranged at the pin in near. (Recommendation: Under 1mm from the pin). (Refer to the 2 in page14)
(2) Connect to Schottky barrier diode among PWM output (VD) to GND (VS).
(3) Zener diode (35V) is connected between PWM output (VS terminal) to GND (VS), and it prevents so that it is prevented so that the voltage exceeding pressure prevention may not be built over a terminal.
(4) Add to the Snaber circuit of CR in-series composition among the PWM output to GND (VS).

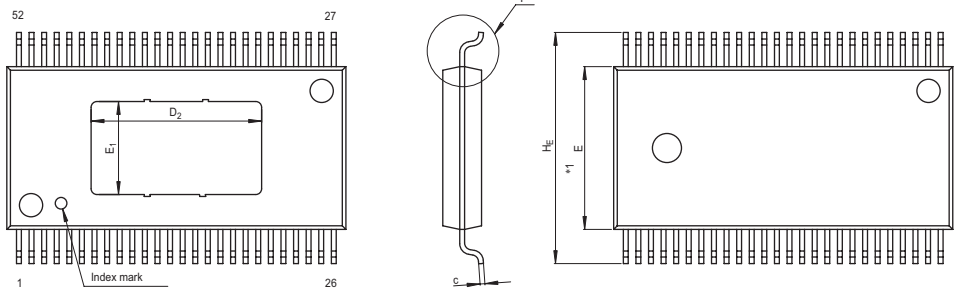


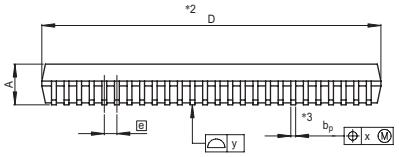
(Note) These descriptions are notes in having our company digital amplifier IC M61571AFP used, and do not guarantee all of the operation and a property.
In a board design, you advise these contents and have it confirmed that operation and a property are satisfactory in your company after IC mounting.

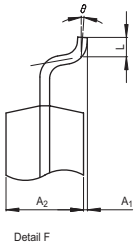
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HSSOP52-8.4x17.5-0.65	PRSP0052JB-B	52P9F-K	0.8g

Under development







Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	17.3	17.5	17.7
E	8.2	8.4	8.6
A_2	—	2.0	—
A	—	—	2.2
A_1	0	0.1	0.2
b_p	0.22	0.27	0.32
c	0.23	0.25	0.3
θ	0°	—	10°
H_E	11.63	11.93	12.23
e	—	0.65	—
x	—	—	0.12
y	—	—	0.10
L	0.3	0.5	0.7
D_2	8.6	8.8	9.0
E_1	4.6	4.8	5.0

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Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .5.0