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May 2009

FST3257 Quad 2:1 Multiplexer / Demultiplexer Bus Switch

Features

- 4Ω Switch Connection Between Two Ports
- Minimal Propagation Delay Through the Switch
- Low I_{CC}
- Zero Bounce in Flow-Through Node
- Control Inputs Compatible with TTL Level

Description

The Fairchild Switch FST3257 is a quad 2:1 high-speed CMOS TTL-compatible multiplexer / demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When /OE is LOW, the select pin connects the A port to the selected B port output. When /OE is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Ordering Information

Part Number	Operating Temperature Range	© Eco Status	Package	Packing Method		
FST3257M	-40 to 85°C	RoHS	16-Lead Small Outline Integrated Circuit			
FST3257MX	-40 to 85°C	KUHS	(SOIC) JEDEC MS-012,0.150 Narrow	Tape and Reel		
FST3257QSC	-40 to 85°C	Green	16-Lead Quarter Size Outline Package	Tubes		
FST3257QSCX	-40 to 85°C	Green	(QSOP) JEDEC MO-137 0.150 Inch Wide	Tape and Reel		
FST3257MTC	-40 to 85°C	RoHS 16-Lead Thin Shrink Small Outline Package		Dalle	16-Lead Thin Shrink Small Outline Package	Tubes
FST3257MTCX	-40 to 85°C	KUHS	(TSSOP) JEDEC MO-153, 4mm Wide	Tape and Reel		

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Pin Assignments

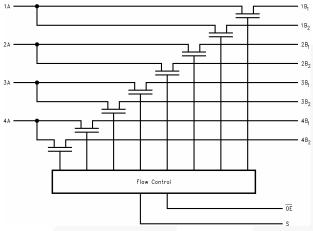


Figure 1. Logic Diagram

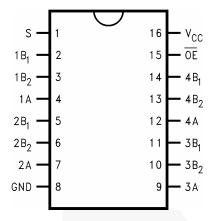


Figure 2. Connection Diagram

Pin Descriptions

Pin #	Names	Description
1	S	Select Input
2, 3, 5, 6, 10, 11, 13, 14	1B ₁ , 1B ₂ , 2B ₁ , 2B ₂ , 3B ₁ , 3B ₂ , 4B ₁ , 4B ₂	Bus B
4, 7, 9, 12	1A, 2A, 3A, 4A	Bus A
8	GND	Ground
15	/OE	Bus Switch Enables
16	VCC	Supply Voltage

Truth Table

Select Inputs	Bus Switch Enabled	Function
S	Logic Level HIGH	Disconnected
Logic Level LOW	Logic Level LOW	A=B ₁
Logic Level HIGH	Logic Level LOW	A=B ₂

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.5	+7.0	V
Vs	DC Switch Voltage	-0.5	+7.0	V
V _{IN}	DC Input Voltage ⁽¹⁾	-0.5	+7.0	V
I _{IK}	DC Input Current		-50	mA
l _{out}	DC Output Sink Current		128	mA
I _{CC} /I _{GND}	DC V _{CC} /GND Current		±100	mA
T _{STG}	Storage Temperature Range	-65	+150	°C

Note:

 The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parame	Min.	Max.	Unit	
Vcc	Power Supply Operating		3.0	5.5	V
V _{IN}	Input Voltage		0	5.5	V
V _{OUT}	Output Voltage		0	5.5	V
4 4.	t _r ,t _f Input Rise and Fall Time	Switch Control Input	0	5	ns/V
t _r ,t _f	Input Rise and Fall Time	Switch I/O	0	DC	115/ V
T _A	Free Air Operating Tempe	erature	-40	+85	°C

Note:

2. Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

	-	0 1141	.,	T _A :			
Symbol	Parameter	Conditions	V _{CC} (V)	Min.	Typ. ⁽³⁾	Max.	Units
V _{IK}	Clamp Diode Voltage	I _{IN} =-18mA	4.5			-1.2	V
VIH	High-Level Input Voltage		3.0 to 3.6 ⁽⁵⁾	1.8			V
VIH	High-Level input voltage		4.0 to 5.5	2.0			V
V_{IL}	Low-Level Input Voltage		3.0 to 3.6 ⁽⁵⁾			0.7	V
۷IL	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I _{IN}	Input Leakage Current	$0 \leq V_{IN} \leq 5.5$	5.5			±1.0	μA
l _{OZ}	Off-state Leakage Current	$0 \le A, B \le V_{CC}$	5.5			±1.0	μΑ
		V _{IN} =0V, I _{IN} =64mA	3.3 ⁽⁵⁾		13	20	
		V _{IN} =0V, I _{IN} =30mA	3.3 ⁽⁵⁾		28	40	
		V _{IN} =2.4V, I _{IN} =15mA	3.3 ⁽⁵⁾		200	230	
В	Switch On Resistance ⁽⁴⁾	V _{IN} =2.4V, I _{IN} =15mA	3.0 ⁽⁵⁾		210	250	
R _{ON}	Switch On Resistance 7	V _{IN} =0V, I _{IN} =64mA	4.5		4	7	Ω
		V _{IN} =0V, I _{IN} =30mA	4.5		4	7	
		V _{IN} =2.4V, I _{IN} =15mA	4.5		8	15	
		V _{IN} =2.4V, I _{IN} =15mA	4.0		11	20	
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND, I _{OUT} =0,	5.5		\	3	μA
Δlcc	Increase in Icc per input	One Input at 3.4V, Other inputs at V _{CC} or GND	5.5			2.5	mA

Notes:

- 3. Typical values are at nominal V_{CC} for the V_{CC} range and $T_A=25$ °C.
- 4. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the A or B pins.
- 5. This parameter is guaranteed by design, but is not tested.

AC Electrical Characteristics

						0 to +85°C, C _L = 50pF, RU=RD=500Ω			Units	Figure
Symbol	Parameter	Conditions		V _{CC} = 4.5 to 5.5V		V _{CC} =4.0V		=3.0 .6V ⁽⁷⁾	Oille	riguie
			Min.	Max.	Min.	Max.	Min.	Max.		
t t	Propagation Delay Bus to Bus ⁽⁶⁾	elay V _{IN=} Open 0.25 0.25		0.25		0.25		Figure 3 Figure 4		
t _{PHL} ,t _{PLH}	Propagation Delay Select to Bus A ⁽⁶⁾			0.23	1.0	6.8	ns			
	Du3 D	e, Select to B V _{IN} =7V for t _{PZL} V _{IN} =0pen for t _{PZH} t _{PZH} 1.0 5.0		5.5	1.0	7.9	- ns	Figure 3 Figure 4		
t _{PZH} ,t _{PZL}	Output Enable Time, Select to Bus /OE				1.0	8.5				
	Output Disable Time, Select to Bus B	V _{IN} =7V for t _{PLZ}	1.5	F 2		F.6	1.0	9.9	20	Figure 3
t _{PHZ} ,t _{PLZ}	Output Disable Time, Select to Bus /OE V _{IN} =Open for t _{PHZ} 1.5 5.3 5.6		5.6	1.5	9.9	ns	Figure 4			

Notes:

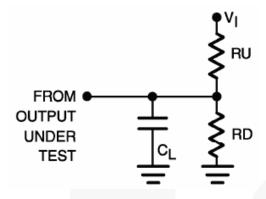
- 6. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).
- 7. These parameters are guaranteed by design, but not tested.

Capacitance

 T_A =+25°C, f=1MHz. Capacitance is characterized by not tested.

Symbol	Parameter		Conditions	Тур.	Max.	Units
C _{IN}	Control Pin Input Capacitance		V _{CC} =5.0V	3.0		pF
		A Port	V _{CC} /OE=5.0V	7.0	Y.	pF
Con	Innut/Output Conscitones	B Port	VCC/OL=5.0V	5.0		ρi
C _{I/O}	Input/Output Capacitance A Port B Port	A Port	V /OF 2.2V	3.0	- y	nE.
		V _{CC} /OE=3.3V	3.5		pF	

AC Loadings and Waveforms



Notes:

- 8. Input driven by 50Ω source terminated in 50Ω .
- 9. CL included load and stray capacitance.
- 10. Input PRR=1.0MHz, tw=500ns.

Figure 3. AC Test Circuit

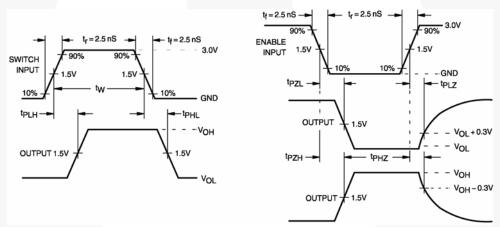


Figure 4. AC Waveforms

Physical Dimensions

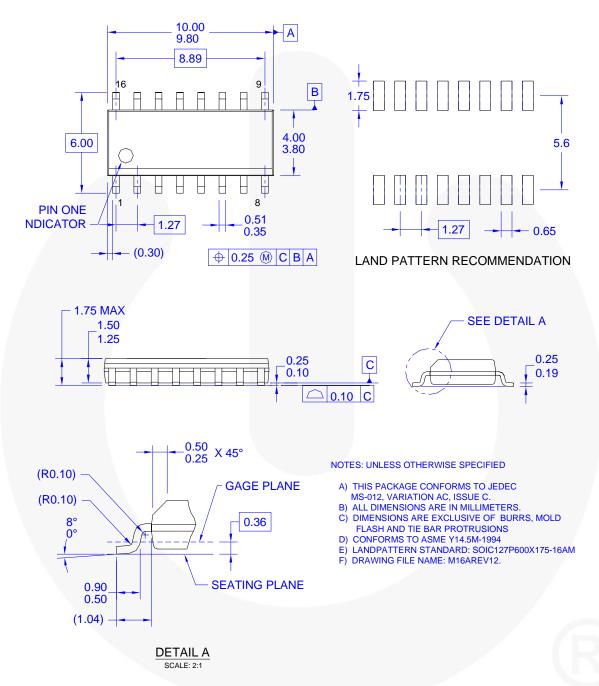


Figure 5. 16-Lead Small Outline Integrated Circuit (SOIC) JEDEC MS-012,0.150 Narrow

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○ 0.10 M A-B [.197] (7.1) (3.7) [.280] [.146] [.154] [.236] (0.635) ○ 0.10 M A-B (0.317) [.025] △ 0.20**M** C 0.635 2X N/2 TIPS [.025 0.27 [.011] **LAND PATTERN** RECOMMENDATION **TOP VIEW** 1.357±0.127 DETAIL A △ 0.10 M C 16 X [.053±0.005] · 10° ±5 0.010 1.6±0.05 [.063±0.002] **END VIEW** SIDE VIEW 0.5 ×45° [.02 ×45°] R0.09 Min NOTES : GAGE .254 PLANE [0.010] A. THIS PACKAGE CONFORMS TO JEDEC MO-137 VARIATION AB B. PRIMARY DIMENSIONS IN MILLIMETERS REFERENCE DIMENSIONS IN INCHES 50-.75 SEATING [0.020-0.0295] PLANE C. DRAWING CONFORMS TO ASME Y14.5M-1994 [0.039] D. DIMENSIONS ARE EXCLUSIVE OF BURRS, **DETAIL A** MOLD FLASH, AND TIE BAR EXTRUSIONS.

Figure 6. 16-Lead Quarter Size Outline Package (QSOP) JEDEC MO-137 0.150 Inch Wide

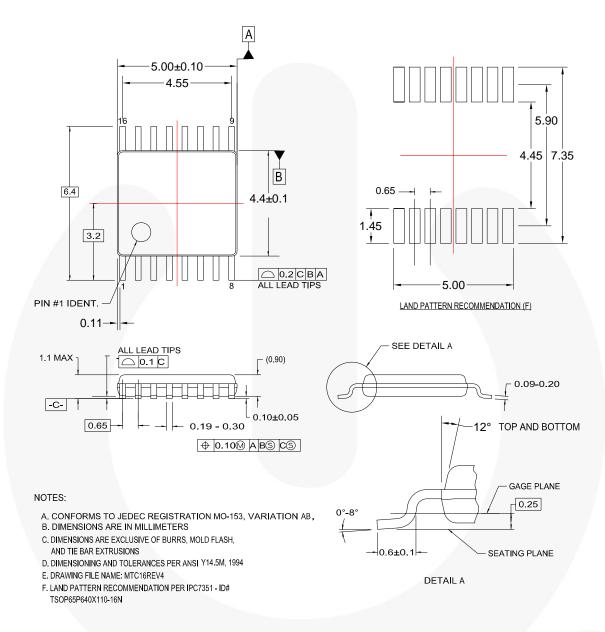
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MQA16AREVB

Physical Dimensions

Physical Dimensions



MTC16rev4

Figure 7. 16-Lead Thin Shrink Small Outline Package (TSSOP) MO-153, 4.4mm Wide

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