

TPS65140/5-Q1 Triple Output LCD Supply with Linear Regulator and Power Good

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1
 - Device HBM ESD Classification Level H2
 - Device CDM ESD Classification Level C5
- Input Voltage Range: 2.7 V to 5.8 V
- V_{O1} Boost Converter
 - Up to 15 V Output Voltage
 - Virtual Synchronous Converter Topology
 - < 1% Output Voltage Accuracy
 - 1.6-MHz Fixed Switching Frequency
 - 2.3-A Switch Current Limit
- V_{O2} Negative Regulated Charge Pump
 - Down to -12 V / 20 mA
- V_{O3} Positive Regulated Charge Pump
 - Up to 30 V / 20 mA
- Three Independently Adjustable Outputs
- Auxiliary 3.3-V Linear Regulator Controller
- Internal Soft Start
- Power Good
- Protection Features
 - Short-Circuit Detection of all Outputs
 - Overvoltage Protection of all Outputs
 - Thermal Shutdown
- Available in TSSOP-24 PowerPAD™ Package

2 Applications

- Infotainment Systems
- Automotive Displays
- Instrument Clusters
- Center Consoles
- Rear Seat Entertainment

3 Description

The TPS65140-Q1 and TPS65145-Q1 devices offer a compact and small power supply solution that provides all three voltages required by thin-film transistor (TFT) LCD displays. The auxiliary linear regulator controller can be used to generate a 3.3-V logic power rail for systems powered by a 5-V supply rail only.

The main output, V_{O1} is a 1.6-MHz fixed-frequency PWM boost converter providing the source-drive voltage for the LCD display. The TPS65140-Q1 device has a typical switch current limit of 2.3 A and the TPS65145-Q1 has a typical switch current limit of 1.37 A.

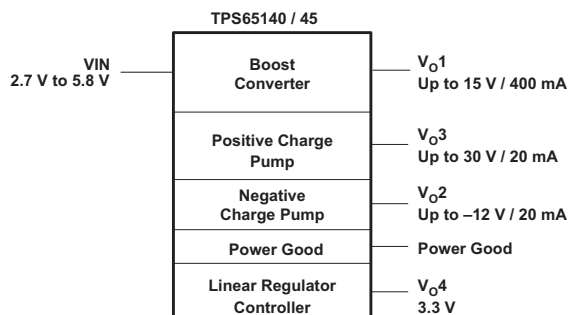
A fully integrated adjustable charge pump doubler and provides the positive LCD gate-drive voltage. An externally adjustable negative charge pump provides the negative LCD gate-drive voltage.

Device Information⁽¹⁾

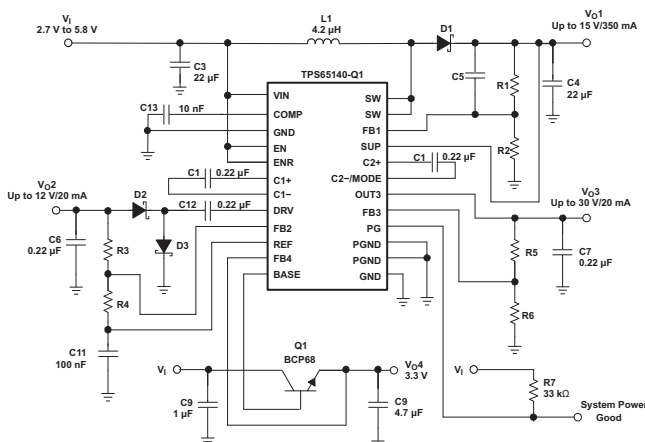
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------------------|-----------------------------|-------------------|
| TPS65140-Q1 TPS65145-Q1 | TSSOP (24) with PowerPAD | 4.40 mm × 7.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Device Block Diagram



Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (April 2008) to Revision B | Page |
|---|------|
| • Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>Specifications</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Dissipation Ratings</i> table and added <i>Thermal Information</i> and <i>ESD Ratings</i> tables..... | 4 |
| • Changed from T_A to T_J in the Conditions statement of <i>Electrical Characteristics</i> and changed temperature from 85°C to 125°C..... | 5 |
| • Changed the MAIN BOOST CONVERTER V_{REF} spec from 1.205 MIN to 1.198, and MAX from 1.219 to 1.230 | 5 |
| • Changed the MAIN BOOST CONVERTER V_{FB} spec from 1.136 MIN to 1.126, and MAX from 1.154 to 1.161 | 5 |
| • Changed the MAIN BOOST CONVERTER $r_{DS(ON)}$ spec for $V_{O1} = 10\text{ V}$, $I_{sw} = 500\text{ mA}$ condition, from 290 to 325 MAX; and, for the $V_{O1} = 5\text{ V}$, $I_{sw} = 500\text{ mA}$ condition, changed from 420 to 455 MAX..... | 5 |
| • Changed the MAIN BOOST CONVERTER f_{SW} spec for $0^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ condition from 1.295 MIN to 1.195 MIN; and, for the $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ condition, changed the MIN from 1.191 to 1.091..... | 6 |
| • Changed the NEGATIVE CHARGE PUMP $V_{O2} V_{ref}$ spec from 1.205 MIN to 1.198, and MAX from 1.219 to 1.226 | 6 |
| • Changed from T_A to T_J in the Conditions statement of <i>Electrical Characteristics</i> and changed temperature from 85°C to 125°C..... | 6 |
| • Changed the POSITIVE CHARGE PUMP $V_{O3} V_{ref}$ spec from 1.205 MIN to 1.198, and MAX from 1.219 to 1.226 | 6 |
| • Changed the POSITIVE CHARGE PUMP V_{FB} spec from 1.187 MIN to 1.180, and MAX from 1.238 to 1.245 | 6 |
| • Changed the POSITIVE CHARGE PUMP $V_{O3} V_o$ spec from 720 mV MAX to 800 mV | 6 |
| • Changed from T_A to T_J in the Conditions statement of <i>Electrical Characteristics</i> and changed temperature from 85°C to 125°C..... | 7 |

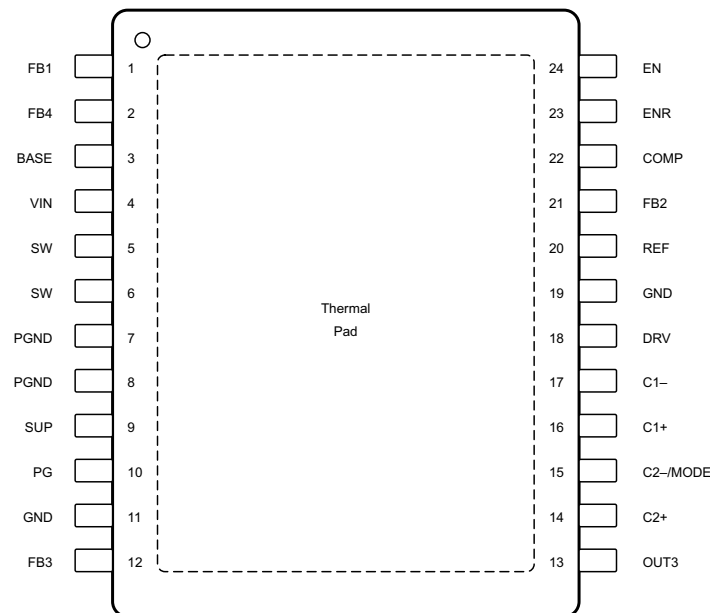
5 Description (Continued)

For compensation of the devices please refer to Application Note: *How to Compensate with the TPS6510x and TPS6514x* [SLVA813](#).

6 Device Comparison

| PART NUMBER | LINEAR REGULATOR OUTPUT VOLTAGE | MINIMUM SWITCH CURRENT LIMIT |
|-------------|---------------------------------|------------------------------|
| TPS65140-Q1 | 3.3 V | 1.6 A |
| TPS65145-Q1 | 3.3 V | 0.96 A |

7 Pin Configuration and Functions



Pin Functions

| TERMINAL | | I/O | DESCRIPTION |
|----------|-----------|-----|--|
| NAME | NO. (PWP) | | |
| VIN | 4 | I | Input voltage pin of the device. |
| EN | 24 | I | Enable pin of the device. This pin should be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device. |
| COMP | 22 | | Compensation pin for the main boost converter. A small capacitor is connected to this pin. |
| PG | 10 | O | Open drain output indicating when all outputs Vo1, Vo2, Vo3 are within 10% of their nominal output voltage. The output goes low when one of the outputs falls below 10% of their nominal output voltage. |
| ENR | 23 | I | Enable pin of the linear regulator controller. This pin should be terminated and not be left floating. Logic high enables the regulator and a logic low puts the regulator in shutdown. |
| C1+ | 16 | | Positive terminal of the charge pump flying capacitor |
| C1- | 17 | | Negative terminal of the charge pump flying capacitor |
| DRV | 18 | O | External charge pump driver |
| FB2 | 21 | I | Feedback pin of negative charge pump |
| REF | 20 | O | Internal reference output typically 1.23 V |
| FB4 | 2 | I | Feedback pin of the linear regulator controller. The linear regulator controller is set to a fixed output voltage of 3.3 V or 3 V depending on the version. |
| BASE | 3 | O | Base drive output for the external transistor |
| GND | 11, 19 | | Ground |

Pin Functions (continued)

| TERMINAL | | I/O | DESCRIPTION |
|---------------------------|-----------|-----|---|
| NAME | NO. (PWP) | | |
| PGND | 7, 8 | | Power ground |
| FB3 | 12 | I | Feedback pin of positive charge pump |
| OUT3 | 13 | O | Positive charge pump output |
| C2-/MODE | 15 | | Negative terminal of the charge pump flying capacitor and charge pump MODE pin. If the flying capacitor is connected to this pin, the converter operates in a voltage tripler mode. If the charge pump needs to operate in a voltage doubler mode, the flying capacitor is removed and the C2-/MODE pin needs to be connected to GND. |
| C2+ | 14 | | Positive terminal for the charge pump flying capacitor. If the device runs in voltage doubler mode, this pin needs to be left open. |
| SUP | 9 | I | Supply pin of the positive, negative charge pump, boost converter, and gate drive circuit. This pin needs to be connected to the output of the main boost converter and cannot be connected to any other voltage source. For performance reasons, it is not recommended for a bypass capacitor to be connected directly to this pin. |
| FB1 | 1 | I | Feedback pin of the boost converter |
| SW | 5, 6 | I | Switch pin of the boost converter |
| PowerPAD™/ Thermal Die | | | The PowerPAD or exposed thermal die needs to be connected to the power ground pins (PGND). |

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|--|---|------------------------|------|
| Voltages on pin VIN ⁽²⁾ | -0.3 | 6 | V |
| Voltages on pin Vo1, SUP, PG ⁽²⁾ | -0.3 | 15.5 | V |
| Voltages on pin EN, MODE, ENR ⁽²⁾ | -0.3 | V _I + 0.3 V | V |
| Voltage on pin SW ⁽²⁾ | | 20 | V |
| Power good maximum sink current (PG) | | 1 | mA |
| Continuous power dissipation | See Thermal Information | | |
| Operating junction temperature | -40 | 150 | °C |
| Storage temperature, T _{stg} | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

8.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 |
| | | Machine model (MM) | ±100 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 Recommended Operating Conditions

| | | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------|-----|-----|-----|------|
| V _{IN} | Input voltage range | 2.7 | | 5.8 | V |
| L | Inductor ⁽¹⁾ | | 4.7 | | μH |
| T _J | Operating junction temperature | -40 | | 125 | °C |

- (1) See the *Application Information Section* for further information.

8.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS65140-Q1 | TPS65145-Q1 | UNIT |
|-------------------------------|--|-------------|-------------|------|
| | | PWP (TSSOP) | PWP (TSSOP) | |
| | | 24 PINS | 24 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 32.3 | 32.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 25.8 | 25.8 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 9.2 | 9.2 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.5 | 0.5 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 9.4 | 9.4 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 2.7 | 2.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

8.5 Electrical Characteristics

V_{IN} = 3.3 V, EN = V_{IN}, Vo1 = 10 V, T_J = -40°C to 125°C, typical values are at T_J = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------------------|--|--|-------|-------|------|---|
| SUPPLY CURRENT | | | | | | |
| V _{IN} | Input voltage range | 2.7 | | 5.5 | V | |
| I _{QIN} | Quiescent current into VIN | ENR = GND, Vo3 = 2 × Vo1, Boost converter not switching | 0.7 | 0.9 | mA | |
| I _{QCharge} | Charge pump quiescent current into SUP | Vo1 = SUP = 10 V, Vo3 = 2 × Vo1 | 1.7 | 2.7 | mA | |
| | | Vo1 = SUP = 10 V, Vo3 = 3 × Vo1 | 3.9 | 6 | | |
| I _{QEN} | LDO controller quiescent current into VIN | ENR = VIN, EN = GND | 300 | 800 | μA | |
| I _{SD} | Shutdown current into VIN | EN = ENR = GND | 1 | 10 | μA | |
| V _{UVLO} | Undervoltage lockout threshold | V _I falling | 2.2 | 2.4 | V | |
| | Thermal shutdown | Temperature rising | 160 | | °C | |
| LOGIC SIGNALS EN, ENR | | | | | | |
| V _{IH} | High level input voltage | 1.5 | | | V | |
| V _{IL} | Low level input voltage | | | 0.4 | V | |
| I _I | Input leakage current | EN = GND or VIN | 0.01 | 0.1 | μA | |
| MAIN BOOST CONVERTER | | | | | | |
| Vo1 | Output voltage range | 5 | | 15 | V | |
| V _{O1-VIN} | Minimum input to output voltage difference | 1 | | | V | |
| V _{REF} | Reference voltage | 1.198 | 1.213 | 1.230 | V | |
| V _{FB} | Feedback regulation voltage | 1.126 | 1.146 | 1.161 | V | |
| I _{FB} | Feedback input bias current | | 10 | 100 | nA | |
| r _{DS(on)} | N-MOSFET on-resistance (Q1) | Vo1 = 10 V, I _{sw} = 500 mA | 195 | 325 | mΩ | |
| | | Vo1 = 5 V, I _{sw} = 500 mA | 285 | 455 | | |
| I _{LIM} | N-MOSFET switch current limit (Q1) | TPS65140 | 1.6 | 2.3 | 2.8 | A |
| | | TPS65145 | 0.96 | 1.37 | 1.7 | A |
| r _{DS(on)} | P-MOSFET on-resistance (Q2) | Vo1 = 10 V, I _{sw} = 100 mA | 9 | 15 | Ω | |
| | | Vo1 = 5 V, I _{sw} = 100 mA | 14 | 22 | | |
| I _{MAX} | Maximum P-MOSFET peak switch current | | | 1 | A | |
| I _{leak} | Switch leakage current | V _{sw} = 15 V | 1 | 10 | μA | |
| | | V _{sw} = 0 V | 1 | 10 | | |

Electrical Characteristics (continued)

$V_{IN} = 3.3\text{ V}$, $EN = V_{IN}$, $Vo1 = 10\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|--|-------|-------|-------|----------|
| f_{SW} | Oscillator frequency | $0^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 1.195 | 1.6 | 2.1 | MHz |
| | | $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ | 1.091 | 1.6 | 2.1 | |
| | Line regulation | $2.7\text{ V} \leq V_I \leq 5.7\text{ V}$; $I_{load} = 100\text{ mA}$ | | 0.012 | | %/V |
| | Load regulation | $0\text{ mA} \leq I_O \leq 300\text{ mA}$ | | 0.2 | | %/A |
| NEGATIVE CHARGE PUMP Vo2 | | | | | | |
| $Vo2$ | Output voltage range | | -2 | | | V |
| V_{ref} | Reference voltage | | 1.198 | 1.213 | 1.226 | V |
| V_{FB} | Feedback regulation voltage | | -36 | 0 | 36 | mV |
| I_{FB} | Feedback input bias current | | | 10 | 100 | nA |
| $r_{DS(on)}$ | Q8 P-Channel switch $r_{DS(on)}$ | $I_O = 20\text{ mA}$ | | 4.3 | 8 | Ω |
| | Q9 N-Channel switch $r_{DS(on)}$ | | | 2.9 | 4.4 | |
| I_O | Minimum output current | | 20 | | | mA |
| | Line regulation | $7\text{ V} \leq Vo1 \leq 15\text{ V}$, $I_{load} = 10\text{ mA}$, $Vo2 = -5\text{ V}$ | | 0.09 | | %/V |
| | Load regulation | $1\text{ mA} \leq I_O \leq 20\text{ mA}$, $Vo2 = -5\text{ V}$ | | 0.126 | | %/mA |
| POSITIVE CHARGE PUMP Vo3 | | | | | | |
| $Vo3$ | Output voltage range | | | | 30 | V |
| V_{ref} | Reference voltage | | 1.198 | 1.213 | 1.226 | V |
| V_{FB} | Feedback regulation voltage | | 1.180 | 1.214 | 1.245 | V |
| I_{FB} | Feedback input bias current | | | 10 | 100 | nA |
| $r_{DS(on)}$ | Q3 P-Channel switch $r_{DS(on)}$ | $I_O = 20\text{ mA}$ | | 9.9 | 15.5 | Ω |
| | Q4 N-Channel switch $r_{DS(on)}$ | | | 1.1 | 1.8 | |
| | Q5 P-Channel switch $r_{DS(on)}$ | | | 4.6 | 8.5 | |
| | Q6 N-Channel switch $r_{DS(on)}$ | | | 1.2 | 2.2 | |
| V_d | D1 – D4 Schottky diode forward voltage | $I_{D1-D4} = 40\text{ mA}$ | | 610 | 800 | mV |
| I_O | Minimum output current | | 20 | | | mA |
| | Line regulation | $10\text{ V} \leq Vo1 \leq 15\text{ V}$, $I_{load} = 10\text{ mA}$, $Vo3 = 27\text{ V}$ | | 0.56 | | %/V |
| | Load regulation | $1\text{ mA} \leq I_O \leq 20\text{ mA}$, $Vo3 = 27\text{ V}$ | | 0.05 | | %/mA |

Electrical Characteristics (continued)

$V_{IN} = 3.3\text{ V}$, $EN = V_{IN}$, $Vo1 = 10\text{ V}$, $T_J = -40^\circ\text{C}$ to 125°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------------------------|--|------|------------|-----|---------------|
| LINEAR REGULATOR CONTROLLER Vo4 | | | | | | |
| Vo4 | Output voltage | $4.5\text{ V} \leq V_I \leq 5.5\text{ V}$; $10\text{ mA} \leq I_O \leq 500\text{ mA}$ | 3.2 | 3.3 | 3.4 | V |
| I_{BASE} | Maximum base drive current | $V_{IN} - Vo4 - V_{BE} \geq 0.5\text{ V}^{(1)}$ | 13.5 | 19 | | mA |
| | | $V_{IN} - Vo4 - V_{BE} \geq 0.75\text{ V}^{(1)}$ | 20 | 27 | | |
| | Line regulation | $4.75\text{ V} \leq V_I \leq 5.5\text{ V}$, $I_{load} = 500\text{ mA}$ | | 0.186 | | %/V |
| | Load regulation | $1\text{ mA} \leq I_O \leq 500\text{ mA}$, $V_I = 5\text{ V}$ | | 0.064 | | %/A |
| | Start up current | $Vo4 \leq 0.8\text{ V}$ | 11 | 20 | 25 | mA |
| SYSTEM POWER GOOD (PG) | | | | | | |
| $V_{(PG, VO1)}$ | Power good threshold ⁽²⁾ | | -12 | -8.75% Vo1 | -6 | V |
| $V_{(PG, VO2)}$ | | | -13 | -9.5% Vo2 | -5 | V |
| $V_{(PG, VO3)}$ | | | -11 | -8% Vo3 | -5 | V |
| V_{OL} | PG output low voltage | $I_{(sink)} = 500\text{ }\mu\text{A}$ | | | 0.3 | V |
| I_L | PG output leakage current | $V_{PG} = 5\text{ V}$ | | 0.001 | 1 | μA |

(1) With V_{IN} = supply voltage of the TPS65140, $Vo4$ = output voltage of the regulator, V_{BE} = basis emitter voltage of external transistor.

(2) The power good goes high when all three outputs ($Vo1$, $Vo2$, $Vo3$) are above their threshold. The power good goes low as soon as one of the outputs is below their threshold.

9 Typical Characteristics

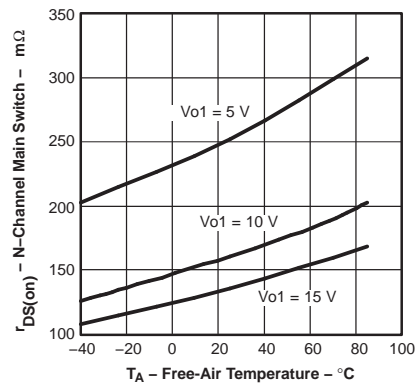


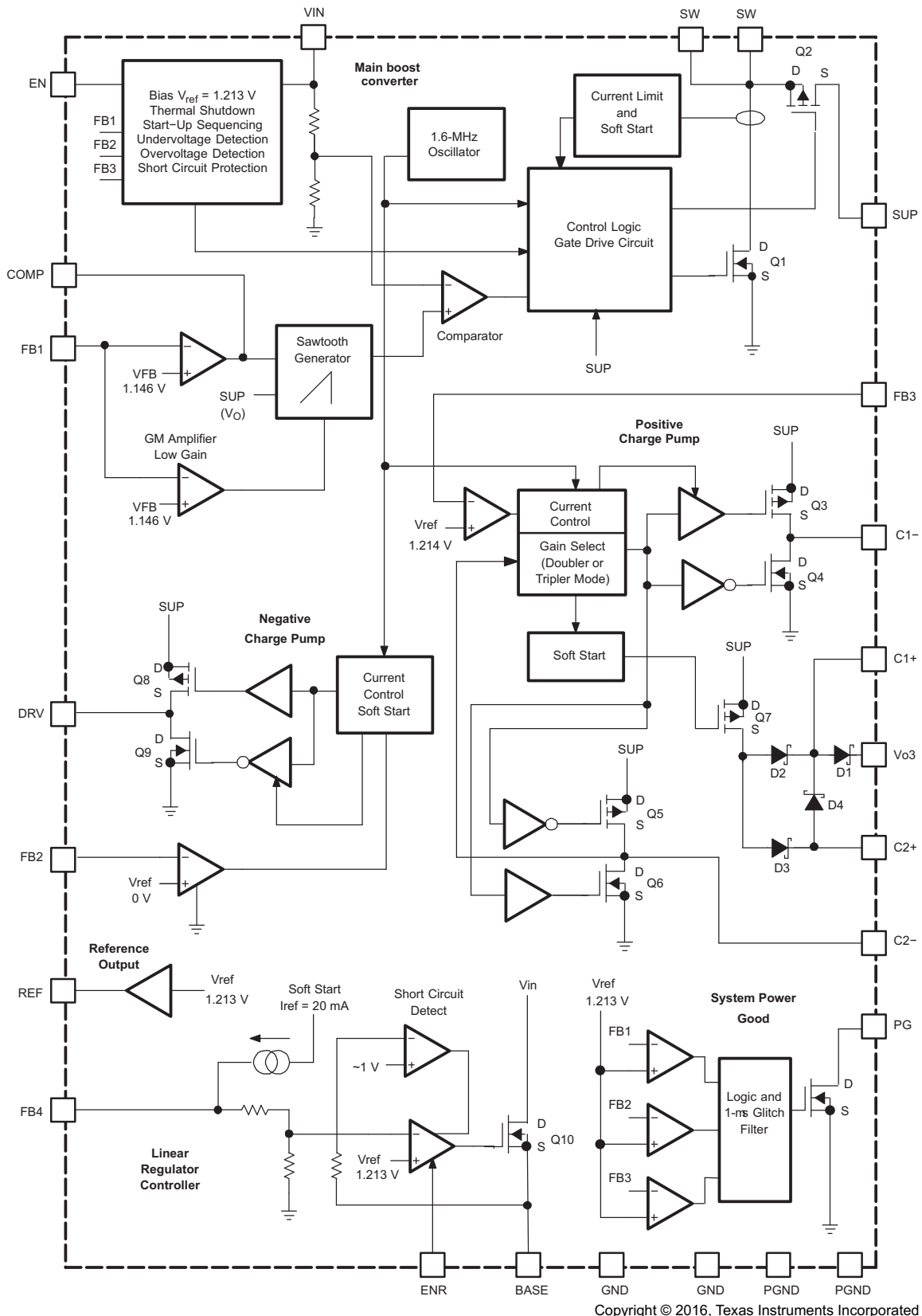
Figure 1. $r_{DS(on)}$ N-Channel Main Switch vs Free-air Temperature

10 Detailed Description

10.1 Overview

The TPS65140-Q1 and TPS65145-Q1 devices consist of a main boost converter operating with a fixed switching frequency of 1.6 MHz to allow for small external components. The boost converter output voltage V_{o1} is also the input voltage for the positive and negative charge pump, connected via the pin SUP. The linear regulator controller is independent from this system with its own enable pin. This allows the linear regulator controller to continue to operate while the other supply rails are disabled or in shutdown due to a fault condition on one of their outputs. Refer to the functional block diagram for more information.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Main Boost Converter

The main boost converter operates with PWM and a fixed switching frequency of 1.6 MHz. The converter uses a unique fast response, voltage mode controller scheme with input voltage feedforward. This achieves excellent line and load regulation (0.2% A load regulation typical) and allows the use of small external components. To add higher flexibility to the selection of external component values, the device uses external loop compensation. Although the boost converter looks like a nonsynchronous boost converter topology operating in discontinuous mode at light load, both devices maintain continuous conduction even at light load currents.

This is achieved with a novel architecture using an external Schottky diode and an integrated MOSFET in parallel connected between SW and SUP (see the functional block diagram). The integrated MOSFET Q2 allows the inductor current to become negative at light load conditions. For this purpose, a small integrated P-channel MOSFET with typically $10\ \Omega$ $r_{DS(on)}$ is sufficient. When the inductor current is positive, the external Schottky diode with the lower forward voltage conducts the current. This causes the converter to operate with a fixed frequency in continuous conduction mode over the entire load current range. This avoids the ringing on the switch pin as seen with a standard nonsynchronous boost converter and allows a simpler compensation for the boost converter.

10.3.2 Power-Good Output

The TPS65140-Q1 and TPS65145-Q1 have an open-drain power-good output with a maximum sink capability of 1 mA. The power-good output goes high as soon as the main boost converter Vo1 and the negative and the positive charge pumps are within regulation. The power-good output goes low as soon as one of the outputs is out of regulation. In this case, the device goes into shutdown at the same time. See the electrical characteristics table for the power-good thresholds.

10.4 Device Functional Modes

10.4.1 Enable and Power-On Sequencing (EN, ENR)

The device has two enable pins. These pins should be terminated and not left floating to prevent faulty operation. Pulling the enable pin (EN) high enables the device and starts the power-on sequencing with the main boost converter Vo1 coming up first, then the negative and positive charge pumps. The linear regulator has an independent enable pin (ENR). Pulling this pin low disables the regulator, and pulling this pin high enables this regulator.

If the enable pin (EN) is pulled high, the device starts its power-on sequencing. The main boost converter starts up first with its soft start. If the output voltage has reached 91.25% of its output voltage, the negative charge pump comes up next. The negative charge pump starts with a soft start and when the output voltage has reached 91% of the nominal value, the positive charge pump comes up with the soft start.

Pulling the enable pin low shuts down the device. Dependent on load current and output capacitance, each of the outputs comes down.

10.4.2 Positive Charge Pump

The TPS65140-Q1 and TPS65145-Q1 has a fully regulated integrated positive charge pump generating Vo3. The input voltage for the charge pump is applied to the SUP pin that is equal to the output of the main boost converter Vo1. The charge pump is capable of supplying a minimum load current of 20 mA. Higher load currents are possible depending on the voltage difference between Vo1 and Vo3. See [Figure 13](#) and [Figure 14](#).

10.4.3 Negative Charge Pump

The TPS65140-Q1 and TPS65145-Q1 has a regulated negative charge pump using two external Schottky diodes. The input voltage for the charge pump is applied to the SUP pin that is connected to the output of the main boost converter Vo1. The charge pump inverts the main boost converter output voltage and is capable of supplying a minimum load current of 20 mA. Higher load currents are possible depending on the voltage difference between Vo1 and Vo2. See [Figure 12](#).

Device Functional Modes (continued)

10.4.4 Linear Regulator Controller

The TPS65140-Q1 and TPS65145-Q1 includes a linear regulator controller to generate a 3.3-V rail which is useful when the system is powered from a 5-V supply. The regulator is independent from the other voltage rails of the device and has its own enable (ENR).

10.4.5 Soft Start

The main boost converter as well as the charge pumps and linear regulator have an internal soft start. This avoids heavy voltage drops at the input voltage rail or at the output of the main boost converter Vo1 during start-up caused by high inrush currents. See [Figure 10](#) and [Figure 11](#).

10.4.6 Fault Protection

All of the outputs of the TPS65140-Q1 and TPS65145-Q1 devices have short-circuit detection and cause the device to go into shutdown. The main boost converter has overvoltage and undervoltage protection. If the output voltage Vo1 rises above the overvoltage protection threshold of typically 5% of Vo1, then the device stops switching, but remains operational.

When the output voltage falls below this threshold, the converter continues operation. When the output voltage falls below the undervoltage protection threshold of typically 8.75% of Vo1, because of a short-circuit condition, the devices go into shutdown. Because there is a direct pass from the input to the output through the diode, the short-circuit condition remains. If this condition needs to be avoided, a fuse at the input or an output disconnect using a single transistor and resistor is required. The negative and positive charge pumps have an undervoltage lockout (UVLO) to protect the LCD panel of possible latch-up conditions due to a short-circuit condition or faulty operation. When the negative output voltage is typically above 9.5% of its output voltage (closer to ground), then the device enters shutdown. When the positive charge pump output voltage, Vo3, is below 8% typical of its output voltage, the device goes into shutdown. See the fault protection thresholds in the electrical characteristics table. The device is enabled by toggling the enable pin (EN) below 0.4 V or by cycling the input voltage below the UVLO of 1.7 V. The linear regulator reduces the output current to 20 mA typical under a short-circuit condition when the output voltage is typically < 1 V. See the [Functional Block Diagram](#). The linear regulator does not go into shutdown under a short-circuit condition.

10.4.7 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown threshold is 160°C. If this temperature is reached, the device goes into shutdown. The device can be enabled by toggling the enable pin to low and back to high or by cycling the input voltage to GND and back to Vi again.

11 Application and Implementation

NOTE

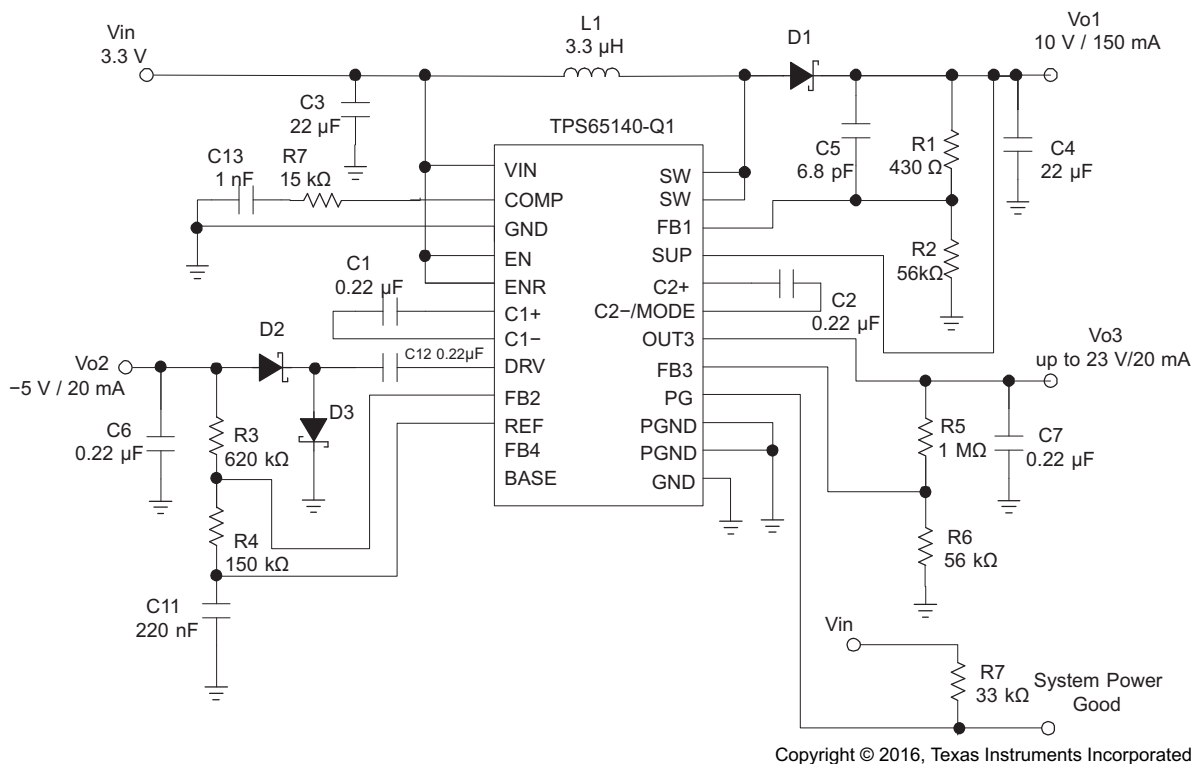
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

This section describes the design of a boost converter example for a 3.3-V to 10-V conversion.

11.2 Typical Application

A typical application requirement is to boost a 3.3-V or 5-V input to a 10-V, 13.5-V, or 15-V output. The section explains the step-by-step development.



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11.2.1 Design Requirements

Table 1 shows the design parameters for this example.

Table 1. Design Requirements

| PARAMETER | Example Value | VALUE |
|-----------------|--|---------------|
| V _I | Input supply voltage | 3.3 V |
| V _{O1} | Boost converter output voltage and current | 10 V @ 300 mA |
| V _{O3} | Positive charge pump output voltage and current | 23 V @ 20 mA |
| V _{O2} | Negative charge pump output voltage and current | -5 V @ 20 mA |
| V _{O4} | Linear regulator controller output voltage and current | 3.3 V |

Table 1. Design Requirements (continued)

| PARAMETER | | Example Value | VALUE |
|-----------------|--------------------------------|---------------|-------|
| V _{SW} | Switch voltage drop | 0.5 V | — |
| V _D | Schottky diode forward voltage | 0.8 V | — |

11.2.2 Detailed Design Procedure

11.2.2.1 Boost Converter Design Procedure

The first step in the design procedure is to calculate the maximum possible output current of the main boost converter under certain input and output voltage conditions.

1. Duty cycle:

$$D = \frac{V_{\text{out}} + V_D - V_{\text{in}}}{V_{\text{out}} + V_D - V_{\text{sw}}} = \frac{10 \text{ V} + 0.8 \text{ V} - 3.3 \text{ V}}{10 \text{ V} + 0.8 \text{ V} - 0.5 \text{ V}} = 0.73 \quad (1)$$

2. Average inductor current:

$$I_L = \frac{I_{\text{out}}}{1 - D} = \frac{300 \text{ mA}}{1 - 0.73} = 1.11 \text{ A} \quad (2)$$

3. Inductor peak-to-peak ripple current:

$$\Delta i_L = \frac{[V_{\text{in}} - V_{\text{sw}}] \times D}{f_s \times L} = \frac{(3.3 \text{ V} - 0.5 \text{ V}) \times 0.73}{1.6 \text{ MHz} \times 4.2 \mu\text{H}} = 304 \text{ mA} \quad (3)$$

4. Peak switch current:

$$I_{\text{swpeak}} = I_L + \frac{\Delta i_L}{2} = 1.11 \text{ A} + \frac{304 \text{ mA}}{2} = 1.26 \text{ A} \quad (4)$$

The integrated switch, the inductor, and the external Schottky diode must be able to handle the peak switch current. The calculated peak switch current has to be equal or lower to the minimum N-MOSFET switch current limit as specified in the electrical characteristics table (1.6 A for the TPS65140 and 0.96 A for the TPS65145). If the peak switch current is higher, then the converter cannot support the required load current. This calculation must be done for the minimum input voltage where the peak switch current is highest. The calculation includes conduction losses like switch $r_{\text{DS(on)}}$ (0.5 V) and diode forward drop voltage losses (0.8 V). Additional switching losses, inductor core and winding losses, etc., require a slightly higher peak switch current in the actual application. The above calculation still allows for a good design and component selection.

11.2.2.1.1 Set the Output Voltage V_{O1} and Select the Feedforward Capacitor

The output voltage is set by the external resistor divider and is calculated as:

$$V_{\text{out}} = 1.146 \text{ V} \times \left[1 + \frac{R1}{R2} \right] \quad (5)$$

Across the upper resistor, a bypass capacitor is required to speed up the circuit during load transients as shown in [Figure 2](#).

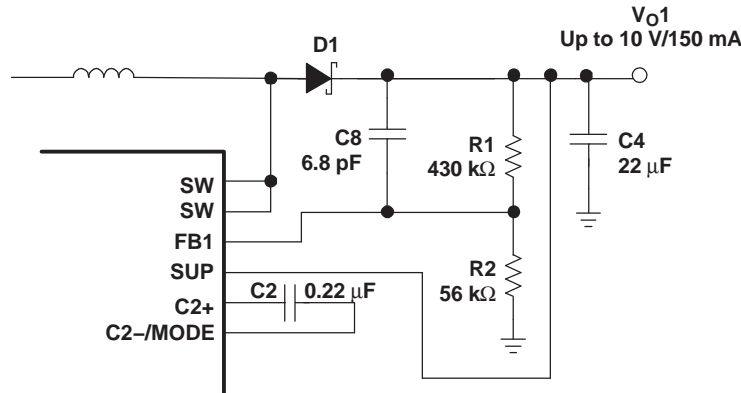


Figure 2. Feed-forward Capacitor

Together with R1 the bypass capacitor C8 sets a zero in the control loop at approximately 50 kHz:

$$C8 = \frac{1}{2 \times \pi \times f_z \times R1} = \frac{1}{2 \times \pi \times 50 \text{ kHz} \times R1} \quad (6)$$

A value closest to the calculated value should be used. Larger feedforward capacitor values reduce the load regulation of the converter and cause load steps as shown in Figure 15.

11.2.2.1.2 Inductor Selection

Several inductors work with the TPS65140. Especially with the external compensation, the performance can be adjusted to the specific application requirements. The main parameter for the inductor selection is the saturation current of the inductor, which should be higher than the peak switch current as calculated above with additional margin to cover for heavy load transients and extreme start-up conditions. Another method is to choose the inductor with a saturation current at least as high as the minimum switch current limit of 1.6 A for the TPS65140 and 0.96 A for the TPS65145. The different switch current limits allow selection of a physically smaller inductor when less output current is required. The second important parameter is the inductor dc resistance. Usually, the lower the dc resistance, the higher the efficiency. However, the inductor dc resistance is not the only parameter determining the efficiency. Especially for a boost converter where the inductor is the energy storage element, the type and material of the inductor influences the efficiency as well. Especially at high switching frequencies of 1.6 MHz, inductor core losses, proximity effects, and skin effects become more important. Usually, an inductor with a larger form factor yields higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS65140, inductor values between 3.3 μH and 6.8 μH are a good choice but other values can be used as well. Possible inductors are shown in Table 2.

Table 2. Inductor Selection

| DEVICE | INDUCTOR VALUE | COMPONENT SUPPLIER ⁽¹⁾ | DIMENSIONS | ISAT/DCR |
|----------|----------------|-----------------------------------|--------------|--------------|
| TPS65140 | 4.7 μH | Coilcraft DO1813P-472HC | 8.89*6.1*5.0 | 2.6 A/54 mΩ |
| | 4.2 μH | Sumida CDRH5D28 4R2 | 5.7*5.7*3 | 2.2 A/23 mΩ |
| | 4.7 μH | Sumida CDC5D23 4R7 | 6*6*2.5 | 1.6 A/48 mΩ |
| | 3.3 μH | Wuerth Elektronik 744042003 | 4.8*4.8*2.0 | 1.8 A/65 mΩ |
| | 4.2 μH | Sumida CDRH6D12 4R2 | 6.5*6.5*1.5 | 1.8 A/60 mΩ |
| | 3.3 μH | Sumida CDRH6D12 3R3 | 6.5*6.5*1.5 | 1.9 A/50 mΩ |
| TPS65145 | 3.3 μH | Sumida CDPH4D19 3R3 | 5.1*5.1*2.0 | 1.5 A/26 mΩ |
| | 3.3 μH | Coilcraft DO1606T-332 | 6.5*5.2*2.0 | 1.4 A/120 mΩ |
| | 3.3 μH | Sumida CDRH2D18/HP 3R3 | 3.2*3.2*2.0 | 1.45 A/69 mΩ |
| | 4.7 μH | Wuerth Elektronik 744010004 | 5.5*3.5*1.0 | 1.0 A/260 mΩ |
| | 3.3 μH | Coilcraft LPO6610-332M | 6.6*5.5*1.0 | 1.3 A/160 mΩ |

(1) See [Third-party Products Disclaimer](#)

11.2.2.1.3 Output Capacitor Selection

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value but depending on the application, tantalum capacitors can be used as well. A 22-μF ceramic output capacitor works for most of the applications. Higher capacitor values can be used to improve load transient regulation. See [Table 3](#) for the selection of the output capacitor. The output voltage ripple can be calculated as:

$$\Delta V_{out} = \frac{I_{out}}{C_{out}} \times \left[\frac{1}{f_s} - \frac{I_p \times L}{V_{out} + V_d - V_{in}} \right] + I_p \times ESR \quad (7)$$

with:

- I_p = Peak current as described in the previous section peak current control
- L = Selected inductor value
- I_{out} = Nominal load current
- f_s = Switching frequency
- V_d = Rectifier diode forward voltage (typically 0.3 V)
- C_{out} = Selected output capacitor
- ESR = Output capacitor ESR value

11.2.2.1.4 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 22-μF ceramic input capacitor is sufficient for most of applications. For better input voltage filtering, this value can be increased. See [Table 3](#) and the *Typical Applications* section for input capacitor recommendations.

Table 3. Input and Output Capacitors Selection

| CAPACITOR | VOLTAGE RATING | COMPONENT SUPPLIER ⁽¹⁾ | COMMENTS |
|------------|----------------|-----------------------------------|------------------|
| 22 μF/1210 | 16 V | Taiyo Yuden EMK325BY226MM | C _{OUT} |
| 22 μF/1206 | 6.3 V | Taiyo Yuden JMK316BJ226 | C _{IN} |

(1) See [Third-party Products Disclaimer](#)

11.2.2.1.5 Rectifier Diode Selection

To achieve high efficiency, a Schottky diode should be used. The voltage rating should be higher than the maximum output voltage of the converter. The average forward current should be equal to the average inductor current of the converter. The main parameter influencing the efficiency of the converter is the forward voltage and the reverse leakage current of the diode; both should be as low as possible. Possible diodes are: On Semiconductor MBRM120L, Microsemi UPS120E, and Fairchild Semiconductor MBRS130L.

11.2.2.1.6 Converter Loop Design and Stability

The TPS65140/45 converter loop can be externally compensated and allows access to the internal transconductance error amplifier output at the COMP pin. A small feedforward capacitor across the upper feedback resistor divider speeds up the circuit as well. To test the converter stability and load transient performance of the converter, a load step from 50 mA to 250 mA is applied and the output voltage of the converter is monitored. Applying load steps to the converter output is a good tool to judge the stability of such a boost converter.

The following will provide quick steps how design the feedforward network:

1. Select the feedback resistor divider to set the output voltage.
2. Select the feedforward capacitor to place a zero at 50 kHz.
3. Select the compensation capacitor on pin COMP. The smaller the value, the higher the low frequency gain.
4. Use a 50-kΩ potentiometer in series to C_c and monitor V_{out} during load transients. Fine tune the load transient by adjusting the potentiometer. Select a resistor value that comes closest to the potentiometer resistor value. This needs to be done at the highest V_{IN} and highest load current because stability is most critical at these conditions.

11.2.2.2 Negative Charge Pump

The negative charge pump provides a regulated output voltage by inverting the main output voltage, V_{O1} . The negative charge pump output voltage is limited by V_{O1} and set with external feedback resistors.

The maximum load current of the negative charge pump depends on the voltage drop across the external Schottky diodes and the internal ON-resistance of the charge pump MOSFETS Q8 and Q9. When the voltage drop across these components is larger than the voltage difference from V_{O1} to V_{O2} , the charge pump is in drop out, providing the maximum possible output current. Therefore, the higher the voltage difference between V_{O1} and V_{O2} , the higher the possible load current. See [Figure 12](#) for the possible output current versus boost converter voltage V_{O1} and the calculations below.

$$V_{OUTmin} = -(V_{O1} - 2V_F - I_O(2 \times r_{DS(on)Q8} + 2 \times r_{DS(on)Q9})) \quad (8)$$

Setting the output voltage:

$$V_{OUT} = -V_{REF} \times \frac{R3}{R4} = -1.213V \times \frac{R3}{R4} \quad (9)$$

$$R3 = R4 \times \frac{|V_{OUT}|}{V_{REF}} = R4 \times \frac{|V_{OUT}|}{1.213} \quad (10)$$

The lower feedback resistor value, $R4$, must be in a range from 40 k Ω to 120 k Ω or the overall feedback resistance must be within 500 k Ω to 1 M Ω . Smaller values load the reference too heavy and larger values may cause stability problems. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode must be twice the load current of the output. For a 20-mA output current, the dual Schottky diode BAT54 or similar is a good choice.

11.2.2.3 Positive Charge Pump

The positive charge pump can be operated in a voltage doubler mode or a voltage tripler mode.

The output voltage needs to be within the voltage ranges of the configuration, see [Voltage Doubler Mode](#) and [Voltage Tripler Mode](#). The output voltage within its limitation is set by the external resistor divider and is calculated as:

$$V_{OUT} = 1.214 \times \left(1 + \frac{R5}{R6}\right) \quad (11)$$

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R6 \times \left(\frac{V_{OUT}}{1.214} - 1\right) \quad (12)$$

The maximum load current of the positive charge pump depends on the voltage drop across the internal Schottky diodes, the internal ON-resistance of the charge pump MOSFETS, and the impedance of the flying capacitor. When the voltage drop across these components is larger than the voltage difference $V_{O1} \times 2$ to V_{O3} (doubler mode) or $V_{O1} \times 3$ to V_{O3} (tripler mode), then the charge pump is in dropout, providing the maximum possible output current. Therefore, the higher the voltage difference between $V_{O1} \times 2$ (doubler) or $V_{O1} \times 3$ (tripler) to V_{O3} , the higher the possible load current. See [Figure 13](#) and [Figure 14](#) for output current versus boost converter voltage, V_{O1} , and the following calculations.

11.2.2.3.1 Voltage Doubler Mode

- Leave C2+ pin open
- Connect C2-/Mode to GND

The following shows first order formulas to calculate the minimum and maximum output voltages of the positive charge pump in doubler mode

- Minimum: $V_{O3min} = V_{O1}$
- Maximum: $V_{O3max} = 2 \times V_{O1} - (2V_F + 2 \times I_O \times (2 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$

For detailed information how to estimate the output voltage ranges refer to [How to Estimate the Output Voltage Range of the Charge Pumps in the TPS6510x and TPS6514x](#), [SLVA918](#).

11.2.2.3.2 Voltage Tripler Mode

- Connect flying capacitor to C2+ and C2-/MODE

The following shows first order formulas to calculate the minimum and maximum output voltages of the positive charge pump in doubler mode

- Minimum: $V_{O3min} = 2 \times V_{O1} - (2 V_F + 2 \times I_O \times (2 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$
- Maximum: $V_{O3max} = 3 \times V_{O1} - (4 \times V_F + 2 \times I_O \times (3 \times r_{DS(on)Q5} + r_{DS(on)Q3} + r_{DS(on)Q4}))$

For detailed information how to estimate the output voltage ranges refer to *How to Estimate the Output Voltage Range of the Charge Pumps in the TPS6510x and TPS6514x*, [SLVA918](#).

11.2.2.4 Linear Regulator Controller

The TPS65140-Q1 and TPS65145-Q1 devices include a linear regulator controller to generate a 3.3-V rail when the system is powered from a 5-V supply. Because an external NPN transistor is required, the input voltage applied to VIN must be higher than the output voltage of the regulator. To provide a minimum base drive current of 13.5 mA, a minimum internal voltage drop of 500 mV from V_I to V_{base} is required. This can be translated into a minimum input voltage on V_I for a certain output voltage as the following calculation shows:

$$V_{I(min)} = V_{O4} + V_{BE} + 0.5 V \tag{13}$$

The base drive current together with the h_{FE} of the external transistor determines the possible output current. Using a standard NPN transistor like the BCP68 allows an output current of 1 A and using the BCP54 allows a load current of 337 mA for an input voltage of 5 V. Other transistors can be used as well, depending on the required output current, power dissipation, and PCB space. The device is stable with a 4.7- μ F ceramic output capacitor. Larger output capacitor values can be used to improve the load transient response when higher load currents are required.

11.2.3 Application Curves

Table 4. Table of Graphs

| | | | FIGURE |
|-----------------------------|--|---|--------|
| Main Boost Converter | | | |
| η | Efficiency V_{O1} | vs Load current | 1 |
| | Efficiency V_{O1} | vs Load current | 2 |
| | Efficiency V_{O1} | vs Input voltage | 3 |
| | PWM operation continuous mode | | 3 |
| | PWM operation at light load | | 4 |
| | Load transient response, $C_O = 22 \mu F$ | | 6 |
| | Load transient response, $C_O = 2 \times 22 \mu F$ | | 7 |
| | Power-up sequencing | | 8 |
| | Soft start V_{O1} | | 9 |
| Negative Charge Pump | | | |
| I_{max} | V_{O2} maximum load current | vs Output voltage V_{O1} | 10 |
| Positive Charge Pump | | | |
| I_{max} | V_{O3} maximum load current | vs Output voltage V_{O1} (doubler mode) | 11 |
| I_{max} | V_{O3} Maximum load current | vs Output voltage V_{O1} (tripler mode) | 12 |

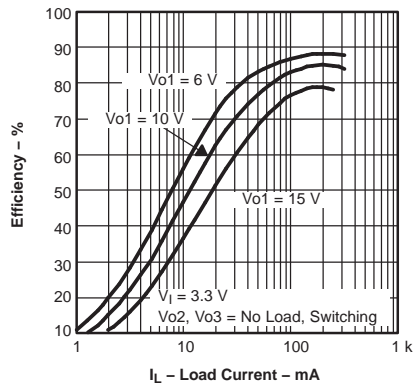


Figure 3. Efficiency V_{O1} vs Load Current

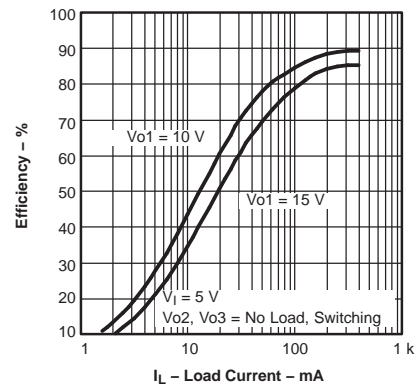


Figure 4. Efficiency V_{O1} vs Load Current

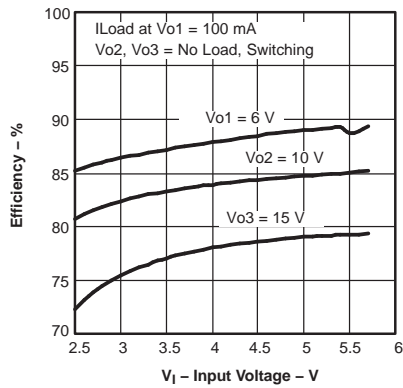


Figure 5. Efficiency V_{O1} vs Input Voltage

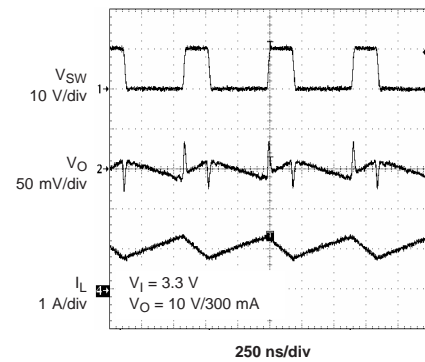


Figure 6. PWM Operation Continuous Mode

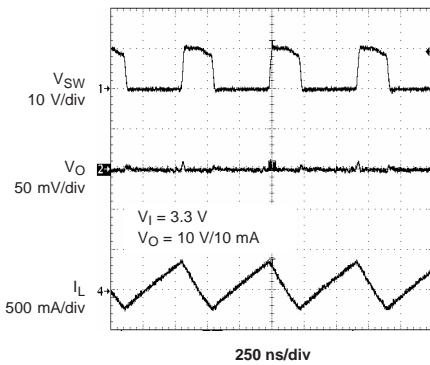


Figure 7. PWM Operation at Light Load

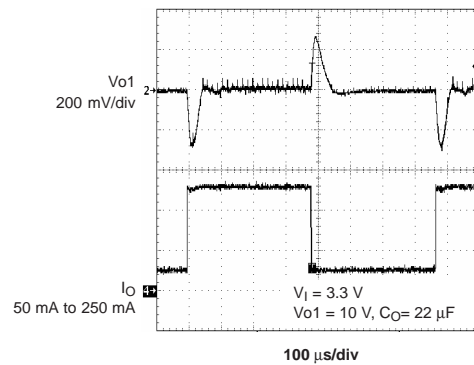


Figure 8. Load Transient Response $1 \times C_O$

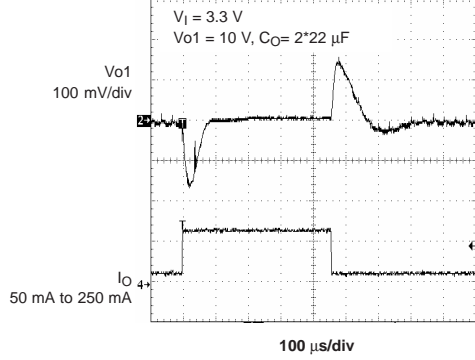


Figure 9. Load Transient Response 2 x C_O

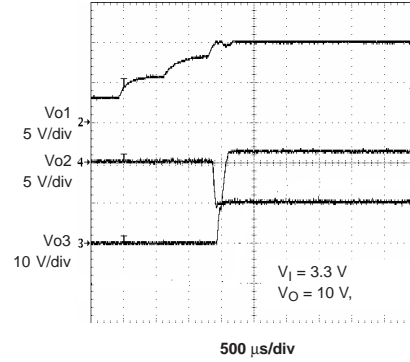


Figure 10. Power-up Sequencing

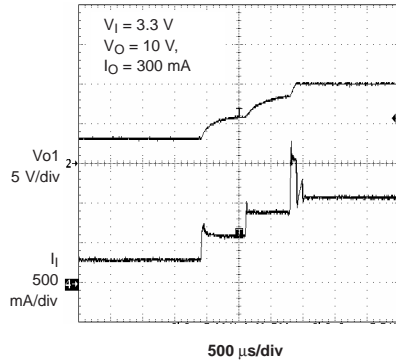


Figure 11. Soft Start V_{O1}

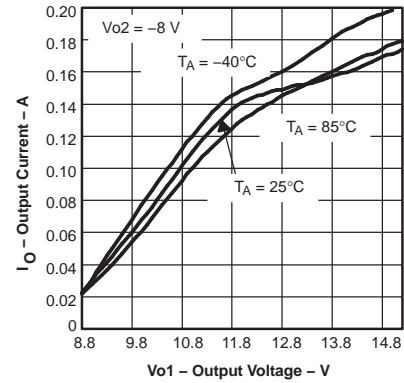


Figure 12. V_{O2} Maximum Load Current

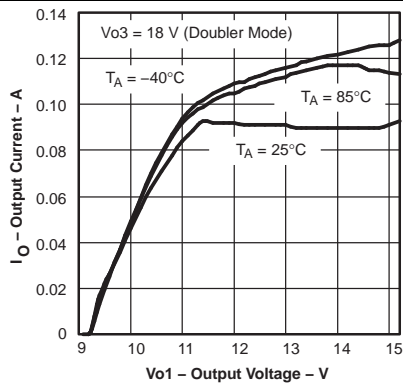


Figure 13. V_{O3} Maximum Load Current (doubler mode)

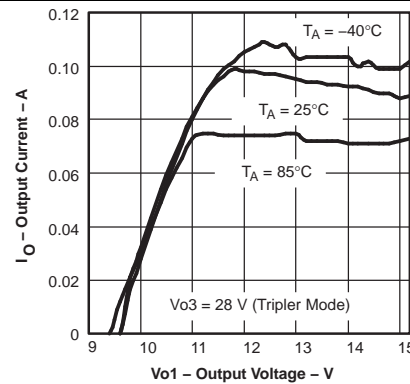


Figure 14. V_{O3} Maximum Load Current (tripler mode)

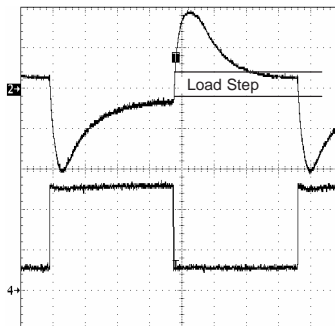


Figure 15. Load Step Caused By A Too Large Feed-forward Capacitor Value

11.3 System Examples

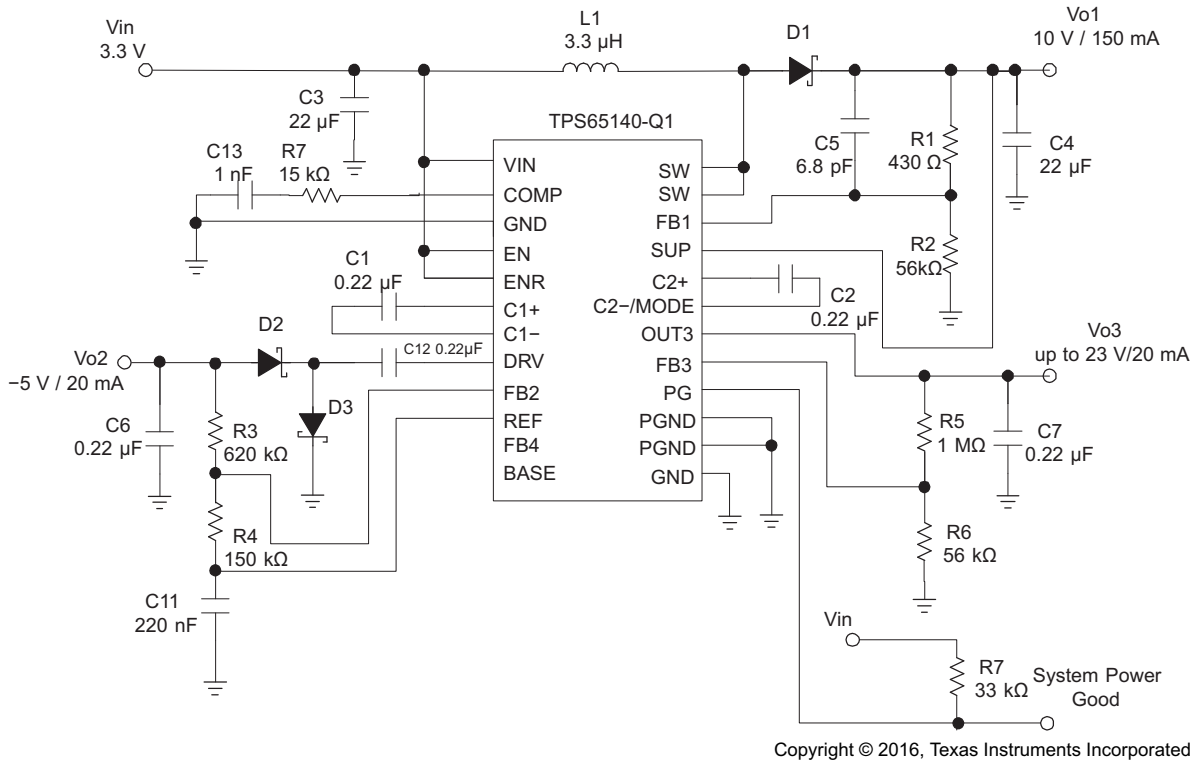


Figure 16. Typical Application, Notebook Supply

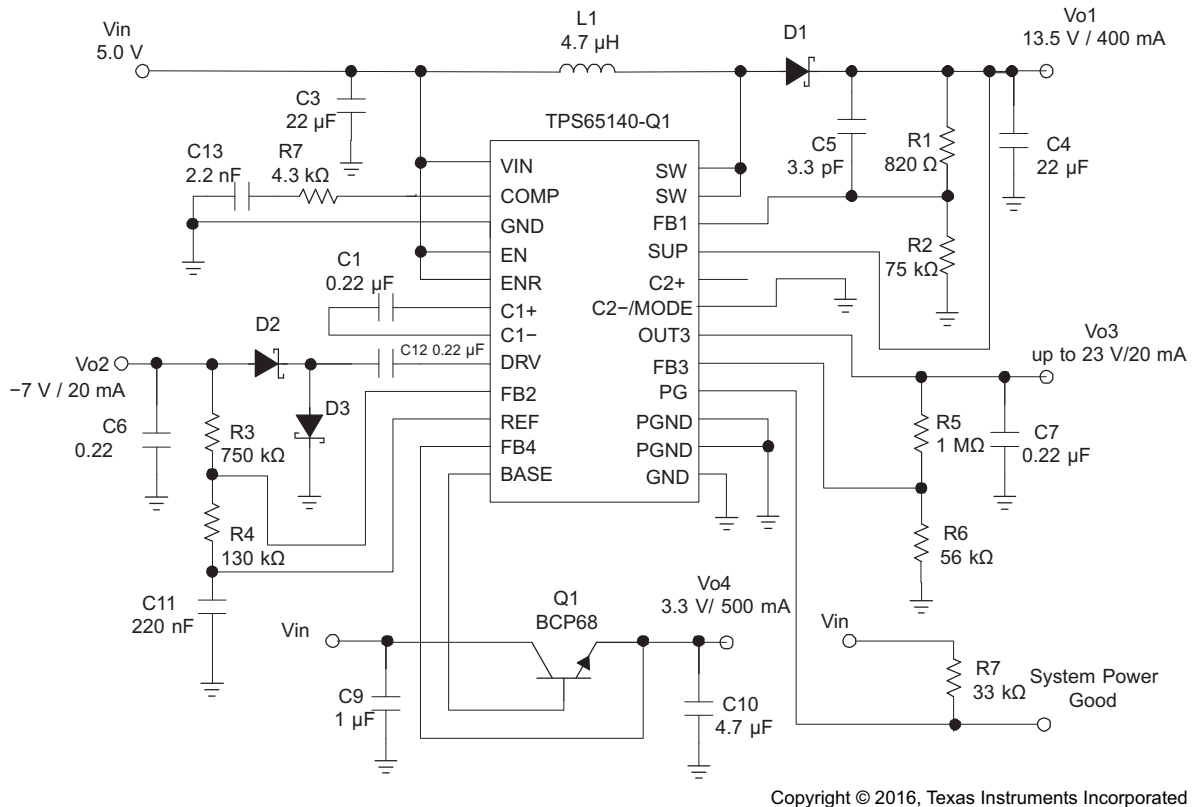


Figure 17. Typical Application, Monitor Supply

12 Power Supply Recommendations

The TPS65140-Q1 and TPS65145-Q1 devices are designed to operate from an input voltage supply range from 2.7 V to 5.8 V. This input supply must be well regulated. The input capacitance shown in the application schematics in this data sheet is sufficient for typical applications.

13 Layout

13.1 Layout Guidelines

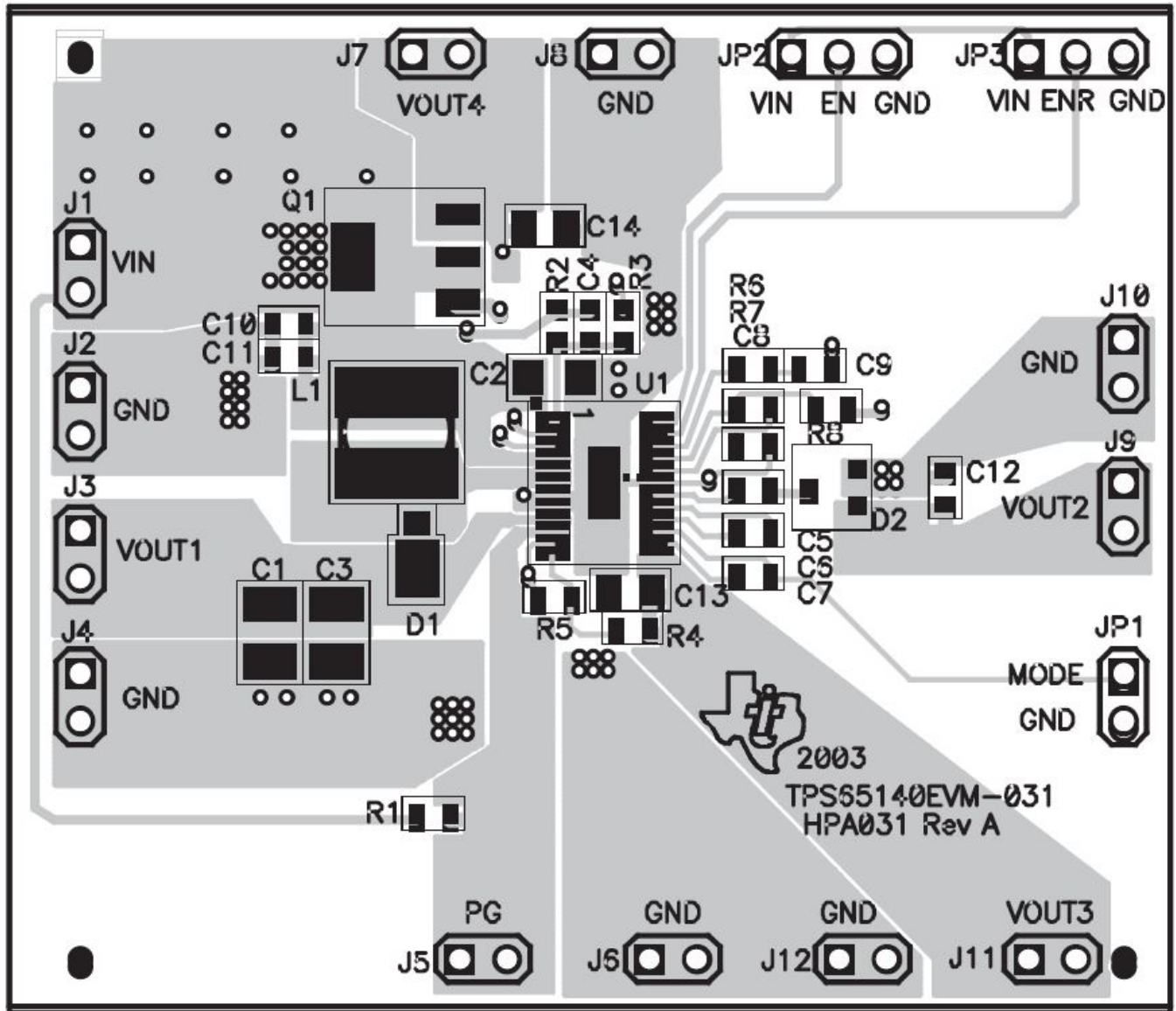
For all switching power supplies, the layout is an important step in the design, especially at high-peak currents and switching frequencies. If the layout is not carefully designed, the regulator might show stability and EMI problems. TI recommends the following PCB layout guidelines for the devices:

- Connect PGND and AGND together on the same ground plane.
- Connect all capacitor grounds and PGND together on a common ground plane.
- Place the input filter capacitor as close as possible to the input pin of the IC.
- Route first the traces carrying high-switching currents with wide and short traces.
- Isolate analog signal paths from power paths.
- If vias are necessary, try to use more than one in parallel to decrease parasitics, especially for power traces.
- Solder the thermal pad to the PCB for good thermal performance

13.2 Thermal Information

An influential component of the thermal performance of a package is board design. To take full advantage of the heat dissipation abilities of the PowerPAD or QFN package with exposed thermal die, a board that acts similar to a heatsink and allows for the use of an exposed (and solderable) deep downset pad should be used. For further information see Texas Instruments application notes (SLMA002) *PowerPAD Thermally Enhanced Package* and (SLMA004) *Power Pad Made Easy*. For the QFN package, see the application report (SLUA271) *QFN/SON PCB Attachment*.

13.3 Layout Example



14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

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14.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 5. Related Links

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TPS65140-Q1 | Click here | Click here | Click here | Click here | Click here |
| TPS65145-Q1 | Click here | Click here | Click here | Click here | Click here |

14.3 Documentation Support

14.3.1 Related Documentation

For related documentation see the following Application Notes and Marketing Selection Guide:

How to Compensate with the TPS6510x and TPS6514x [SLVA813](#).

Basic Calculation of a Boost Converter's Power Stage [SLVA372](#)

Customizing your TPS6510x/TPS6514x [SLVA192](#)

Power Management Guide 2016 at www.ti.com

14.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.5 Community Resources

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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14.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS65140IPWPRQ1 | ACTIVE | HTSSOP | PWP | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65140IQ1 | Samples |
| TPS65145IPWPRQ1 | ACTIVE | HTSSOP | PWP | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 65145IQ1 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS65140-Q1, TPS65145-Q1 :

- Catalog: [TPS65140](#), [TPS65145](#)

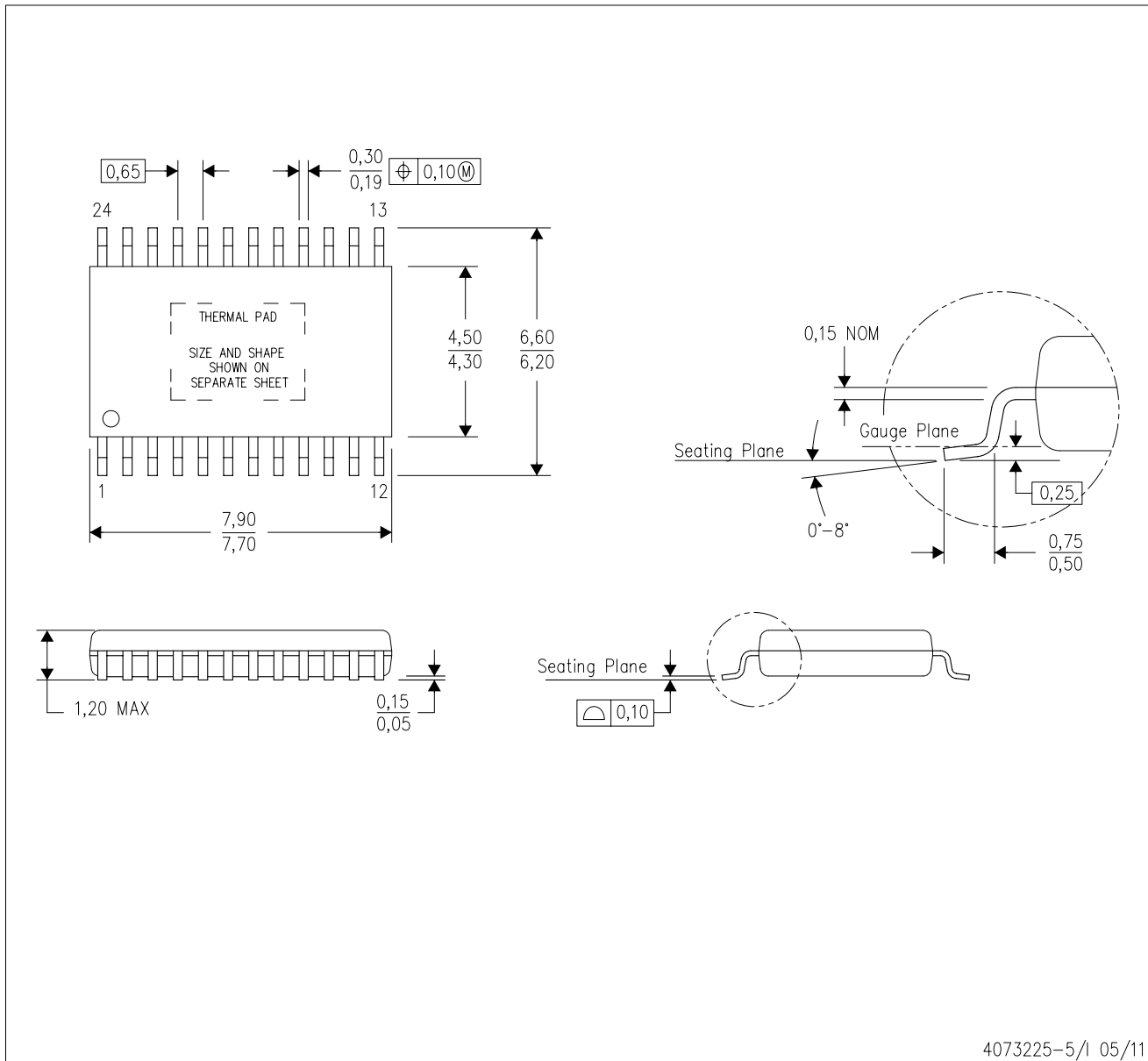
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

MECHANICAL DATA

PWP (R-PDSO-G24)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

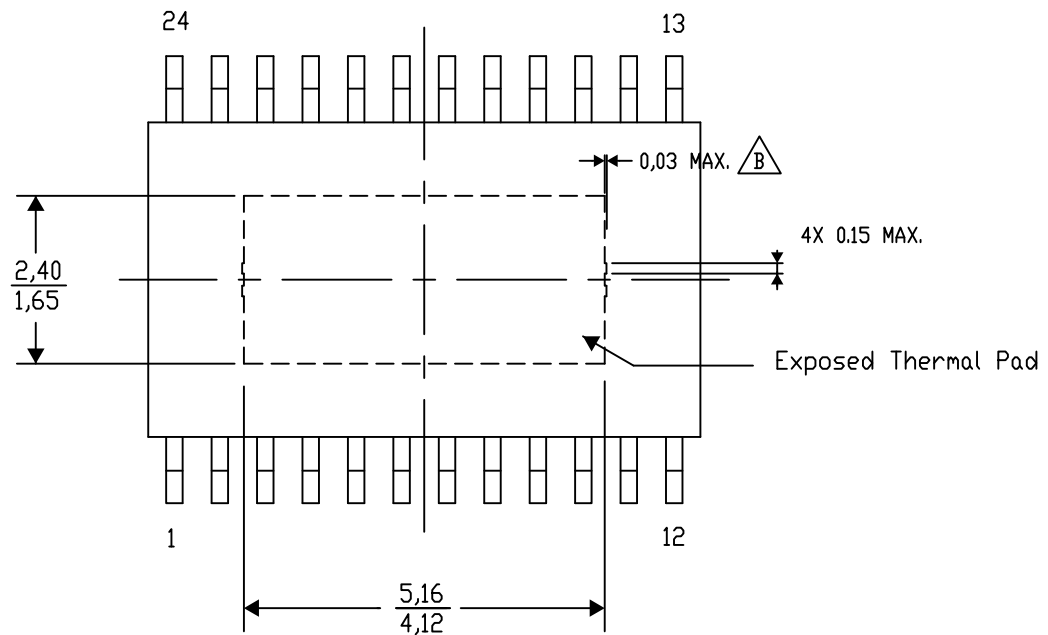
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-29/AO 01/16

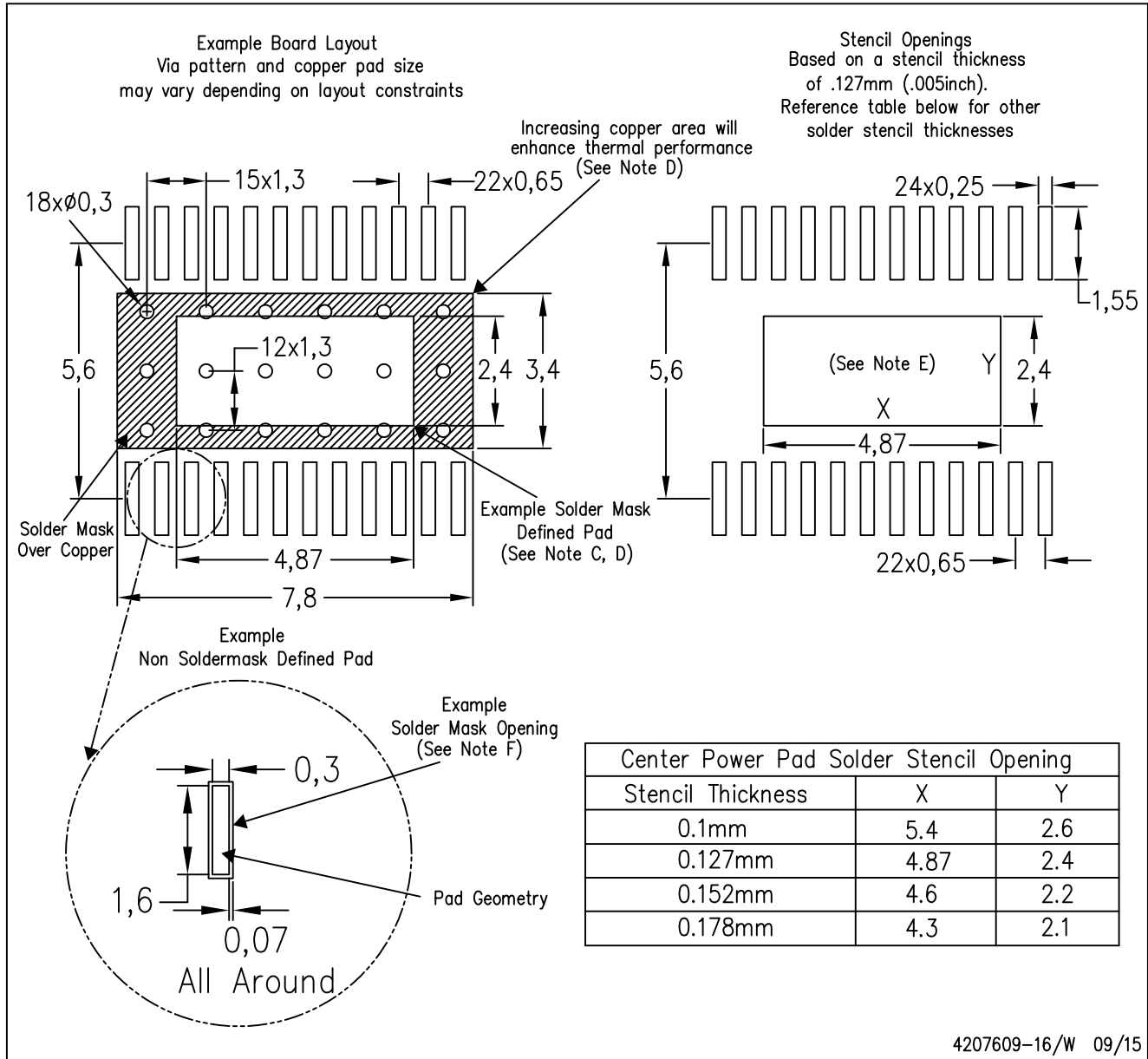
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G24)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

THERMAL PAD MECHANICAL DATA

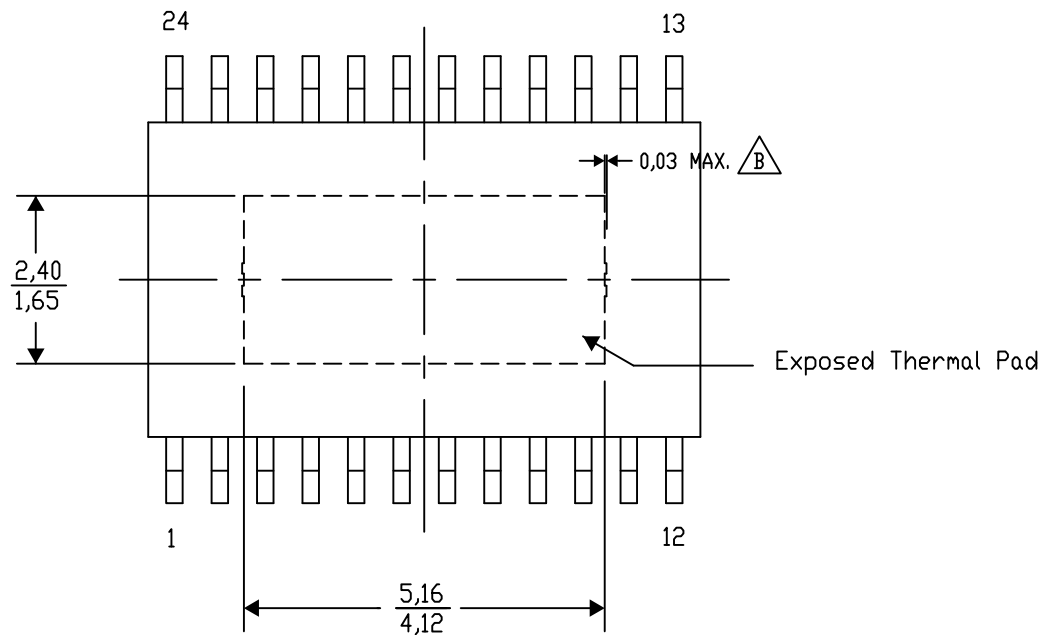
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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Top View

Exposed Thermal Pad Dimensions

4206332-54/AO 01/16

NOTE: A. All linear dimensions are in millimeters

 B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

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