











#### SN54LV165A, SN74LV165A

SCLS402O - APRIL 1998-REVISED NOVEMBER 2016

# SNx4LV165A Parallel-Load 8-Bit Shift Registers

#### 1 Features

- 2-V to 5.5-V V<sub>CC</sub> Operation
- Max t<sub>pd</sub> of 10.5 ns at 5 V
- Support Mixed-Mode Voltage Operation on All Ports
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- IP Routers
- Enterprise Switches
- Access Control and Security: Access Keypads and Biometrics
- Smart Meters: Power Line Communication

### 3 Description

The 'LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V  $V_{CC}$  operation.

When the devices are clocked, data is shifted toward the serial output  $Q_H$ . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/ $\overline{LD}$ ) input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output,  $\overline{Q}_H$ .

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while SH/LD is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH must be changed to the high level only while CLK is high. Parallel loading is inhibited when SH/LD is held high. The parallel inputs to the register are enabled while SH/LD is held low, independently of the levels of CLK, CLK INH, or SER.

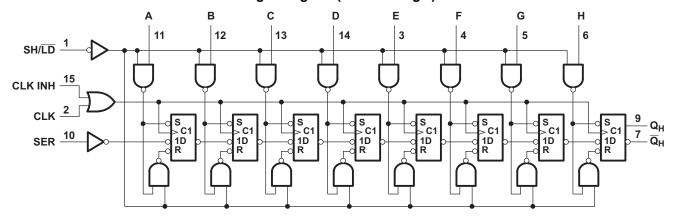
These devices are fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4LV165AD	SOIC (16)	9.90 mm × 3.91 mm
SNx4LV165ADB	SSOP (16)	6.20 mm × 5.30 mm
SNx4LV165ANS	SO (16)	10.30 mm × 5.30 mm
SNx4LV165APW	TSSOP (16)	5.00 mm × 4.40 mm
SNx4LV165ADGV	TVSOP (16)	3.60 mm × 4.40 mm
SNx4LV165ARGY	VQFN (16)	4.00 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)





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### 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from Revision N (July 2013) to Revision O

**Page** 

Added Applications section, Device Information table, Table of Contents, Pin Configuration and Functions section,
Specifications section, ESD Ratings table, Thermal Information table, Typical Characteristics section, Detailed
Description section, Application and Implementation section, Power Supply Recommendations section, Layout
section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section......

#### Changes from Revision M (December 2010) to Revision N

Page

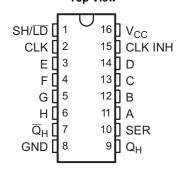
Extended maximum temperature operating range from 85°C to 125°C......

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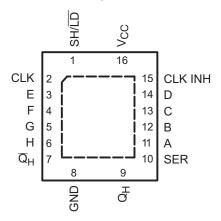


# 5 Pin Configuration and Functions

SN74LV165A: D, DB, DGV, NS or PW Package SN54LV165A: J or W Package 16-Pin SOIC, SSOP, TVSOP, SOP, TSSOP Top View



#### SN74LV165A: RGY Package 16-Pin VQFN Top View



#### **Pin Functions**

F	PIN		DECODIDATION
NAME NO.		I/O	DESCRIPTION
A	11	I	Serial input A
В	12	1	Serial input B
С	13	1	Serial input C
CLK	2	1	Storage clock
CLK INH	15	I	Storage clock
D	14	I	Serial input D
E	3	1	Serial input E
F	4	1	Serial input F
G	5	I	Serial input G
GND	8	_	Ground pin
Н	6	I	Serial input H
	7	0	Output H
Q <sub>H</sub>	9	O	Ουιραί Η
SH/LD	1	I	Load Input
SER	10	I	Serial input
V <sub>CC</sub>	16	_	Power pin



### 6 Specifications

#### 6.1 Absolute Maximum Ratings

see (1)

			MIN	MAX	UNIT
	Supply voltage		-0.5	7	V
	Input voltage <sup>(2)</sup>			7	V
	Voltage range applied to any output in the high-impedance or power	-0.5	7	V	
	Output voltage (2)(3)				V
	Input clamp current	V <sub>I</sub> < 0		-20	mA
	Output clamp current	V <sub>O</sub> < 0		<b>-</b> 50	mA
	Continuous output current	$V_O = 0$ to $V_{CC}$		±25	mA
	Continuous current through V <sub>CC</sub> or GND	•		±50	mA
T <sub>jmax</sub>	Maximum virtual junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic dischause	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000	\/
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

<sup>(2)</sup> The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>(3)</sup> This value is limited to 5.5 V maximum.



### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
	High lavel construction	V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 2 V		0.5	
. /	Low lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V	<sub>CC</sub> × 0.3	V
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	V	<sub>CC</sub> × 0.3	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	V	<sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	V
Vo	Output voltage		0	V <sub>CC</sub>	V
•0		V <sub>CC</sub> = 2 V		-50	μA
	Library and and an annual an annual and an annual an a	V <sub>CC</sub> = 2.3 V to 2.7 V		-2	
Іон	High-level output current	V <sub>CC</sub> = 3 V to 3.6 V		-6	mΑ
		V <sub>CC</sub> = 4.5 V to 5.5 V		-12	
		V <sub>CC</sub> = 2 V		50	μA
	Low lovel output ourrent	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2	
l <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3 V to 3.6 V		6	mΑ
		V <sub>CC</sub> = 4.5 V to 5.5 V		12	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200	
Δt/Δν	Input transition rise or fall rate	V <sub>CC</sub> = 3 V to 3.6 V		100	ns/\
		V <sub>CC</sub> = 4.5 V to 5.5 V		20	
т	Operating free air temperature	SN54LV165A	-55	125	°C
T <sub>A</sub>	Operating free-air temperature	SN74LV165A	-40	125	

<sup>(1)</sup> All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the *Implications of Slow or Floating CMOS Inputs* application report.

#### 6.4 Thermal Information

		SN74LV165A						
т	THERMAL METRIC <sup>(1)</sup>		DB (SSOP)	NS (SO)	PW (TSSOP)	DGV (TVSOP)	RGY (VQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.2	102.8	89.4	113.3	125.9	48.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.1	53.3	47.9	48.3	51	46.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.8	53.5	49.8	58.4	57.7	24.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	13.2	16.6	16.6	6.4	5.7	2	°C/W
ΨЈВ	Junction-to-board characterization parameter	43.5	52.9	49.5	57.8	57.2	24.9	°C/W
R <sub>θ</sub> JC(bot)	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	11.7	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Product Folder Links: SN54LV165A SN74LV165A



#### 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Recommended  $T_A = -40$  °C to +125 °C

	PARAMETER	V <sub>cc</sub>	T <sub>A</sub>	MIN	TYP	MAX	UNIT
			-55°C to +125°C	V <sub>CC</sub> - 0.1			
	$I_{OH} = -50 \text{ mA}$	2 V to 5.5 V	-40°C to +85°C	<sub>CC</sub> - 0.1			
			-40°C to +125°C	V <sub>CC</sub> - 0.1			
			-55°C to +125°C	2			
	$I_{OH} = -2 \text{ mA}$	2.3 V	-40°C to +85°C	2			
.,			-40°C to +125°C	2			
V <sub>OH</sub>			-55°C to +125°C	2.48			V
	$I_{OH} = -6 \text{ mA}$	3 V	-40°C to +85°C	2.48			
			-40°C to +125°C	2.48			
			-55°C to +125°C	3.8			
	$I_{OH} = -12 \text{ mA}$	4.5 V	-40°C to +85°C	3.8			
			-40°C to +125°C	3.8			
			-55°C to +125°C			0.1	
	$I_{OL} = 50 \text{ mA}$	2 V to 5.5 V	-40°C to +85°C			0.1	
			-40°C to +125°C			0.1	
	I <sub>OL</sub> = 2 mA	2.3 V	-55°C to +125°C			0.4	
			-40°C to +85°C			0.4	
			-40°C to +125°C			0.4	.,
/ <sub>OL</sub>		3 V	-55°C to +125°C			0.44	V
	I <sub>OL</sub> = 6 mA		-40°C to +85°C			0.44	
			-40°C to +125°C			0.44	
			-55°C to +125°C			0.55	
	I <sub>OL</sub> = 12 mA	4.5 V	-40°C to +85°C			0.55	
			-40°C to +125°C			0.55	
			-55°C to +125°C			±1	
ı	$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V	-40°C to +85°C			±1	μΑ
			-40°C to +125°C			±1	
			-55°C to +125°C			20	
СС	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	-40°C to +85°C			20	μΑ
			-40°C to +125°C			20	
			-55°C to +125°C			5	
off	$V_I$ or $V_O = 0$ to 5.5 V	0	-40°C to +85°C			5	μΑ
			-40°C to +125°C			5	
			-55°C to +125°C		1.7		
$C_{i}$	$V_I = V_{CC}$ or GND	$V_{I} = V_{CC} \text{ or GND}$ 3.3 V $-40^{\circ}\text{C to } +85^{\circ}\text{C}$ 1.7		pF			
			-40°C to +125°C		1.7		•

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# 6.6 Timing Requirements— $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range,  $V_{CC}$  = 2.5 V  $\pm$  0.2 V (unless otherwise noted) (see Figure 2)

	PARAMETER	TEST CONDITION	T <sub>A</sub>	MIN	MAX	UNIT
			25°C	8.5		
		CLK high or low	−55°C to +125°C	9		
		CLK high or low	-40°C to +85°C	9		
		-40°C to +125°C	9			
w	Pulse duration		25°C	11		ns
		0.1/25	−55°C to +125°C	13		
		SH/LD low	-40°C to +85°C	13		
			-40°C to +125°C	13		
			25°C	7		
		CIVID bink before CIVA	−55°C to +125°C	8.5		
		SH/LD high before CLK↑	-40°C to +85°C	8.5		
			-40°C to +125°C	8.5		
			25°C	8.5		
		050 1 ( 0146	−55°C to +125°C	9.5		
		SER before CLK↑	-40°C to +85°C	9.5		
			-40°C to +125°C	9.5		
su Setup time		25°C	7		ns	
		CLK INH before CLK↑	−55°C to +125°C	7		
			-40°C to +85°C	7		
			-40°C to +125°C	7		
			25°C	11.5		
			−55°C to +125°C	12		
		Data before SH/LD↑	-40°C to +85°C	12		
			-40°C to +125°C	12		
			25°C	-1		
		255 1	−55°C to +125°C	0		
		SER data after CLK↑	-40°C to +85°C	0		
			-40°C to +125°C	0		
			25°C	0		
			-55°C to +125°C	0.5		
t <sub>h</sub> Hold time	Parallel data after SH/ <del>LD</del> ↑	-40°C to +85°C	0.5		ns	
			-40°C to +125°C	0.5		
			25°C	0		
			−55°C to +125°C	0		
		SH/ <del>LD</del> high after CLK↑	-40°C to +85°C	0		
			-40°C to +125°C	0		

### 6.7 Timing Requirements— $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)

	PARAMETER	TEST CONDITION	T <sub>A</sub>	MIN	MAX	UNIT
			25°C	6		
		CLK high or law	−55°C to +125°C	7		
	CLK high or low	-40°C to	-40°C to +85°C	7		
	Dulas duration		-40°C to +125°C	7		
t <sub>w</sub>	Pulse duration		25°C	7.5		ns
		CIVITE Issue	−55°C to +125°C	9		
		SH/LD low	-40°C to +85°C	-40°C to +85°C 9		
			-40°C to +125°C	9		

Product Folder Links: SN54LV165A SN74LV165A



# Timing Requirements— $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (continued)

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)

PARAMETER	TEST CONDITION	T <sub>A</sub>	MIN	MAX	UNIT
		25°C	5		
	SH/LD high before CLK↑	−55°C to +125°C	6		
	SH/LD nigh before CLK?	-40°C to +85°C	6		
		-40°C to +125°C	6		
		25°C	5		
	CED hafara CLIVA	−55°C to +125°C	6		
	SER before CLK↑	-40°C to +85°C	6		
Oaton time		-40°C to +125°C	6		
u Setup time		25°C	5		ns
		-55°C to +125°C	5		
	CLK INH before CLK↑	-40°C to +85°C	5		
		-40°C to +125°C	5		
		25°C	7.5		
	Data before SH/ <del>LD</del> ↑	-55°C to +125°C	8.5		
		-40°C to +85°C	8.5		
		-40°C to +125°C	8.5		
		25°C	0		
	CED data after OLIVA	−55°C to +125°C	0		
	SER data after CLK↑	-40°C to +85°C	0		
		-40°C to +125°C	0		
		25°C	0.5		
11.11.6	D	−55°C to +125°C	0.5		
Hold time	Parallel data after SH/ <del>LD</del> ↑	-40°C to +85°C	0.5		ns
		-40°C to +125°C	0.5		
		25°C	0		
	01/10	−55°C to +125°C	0		
	SH/LD high after CLK↑	-40°C to +85°C	0		
		-40°C to +125°C	0		

### 6.8 Timing Requirements— $V_{cc} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

	PARAMETER	TEST CONDITION	T <sub>A</sub>	MIN	MAX	UNIT		
			25°C	4				
		OLK birth and law	-55°C to +125°C	4				
		CLK high or low  -40°C to +85°C 4  -40°C to +125°C 4  25°C 5  -55°C to +125°C 5  -40°C to +85°C 6  -40°C to +125°C 6	CLK nigh or low	-40°C to +85°C	-40°C to +85°C	4		
	Dulas duration		-40°C to +125°C	4				
ι <sub>w</sub>	Pulse duration		25°C	5		ns		
			–55°C to +125°C	5				
			6					
			-40°C to +125°C	6				

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# Timing Requirements— $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (continued)

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V  $\pm$  0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	TEST CONDITION	T <sub>A</sub>	MIN	MAX	UNIT
		25°C	4		
	01/15	−55°C to +125°C	4		
	SH/LD high before CLK↑	-40°C to +85°C	4		
		-40°C to +125°C	4		
		25°C	4		
	OFD before OLIVA	−55°C to +125°C	4		
u Setup time	SER before CLK↑	-40°C to +85°C	4		
		-40°C to +125°C	4		
		25°C	3.5		ns
	OLIK BULL ( OLIK	−55°C to +125°C	3.5		
	CLK INH before CLK↑	-40°C to +85°C	3.5		
		-40°C to +125°C			
		25°C	5		
	D	−55°C to +125°C	5		
	Data before SH/ <del>LD</del> ↑	-40°C to +85°C	5		
		-40°C to +125°C	5		
		25°C	0.5		
	OFD data affect OLIVA	−55°C to +125°C	0.5		
	SER data after CLK↑	-40°C to +85°C	0.5		
		-40°C to +125°C	0.5		
		25°C	1		
11.112	D	−55°C to +125°C	1		
h Hold time	Parallel data after SH/LD↑	-40°C to +85°C	1		ns
		-40°C to +125°C	1		
		25°C 0.5			
	011/10	-55°C to +125°C			
	SH/LD high after CLK↑	-40°C to +85°C	0.5		
		-40°C to +125°C	0.5		



# 6.9 Switching Characteristics— $V_{CC}$ = 2.5 V ± 0.2 V

over operating free-air temperature range,  $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted), (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T <sub>A</sub>	MIN	TYP	MAX	UNIT
				25°C	50 <sup>(1)</sup>	80 <sup>(1)</sup>		
			0 45 - 5	-55°C to +125°C	45 <sup>(1)</sup>			
			C <sub>L</sub> = 15 pF	-40°C to +85°C	45			
,				-40°C to +125°C	45			
f <sub>max</sub>				25°C	40	65		MHz
			0 50 5	-55°C to +125°C	35			
			C <sub>L</sub> = 50 pF	-40°C to +85°C	35			
				-40°C to +125°C	35			
				25°C		12.2 <sup>(1)</sup>	19.8 <sup>(1)</sup>	
	0114			-55°C to +125°C	1 <sup>(1)</sup>		22 <sup>(1)</sup>	
	CLK			-40°C to +85°C	1		22	
				-40°C to +125°C	1		22	
	SH/LD	$Q_H$ or $\overline{Q}$		25°C		13.1 <sup>(1)</sup>	21.5 <sup>(1)</sup>	
				-55°C to +125°C	1 <sup>(1)</sup>		23.5 <sup>(1)</sup>	
t <sub>pd</sub>			C <sub>L</sub> = 15 pF	-40°C to +85°C	1		23.5	ns
				-40°C to +125°C	1		23.5	
				25°C		12.9 <sup>(1)</sup>	21.7 <sup>(1)</sup>	
				-55°C to +125°C	1 <sup>(1)</sup>		24 <sup>(1)</sup>	
	Н			-40°C to +85°C	1		24	
				-40°C to +125°C	1		24	
				25°C		15.3	23.3	
	0114			-55°C to +125°C	1		26	
	CLK			-40°C to +85°C	1		26	
				-40°C to +125°C	1		26	
				25°C		16.1	25.1	
	0.1/5	<u> </u>	0 50 5	-55°C to +125°C	1		28	
t <sub>pd</sub>	SH/LD	$Q_H$ or $\overline{Q}$	C <sub>L</sub> = 50 pF	-40°C to +85°C	1		28	ns
				-40°C to +125°C	1		28	
		1		25°C		15.9	25.3	
				−55°C to +125°C	1		28	
	Н			-40°C to +85°C	1		28	
				-40°C to +125°C	1		28	

<sup>(1)</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# 6.10 Switching Characteristics— $V_{CC}$ = 3.3 V ± 0.3 V

over operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted), (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T <sub>A</sub>	MIN	TYP	MAX	UNIT
				25°C	65 <sup>(1)</sup>	115 <sup>(1)</sup>		
			0 45 -5	-55°C to +125°C	55 <sup>(1)</sup>			
			$C_L = 15 \text{ pF}$	-40°C to +85°C	55			
£				-40°C to +125°C	55			N 41 1-
f <sub>max</sub>				25°C	60	90		MHz
			0 50 - 5	-55°C to +125°C	50			
			C <sub>L</sub> = 50 pF	-40°C to +85°C	50			
				-40°C to +125°C	50			
				25°C		8.6 <sup>(1)</sup>	15.4 <sup>(1)</sup>	
	OL K			-55°C to +125°C	1 (1)		18 <sup>(1)</sup>	
	CLK			-40°C to +85°C	1		18	
				-40°C to +125°C	1		18	
t <sub>pd</sub>	SH/LD	$Q_H$ or $\overline{Q}$		25°C		9.1 <sup>(1)</sup>	15.8 <sup>(1)</sup>	
			C <sub>L</sub> = 15 pF	-55°C to +125°C	1 (1)		18.5 <sup>(1)</sup>	
				-40°C to +85°C	1		18.5	ns
				-40°C to +125°C	1		18.5	
				25°C		8.9 <sup>(1)</sup>	14.1 <sup>(1)</sup>	
	н			-55°C to +125°C	1 (1)		16.5 <sup>(1)</sup>	
				-40°C to +85°C	1		16.5	
				-40°C to +125°C	1		16.5	
				25°C		10.9	14.9	
	CLK			-55°C to +125°C	1		16.9	
	CLK			-40°C to +85°C	1		16.9	
				-40°C to +125°C	1		16.9	
				25°C		11.3	19.3	
	SH/LD	0 0	0 50 - 5	-55°C to +125°C	1		22	
$t_{pd}$	SH/LD	$Q_H$ or $\overline{Q}$	C <sub>L</sub> = 50 pF	-40°C to +85°C	1		22	ns
				-40°C to +125°C	1		22	
				25°C		11.1	17.6	
	н			-55°C to +125°C	1		20	
	П			-40°C to +85°C	1		20	
				-40°C to +125°C	1		20	

<sup>(1)</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

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# 6.11 Switching Characteristics— $V_{cc} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range,  $V_{CC}$  = 5 V  $\pm$  0.5 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAP	T <sub>A</sub>	MIN	TYP	MAX	UNIT	
				25°C	110 <sup>(1)</sup>	165 <sup>(1)</sup>			
			0 45 -5	-55°C to +125°C	90 <sup>(1)</sup>	·			
			$C_L = 15 pF$	-40°C to +85°C	90	·			
£				-40°C to +125°C	90	·		MHz	
f <sub>max</sub>				25°C	95	125		IVIHZ	
			C <sub>L</sub> = 50 pF	-55°C to +125°C	85				
			C <sub>L</sub> = 50 pr	-40°C to +85°C	85				
				-40°C to +125°C	85	·			
				25°C		6 <sup>(1)</sup>	9.9 <sup>(1)</sup>		
	OL K			-55°C to +125°C	1 <sup>(1)</sup>	·	11.5 <sup>(1)</sup>		
	CLK			-40°C to +85°C	1	·	11.5		
				-40°C to +125°C	1	·	11.5		
	SH/LD	$Q_H$ or $\overline{Q}$		25°C		6 <sup>(1)</sup>	9.9 <sup>(1)</sup>		
			C <sub>L</sub> = 15 pF	-55°C to +125°C	1 <sup>(1)</sup>	·	11.5 <sup>(1)</sup>		
t <sub>pd</sub>				-40°C to +85°C	1	·	11.5	ns	
				-40°C to +125°C	1	·	11.5		
	н			25°C		6 <sup>(1)</sup>	9.9 <sup>(1)</sup>		
				-55°C to +125°C	1 <sup>(1)</sup>	·	10.5 <sup>(1)</sup>		
				-40°C to +85°C	1	·	10.5		
				-40°C to +125°C	1	·	10.5		
				25°C		7.7	11.9		
	OL K			-55°C to +125°C	1	·	13.5		
	CLK			-40°C to +85°C	1	·	13.5		
				-40°C to +125°C	1	·	13.5		
				25°C		7.7	11.9		
	SH/LD	0 0	C 50F	-55°C to +125°C	1	·	13.5		
t <sub>pd</sub>	2U/LD	$Q_H$ or $\overline{Q}$	$C_L = 50 \text{ pF}$	-40°C to +85°C	1		13.5	ns	
				-40°C to +125°C	1	·	13.5		
			25°C 7.6		7.6	11			
					-55°C to +125°C	1		12.5	
	H			-40°C to +85°C	1		12.5		
				-40°C to +125°C	1	·	12.5		

<sup>(1)</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.

# 6.12 Operating Characteristics

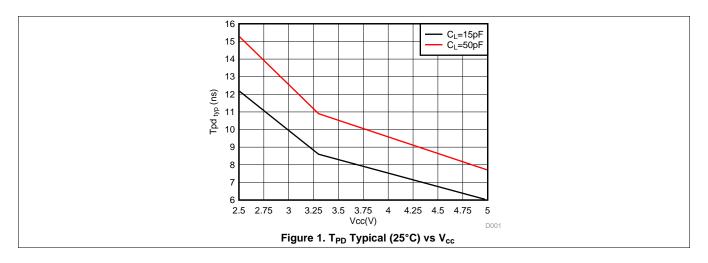
 $T_A = 25^{\circ}C$ 

	PARAMETER	TEST CO	ONDITIONS	V <sub>CC</sub>	TYP	UNIT
0	Dower dissination conscitons	C	f 40 MH=	3.3 V	36.1	۲
$C_{pd}$	Power dissipation capacitance	$C_L = 50 \text{ pF}$	f = 10 MHz	5 V	37.5	p⊦

Product Folder Links: SN54LV165A SN74LV165A

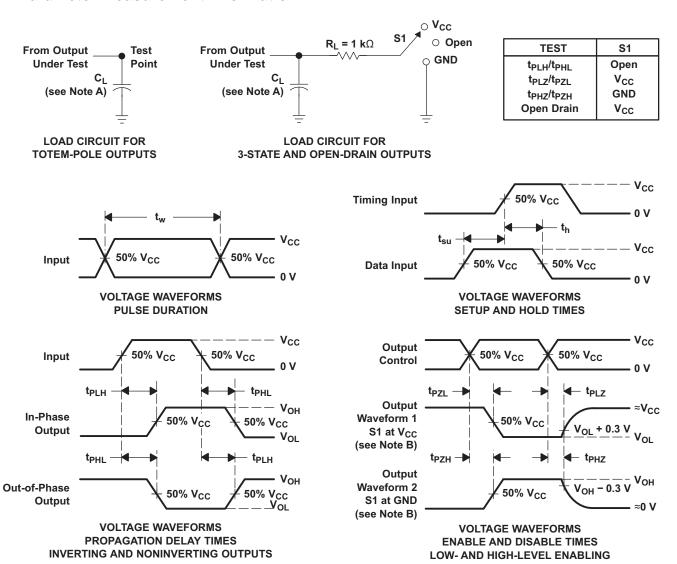


# 6.13 Typical Characteristics





#### 7 Parameter Measurement Information



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
  - Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  3 ns,  $t_f \leq$  3 ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



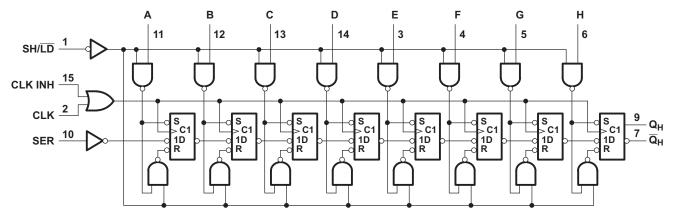
### 8 Detailed Description

#### 8.1 Overview

The 'LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V V<sub>CC</sub> operation.

When the devices are clocked, data is shifted toward the serial output  $Q_H$ . Parallel-in access to <u>each</u> stage is provided by eight individual direct data inputs that are enabled by a low level at the <u>shift/load (SH/LD)</u> input. The 'LV165A devices feature a clock-inhibit function and a complemented serial output,  $\overline{Q}_H$ .

#### 8.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, NS, PW, RGY, and W packages.

Figure 3. Logic Diagram (Positive Logic)

Product Folder Links: SN54LV165A SN74LV165A



#### **Functional Block Diagram (continued)**

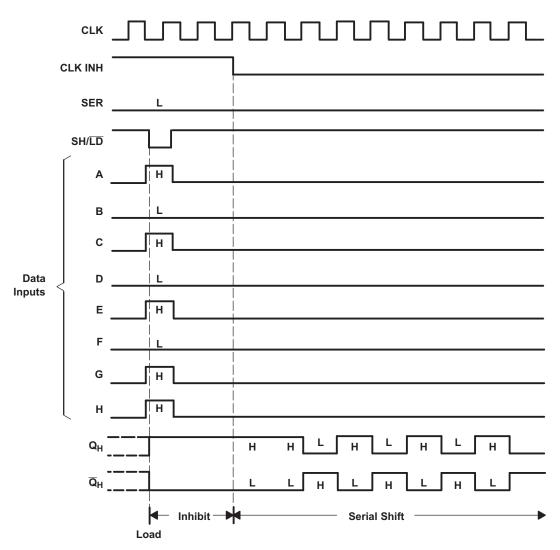


Figure 4. Typical Shift, Load, and Inhibit Sequences

#### 8.3 Feature Description

The wide operating range allows the device to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.



### 8.4 Device Functional Modes

Table 1 lists the functional modes of SNx4LV165A.

**Table 1. Device Functional Modes** 

	INPUTS		OPERATION
SH/LD	CLK	OPERATION	
L	X	X	Parallel load
Н	Н	X	$Q_0$
Н	X	Н	$Q_0$
Н	L	1	Shift
Н	1	L	Shift



### 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LV165A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low-drive and slow-edge rates minimize overshoot and undershoot on the outputs.

#### 9.2 Typical Application

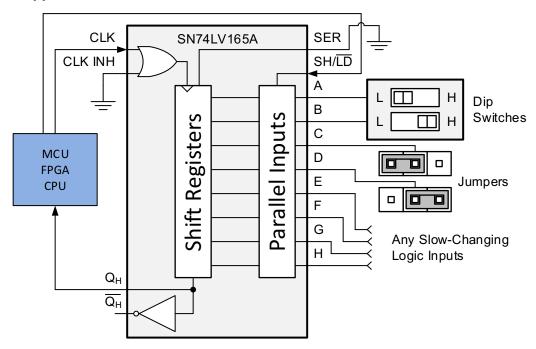


Figure 5. Input Expansion with Shift Registers

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that can exceed maximum limits. The high drive also creates fast edges into light loads so consider routing and load conditions to prevent ringing.

#### 9.2.2 Detailed Design Procedure

Recommended input conditions:

- Rise time and fall time specs. See the Recommended Operating Conditions section, (Δt/ΔV)
- Specified high and low level. See the Recommended Operating Conditions section, (V<sub>IH</sub> and V<sub>II</sub>)
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V<sub>CC</sub>

Recommended output conditions:

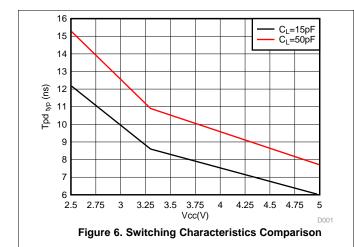
- Load currents must not exceed 25 mA per output and 50 mA total for the part.
- Outputs must not be pulled above V<sub>CC</sub>.

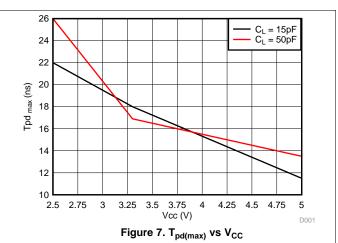
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# **Typical Application (continued)**

# 9.2.3 Application Curves







### 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Absolute Maximum Ratings section. Each V<sub>CC</sub> terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-μF capacitor and if there are multiple V<sub>CC</sub> terminals then TI recommends a 0.01-μF or 0.022-μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

#### Layout

#### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V<sub>CC</sub> whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it disables the outputs section of the part when asserted. This does not disable the input section of the IOs so they also cannot float when disabled.

#### 11.2 Layout Example



Figure 8. Layout Example



#### 12 Device and Documentation Support

#### 12.1 Related Documentation

For related documentation see the following:

- Power-Up Behavior of Clocked Devices
- Introduction to Logic

#### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV165A	Click here	Click here	Click here	Click here	Click here
SN74LV165A	N74LV165A Click here		Click here	Click here	Click here

#### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

#### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Lise

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

#### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

#### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 12.7 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

### 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





10-Jun-2014

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRG3	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ADRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV165A	Samples
SN74LV165APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRG3	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples
SN74LV165APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV165A	Samples



### PACKAGE OPTION ADDENDUM

10-Jun-2014

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV165A	Samples
SN74LV165ARGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV165A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



### **PACKAGE OPTION ADDENDUM**

10-Jun-2014

#### OTHER QUALIFIED VERSIONS OF SN74LV165A:

● Enhanced Product: SN74LV165A-EP

NOTE: Qualified Version Definitions:

• Enhanced Product - Supports Defense, Aerospace and Medical Applications

# PACKAGE MATERIALS INFORMATION

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### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV165ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV165ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV165ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG3	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV165ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV165ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV165ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV165ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV165ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV165ADRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV165ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV165APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV165APWRG3	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV165APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV165APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV165ARGYR	VQFN	RGY	16	3000	355.0	350.0	50.0

# D (R-PDS0-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



# D (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G16)

### PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



# PW (R-PDSO-G16)

# PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



### DB (R-PDSO-G\*\*)

### PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



# RGY (R-PVQFN-N16)

#### PLASTIC QUAD FLATPACK NO-LEAD

#### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



# RGY (R-PVQFN-N16)

# PLASTIC QUAD FLATPACK NO-LEAD



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="https://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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