8bit High-speed ADC

PRODUCT DESCRIPTION

The MS5510 is a 8-bit, 20MSPS analog-to-digital converter (ADC) using semiflash architecture. The MS5510 operates in 5V supply and the typical power dissipation is only 130mW. The MS5510 includes an internal sample-and-hold circuit, parallel output with high-impedance mode, and internal reference resistor.

The semiflash architecture reduces power dissipation and die size compared with flash converter. By completing the conversion in a 2-step process, the number of comparator can be greately reduced. The wait time of converted data is 2.5 clocks.

The MS5510 has two operation modes. Mode 1: use three internal reference resistors to connect with VDDA, which can generate a standard 2V full-scale conversion range. Only external jumper is needed to complete this option. Mode 2: by internal resistor section, a standard 4V full-scale conversion range is generated, which reduces the requirements for external reference or resistor. Differential linearity is 0.5LSB at 25°C and the maximum is 0.75LSB over the full operating temperature range. Typical dynamic specifications include a differential gain of 1% and differential phase of 0.7 degrees.

The operating temperature ranges from -20°C to 75°C.

FEATURES

- Analog Signal Input Range : Mode 1: 2V (Max); Mode 2: 4V (Max)
- Resolution : 8bit
- INL: ±0.75 LSB (25°C); ±1 LSB (-20°C-75°C)
- DNL: ±0.5 LSB (25°C); ±0.75 LSB (-20°C-75°C)
- Fastest Conversion Rate : 20MSPS
- 5VSingle Power Supply
- Low Power Dissipation : Mode 1 : 127.5mW ; Mode 2: 150mW

SOP24

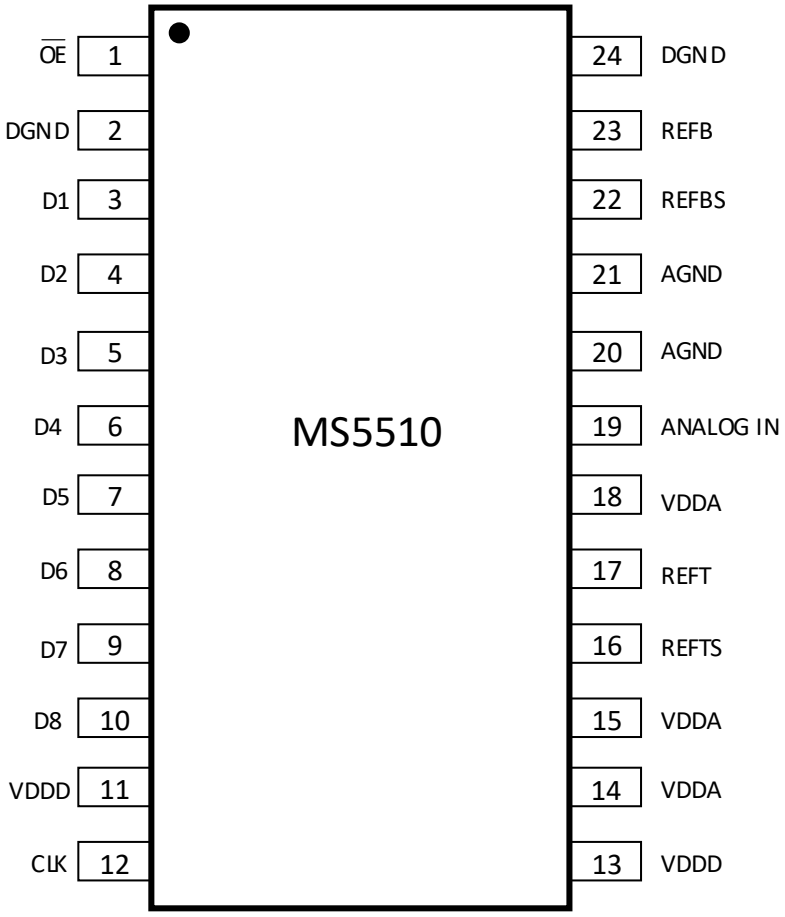
APPLCATIONS

- DTV
- Multimedia Image Process
- Video Conference
- High-speed Data Conversion
- Quadrature Demodulator

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS5510	SOP24	MS5510

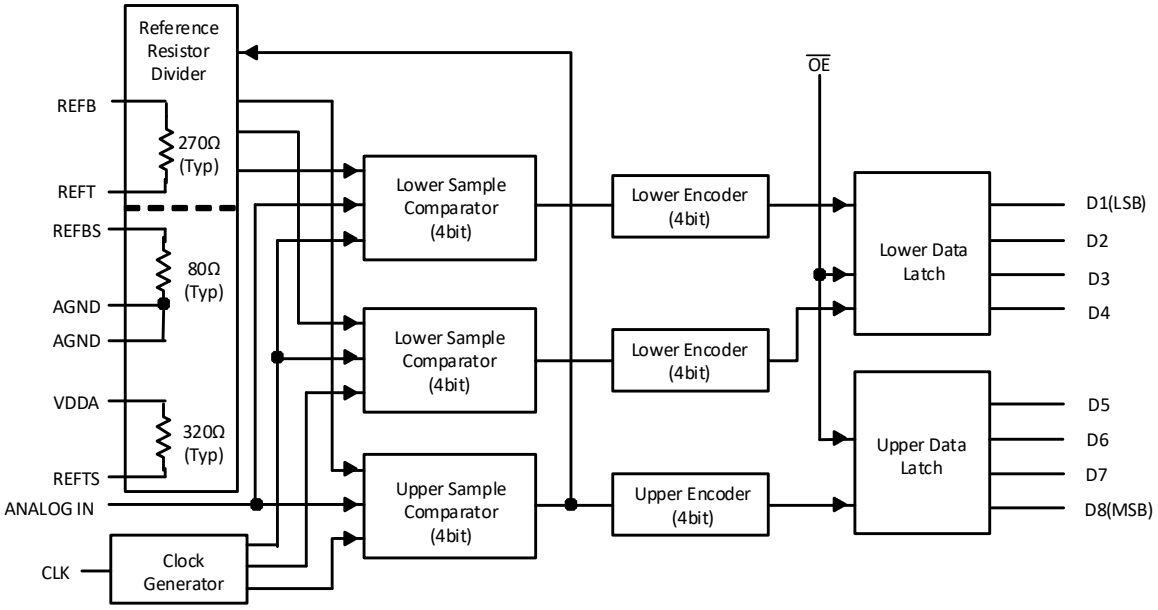
PIN CONFIGURATION



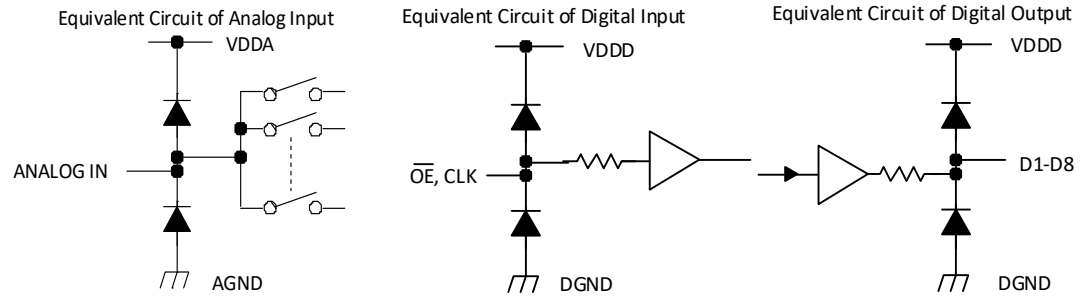
PIN DESCRIPTION

Pin	Name	Type	Description
AGND	20, 21	-	Analog Ground
ANALOG IN	19	I	Analog Input
CLK	12	I	Clock Input
DGND	2,24	-	Digital Ground
D1-D8	3-10	O	Digital Data Output. D1=LSB, D8=MSB
$\overline{OE}$	1	I	Output Enable. When $\overline{OE}$ is 0, output data; When $\overline{OE}$ is 1, output high-impedance
VDDA	14,15,18	-	Analog Power Supply
VDDD	11,13	-	Digital Power Supply
REFB	23	I	Low Reference Voltage Input
REFBS	22	-	Low Reference Voltage. When using mode 1, internal voltage divider generates a rated 2V reference and REFBS is shorted to REFB. When using mode 2, REFBS is connected to ground.
REFT	17	I	High Reference Voltage Input
REFTS	16	-	High Reference Voltage. When using mode 1, internal voltage divider generates a rated 2V reference and REFTS is shorted to REFT. When using mode 2, REFBS is connected to VDDA.

BLOCK DIAGRAM



Input/Output Structure Diagram



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Ratings	Unit
Power Supply	V_{DDA}, V_{DDD}	7V	V
Reference Voltage Input	V_{REFT}, V_{REFB}	AGND ~ V_{DDA}	V
Analog Input Voltage	V_I(ANLG)	AGND ~ V_{DDA}	V
Digital Input Voltage	V_I (DGTL)	DGND ~ V_{DDD}	V
Digital Output Voltage	V_O (DGTL)	DGND ~ V_{DDD}	V
Operating Temperature	T_A	-20 ~ 75	°C
Storage Temperature	T_{stg}	-55 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Condition	Min	Typ	Max	Unit
Power Supply	V_{DDA}-AGND	4.75	5	5.25	V
	V_{DDD}-AGND	4.75	5	5.25	
	AGND-DGND	-100	0	100	mV
Reference Input Voltage (Top), $V_{ref\ (T)}$	Mode 2	V_{REFB+2}		4	V
Reference Input Voltage (Bottom), $V_{ref\ (B)}$	Mode 2	0		V_{REFT-4}	V
Analog Input Voltage, $V_{I\ (ANLG)}$		V_{REFB}		V_{REFT}	V
High-level Input Voltage, V_{IH}		4			V
Low-level Input Voltage, V_{IL}				1	V
Pulse Width, Clock High-level, $t_{W\ (H)}$		25			ns
Pulse Width, Clock Low-level, $t_{W\ (L)}$		25			ns

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{DD}=5V, V_{REFT}=2.5V, V_{REFB}=0.5V, $f_{(CLK)}$=20MHz, T_A=25° C.

Digital I/O

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Input Current	I_{IH}	V_{DD}=MAX, V_{IH}=V_{DD}			5	μA
Low-level Input Current	I_{IL}	V_{DD}=MAX, V_{IL}=0			5	
High-level Output Current	I_{OH}	$\overline{OE}$ =GND, V_{DD}=MIN,V_{OH}=V_{DD}-0.5V	-1.5			mA
Low-level Output Current	I_{OL}	$\overline{OE}$ =GND, V_{DD}=MIN, V_{OL}=0.4V	2.5			
High-level High-impedance Output Leakage Current	I_{OZH}	$\overline{OE}$ =V_{DD},V_{DD}=MAX,V_{OH}=V_{DD}			16	μA
Low-level High-impedance Output Leakage Current	I_{OZL}	$\overline{OE}$ =V_{DD},V_{DD}=MIN,V_{OL}=0			16	

Power Dissipation

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Power Supply Current	I_{DD}	$f_{(CLK)}$=20MHz, NTSC Slope-wave Input			18	27	mA
Reference Voltage Current	I_{ref}	Mode 1	V_{ref}=REFT-REFB=2V	5.2	7.5	10.5	mA
		Mode 2	V_{ref}=REFT-REFB=4V	10.4	15	21	mA

Static Performance

Parameter	Symbol	Condition			Min	Typ	Max	Unit
Self-bias (1)	REFB	REFB is shorted to REFBS.			0.57	0.61	0.65	V
Self-bias (2)	REFT-REFB	REFT is shorted to REFTS			1.9	2.02	2.15	V
Self-bias (3)	REFT	REFB is connected to AGND. REFT is connected to REFTS			2.18	2.29	2.4	V
Reference Voltage Resistor	R_{ref}	Between REFT and REFB			190	270	350	Ω
Analog Input Capacitance	C_i	$V_{I\ (ANLG)}$=1.5V+0.07V_{rms}				16		pF
Integral Nonlinearity	INL	Mode 1	$f_{(CLK)}$=20MHz, V_I=0.5V to 2.5V	T_A=25°C		±0.4	±0.75	
				T_A=-20°C-75°C			±1	
		Mode 2	$f_{(CLK)}$=20MHz, V_I=0 to 4V	T_A=25°C		±0.4	±0.7	
				T_A=-20°C-75°C			±1	

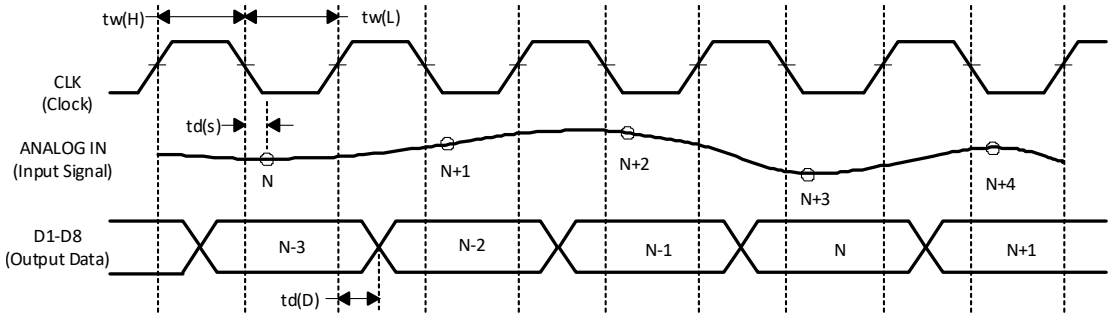
Parameter	Symbol	Condition			Min	Typ	Max	Unit
Differential Nonlinearity	DNL	Mode 1	$f_{(CLK)}$=20MHz, V_I=0.5V to 2.5V	T_A=25°C		±0.3	±0.5	
				T_A=-20°C-75°C			±0.7	
		Mode 2	$f_{(CLK)}$=20MHz, V_I=0 to 4V	T_A=25°C		±0.3	±0.5	
				T_A=-20°C-75°C			±0.7	
Zero-scale Error	E_{ZS}	Mode 1	V_{ref}=REFT-REFB=2V		-18	-43	-68	mV
		Mode 2	V_{ref}=REFT-REFB=4V		-36	-86	-136	mV
Full-scale Error	E_{FS}	Mode 1	V_{ref}=REFT-REFB=2V		-20	0	20	mV
		Mode 2	V_{ref}=REFT-REFB=4V		-40	0	40	mV

Operating Characteristics

Unless otherwise noted,V_{DD}=5V, V_{REFT}=2.5V, V_{REFB}=0.5V, $f_{(CLK)}$=20MHz, T_A=25ºC.

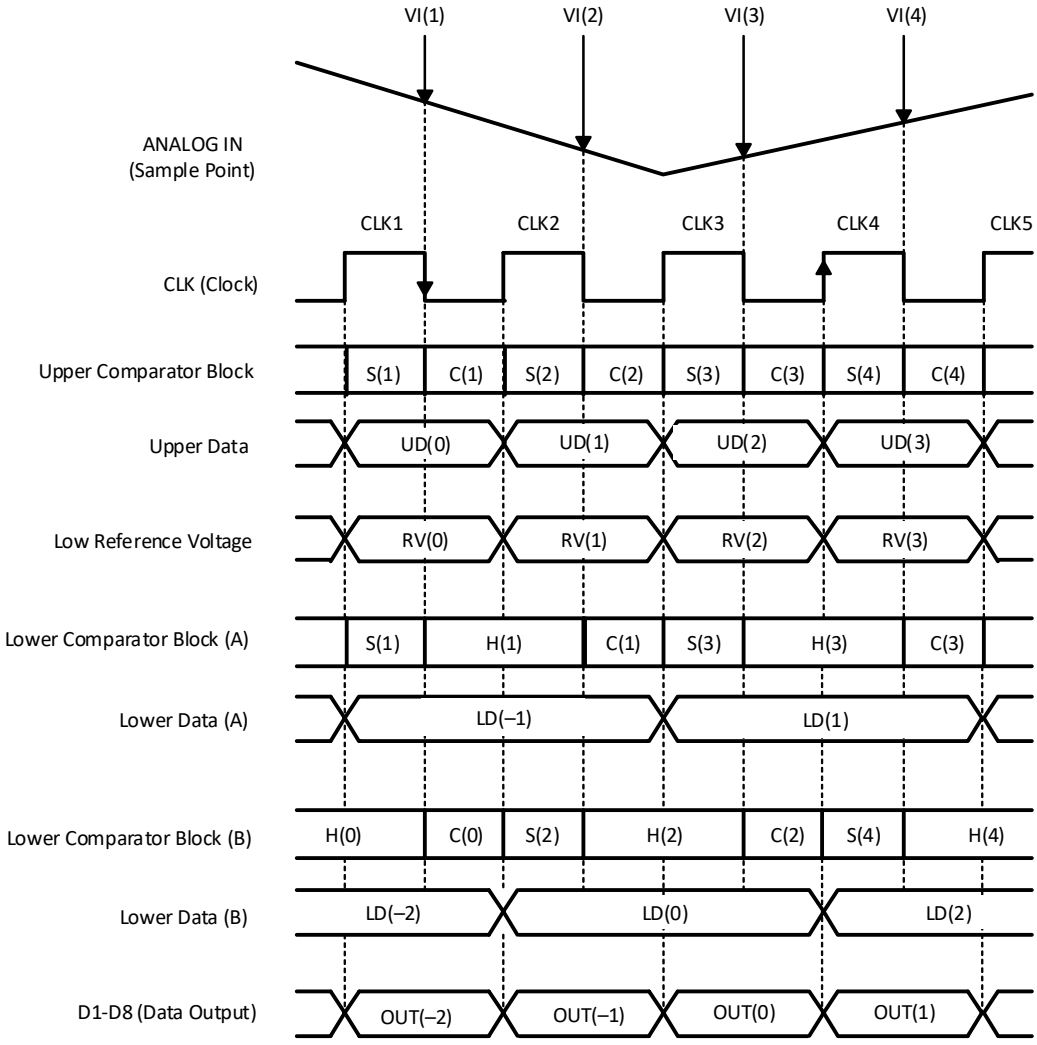
Parameter	Symbol	Condition			Min	Typ	Max	Unit
Maximum Conversion Ratio	f_{conv}	Mode 1	f_I=1kHz	$V_{I\ (ANLG)}$=0.5-2.5V			20	MSPS
		Mode 2	Slope-wave	$V_{I\ (ANLG)}$=0-4V			20	MSPS
Analog Input Bandwidth	BW	@-1dB				14		MHz
Digital Output Delay	$t_{d\ (D)}$	C_L≤10pF				18	30	ns
Differential Gain		NTSC40 IRE Modulation Wave,				1%		
Differential Phase		f_{conv}=14.3MSPS				0.7		°
Sample Jitter Time	t_{AJ}					30		ps
Sample Delay Time	$t_{d\ (s)}$					4		ns
Enable Time. $\overline{OE}$ Falling Edge to Output Valid Data	t_{en}	C_L=10pF				5		ns
Disable Time. $\overline{OE}$ Rising Edge to Output High-impedance	t_{dis}	C_L=10pF				7		ns
Spurious Free Dynamic Range	SFDR	Input 1MHz		T_A=25°C		45		dB
				Full Range		43		
		Input 3MHz		T_A=25°C		45		
				Full Range		46		
		Input 6MHz		T_A=25°C		43		
				Full Range		42		
		Input 10MHz		T_A=25°C		39		
				Full Range		39		
Signal to Noise Ratio	SNR	T_A=25°C				46		dB
		Full Range				44		

I/O Timing


tw(H)
tw(L)
CLK
(Clock)
td(s)
ANALOG IN
(Input Signal)
N
N+1
N+2
N+3
N+4
D1-D8
(Output Data)
N-3
N-2
N-1
N
N+1
td(D)

FUNCTION DESCRIPTION

The MS5510 is a semiflash ADC with two lower comparator blocks (a comparator every four bits). As shown in following diagram, input voltage VI(1) is sampled on the falling edge of CLK1 and enter into the upper comparator block and the lower comparator block(A), S(1). The upper comparator block determines the upper data UD(1) on the rising edge of CLK2. At the same time, low reference voltage generates voltage RV(1) corresponding to the upper data. The lower comparator block (A) determines the lower data LD(1) on the rising edge of CLK3. UD(1) and LD(1) are combined and output as OUT(1) on the rising edge of CLK4. As described above, output data is delayed 2.5 clocks from the analog input voltage sampling point. Input voltage VI(2) is sampled on the falling edge of CLK2. UD(2) is determined on the rising edge of CLK3. LD(2) is determined on the rising edge of CLK4 by the lower comparator block(B). OUT(2) data is output on the rising edge of CLK5.

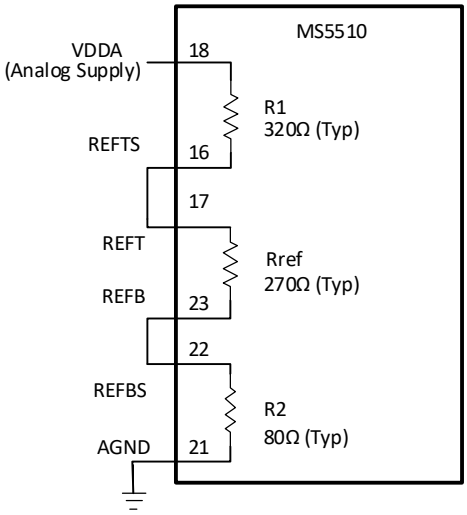


Internal Reference

Operation Mode 1

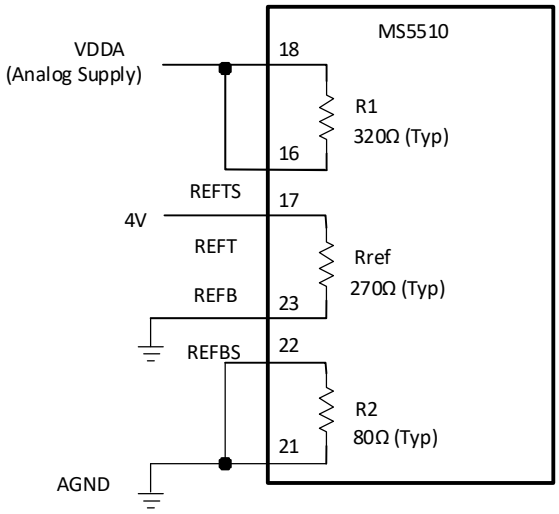
The MS5510 has three internal resistors to generate internal reference voltage. These resistors are connected to VDDA, REFTS, REFT, REFB, REFBS and AGND.

Using the internal reference is shown as follows. The connection provides the standard video 2V reference for the rated digital output.



Operation Mode 2

Analog input voltage range is 4V. REFT is connected with 4V, REFB is connected to ground and other connections are as follows. This connection provides the 4V reference for digital output with 0-4V analog input on ANALOG IN pin.



Function Table

Input Signal Voltage	Step	Digital Output Coding
		MSB LSB
V_{ref}(B)	255	0 0 0 0 0 0 0 0
.	.	. . . .
.	.	. . . .
.	128	0 1 1 1 1 1 1 1
.	127	1 0 0 0 0 0 0 0
.	.	. . . .
.	.	. . . .
V_{ref}(T)	0	1 1 1 1 1 1 1 1

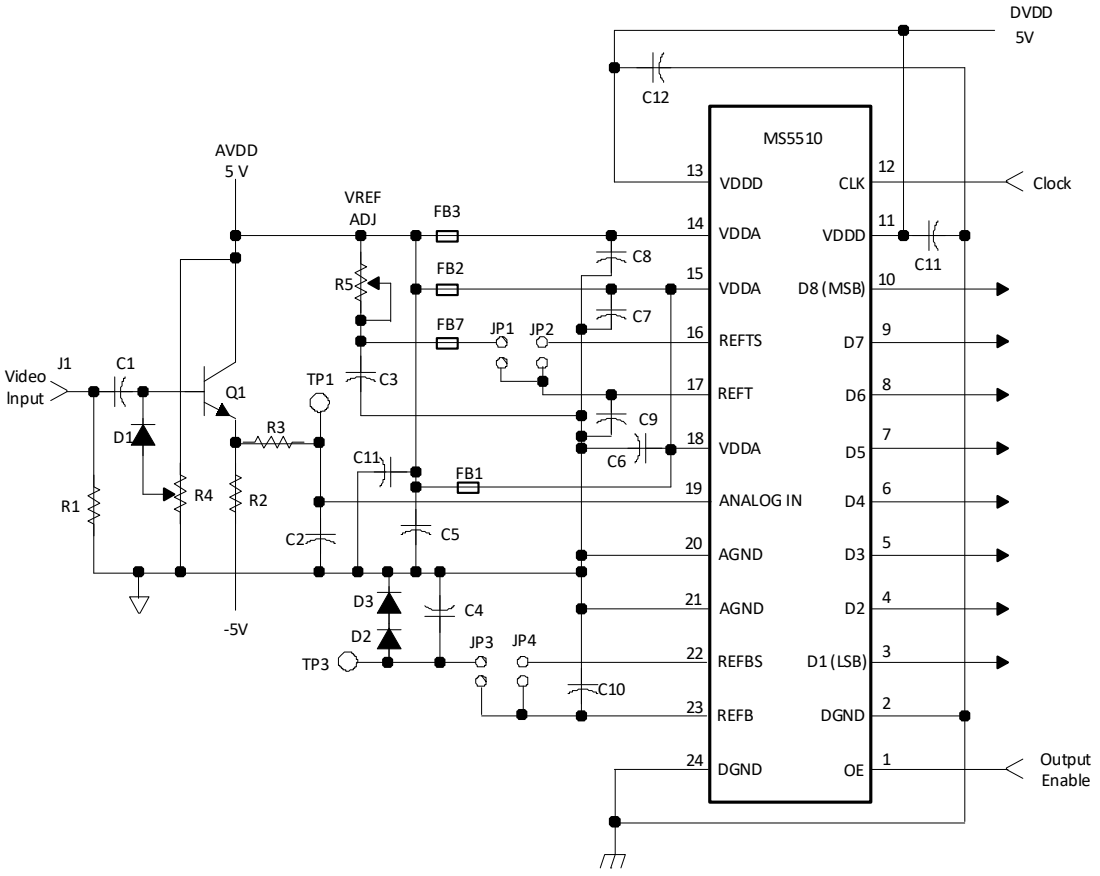
APPLICATION INFORMATION

The following contents are design recommendation items used with the MS5510.

- External analog and digital circuit should be separated and shielded in order to reduce system noise.
- RF test board or PCB technology should be used during the evaluation and production process. And he test board should be copperized.
- Because AGND and DGND are not connected internally, these pins need to be connected externally. These ground traces should be connected with separate trace having better power bypass. In order to minimize the noise pickup, power line should use twisted-pair cables. An analog and digital ground plane should be used on PCB layout.
- VDDA to AGND and VDDD to DGND should be decoupled with 0.1μF capacitors respectively, which are placed as close as possible to these pins. Be careful to test in order to ensure a solid noise-free ground connection for the analog and digital ground.
- VDDA, AGND, and ANALOG IN should be separated from the high-frequency pins, CLK and D0–D7. When possible, AGND traces should be placed on both sides of the ANALOG IN on the PCB for shielding.
- When testing or using the MS5510, the resistance of the driving source connected to the analog input should be 10Ω or less within the analog frequency range.

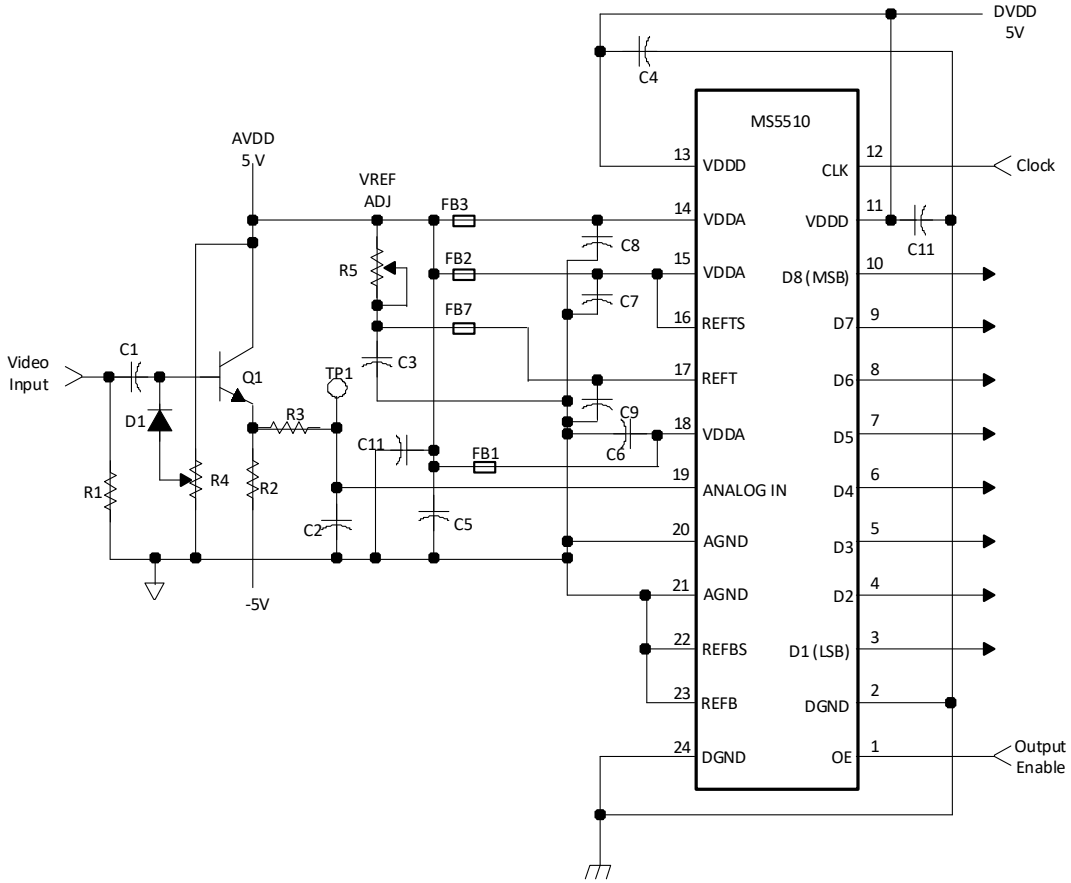
Evaluation and Test Diagram

Mode 1



Element	Description
C1,C3-C4,C6-C12	0.1μf
C2	10pf
C5	47μf
FB1,FB2,FB3,FB7	Ferrite Ring
Q1	2N3414 or Equivalent Device
R1,R3	75Ω
R2	500Ω
R4	10kΩ
R5	300Ω

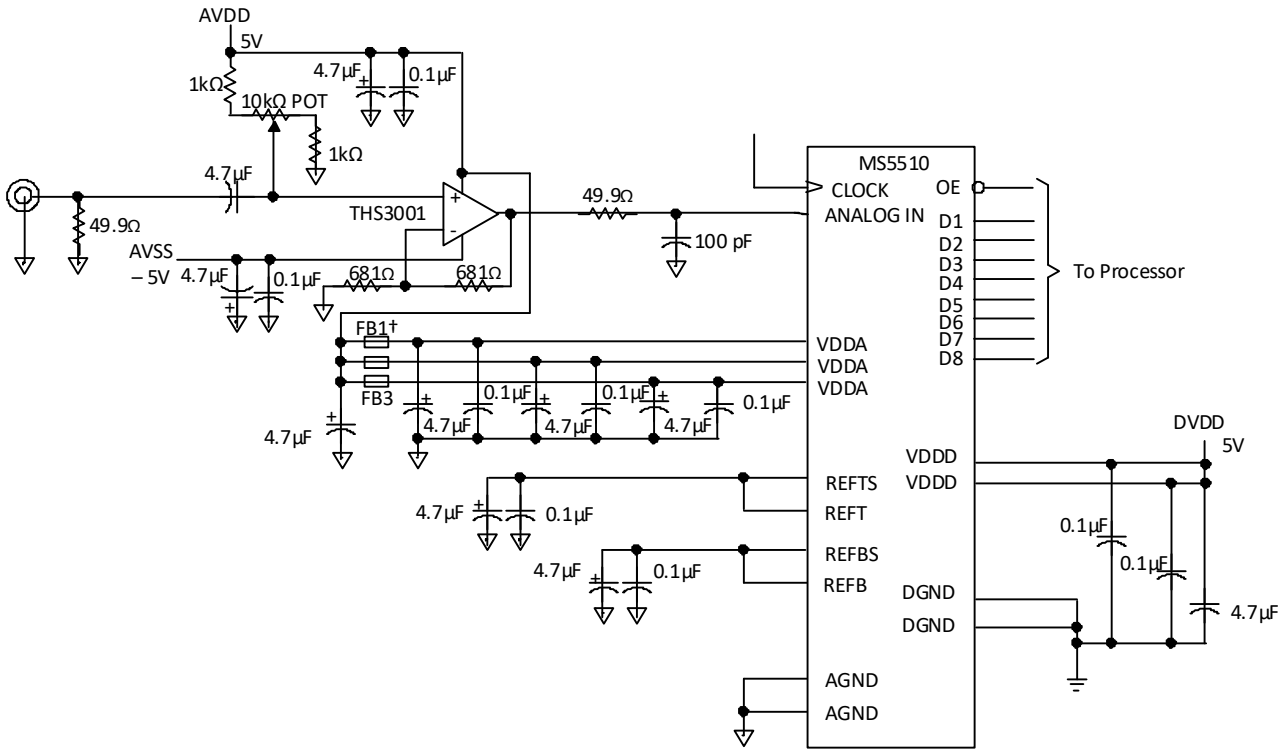
Mode 2



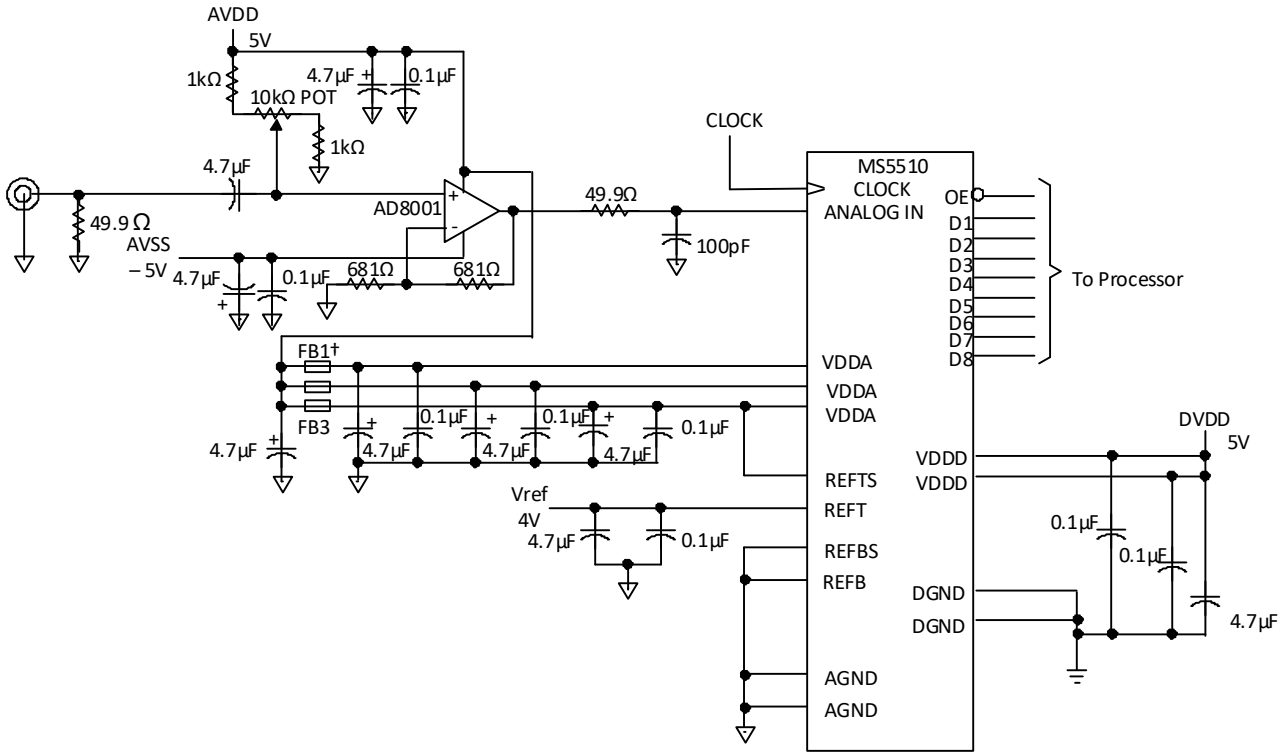
Element	Description
C1,C3-C4,C6-C11	0.1μf
C2	10pf
C5	47μf
FB1,FB2,FB3,FB7	Ferrite Ring
Q1	2N3414 or Equivalent Device
R1,R3	75Ω
R2	500Ω
R4	10kΩ
R5	300Ω

Application Diagram

Mode 1

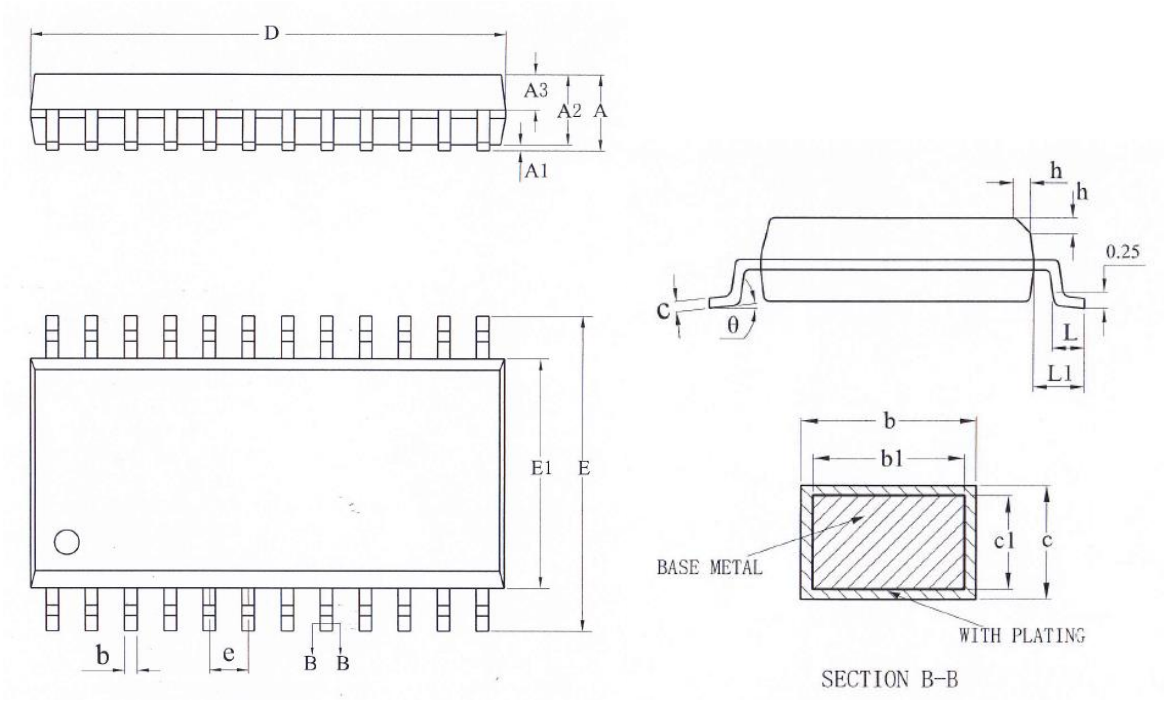


Mode 2


AVDD
5V
1kΩ
10kΩ POT
4.7µF
0.1µF
1kΩ
4.7µF
49.9Ω
AVSS
−5V
AD8001
681Ω
681Ω
4.7µF
0.1µF
49.9Ω
100pF
CLOCK
MS5510
CLOCK
ANALOG IN
OE
D1
D2
D3
D4
D5
D6
D7
D8
To Processor
FB1
FB3
VDDA
VDDA
VDDA
0.1µF
0.1µF
0.1µF
0.1µF
4.7µF
4.7µF
4.7µF
4.7µF
Vref
4V
4.7µF
0.1µF
REFTS
REFT
REFBS
REFB
AGND
AGND
DVDD
5V
VDDD
VDDD
0.1µF
0.1µF
4.7µF
DGND
DGND

PACKAGE OUTLINE DIMENSIONS

SOP24



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	2.36	2.54	2.64
A1	0.10	0.20	0.30
A2	2.26	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	15.30	15.40	15.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	-	1.00
L1	1.40REF		
h	0.25	-	0.75
θ	0	-	8°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS5510

Product Code : XXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS5510	SOP24	1000	1	1000	8	8000

STATEMENT

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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