STN3NF06L



N-channel 60 V, 0.07 Ω typ., 4 A STripFET™ II Power MOSFET in a SOT-223 package

Datasheet - production data

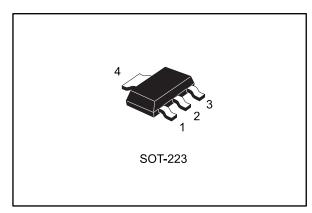
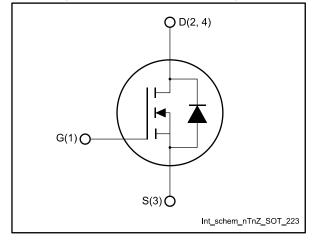


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	ID
STN3NF06L	60 V	0.1 Ω	4 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low threshold drive

Applications

Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STN3NF06L	3NF06L	SOT-223	Tape and reel

Contents STN3NF06L

Contents

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STN3NF06L Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _{DS}	Drain-source voltage	60	V	
V _{GS}	Gate-source voltage	±16	V	
I _D ⁽¹⁾	Drain current (continuous) at Tc = 25 °C	4	Α	
I _D	Drain current (continuous) at T _c = 100 °C	2.9	Α	
I _{DM} ⁽²⁾	Drain current (pulsed)	16	Α	
Ртот	Total dissipation at T _{pcb} = 25 °C 3.3			
dv/dt (3)	Peak diode recovery voltage slope	10	V/ns	
E _{AS} ⁽⁴⁾	Single pulse avalanche energy 200		mJ	
Tj	Operating junction temperature range	55 to 150	°C	
T _{stg}	Storage temperature range	- 55 to 150 °C		

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-pcb}	Thermal resistance junction-pcb (1)	38	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb ⁽²⁾	100	°C/W

Notes:

⁽¹⁾Current limited by the package.

⁽²⁾Pulse width limited by safe operating area.

 $^{^{(3)}}I_{SD} \leq 3$ A, di/dt ≤ 150 A/µs, V_{DD} $\leq V_{(BR)DSS}$

 $^{^{(4)}}$ Starting T_j = 25 °C, I_D = 4 A, V_{DD} = 30 V

 $[\]ensuremath{^{(1)}}\xspace$ When Mounted on FR-4 board 1 inch² pad, 2 oz. of Cu and t <10 s.

⁽²⁾When mounted on minimum recommended footprint.

Electrical characteristics STN3NF06L

2 Electrical characteristics

 $T_C = 25$ °C unless otherwise specified

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
	I _{DSS} Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 60 \text{ V}$			1	μΑ
I _{DSS}		$V_{GS} = 0 \text{ V}, V_{DS} = 60 \text{ V}$ $T_{C} = 125 \text{ °C}^{(1)}$			10	μΑ
Igss	Gate body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 16 \text{ V}$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1		2.8	V
Static drain-source	V _{GS} = 10 V, I _D = 1.5 A		0.07	0.10	Ω	
► DS(on)	R _{DS(on)} on-resistance	V _{GS} = 5 V, I _D = 1.5 A		0.085	0.12	Ω

Notes:

Table 5: Dynamic

Table of Dynamic						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		ı	340		pF
Coss	Output capacitance	V _{DS} =25 V, f=1 MHz, V _{GS} =0 V	-	63		pF
Crss	Reverse transfer capacitance	7 V20 -20 V, I=1 IIII I2, V30-0 V	-	30		pF
Qg	Total gate charge	V _{DD} = 48 V, I _D = 3 A	-	7	9	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 5 V	-	1.5		nC
Q_{gd}	Gate-drain charge	(see Figure 14: "Test circuit for gate charge behavior")	-	2.8		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 30 V, I _D = 1.5 A,	-	9	-	ns
t _r	Rise time	$R_G = 4.7 \Omega$	-	25	-	ns
t _{d(off)}	Turn-off delay time	V _{GS} = 5 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	20	-	ns
t _f	Fall time		-	10	-	ns

 $[\]ensuremath{^{(1)}}\mbox{Defined}$ by design, not subject to production test.

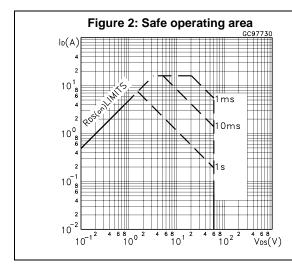
Table 7: Source-drain diode

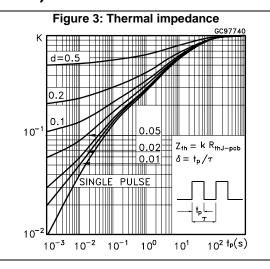
Table 1. Course drain diode						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I _{SD} = 4 A, V _{GS} =0 V	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 4 A, di/dt = 100 A/μs,	-	50		ns
Qrr	Reverse recovery charge	V _{DD} =25 V, T _j =150 °C (see <i>Figure 15: "Test circuit for</i>	-	88		nC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	3.5		Α

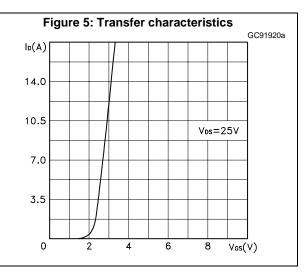
Notes:

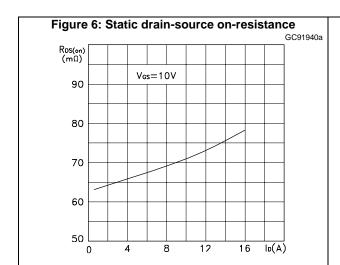
 $^{^{(1)}\}text{Pulsed:}$ pulse duration = 300 $\mu\text{s},$ duty cycle 1.5%

2.1 Electrical characteristics (curves)









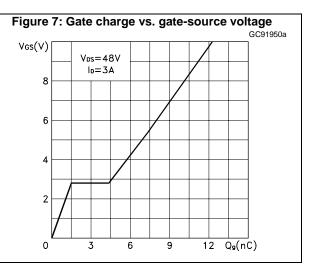


Figure 10: Normalized on-resistance vs temperature

GC91980a

Ros(on)
(norm)

2.0

1.6

1.2

0.8

0.4

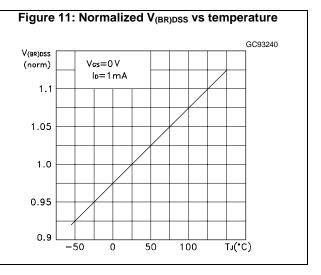
-50

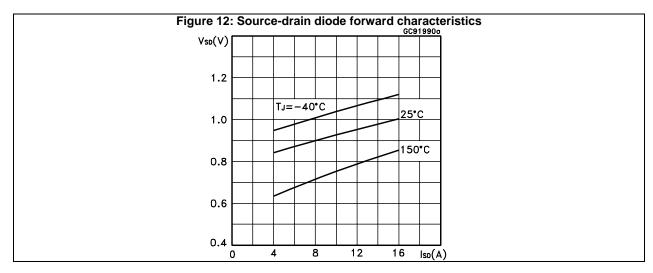
0

50

100

TJ(*C)





Test circuits STN3NF06L

3 Test circuits

Figure 13: Test circuit for resistive load switching times

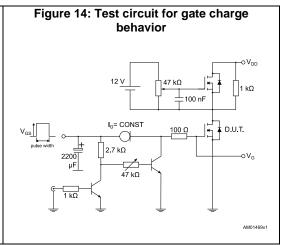
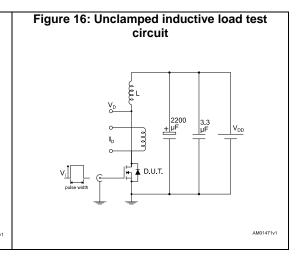
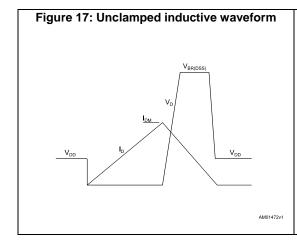
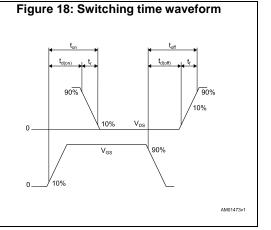


Figure 15: Test circuit for inductive load switching and diode recovery times







4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 SOT-223 package information

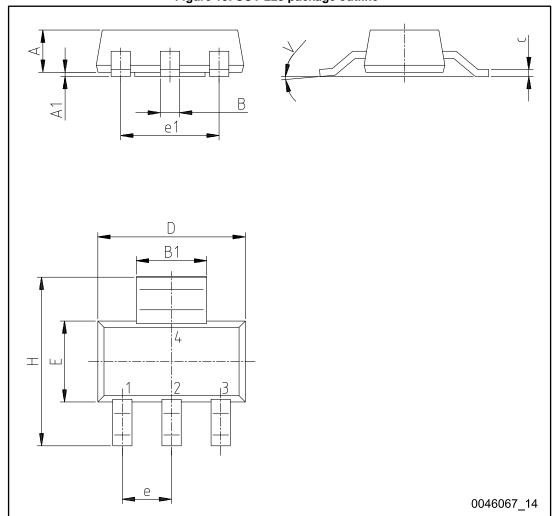
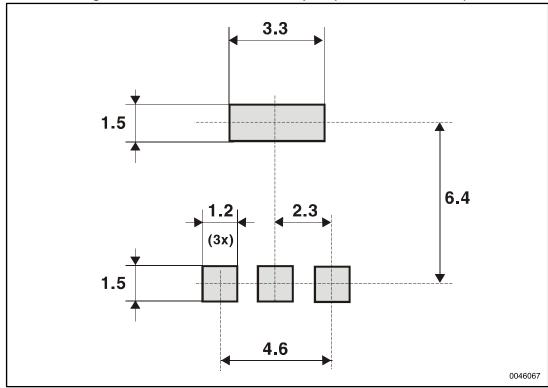


Figure 19: SOT-223 package outline

Table 8: SOT-223 package mechanical data

Dim.	mm				
Dim.	Min.	Тур.	Max.		
A			1.8		
A1	0.02		0.1		
В	0.6	0.7	0.85		
B1	2.9	3	3.15		
С	0.24	0.26	0.35		
D	6.3	6.5	6.7		
е		2.3			
e1		4.6			
Е	3.3	3.5	3.7		
Н	6.7	7.0	7.3		
V			10°		

Figure 20: SOT-223 recommended footprint (dimensions are in mm)



STN3NF06L Revision history

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
21-Jun-2004	5	Complete version.
04-Oct-2006	6	New template, no content change.
01-Feb-2007	7	Typo mistake on Table 2.
12-Jun-2008	8	Corrected marking on Table 1
03-Jul-2017	9	Modified internal schematic diagram on cover page. Updated Section 4: "Package information". Minor text changes.

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