

**Typical Applications**

- Electric Power Steering (EPS)
- Anti-lock Braking System (ABS)
- Wiper Control
- Climate Control
- Power Door

**Benefits**

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

**Description**

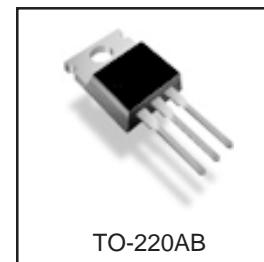
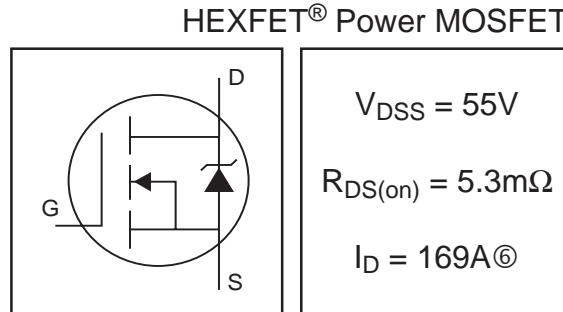
Specifically designed for Automotive applications, this Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

**Absolute Maximum Ratings**

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	169@	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	118@	
I <sub>DM</sub>	Pulsed Drain Current ①	680	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	560	mJ
I <sub>AR</sub>	Avalanche Current	See Fig.12a, 12b, 15, 16	A
E <sub>AR</sub>	Repetitive Avalanche Energy ⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	0.45	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient	—	62	



**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.057	—	$\text{V}/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	4.6	5.3	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}, I_D = 101\text{A}$ ④
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{\text{DS}} = 10\text{V}, I_D = 250\mu\text{A}$
$g_{\text{fs}}$	Forward Transconductance	69	—	—	S	$V_{\text{DS}} = 25\text{V}, I_D = 110\text{A}$
$I_{\text{DSS}}$	Drain-to-Source Leakage Current	—	—	20	$\mu\text{A}$	$V_{\text{DS}} = 55\text{V}, V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 44\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 150^\circ\text{C}$
$I_{\text{GSS}}$	Gate-to-Source Forward Leakage	—	—	200	$\text{nA}$	$V_{\text{GS}} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -20\text{V}$
$Q_g$	Total Gate Charge	—	170	260	$\text{nC}$	$I_D = 101\text{A}$
$Q_{\text{gs}}$	Gate-to-Source Charge	—	44	66		$V_{\text{DS}} = 44\text{V}$
$Q_{\text{gd}}$	Gate-to-Drain ("Miller") Charge	—	62	93		$V_{\text{GS}} = 10\text{V}$ ④
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	13	—	$\text{ns}$	$V_{\text{DD}} = 38\text{V}$
$t_r$	Rise Time	—	190	—		$I_D = 110\text{A}$
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	130	—		$R_G = 1.1\Omega$
$t_f$	Fall Time	—	110	—		$V_{\text{GS}} = 10\text{V}$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	$\text{nH}$	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{\text{iss}}$	Input Capacitance	—	5480	—	$\text{pF}$	$V_{\text{GS}} = 0\text{V}$
$C_{\text{oss}}$	Output Capacitance	—	1210	—		$V_{\text{DS}} = 25\text{V}$
$C_{\text{rss}}$	Reverse Transfer Capacitance	—	280	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{\text{oss}}$	Output Capacitance	—	5210	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 1.0\text{V}, f = 1.0\text{MHz}$
$C_{\text{oss}}$	Output Capacitance	—	900	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 44\text{V}, f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance ⑤	—	1500	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 0\text{V to } 44\text{V}$

**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	169⑥	$\text{A}$	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{\text{SM}}$	Pulsed Source Current (Body Diode) ①	—	—	680		
$V_{\text{SD}}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 101\text{A}, V_{\text{GS}} = 0\text{V}$ ④
$t_{\text{rr}}$	Reverse Recovery Time	—	88	130	ns	$T_J = 25^\circ\text{C}, I_F = 101\text{A}$
$Q_{\text{rr}}$	Reverse Recovery Charge	—	250	380	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

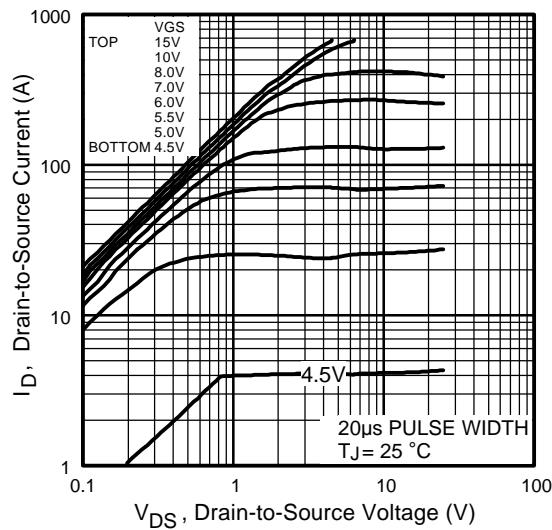
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}, L = 0.11\text{mH}$   
 $R_G = 25\Omega, I_{AS} = 101\text{A}$ . (See Figure 12).
- ③  $I_{SD} \leq 101\text{A}$ ,  $di/dt \leq 210\text{A}/\mu\text{s}$ ,  $V_{\text{DD}} \leq V_{(\text{BR})\text{DSS}}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

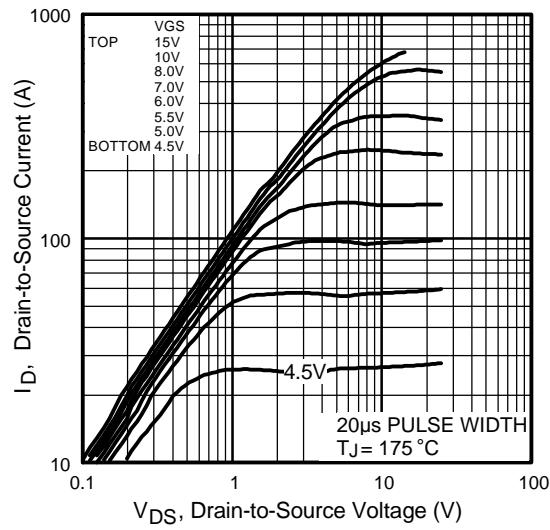
⑤  $C_{\text{oss eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{\text{DSS}}$ .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

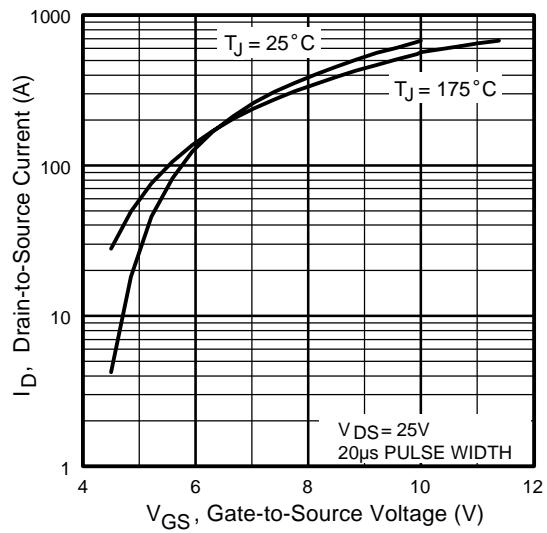
⑦ Limited by  $T_{J\text{max}}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.



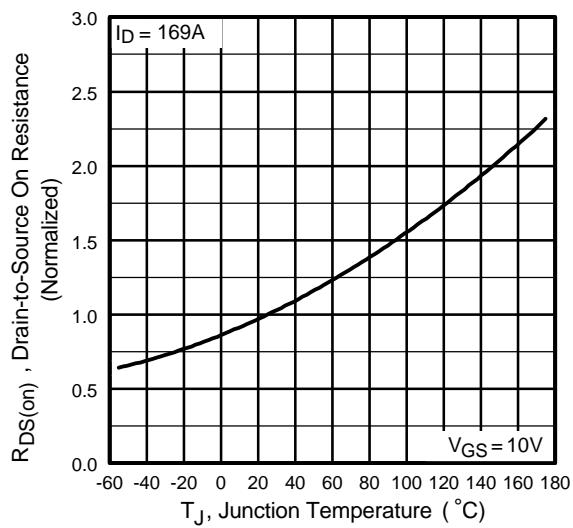
**Fig 1.** Typical Output Characteristics



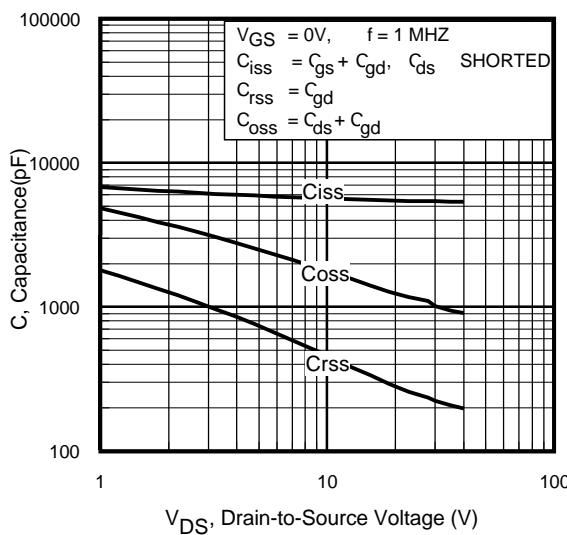
**Fig 2.** Typical Output Characteristics



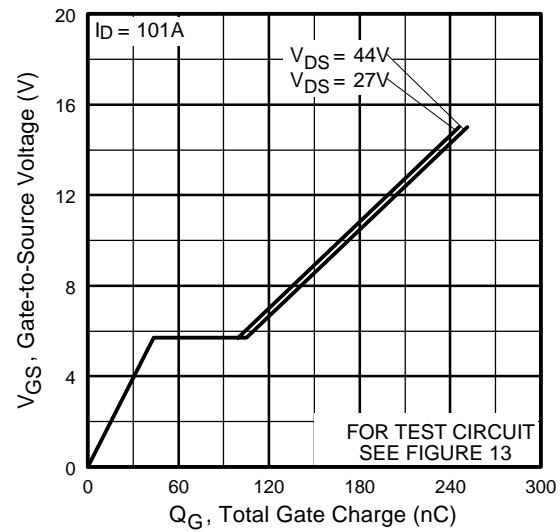
**Fig 3.** Typical Transfer Characteristics



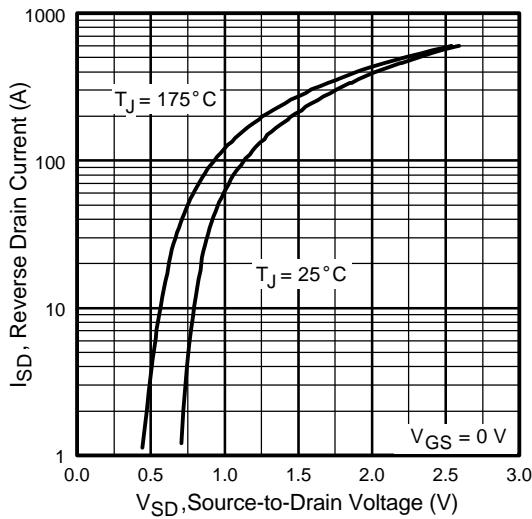
**Fig 4.** Normalized On-Resistance Vs. Temperature



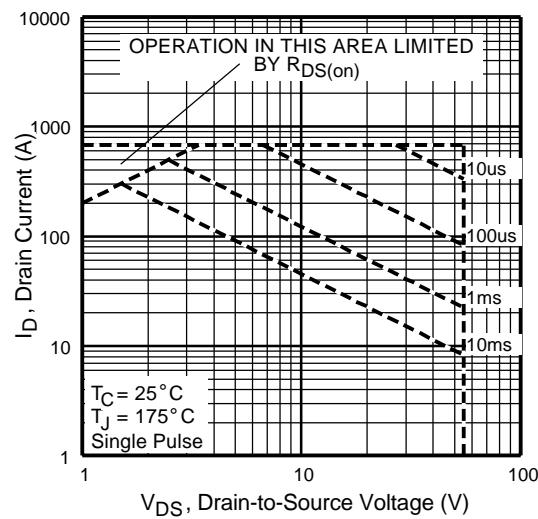
**Fig 5.** Typical Capacitance Vs.  
Drain-to-Source Voltage



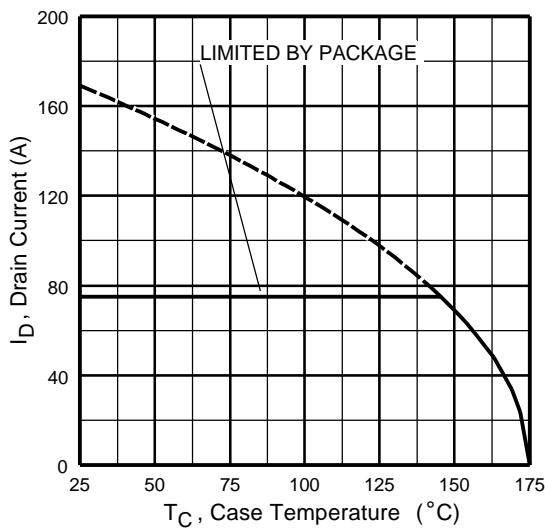
**Fig 6.** Typical Gate Charge Vs.  
Gate-to-Source Voltage



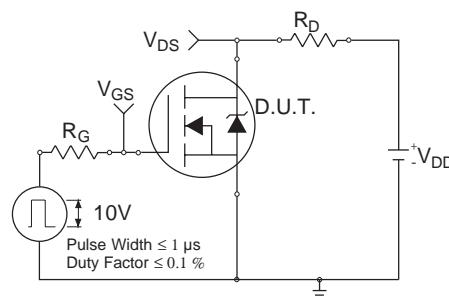
**Fig 7.** Typical Source-Drain Diode  
Forward Voltage



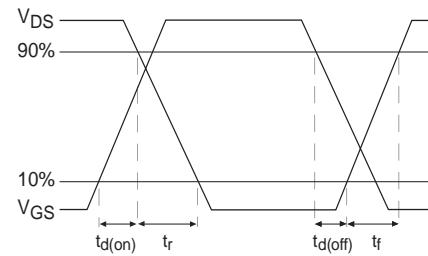
**Fig 8.** Maximum Safe Operating Area



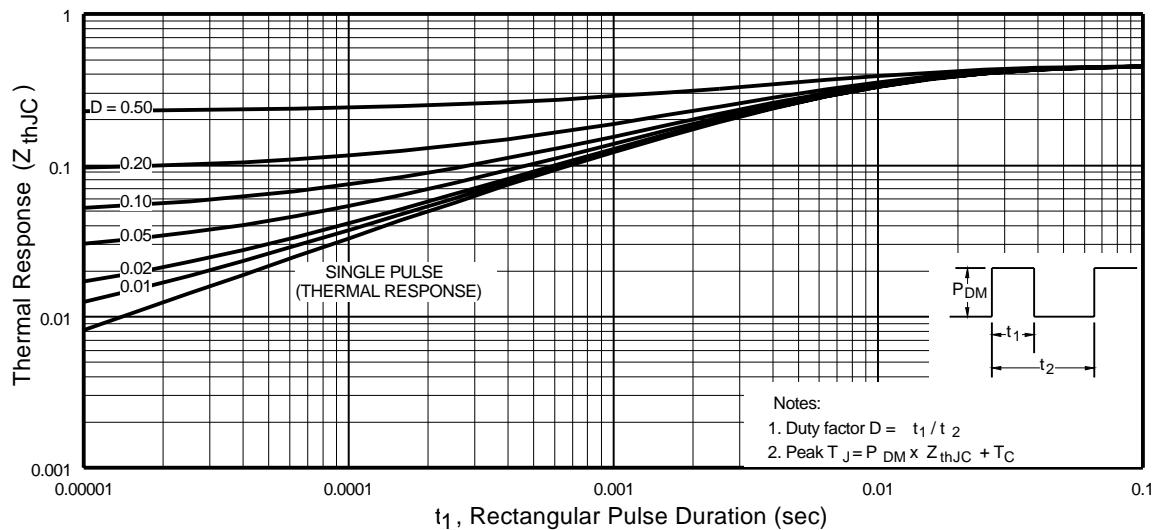
**Fig 9.** Maximum Drain Current Vs. Case Temperature



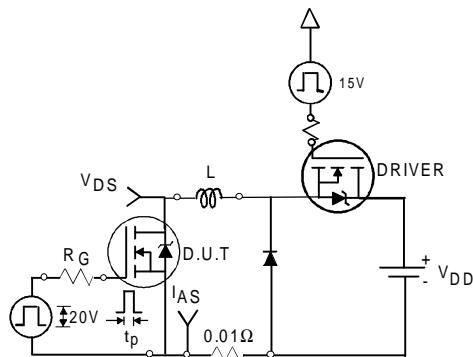
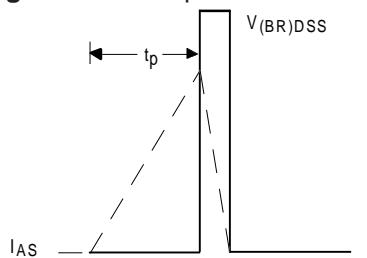
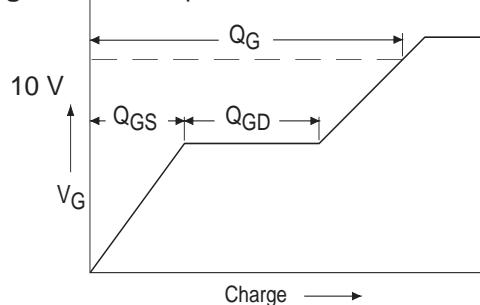
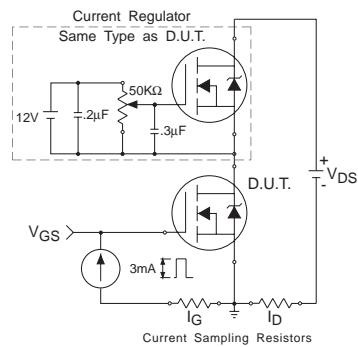
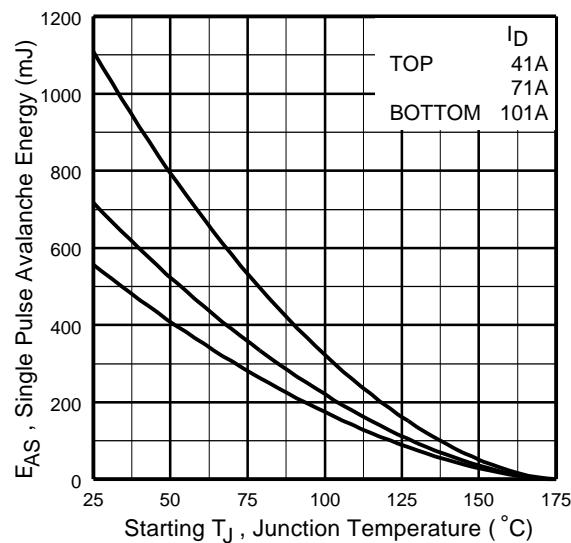
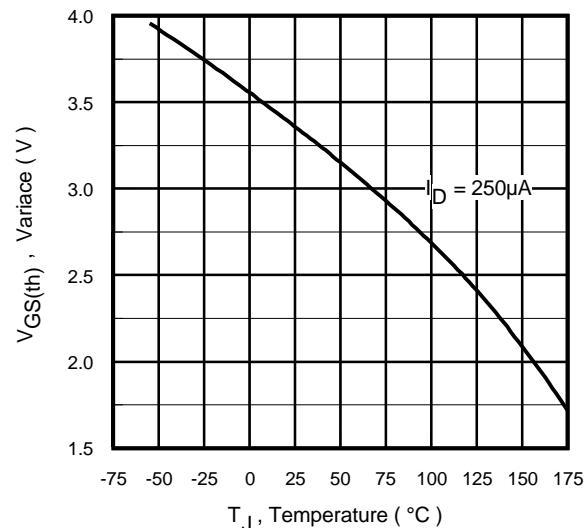
**Fig 10a.** Switching Time Test Circuit

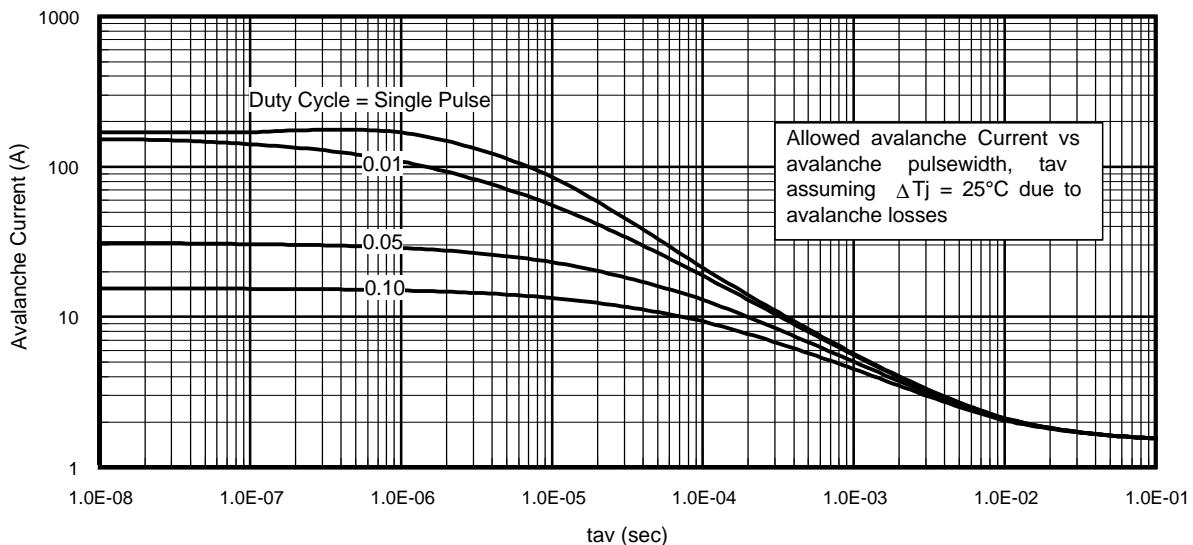


**Fig 10b.** Switching Time Waveforms

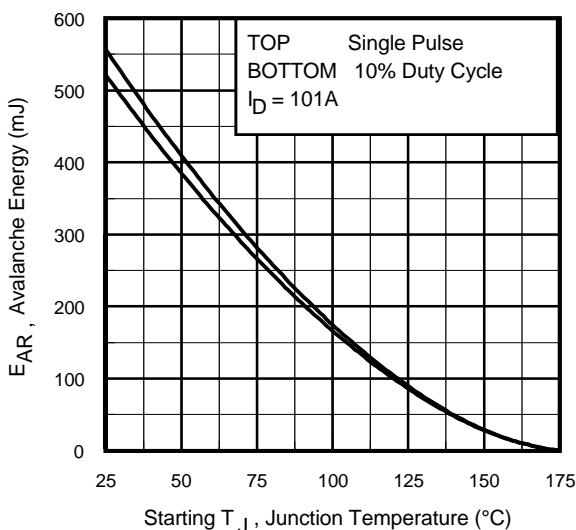


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Fig 12a.** Unclamped Inductive Test Circuit**Fig 12b.** Unclamped Inductive Waveforms**Fig 13a.** Basic Gate Charge Waveform**Fig 13b.** Gate Charge Test Circuit**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current**Fig 14.** Threshold Voltage Vs. Temperature



**Fig 15.** Typical Avalanche Current Vs.Pulsewidth



**Fig 16.** Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))**

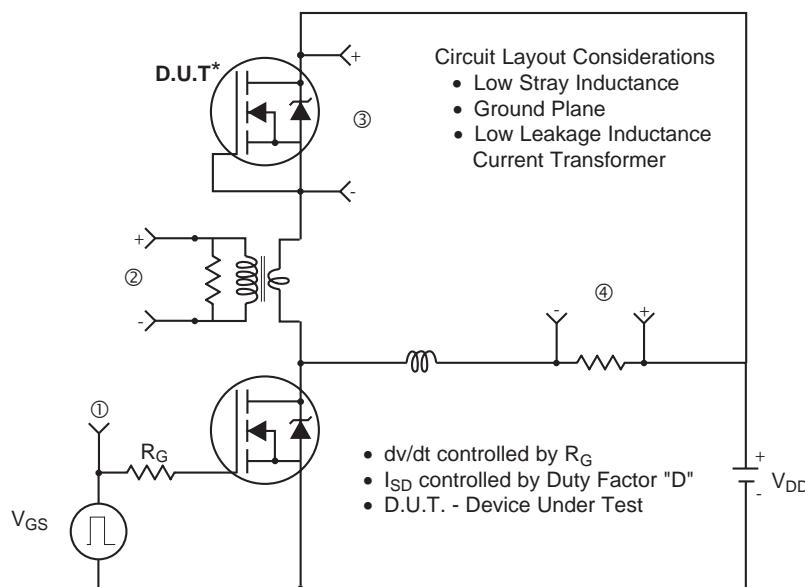
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as  $25^\circ\text{C}$  in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

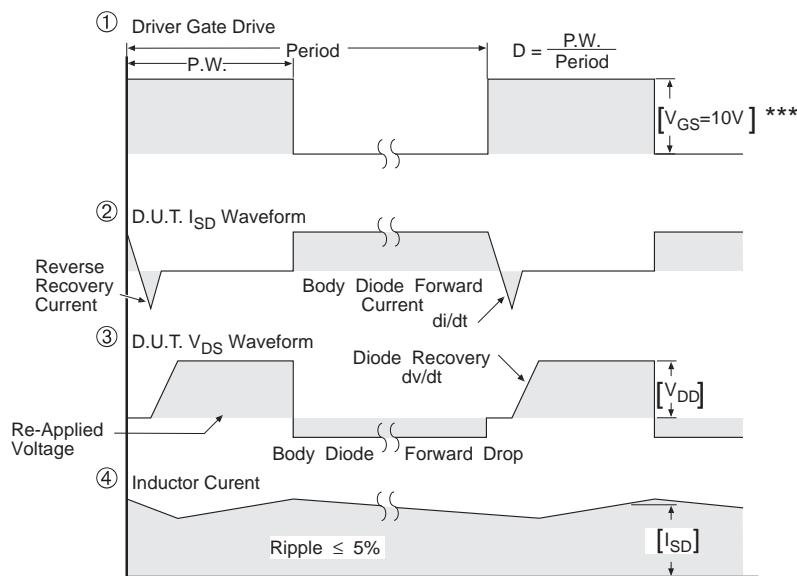
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

### Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 17.** For N-channel HEXFET® power MOSFETs