

Features

- Senses Bus Voltages From 0V to 36V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power
- High Accuracy
- Configurable Averaging Options
- 16 Programmable Addresses
- Operates from 2.7-V to 5.5-V Power Supply
- 10-Pin, MSOP Package

Applications

- Power management
- Servers
- Telecom Equipment
- Computing
- Test Equipment

Description

The TPA626 is a current and power monitor, with I²C or SMBUS-compatible interface. The device monitors both a shunt voltage drop and bus supply voltage.

The TPA626 common mode input voltage can vary from 0V to 36V.

The TPA626 features up to 16 programmable addresses on the I²C-compatible interface.

Function block or application schematic

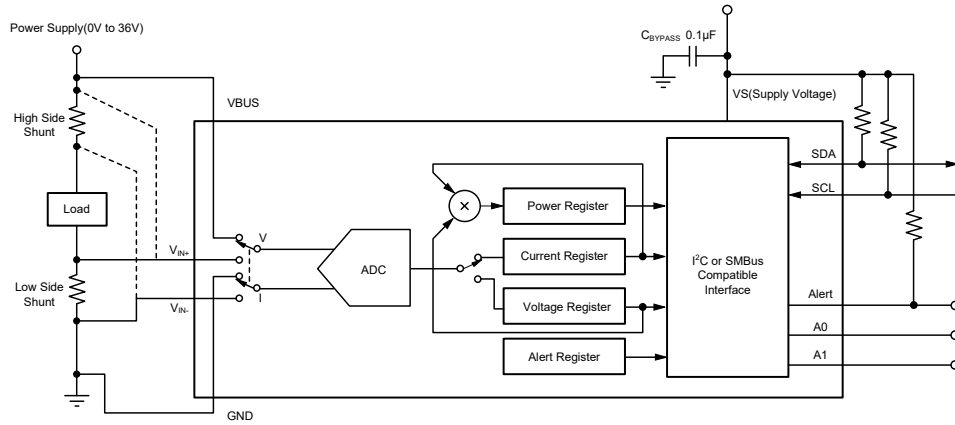
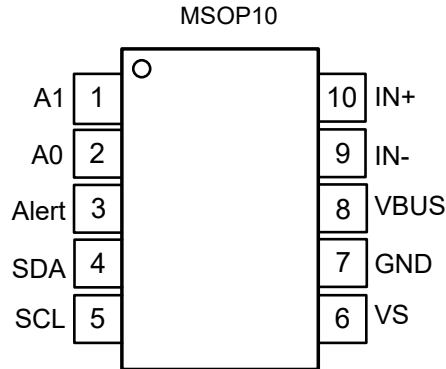


Figure 1.

Table of Contents

Features	1
Applications.....	1
Description.....	1
Function block or application schematic	2
Table of Contents	3
Pin Configuration and Functions	4
Pin Functions	4
Order Information.....	4
Absolute Maximum Ratings	5
ESD, Electrostatic Discharge Protection.....	5
Thermal Information	5
Electrical Characteristics	6
Electrical Characteristics-.....	7
Typical Performance Characteristics-.....	8
Detailed description.....	10
Programming.....	10
I2C address	10
Register map	11
Tape And Reel Information.....	16
Package Outline Dimensions.....	17
Revision History	18

Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	2	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
A1	1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS.
Alert	3	Digital output	Multi-functional alert, open-drain output.
GND	7	Analog	Ground.
IN+	10	Analog input	Connect to supply side of shunt resistor.
IN-	9	Analog input	Connect to load side of shunt resistor.
SCL	5	Digital input	Serial bus clock line, open-drain input.
SDA	4	Digital I/O	Serial bus data line, open-drain input/output.
VBUS	8	Analog input	Bus voltage input.
VS	6	Analog	Power supply, 2.7 V to 5.5 V.

Order Information

Model Name	Order Number	Package	MSL Level	Transport Media, Quantity	Marking Information
TPA626	TPA626-VR	MSOP10	1	Tape and Reel, 3000	TPA626

Absolute Maximum Ratings

Cover operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{VS}	Supply voltage		6	V
Analog Inputs, IN+, IN-	Differential (V _{IN+} - V _{IN-}) ⁽²⁾	-40	40	V
	Common-Mode (V _{IN+} + V _{IN-}) / 2	-0.3	40	
V _{VBUS}		-0.3	40	V
V _{SDA}		GND - 0.3	6	V
V _{SCL}		GND - 0.3	V _{VS} + 0.3	V
I _{IN}	Input current into any pin		5	mA
I _{OUT}	Open-drain digital output current		10	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) IN+ and IN- may have a differential voltage between -40 V and 40 V. However, the voltage at these pins must not exceed the range -0.3 V to 40 V.

ESD, Electrostatic Discharge Protection

		VALUE	UNIT
V _(ESD)	Electrostatic		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000		

Thermal Information

Package Type	θ _{JA}	θ _{JC}	Unit
MSOP10	171	42.9	°C/W

Electrical Characteristics

$T_A = 25^\circ\text{C}$, $V_{VS} = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽⁵⁾
INPUT							
	Shunt voltage input range		-81.9175		81.92	mV	A
	Bus voltage input range ⁽¹⁾		0		36	V	A
CMRR	Common-mode rejection	$0\text{ V} \leq V_{IN+} \leq 36\text{ V}$	120	140		dB	A
V_{OS}	Shunt offset voltage, RTI ⁽²⁾			± 2.5	± 30	μV	A
	Shunt offset voltage, RTI ⁽²⁾ vs temperature	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		0.15		$\mu\text{V}/^\circ\text{C}$	B
PSRR	Shunt offset voltage, RTI ⁽²⁾ vs power supply	$2.7\text{ V} \leq V_S \leq 5.5\text{ V}$		5		$\mu\text{V}/\text{V}$	A
V_{OS}	Bus offset voltage, RTI ⁽²⁾			± 10	± 20	mV	A
	Bus offset voltage, RTI ⁽²⁾ vs temperature	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		60		$\mu\text{V}/^\circ\text{C}$	B
PSRR	Bus offset voltage, RTI ⁽²⁾ vs power supply			1		mV/V	A
I_B	Input bias current				10	μA	A
	VBUS input impedance			830		k Ω	A
	Input leakage ⁽³⁾	(IN+ pin) + (IN- pin), Power-down mode		1		μA	A
DC ACCURACY							
	ADC native resolution			16		Bits	A
	1 LSB step size	Shunt voltage		2.5		μV	A
		Bus voltage		1.25		mV	A
	Shunt voltage gain error			0.02%	0.4%		A
	Shunt voltage gain error vs temperature	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		50		ppm/ $^\circ\text{C}$	B
	Shunt voltage linearity				0.5%		A
	Bus voltage gain error			0.02%	0.4%		A
	Bus voltage gain error vs temperature	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		50		ppm/ $^\circ\text{C}$	B
	Bus voltage linearity				0.5%		A
t_{CT}	ADC conversion time	CT bit = 000		66		μs	B
		CT bit = 001		134			B

	CT bit = 010	269		μs	B
	CT bit = 011	542			B
	CT bit = 100	1085			B
	CT bit = 101	2170			B
	CT bit = 110	4341			B
	CT bit = 111	8682			B
SMBus					
	SMBus timeout ⁽⁴⁾	28		ms	B

(1) While the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V.

(2) RTI = Referred-to-input.

(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.

(4) SMBus timeout in the TPA626 resets the interface any time SCL is low for more than 28 ms.

(5) Test Levels: (A) Tested at final test. Overtemperature limits are set by characterization and simulation. (B) Set by characterization and simulation. (C) Typical value only for information, provided by design simulation.

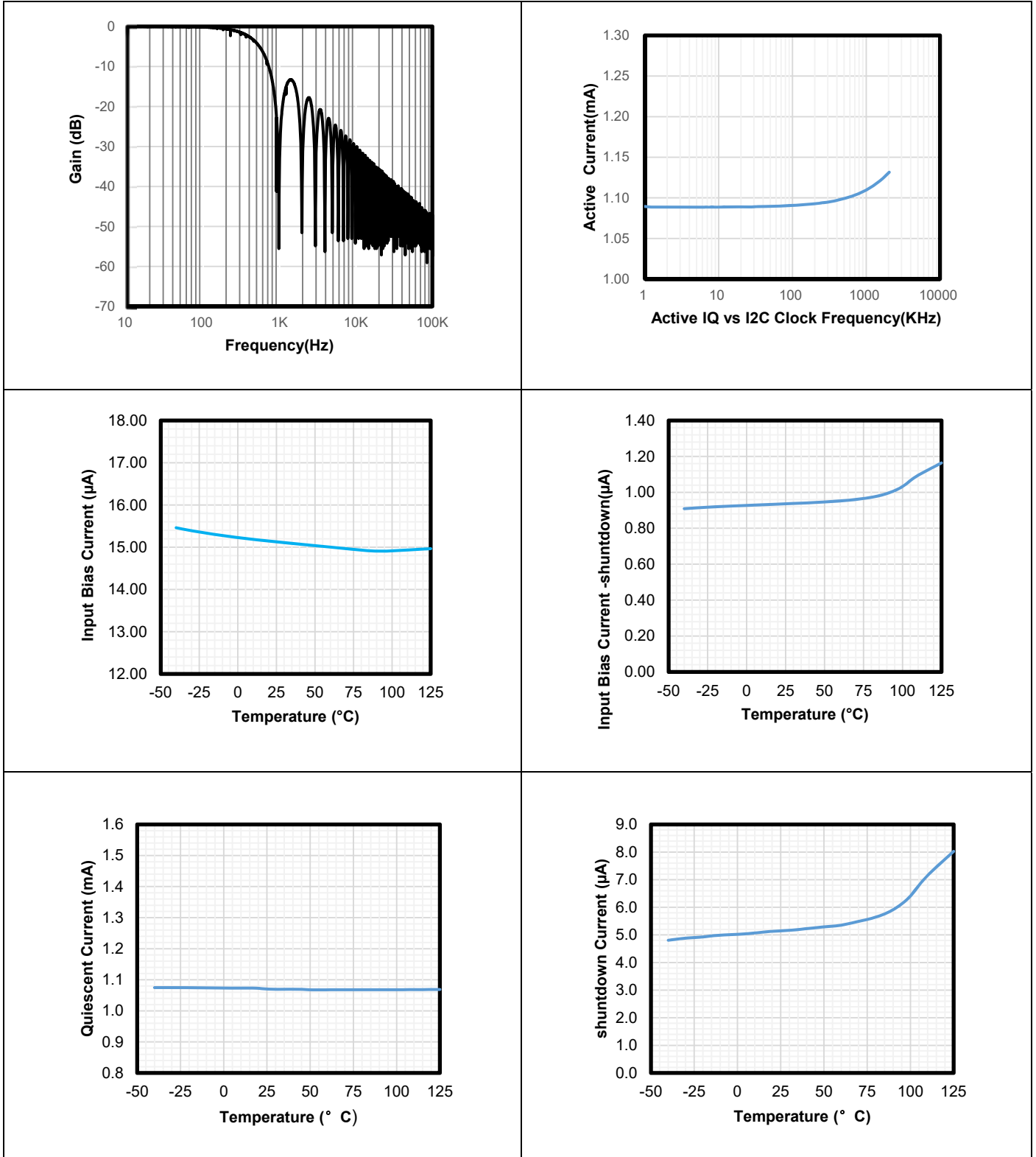
Electrical Characteristics-

$T_A = 25^\circ\text{C}$, $V_{VS} = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted

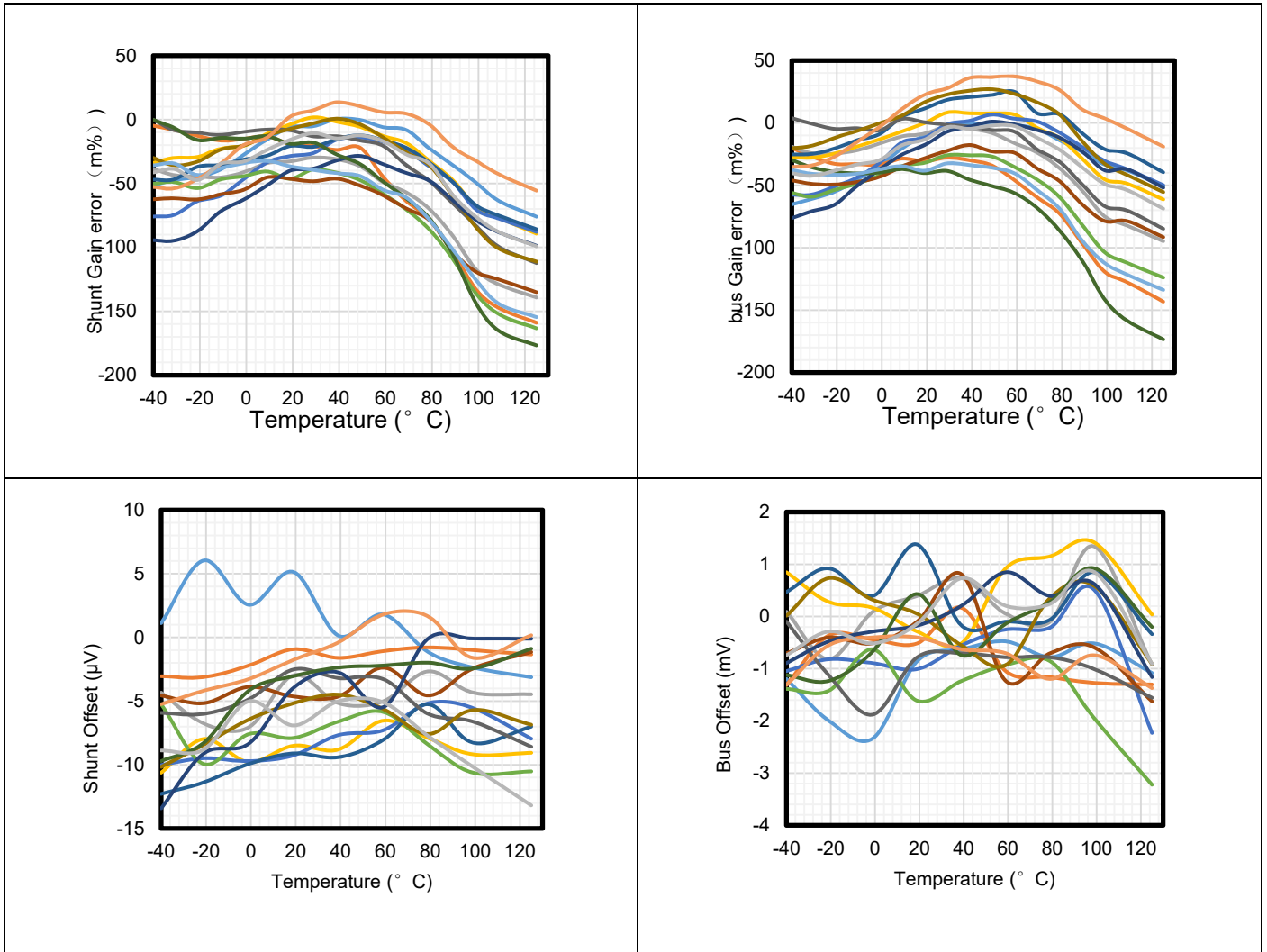
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Test Level ⁽⁵⁾
DIGITAL INPUT/OUTPUT						
Input capacitance			3		pF	C
Leakage input current	$0\text{ V} \leq V_{SCL} \leq V_{VS}$, $0\text{ V} \leq V_{SDA} \leq V_{VS}$, $0\text{ V} \leq V_{Alert} \leq V_{VS}$, $0\text{ V} \leq V_{A0} \leq V_{VS}$, $0\text{ V} \leq V_{A1} \leq V_{VS}$		0.1		μA	A
V_{IH}	High-level input voltage	$0.7 \times V_{VS}$			V	A
V_{IL}	Low-level input voltage		$0.3 \times V_{VS}$		V	A
V_{OL}	Low-level output voltage, SDA, Alert	0		0.4	V	A
	Hysteresis		150		mV	C
POWER SUPPLY						
	Operating supply range	2.7		5.5	V	A
I_Q	Quiescent current		1100		μA	A
	Quiescent current, power-down (shutdown) mode		8		μA	A
V_{POR}	Power-on reset threshold		2.2		V	B

Typical Performance Characteristics-

At $T_A = 25^\circ\text{C}$, $V_{VS} = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted.



At $T_A = 25^\circ\text{C}$, $V_{VS} = 3.3\text{ V}$, $V_{IN+} = 12\text{ V}$, $V_{SENSE} = (V_{IN+} - V_{IN-}) = 0\text{ mV}$ and $V_{VBUS} = 12\text{ V}$, unless otherwise noted.



Detailed description

The TPA626 is a digital current sense amplifier with an I2C- and SMBus-compatible interface. It performs two measurements on the power-supply bus: The differential shunt voltage created by load current flowing through a shunt resistor is measured at the IN+ and IN- pins. And the power supply bus voltage is measured at the VBUS pin.

Programming

Table 1 lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 1 Calculating Current and Power

STEP	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Step 1	Configuration Register	00h	4127h	—	—	—
Step 2	Shunt Register	01h	1F40h	8000	2.5 μ V	20 mV
Step 3	Bus Voltage Register	02h	2570h	9584	1.25 mV	11.98 V
Step 4	Calibration Register	05h	A00h	2560	—	—
Step 5	Current Register	04h	2710	10000	1 mA	10 A
Step 6	Power Register	03h	12B8h	4792	25 mW	119.82 W

I2C address

The device has two address pins, A0 and A1. The device samples the state of pins A0 and A1 on every bus communication. Following table lists the pin logic levels for each of the 16 possible addresses.

Table 2 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110

SCL	SCL	1001111
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Register map

Table 3 Register Set Summary

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE ⁽¹⁾
			BINARY	HEX	
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	01000001 00100111	4127	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	00000000 00000000	0000	R
02h	Bus Voltage Register	Bus voltage measurement data.	00000000 00000000	0000	R
03h	Power Register ⁽²⁾	Contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
04h	Current Register ⁽²⁾	Contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R

Table 4

POINTER ADDRESS	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE ⁽¹⁾
			BINARY	HEX	
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	00000000 00000000	0000	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	00000000 00000000	0000	R/W
FEh	Manufacturer ID Register	Contains unique manufacturer identification number.	0101010001001001	5549	R
FFh	Die ID Register	Contains unique die identification number.	0010001001100000	2260	R

Table 5 Configuration Register (00h) (Read/Write) Descriptions

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT2	VBUSCT1	VBUSCT0	VSHCT2	VSHCT1	VSHCT0	MODE3	MODE2	MODE1
POR VALUE	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

Table 6 AVG Bit Settings[11:9] Combinations

AVG2 D11	AVG1 D10	AVG0 D9	NUMBER OF AVERAGES ⁽¹⁾
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

(1) Shaded values are default.

Table 7 VBUSCT Bit Settings [8:6] Combinations

VBUSCT2 D8	VBUSCT1 D7	VBUSCT0 D6	CONVERSION TIME (μS)
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170
1	1	0	4341
1	1	1	8682

Table 8 VSHCT Bit Settings [5:3] Combinations

VSHCT2 D5	VSHCT1 D4	VSHCT0 D3	CONVERSION TIME ⁽¹⁾
0	0	0	66
0	0	1	134
0	1	0	269
0	1	1	542
1	0	0	1085
1	0	1	2170

1	1	0	4341
1	1	1	8682

Table 9 Mode Settings [2:0] Combinations

MODE3 D2	MODE2 D1	MODE1 D0	MODE ⁽¹⁾
0	0	0	Power-Down (or Shutdown)
0	0	1	Shunt Voltage, Triggered
0	1	0	Bus Voltage, Triggered
0	1	1	Shunt and Bus, Triggered
1	0	0	Power-Down (or Shutdown)
1	0	1	Shunt Voltage, Continuous
1	1	0	Bus Voltage, Continuous
1	1	1	Shunt and Bus, Continuous

Table 10 Shunt Voltage Register (01h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 11 Bus Voltage Register (02h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	BD14	BD13	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 12 Power Register (03h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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Table 13 Current Register (04h) (Read-Only) Register Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14 Calibration Register (05h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15 Mask/Enable Register (06h) (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 16 Alert Limit Register (07h) (Read/Write) Description

ddBIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17 Manufacturer ID Register (FEh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

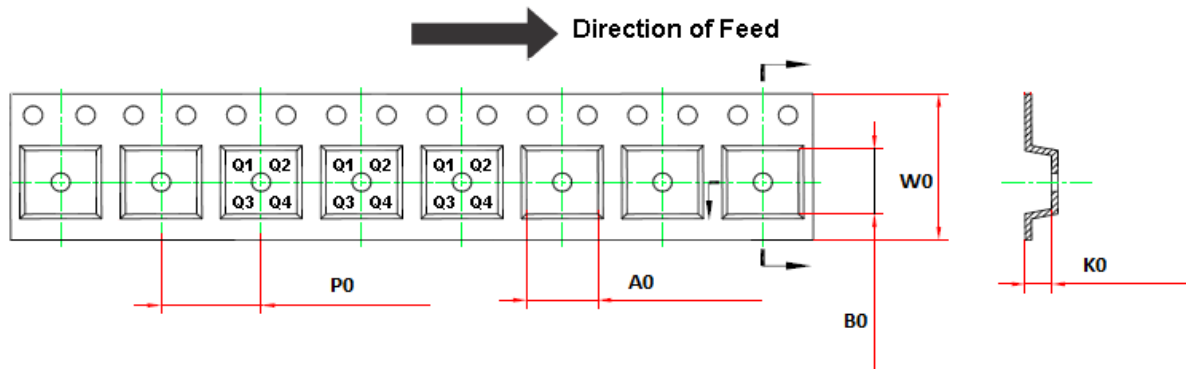
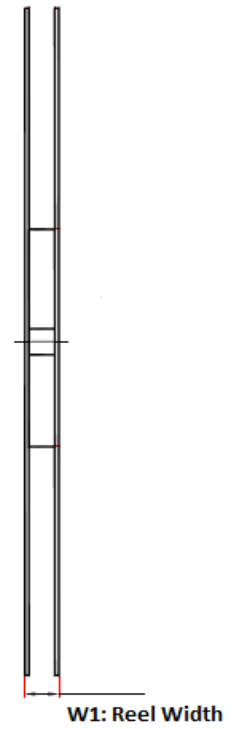
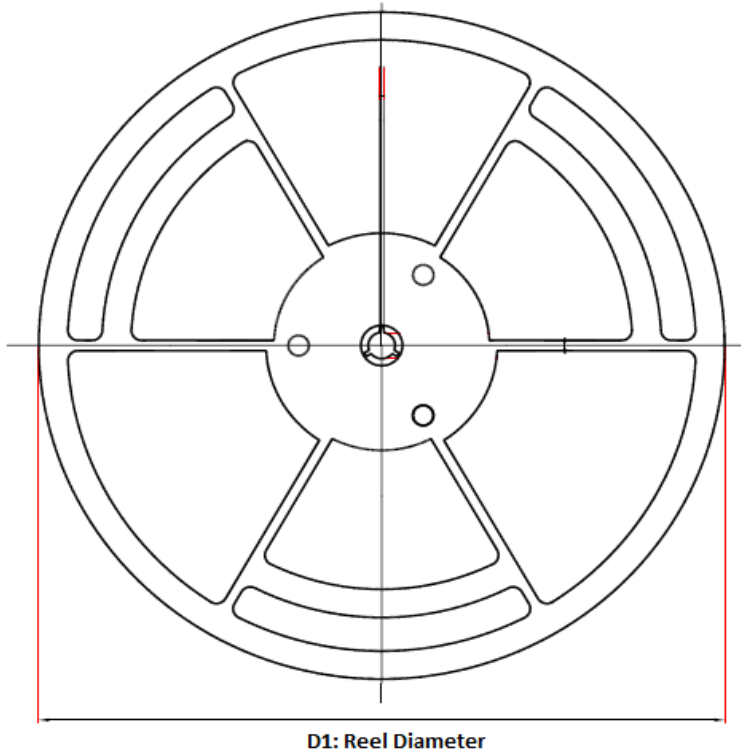
Bi-Directional Current and Power Monitor

BIT NAME	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
POR VALUE	0	1	0	1	0	1	0	1	0	1	0	0	1	0	0	1

Table 18 Die ID Register (FFh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	RID3	RID2	RID1	RID0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

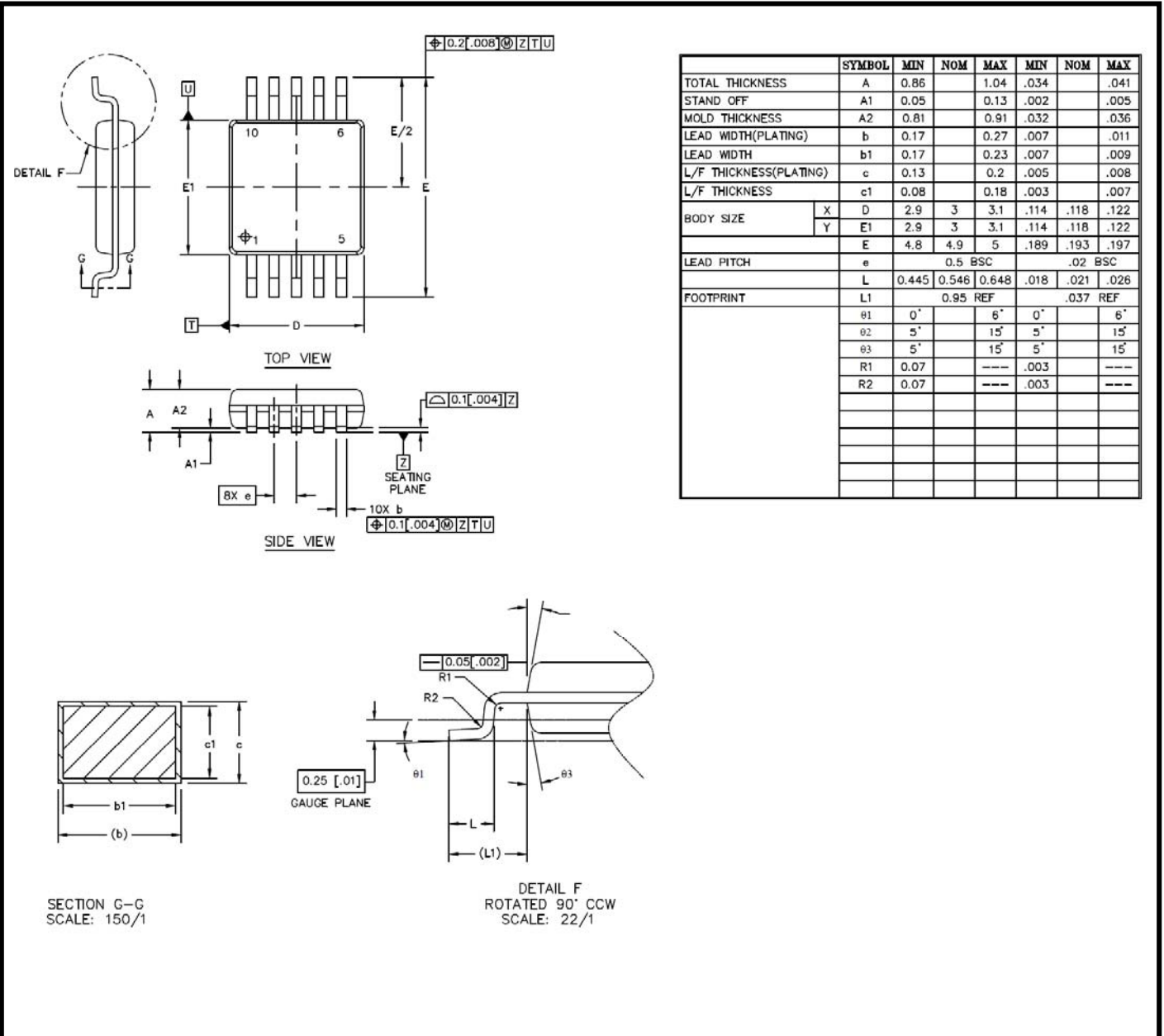
Tape And Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
	MSOP10	330.0	17.6	5.20	3.30	1.50	8.0	12.0	Q1

Package Outline Dimensions

MSOP10



Revision History

Date	Version	Note
2019/9/6	A.01	First version
2019/11/23	A.02	Add Ib bias current max limit. Add shunt and bus linearity parameters. Correct register bit number typo in Table 8